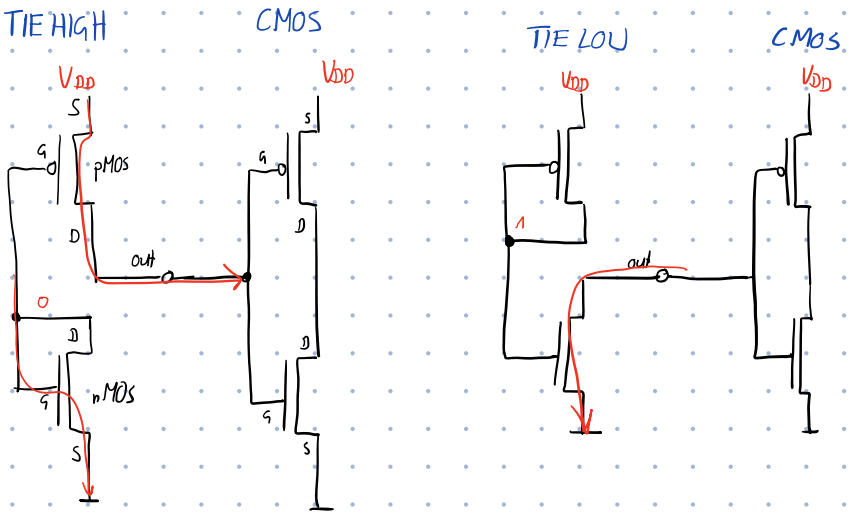
PHYSICAL CELLS - DESIGN FOR MANUFACTURABILITY

- no logic function, (no input), added to improve yield

TIE CELLS

- Purpose: connect the gate to either V_{DD} / GND (has no input)
- Problem
  - V_{DD} may spike due to ESD
  - these spikes could destroy the thin gate oxide
- solution: don't connect gate directly to V_{DD}/GND but have a Tie Cell in between that filters the signal



$V_g = V_d \longrightarrow V_{gs} = V_{DS} \longrightarrow V_{DS} > V_{gs} - V_t$

- NMOS is always in saturation (ON) region
- PMOS is always is saturation (ON) region
- CMOS gate always connected to V_{DD}
- CMOS gate always connected to V_{SS}/GND

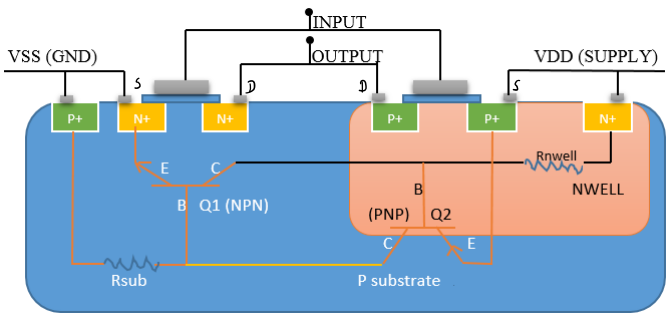
TAP CELLS / WELL TAP

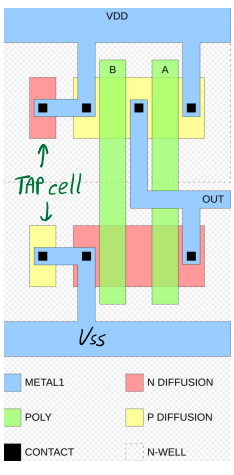
NAND

Purpose: prevent short between V_{DD} to V_{SS} due to latch up issue

Problem:
- PNP (PMOS) and NPN (NMOS) junctions are formed which behave like parasitic transistors
- if both are ON, than current flows directly from V_{DD} to GND, likely destroying the transistor
- this happen if either IN and OUT > V_{DD} or IN and OUT < V_{SS}

Solution:
- prevent voltage build up by reducing resistance of Nwell (PMOS) and P substrate
- increase current path via Tap Cells



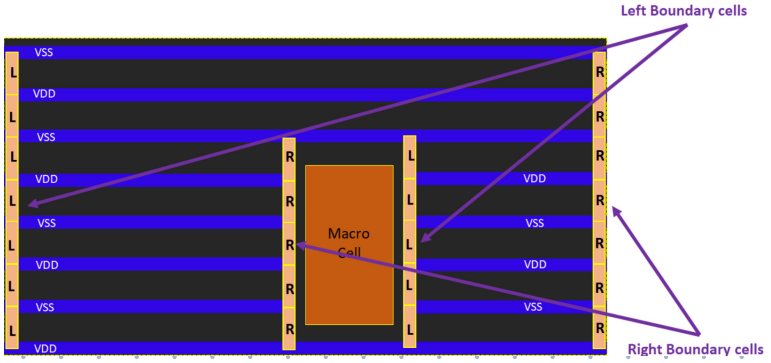


END CAP CELLS / BOUNDARY CELLS

- end cap cells ensure continuity of diffusion regions, wells or metal densities

Problems
- standard cells may have open diffusion (implantation) regions (source/drain regions) that may be floating at the edges → leakage
- processes like CMP require uniform densities (proportion of diffusion layer coverage per area) (also min/max density constraints must be met)
- routing of metal at the edge may have unintended parasitic effects
- uncapped edges introduce parasitics (C,R) that affect signal integrity

Solution: add an end cap cell to both ends of a cell row and around blocks



Random Number Expansion

Data Integrity: Checksum / Error Detection

512 bit not enough : Post Quantum Crypotography

LEF Geometry, Placement rules — NDR

LIB Timing, Voltage, Resistance