1 Signal naming conventions

Signal postfix	Description
_i	Input port
_o	Output port
_io	Bi-directional port
_clk_i	Clock input port
_clk_o	Clock output port
_rst_i	Reset input port
_rst_o	Reset output port

2 Directory structure

- `blockname` ..... Top level directory of a core
  - `backend` ..... Top level backend directory
    - `<vendor>` ..... Vendor specific floorplan, place and route directory structure
  - `sim` ..... Top level simulations directory
    - `rtl_sim` ..... RTL simulations
      - `bin RTL` ..... simulation scripts
      - `run For` ..... running RTL simulations
      - `src` ..... Special sources for RTL simulations
      - `out` ..... Dump and other useful output from RTL simulation
      - `log` ..... Log files
    - `gate_sim` ..... Gate-level simulations
      - `bin` ..... Gate-level simulation scripts
      - `run` ..... For running gate-level simulations
      - `src` ..... Special sources for gate-level simulations
      - `out` ... Dump and other useful output from gate-level simulation
      - `log` ..... Log files
  - `syn` ..... Synthesis
    - `<vendor>` ..... Each synthesis tool has separate directory
      - `bin` ..... For synthesis scripts
      - `run` ..... For running synthesis scripts
      - `src` ..... Special sources for synthesis
      - `out` ..... For generated netlists (Synopsys db, verilog)
      - `log` ..... Log files (including reports)
  - `rtl` ..... RTL sources (.vhd or .vhdl)
  - `bench` ..... Bench sources
  - `doc` ..... ut specification, design and other PDF documents here
  - `src` ..... Source version of all documents (Latex etc.)
  - `sw` ..... Put sources for utilities or software test cases