### 1 Introduction

This document contains the conventions used within all projects in this repository. Good conventions make following code easier and is thus considerd good practice. This document is mainly intended for personal use but may also be used by someone whom might want to build on some of these projects.

## 2 Signal naming conventions

Signal names must adhere to the following conventions:

#### Lower-case

All signal names should be in lower-case.

#### Descriptive

All signal names should be descriptive and its use must be clearly stated by its definition.

#### Prefix

Signals driven localy within the entity should be prefixed by a lower-case 'l'. All other signals except the inputs and outputs of the entity should be given a prefix unique to the module driving it.

#### Postfix

All inputs and outputs of an entity should be prefixed by 'i' and 'o' respectively. Special I/O's also needs an extra prefix as listed in Table 1.

Signal postfix	Description
_i	Input signals
_O	Output signals
_io	Bi-directional signals
_clk_i	Clock input signals
_clk_o	Clock output signals
_rst_i	Reset input signals
_rst_o	Reset output signals

Table 1: Signal postfixes

## 3 Directory structure

The directory structure used for the projects is based on the recommendations found in OpenCores' HDL modeling guidelines article.[1] This is the initial directory structure and may still be subject to small changes over time. Figure 1 shows the standard directory structure used for all projects.

blockname
_ <vendor> Vendor specific floorplan, place and route directory</vendor>
structure
sim
rtl_sim
bin RTL simulation scripts
run For running RTL simulations
srcSpecial sources for RTL simulations
outDump and other useful output from RTL simulation
logLog files
gate_sim
bin
run
srcSpecial sources for gate-level simulations
out Dump and other useful output from gate-level simulation
log
syn
<pre></pre>
bin
run For running synthesis scripts
src
out For generated netlists (Synopsys db, verilog)
log
rtl
bench
doc ut specification, design and other PDF documents here
src
swPut sources for utilities or software test cases

Figure 1: Directory structure

# References

[1] OpenCores HDL modeling guidelines.