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Question 1 (1 mark)

Report the number of pins and logic modules used to fit your design on the FPGA board

	Half-Adder	Full-Adder	4-bit Ripple Carry Adder	
	Structural	Structural	Structural	Behavioral
Logic Utilization (in ALMs)	2/32070	2/32070	4/32070	3/32070
Total pins	4	5	13	13

Question 2 (1 mark)

Give the VHDL code that you wrote to instantiate:

The half-adders in Part 3.2

```
s <= a xor b;
c <= a and b;
```

The full-adders in Part 3.3

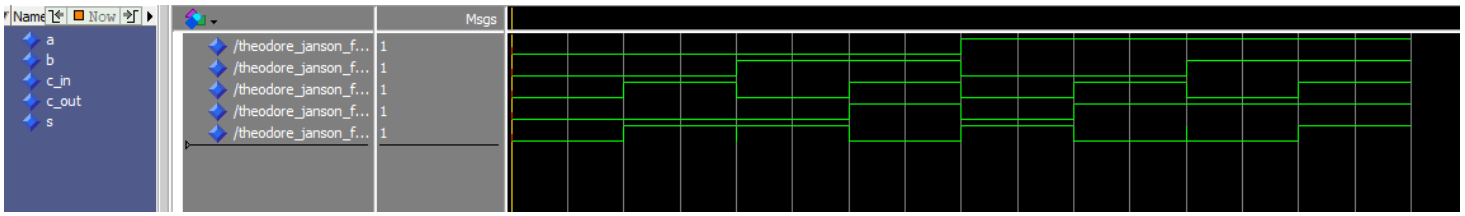
```
M1 :  Theodore_Janson_HALF_ADDER PORT MAP(a => a, b => b, s => wire0, c => wire1);
M2 :  Theodore_Janson_HALF_ADDER PORT MAP(a => wire0, b => c_in, s => s, c => wire2);
c_out <= wire1 or wire2;
```

Question 3 (1 mark)

Show representative simulation plots for the half-adder circuit for all the possible input values. You can simply include below a snapshot from the waveform that you obtained from ModelSim. In order to fully capture all the signals from the waveform, you can adjust the display range using the magnifier icons.

Question 4 (1 mark)

Show representative simulation plots for the full-adder circuit for all the possible input values. You can simply include below a snapshot from the waveform that you obtained from ModelSim. In order to fully capture all the signals from the waveform, you can adjust the display range using the magnifier icons.



Question 5 (1 mark)

Show representative simulation plots of *both the behavioral and structural* 4-bit ripple-carry adder descriptions for all the possible input values. You can simply include below snapshots from the waveform that you obtained from ModelSim. In order to fully capture all the signals from the waveform, you can adjust the display range using the magnifier icons.