Coding group #	21
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Question 1 (2 marks)

Give the VHDL code that you wrote for the clock divider.

What is the value of T that you used? T= 50000000

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity g21_clock_divider is
Port (
enable : in std_logic;
reset : in std_logic;
clk : in std_logic;
en_out : out std_logic
);
end g21_clock_divider;

architecture behavioral of g21_clock_divider is
signal T : integer := 50000000;
signal count: integer:= T-1;

BEGIN
process(clk, enable, reset)

BEGIN
if reset = '0' then
    en_out <= '0';
elsif enable = '1' then
    if rising_edge(clk) then
        if count = 0 then
            en_out <= '1';
            count <= 50000000-1;
    else
        en_out <= '0';
        count <= (count - 1);
    end if;
end if;
end if;
end process;
end behavioral;
```
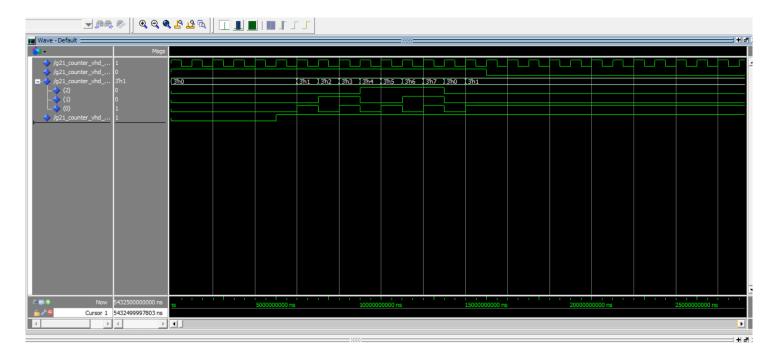
Question 2 (2 marks)

Give the VHDL code that you wrote for the 3-bit counter..

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity g21_counter is
Port ( enable : in std_logic;
reset : in std_logic;
clk : in std_logic;
count : out std_logic_vector(2 downto 0)
);

end g21_counter;

architecture behavioral of g21_counter is
signal temp : std_logic_vector(2 downto 0) := "000";

BEGIN
process(clk, enable, reset)

 BEGIN

if reset = '0' then
     count <= "000";
     temp <= "000";
elsif enable = '1' then
     if rising_edge(clk) then
          if temp = "111" then
          temp <= "000";
          count <= temp;
          else
          temp <= temp + "1";
          count <= temp;
          end if;
     end if;
end if;
end process;
end behavioral;
```

Question 3 (2 marks)

Show a representative simulation plot of your `gNN_counter` circuit. You can simply include a snapshot from the waveform that you obtained from ModelSim. In order to fully capture all the signals from the waveform, you can adjust the display range using the magnifier icons.