Isolated Three-Phase High Power Factor Rectifier Based on the SEPIC Converter Operating in Discontinuous Conduction Mode

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***Abstract* – This paper presents the analysis and design of a three-phase high power factor rectifier, based on the dc-dc SEPIC converter operating in discontinuous conduction mode, with output voltage regulation and high frequency isolation. The input high power factor is naturally attained through the operational mode without the use of current sensors and a current control loop. To validate the theoretical analysis, a design example and experimental results for a 4 kW, 380 V line-to-line input voltage, 400 V output voltage, 0.998 power factor, 40 kHz switching frequency and 4% input current THD laboratory prototype are presented, considering two distinct modulators. In addition, experimental results for the output voltage closed-loop control are presented.**

***Index Terms:* ac-dc converter, discontinuous conduction mode, power factor correction, SEPIC converter, three-phase rectifier.**

NOMENCLATURE

V_p	Peak value of line-to-neutral input voltage
V_o	Output voltage
f_s	Switching frequency
f_r	Main frequency
R_o	Load resistance
D	Duty cycle
C_o	Output capacitor
C_s	SEPIC capacitor
$V_{1,2,3}$	Input source voltage
T_r	Main period
T_s	Switching period
ϕ	Shifted angle
θ	Phase angle
P_o	Output power
P_i	Input power
$P_{3\phi}$	Three-phase input power
I_p	Peak value of line-to-neutral input current
G	Converter gain
ΔI_{Li}	Input current ripple
L_i	Input inductor
V_{tp}	Triangular carrier peak voltage
ε	Non-compensated error
ε_c	Compensated error
K_c	Compensator gain
ω_z	Compensator zero frequency
ω_p	Compensator pole frequency

I. INTRODUCTION

In 1997, a complete classification of three-phase rectifier topologies with low effect on the mains was presented [1], where the first division distinguished active and passive rectifiers. Some are purely passive topologies, such as the 12 and 18-pulse rectifiers with or without isolation [2], while others are hybrid structures [3, 4]. In the case of active structures the input current, output voltage or both are controlled, resulting in many other sub-divisions: direct three-phase systems or those composed of a combination of single-phase systems, with low or high-frequency isolation, unidirectional or bidirectional systems, single or multiple stage converters, and those related to continuous or discontinuous operational modes.

In summary, if only the structures that result in a unity power factor, low input current total harmonic distortion (THD), controlled output voltage and isolation from the mains are considered, three criteria may be highlighted: number of stages, isolation and control strategy.

In relation to the number of stages, systems with two or more stages are commonly found, where the first stage is responsible for the rectification and the power factor (PF) correction and the second for the isolation and output voltage regulation.

Even with the individual efficiency of each block being high, the global efficiency of this kind of structure is generally low. Thus, in the search for better efficiency, the application of structures that accomplish all the energy processing in a single-stage is an interesting approach.

In relation to the isolation, some aspects must be considered: the first relates to the increased loss in isolated converters and, thus, this kind of application must be as efficient as possible. This feature is obtained through the use of high-frequency rather than low-frequency transformers, leading to the second aspect which is related to the structure volume reduction, also achieved through the use of high-frequency isolation.

In the case of the three-phase rectifier structure control, usually applied for power factor correction (PFC), is generally complex and involves the monitoring of input currents and complicated control loops. Besides the input current control, the output voltage must be stable even with load changes, adding another control loop to the system. Thus, the employment of simpler control loops and a reduced number of sensors provide several structural advantageous, when cost and reliability are considered.

In this context, this paper presents a single-stage three-phase rectifier with high-frequency isolation and output voltage control, based on the SEPIC dc-dc converter operating in discontinuous conduction mode (DCM), which provides a PF close to unity and low THD, without the use of any current sensors or a current control loop.

II. PROPOSED SYSTEM

In order to generate the proposed topology, the basic dc-dc SEPIC converter, shown in Fig. 1 (a), was initially modified to

operate as a single-phase isolated rectifier, similarly to the boost and other rectifiers [5-7], as can be observed in Fig. 1 (b). From the last stage, it is possible to obtain sinusoidal input currents, using an appropriate current control [8], or operating the SEPIC converter in DCM [9-11].

The single-stage structure may be replicated for each phase of a three-phase three-wire system, resulting in a circuit in which each output stage can be connected in series or in parallel. The three-phase structure presented in this paper is composed of parallel connection, a technique commonly employed, as discussed in [12, 13]. The resulting topology, with the inductors allocated on the ac side, is shown in Fig. 1(c).

Three-phase topologies with analog power stage structures are presented in [14-18]. However, these topologies operate in the continuous conduction mode (CCM) and, therefore, an input current control loop is required.

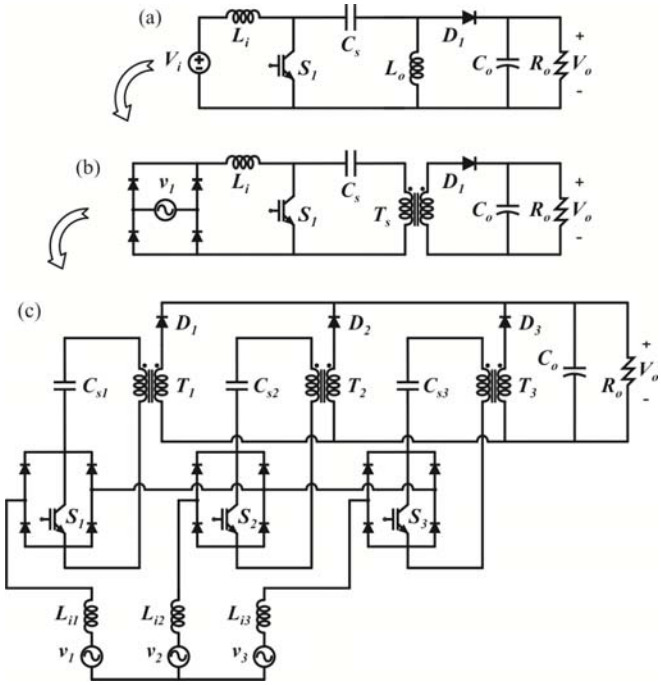

Fig. 1 – (a) Non-isolated dc-dc SEPIC; (b) SEPIC-based, isolated, unity power factor single-stage rectifier; (c) Proposed three-phase rectifier structure power stage.

From the power electronics point of view, a converter is defined by the power stage along with its modulator. Therefore, for the power converter presented herein, two PWM modulators are proposed. The first one is that in which all the switches are gated simultaneously (conventional modulator). In the second one a 120º delay between the gate pulses is employed (phase-shift modulator). The mathematical results presented in this paper were obtained considering the converter employing the conventional modulator, although experimental results for both modulators are presented.

III. Principle of Operation and Analysis

The SEPIC DCM operation is defined by the current discontinuity on the output diode, when the switch is blocked. Therefore, in addition to the two operation stages of the SEPIC dc-dc converter operating in CCM there is a third stage, before the switch conduction, for which the output diode current is null.

When this operation mode is ensured, the converter is able to emulate a resistance, naturally providing a sinusoidal input current in phase with the input voltage. As a result, only a simple control loop is needed to control the system output voltage.

In the three-phase system, the DCM is characterized by the same criteria. Thus, to obtain the converter operation in this mode, it is necessary to ensure discontinuous currents across the three output diodes.

In order to perform a simplified mathematical analysis, the three-phase power stage proposed in Fig. 1 (c) is redrawn according to Fig. 2 (a), where the isolation and the output connections have been removed, but the relation given by (1) must be maintained. Additionally, the conventions adopted for voltages and currents are also illustrated in Fig. 2 (a).

$$\begin{cases} V_o = V_{o1} = V_{o2} = V_{o3} \\ i_o = i_{o1} + i_{o2} + i_{o3} \end{cases} \tag{1}$$

The three-phase input voltages are sinusoidal, as can be seen in Fig. 3 (a); however, due to the symmetry, the system presents the same behavior for each sector of 30º. Therefore, in order to reduce the mathematical complexity, it is possible to analyze the system only for one sector and expand it to a whole main grid period.

In the case of the fifth sector (Fig. 3 (a)), for instance, the input voltages are featured in the relations expressed by (2). In this situation, any dc-dc voltage source, respecting the relations in (2), may be adopted to represent the system operation in this sector.

$$\begin{cases} |V_3| > |V_1| > |V_2| \\ V_1 > 0 \quad V_2 > 0 \quad V_3 < 0 \end{cases} \tag{2}$$

Considering that the controlled switches are simultaneously commanded, and the system is operating in DCM, for a proper operation, besides (2), the input inductances need to be higher than the output ones, as described in (3). Furthermore, the instantaneous voltage across each SEPIC capacitor is assumed to be equal to the respective input rectified voltage, according to (4) and, due to the constructive symmetry, the relations in (5) are also valid.

$$\begin{cases} L_{i1} >> L_{o1} \\ L_{i2} >> L_{o2} \\ L_{i3} >> L_{o3} \end{cases} \tag{3}$$

$$\begin{cases} V_{Cs1} = |V_1| \\ V_{Cs2} = |V_2| \\ V_{Cs3} = |V_3| \end{cases} \tag{4}$$

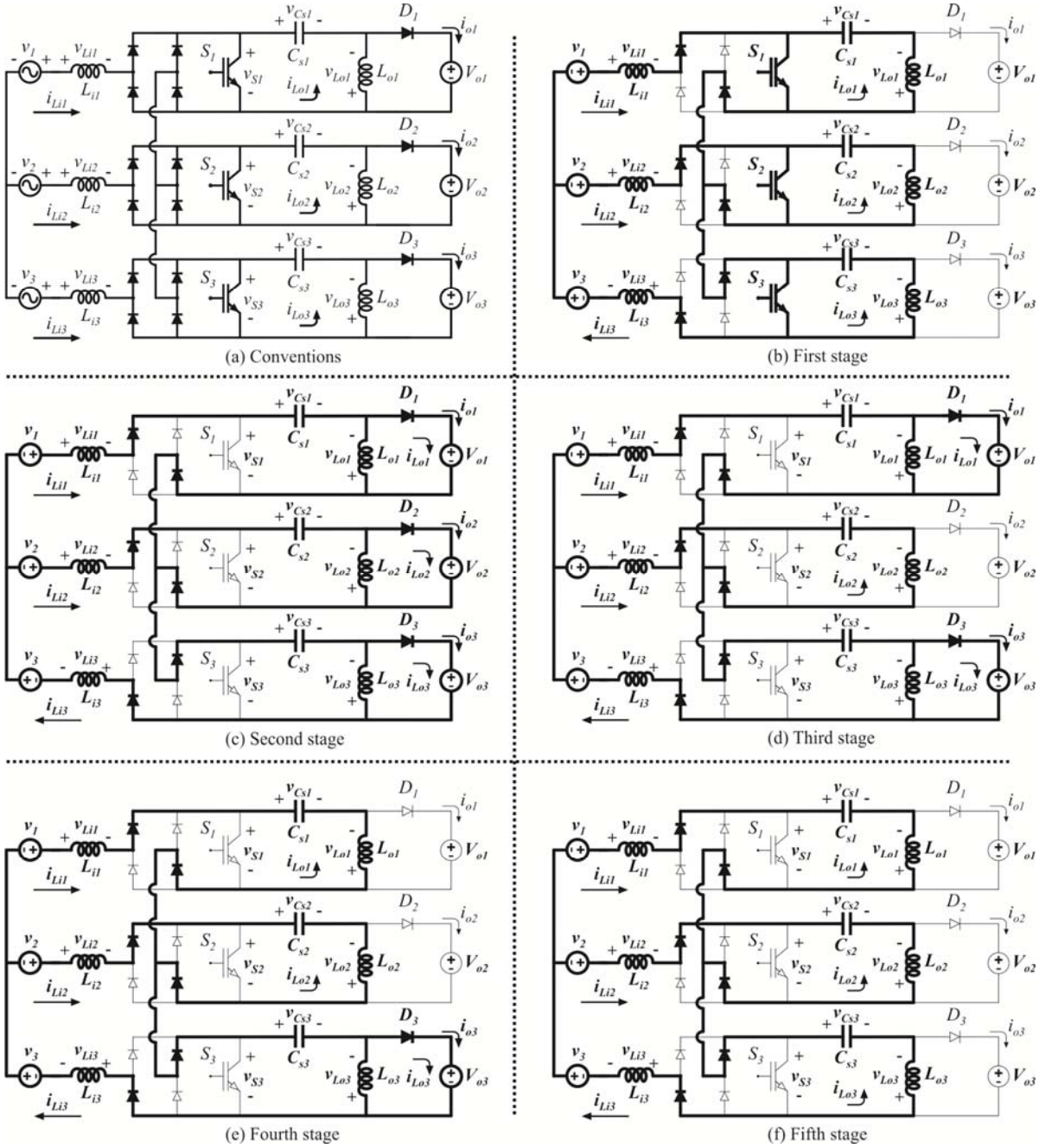

Fig. 2 – Conventions and operation stages for one sector analysis.

$$\begin{cases} L_{i1} = L_{i2} = L_{i3} = L_i \\ L_{o1} = L_{o2} = L_{o3} = L_o \\ C_{s1} = C_{s2} = C_{s3} = C_s \end{cases} \quad (5)$$

From the switching frequency point of view, five distinct operation stages are identified, as illustrated Fig. 3 (b). The first stage begins when the three switches are commanded to conduct. Under this condition, the output diodes are blocked and energy is stored in the input inductors, while the SEPIC capacitors transfer energy to the output inductors. This operating stage is highlighted in Fig. 2 (b).

The second stage starts when the three switches are commanded to block (time t_1), leading to conduction by the three output diodes, as described in Fig. 2 (c). During this stage the energy stored in the output inductors is transferred to the system output. On the other hand, the energy stored in the input inductors is simultaneously transferred to the system output and SEPIC capacitors.

Since the input voltage levels differ from one other, the energy levels stored in the respective elements are also distinct and therefore the currents across the output diodes become null at different time instants. For instance, for the sector under analysis, the lowest input voltage is V_2 and thus the diode D_2 is the first to be blocked, exactly at the moment at which the currents in the input and output inductors (i_{Li2} and i_{Lo2}) assume the same value, but in an opposite way,

configuring the third stage, as shown in Fig. 2 (d).

The third stage remains until the next output diode blocks. At this instant, the fourth stage is accomplished. For the sector in question, once $V_1<V_3$, the fourth stage begins when D_1 is blocked, in accordance with Fig 2 (e).

Finally, the last stage is established when D_3 is blocked, as shown in Fig. 2 (f). Note that the DCM may also be characterized by this stage, because the three diodes are blocked, when $i_{Li}+i_{Lo}=0$, and there is no power transfer for the system output.

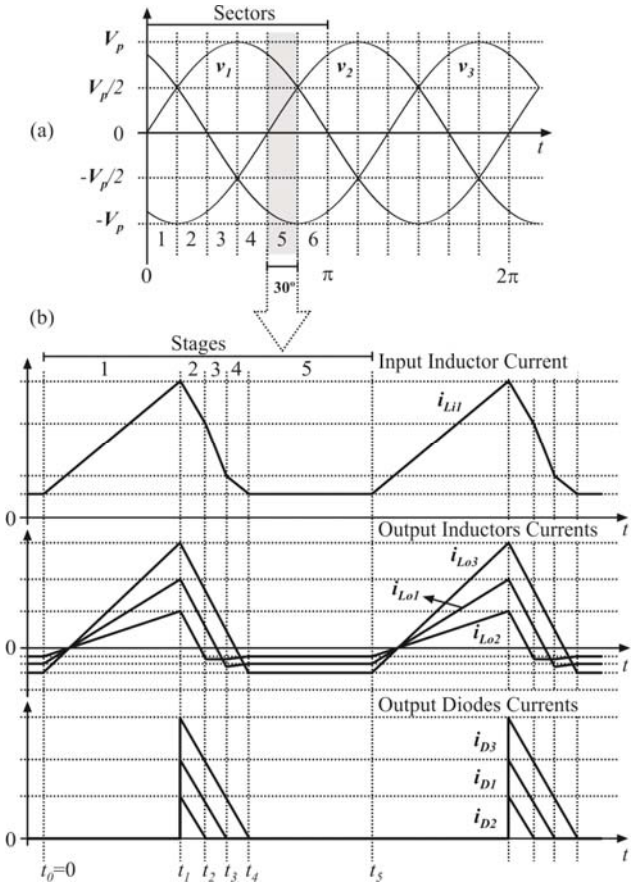

Fig. 3 – Three-phase converter operation stage analysis: (a) input voltages; (b) main waveforms from the high frequency point of view.

A. Mathematical Analysis

From the description of the operation stages it is possible to obtain the equivalent circuits whose analysis results in a linear system that, when solved, provides the system solution. The interaction of the system phases can be observed from the input current waveform, Fig. 3 (b), in which, in contrast to a single-phase converter, there is a behavioral change in the input current, between the active switch turn-off and subsequent turn-on, evidenced by stages 2 through 5.

The three-phase system was mathematically solved considering the complete system, and the important results are those related to the average values reported herein.

The average value for the output current is given by (6). This expression confirms that the three-phase system is equivalent to three single-phase systems connected in parallel. The parameter L_{eq} results from the parallel association of the input and output inductances, (7).

The parameterized average output current expression, considering the transformer turns ratio, n, is given by (8) and the average output voltage is given by (9). The load characteristic is a function of the static gain and the parameterized output current, given by expression (10), and it is shown in Fig. 4, where the duty cycle limit, D_{lim}, between CCM and DCM is defined by equation (11). Through the application of (6) it is possible to derive an expression for the output power. In addition, considering the system operating with unitary efficiency, the input power is equal to the output power, according to (12). Equation (12) also shows the advantage referred to the three-phase system employment, since the input power is constant.

$$I_o = \frac{3}{4}\frac{V_p^2 D^2}{V_o f_s L_{eq}} \tag{6}$$

$$L_{eq} = \frac{L_i L_o}{L_i + L_o} \tag{7}$$

$$\overline{I_o} = D^2 \frac{V_p}{V_o n} \tag{8}$$

$$V_o = V_p D \sqrt{\frac{3R_o}{4 f_s L_{eq}}} \tag{9}$$

$$G = \frac{D^2}{\overline{I_o}} \tag{10}$$

$$D_{lim} < \frac{G}{(1+G)} \tag{11}$$

$$P_o = P_i = P_{3\phi} = \frac{3}{2} V_p I_p = \frac{3}{4}\frac{V_p^2 D^2}{f_s L_{eq}} \tag{12}$$

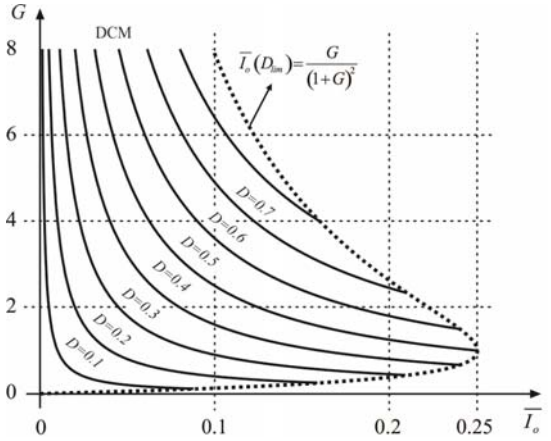

Fig. 4 – Load characteristic: static gain as a function of the parameterized average output current.

Simplifying (12) and taking into account that the voltage grid for any phase is given by (13), an equation for the input current can be obtained, according to (14), where the equivalent resistance R_{eq} is defined by (15).

$$v(\theta) = V_p \, sin(\theta) \tag{13}$$

$$i(\theta) = I_p \, sin(\theta) = \frac{v(\theta)}{R_{eq}} \tag{14}$$

$$R_{eq} = \frac{D^2}{2 f_s L_{eq}} \tag{15}$$

The relation given by (14) is crucial for proceeding to the system analysis, since it emphasizes the SEPIC behavior as a resistance, from the main grid point of view, leading to a high power factor, even with the system operating without a closed control loop for input currents.

B. Influence of the modulation-type

As previously noted, the classical modulator is considered in all of the above descriptions. Under this condition, the complete system is characterized by the waveforms shown in Fig. 5 (a), from which it can be noted that the input current and voltage (depicted only for one phase) are sinusoidal and in phase with one other. Additionally, it is observed that the voltage across the SEPIC capacitor follows the input voltage, confirming the supposition of (4).

A second alternative is to employ a modulator, from where the switches are commuted with a 120º phase shift. Consequently, as detailed in Fig. 5 (b), the input current ripple, for the same inductance value, is reduced and presents a minor current waveform distortion in the zero crossing.

There are no significant changes in the high-frequency operation on comparing the two modulators, but the number of operation stages is increased in the second one, resulting in a more complicated mathematical analysis. The component stresses are similar, but now there is an advantage associated with the output current. Due to the shift of the module operation, the currents of the output diodes are also shifted, implying that their peaks do not appear together, as observed in Fig. 5 (c), reducing the current stresses on the output capacitor.

IV. Design Criteria and Control Strategy

From the curves presented in Fig. 4, for a certain design specification, it is possible to obtain the critical parameters of the converter which ensure its operation in the desired mode.

Thus, once the system solution is known, the current and voltage levels, for the entire system, can be obtained analytically or by simulation, and the proposed converter design may be developed.

The main aspects regarding the converter design are related to the SEPIC capacitor selection. The capacitors must be designed in order to present a low high-frequency voltage ripple, but they must also reproduce the rectified input voltages, resulting in the expected structure operation. The output capacitor was designed to meet effective current and hold-up time criteria.

Due to the fact that the proposed structure is isolated, the transformer leakage inductances must be minimized, with the purpose of reducing, or even avoiding, the use of dissipative or non-dissipative snubbers/clampers in the switch.

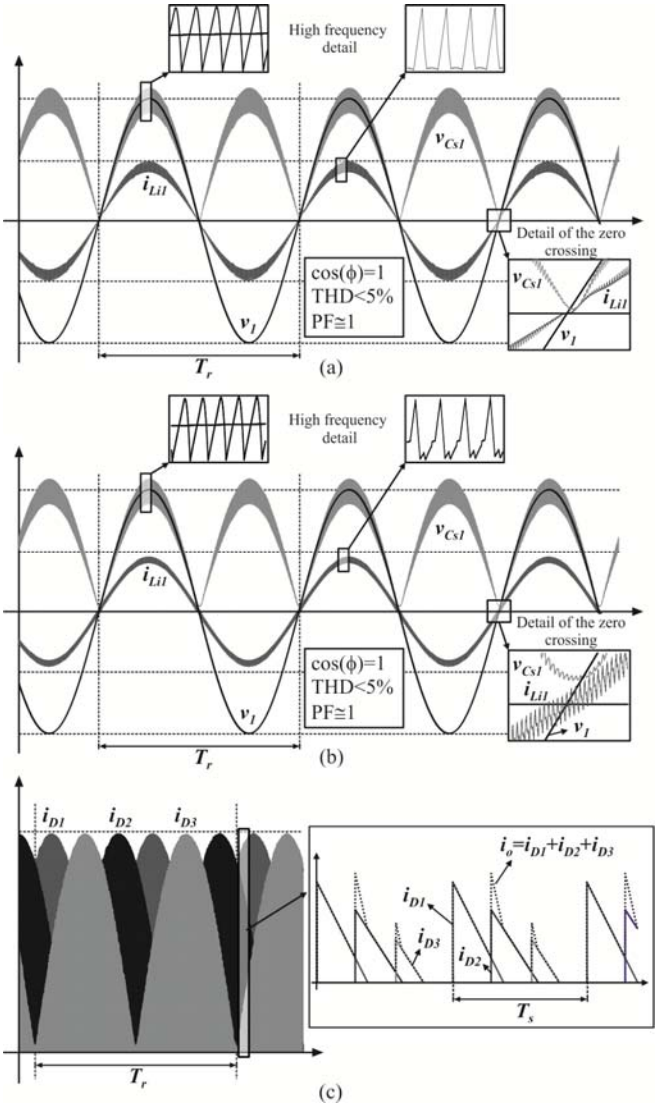

Fig. 5 – Input current, input voltage and SEPIC capacitor voltage with conventional modulator (a) and with phase-shift modulator (b). (c) Currents of the output diodes and high frequency (in detail) with phase-shift modulator.

The maximum ripple input current value is defined by the input inductance, according to (16).

$$\Delta I_{Li\,max} = \frac{V_p D}{L_i f_s} \tag{16}$$

The output voltage control is achieved by the use of a simple controller, which requires minimal effort for its design, since the output voltage behavior for duty-cycle perturbations may be modeled by a first-order response. The block diagram for the proposed control strategy is presented in Fig. 6.

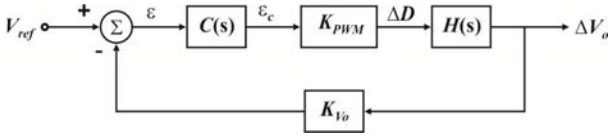

Fig. 6 – Block diagram of the proposed control strategy.

The output voltage transfer function model is obtained from the small signal average model. The equivalent simplified circuit employed to obtain the system transfer function is shown in Fig. 7, resulting in (17), where the constant K is defined by (18).

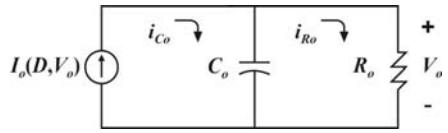

Fig. 7 – Equivalent circuit for output voltage transfer function modeling.

The additional blocks from the block diagram refer to the PWM modulator (K_{PWM}) and proportional-integral with filter compensator ($C(s)$) described, respectively, by (19) and (20). The voltage sensor gain block (K_{Vo}) refers to a constant gain defined by the designer.

$$H(s)=\frac{\Delta V_o(s)}{\Delta D(s)}=\frac{2K}{1+\frac{KD}{V_o}+R_oC_os} \tag{17}$$

$$K=\frac{3}{4}\frac{V_p^2DR_o}{nV_of_sL_{eq}} \tag{18}$$

$$K_{PWM}=\frac{1}{V_{tp}} \tag{19}$$

$$C(s)=K_c\frac{(s+\omega_z)}{s(s+\omega_p)} \tag{20}$$

V. Experimental Results

In order to confirm the operating principle of the proposed converter and validate the analysis results, a laboratory prototype was designed and built, with the specifications given in Table I. In Fig. 8, the complete power stage schematic, including the clamping circuit, is detailed. The results of the design are presented in Table II and Table III. A photograph of the implemented laboratory prototype is shown in Fig. 9.

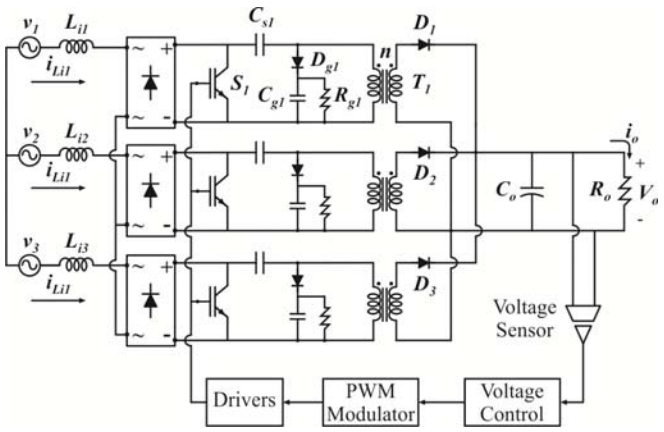

Fig. 8 – Simplified diagram of the proposed three-phase rectifier, including dissipative clamping circuit and control blocks.

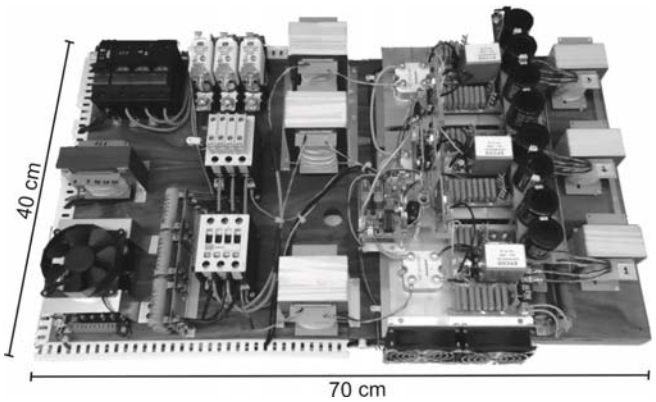

Fig. 9 – Photo of the 4 kW three-phase SEPIC rectifier prototype.

TABLE I
Specifications

Rated power	4 kW
dc-bus voltage	400 V
Switching frequency	40 kHz
ac input source peak voltage	311 V
ac source line frequency	60 Hz

TABLE II
Design Parameters

Power Stage	
Designed duty cycle (D_{max})	0.523
Duty cycle at rated power (D)	0.459
Input inductances ($L_{i(1-3)}$)	3.631 mH
Output inductances ($L_{o(1-3)}$)	97.72 µH
SEPIC capacitances ($C_{s(1-3)}$)	1.5 µF (320 V / 9 A*)
Switch stresses ($S_{(1-3)}$)	650 V / 40 A (peak)
Output diode stresses ($D_{(1-3)}$)	850 V / 30 A (peak)
Bridge diode stresses ($D_{b(1-3)(a-d)}$)	650 V / 12 A (peak)
Output capacitance (C_o)	2000 µF (450 V / 15 A*)
Clamper capacitances ($C_{q(1-3)}$)	500 nF (850 V / 1 A*)
Clamper resistances ($R_{g(1-3)}$)	10 kΩ
Clamper diode stresses ($D_{q(1-3)}$)	1000 V / 40 A (peak)
* Values in rms	
Transformer	
Turns ratio (n)	0.776
Primary number of turns (N_p)	24
Secondary number of turns (N_s)	31
Measurement leakage inductance (L_d)	1 µH
Gap (l_{Lo})	3 mm
Inductor	
Number of turns (N_{Li})	111
Gap (l_{Li})	2.75 mm

TABLE III
Main Components List

Switches	IGW40N120H3
SEPIC capacitors	B32656-S0155-K501
Output diodes	STTH9012TV1
Clamper diodes	MUR5150E
Input bridge rectifiers	SKB 30/12A1
Drivers	SKHI 10op
PWM modulator	DSPIC30F2020

In Fig 10, relevant voltage and current waveforms are shown, for rated power and voltages, which are in agreement with the expected results. It can be observed that the maximum voltage across the active power switch is equal to the sum of the line-to-neutral input peak voltage and the load voltage referred to the transformer primary side. The currents on the semiconductors and, consequently, the conduction

power loss are increased because the converter operates in DCM and this is the major downside of the topology.

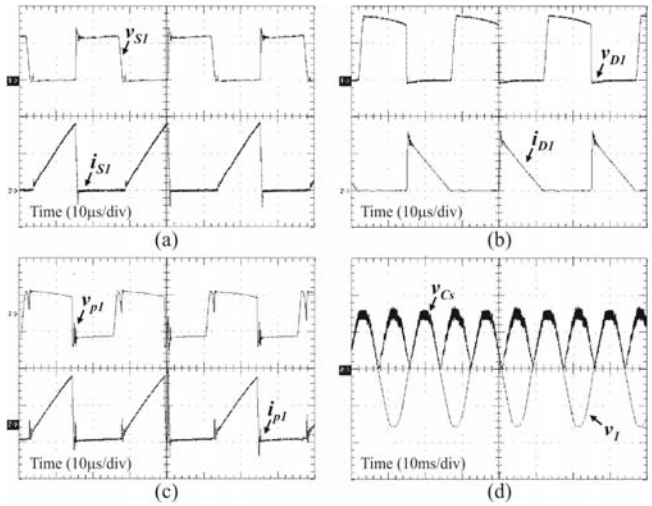

Fig. 10 – Experimental waveforms: (a) switch voltage (500V/div) and current (20A/div); (b) output diode voltage (500V/div) and current (20A/div); (c) transformer primary-side voltage (500V/div) and current (20A/div); (d) SEPIC capacitor voltage (200V/div) and input phase voltage (200V/div).

Figure 11 (a) shows the output current before the filter, along with the currents through the output diodes, for the conventional modulator. The peak currents of the diodes appear simultaneously, as expected. Figure 11(b) shows the same currents, for the modulator with phase-shift. These waveforms confirm the DCM operation since the currents of the output diodes reach zero before the next switching period.

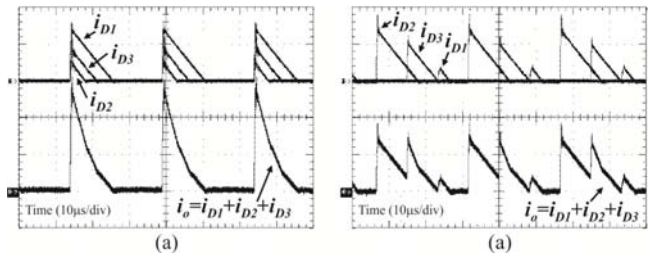

Fig. 11 – Experimental diode and output currents (20A/div) for (a) the classical and (b) the phase-shift modulators.

The main contribution of the phase-shift modulator is the reduction of the output capacitor current stress, without affecting the average current.

The converter input current waveforms and harmonic spectrum are presented in Fig. 12, demonstrating that it operates with low harmonic distortion (4%) and a unity power factor.

Figure 13 shows the converter response with closed loop voltage control, when submitted to a load step change from 50% to 100% of the rated load, showing a satisfactory behavior. The compensator designing criteria were developed for allowing voltage loop bandwidth of 133 Hz, since there is no oscillation around 120 Hz, as it occurs on single-phase systems.

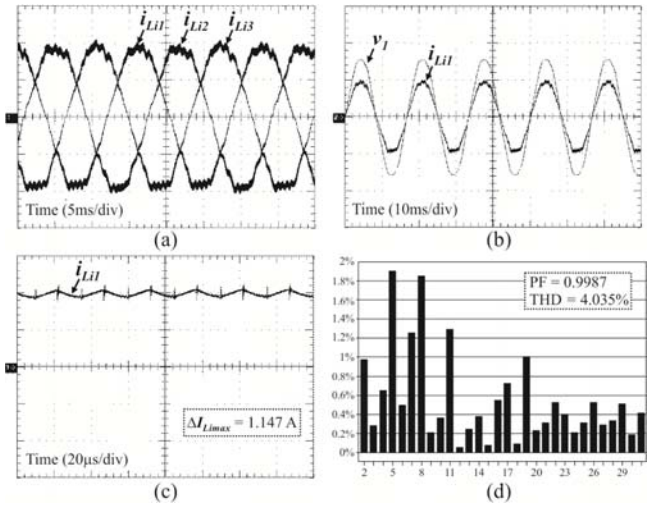

Fig. 12 – Experimental waveforms: (a) input current for each phase (5A/div); (b) input voltage (200V/div) and input current (10A/div) for one phase; (c) maximum input current ripple in detail; (d) input current harmonic spectrum.

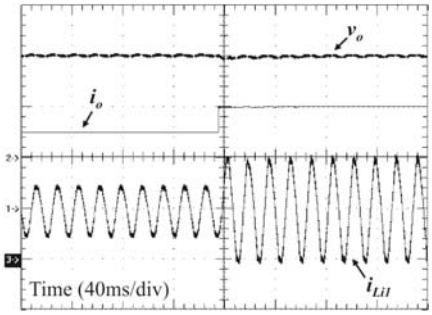

Fig. 13 – Experimental waveforms for load disturbance from 50% to 100% of the rated power, with closed loop voltage control: output voltage (100V/div), output current (10A/div) and input inductor current (10A/div).

The measured efficiency curve of the non-optimized laboratory prototype, designed and built only for concept proof purposes, is shown in Fig. 14. The efficiency is 90% for the rated power operation. It is possible to improve the converter efficiency by employing better magnetic material, low conduction loss power semiconductors and regenerative clamping or snubber circuits.

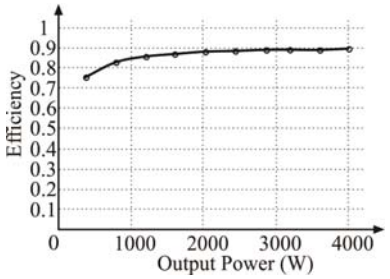

Fig. 14 – Measured efficiency curve.

VI. Conclusions

In this paper a three-phase isolated high power factor rectifier topology based on the SEPIC dc-dc converter operating in the DCM was presented. Theoretical analysis was detailed, summarizing the converter operation.

Experimental results confirmed that the proposed topology

operates with input sinusoidal currents, without current sensors or a control loop strategy for this purpose, leading to a cost reduction, simplicity and robustness.

A second advantage comes from the use of a simple control loop to regulate the output voltage, as verified from the experimental results, obtained using two distinct modulators.

There are many possible applications for the proposed converter, including in telecommunications and battery chargers.

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