High Voltage Gain Boost Converter Based on Three-State Commutation Cell for Battery Charging Using PV Panels in a Single Conversion Stage

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Abstract—**This paper presents a novel high voltage gain boost converter topology based on the three-state commutation cell for battery charging using PV panels and a reduced number of conversion stages. The presented converter operates in zero voltage switching (ZVS) mode for all switches. By using the new concept of single-stage approaches, the converter can generate a DC bus with a battery bank or a photovoltaic (PV) panel array, allowing the simultaneous charge of the batteries according to the radiation level. The operation principle, design specifications, and experimental results from a 500-W prototype are presented in order to validate the proposed structure.**

Index Terms **– DC-DC power conversion, Photovoltaic power systems, Battery chargers.**

I. INTRODUCTION

The increasing use of renewable energy in applications regarding distributed generation systems such as photovoltaic panels, fuel cells, and wind turbines leads power electronics researchers to new challenges.

In this kind of application, one of the major concerns is the need of a high output DC voltage bus (from 200 to 400 Vdc), which is necessary to supply inverters, UPS, etc., from low input voltage levels. This issue has lead to the conception new several converter topologies. Nowadays, non-isolated DC-DC converters with high voltage gain have been highlighted in different applications.

The traditional high-frequency isolated converters typically required a transformer responsible for processing the total rated paper, with consequent increase of size, weight, and volume and reduction of efficiency. Converters with switched capacitors develop significant current peaks which limit the efficiency and the maximum processed power. A study on energy-efficiency of switched-capacitor converters was present by [1] the authors presented some design rules useful for developing high-efficiency switched-capacitor converters, based on their analysis. In [2] was presented several modular converter topologies based on a switched-capacitor cell concept, a soft-switched scheme was used in order to reduce the switching loss and electromagnetic interference.

In [3], a survey of high step up DC-DC converters based on coupled inductors and multiplier cells are presented and the major challenges were summarized. Some topologies employ coupled inductors, with consequently reduce the voltage stress across the switches, although the input current is discontinuous and the use of an LC filter may be necessary. A voltage doubler rectifier as the output stage of an interleaved boost converter with coupled inductors was present in [4]. The obtained voltage gain is twice that of traditional boost converters due to the doubler stage, as coupled inductors provide additional voltage gain, although voltage stress across the switches is not increased. In [5] was described a cascade high step-up DC-DC converter based on quadratic boost converter with coupled inductor in the second boos converter. A study of a topology based on two for-switch bridges around a LC circuit that does not utilize iron core transformers applied in megawatt level power transfers was present in [6]. In [7] the authors described a high step-up ZVT interleaved boost converter applied to grid-connected PV power system. This interleaved boost converter use an active-clamp circuit as the first power processing stage, which can boost a low voltage from PV array up to the high DC bus. A topology using the boost converter output terminal and flyback converter output terminal serially connected to increase the output voltage gain with the coupled inductor was presented in [8]. A family of high-efficiency, high step-up DC–DC converters with simple topologies was proposed in [9]. The proposed converters, use diodes and coupled windings instead of active switches to realize functions similar to those of active clamps, perform better than their active-clamp counterparts. The topology introduced in [10] consists in an interleaved boost converter, where the inductor current ripple and the current stress through the main switches are reduced. Besides, reduction of volume, size and weight is expected because the inductors are designed for twice the switching frequency. The converter presented in [11] uses voltage multiplier cells that allow high voltage step-up with reduced stress regarding the semiconductor elements. The interleaved configuration allows the very reduction of the input inductors and the output capacitors, at the cost of high component count as additional multiplier cells are includes. A similar topology based on the three-state commutation cell was proposed in [12][13], where the current sharing problem of the interleaved converter can be eliminated. The converter shown in [14] presents low input current ripple and uses an autotransformer with is designed for part of the rated power, while it is possible to achieve high voltage gain with reduced voltage stress across the switch. However, the use of such converter is limited to duty cycle value higher than 0.5.

Summarizing, the aforementioned topologies employ such techniques: the use of high frequency transformers, coupled inductors associated with voltage multiplier cells or switched capacitors.

Although the development of novel topologies with wide conversion ratio and high efficiency is necessary, their interconnection with photovoltaic panels (PV), battery banks, and the inverters DC link has a great interest for both industry and academy.

Within this context, the use of single stage converters, as presented by [15][16][17][18], they employ a single stage topology to achieve both voltage step-up and DC-AC capabilities. However, in this kind of technique, the semiconductors deal with high voltage and current stresses, as result in low efficiency.

Therefore, the interconnection among photovoltaic panels (PV), battery banks, and the inverters' DC link is usually achieved by using two or more DC-DC converters [19][20]. Nevertheless in this architecture, the energy flows through many conversion stages [21]. The proposed architecture allows such interconnection in a single stage which was introduced by [21].

This paper deals a single stage soft switching non-isolated DC-DC converter interconnecting battery charger, photovoltaic panels, and a high gain boost converter. The proposed topology aims to reduce the number of conversion stages, thus increasing the converter efficiency and simplifying the control system.

II. PROPOSED TOPOLOGY

A. CONCEPTION OF THE TOPOLOGY

In the low voltage side, the bidirectional characteristic of the topology allows the MOSFET bridge to be supplied by either the battery or the PV array. Besides, the use of resonant capacitors in the full-bridge capacitors provides zero voltage switching (ZVS) of the switches. The integrated topology resulting from the boost converter and the three-state switching cell is shown in Fig. 1. The main advantage of this topology is the low voltage stress across the active switches, low input current ripple, and simplicity, what results in higher efficiency.

Some high voltage gain topologies are supposed to contain three dc links as shown in Fig. 2, where VDC3 feeds the inverter with a higher voltage than that of the remaining ones. According to the proposal, the battery bank and the photovoltaic panel can be connected to the low voltage side at VDC1 or VDC2, depending on the available voltage levels. Considering typical applications under 2 kW, battery bank voltage levels can be 12 V, 24 V, or 48V (in order to avoid the connection of many units in series) and photovoltaic panels can be arranged to establish a dc link with voltage level equal to about twice that of the former link.

The proposed topology is formed by one input inductor L_{IN}, four controlled power switches S1-S4, two rectifier diodes D1 and D2, two transformers T1 (windings T1a and T1b) and T2 (windings T2a, T2b, T2c and T2d) and four output capacitors C1-C4. Even though additional components are included, current sharing is maintained between (S1, S2, T1a, T2a) and (S3, S4, T1b, T2c). Then, besides the reduced current stress through the components, the instantaneous current during the turn off of the switches is significantly reduced for D>50%, thus leading to minimized switching losses. Also, the transformer is designed for about only 70% of the total output power. Within this context, it must be considered that there is no energy transfer from the input to the output during the 2nd and 5th stages only. As a consequence, high efficiency is expected.

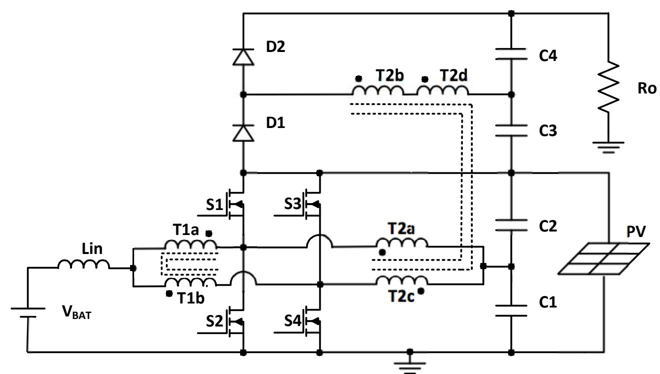

Figure 1. Proposed topology using a PV array.

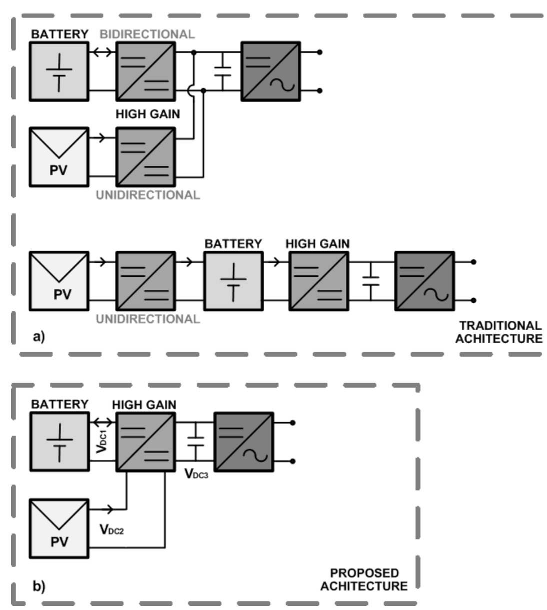

Figure 2. a) Conventional Architecture b) Proposed Architecture

B. *OPERATION PRINCIPLE*

The proposed converter has two operation regions, which work analogously. The duty cycle is applied to the lower switches of each leg (S2 and S4), which operate in opposite phase. The converter behavior and the operation region are defined by the applied duty cycle. If the duty cycle is higher than 50%, the lower switches work in overlapping mode. However, if the duty cycle is lower than 50%, then only the upper switches are in overlapping mode. As the operation principle regarding the switches is analogous, only the case for D>50% is presented.

The converter presents six operation stages, while Figure 2 presents the theoretical waveforms. As it can be observed, the current through the input inductor has a frequency which is twice higher than the switching frequency, which characterizes the three-state commutation cell behavior. This current is then equally shared between the windings of the autotransformers, which leads to reduced current stresses. The windings T2a and T2c correspond to the transformer primary side, which are responsible for stepping the voltage up and allowing the switches to operate in ZVS mode, increasing the system efficiency.

First Stage [$t_0 – t_1$] - This stage begins when S1 is turned off, causing a current flow through the anti-parallel diode of switch S2, allowing the turn on in ZVS mode. At this moment, S3 is turned off, and S4 is turned on. The current flowing through the input inductor 'I_{IN}' increases linearly and is equally divided between the two switching cells, reducing the associated stresses of the active semiconductors. The current in the primary side T2a decreases linearly, while the current through T2c increases linearly. This stage ends when the currents in T2a and T2c reach zero, and the current through S2 is equal to that through S4.

Second Stage [$t_1 – t_2$] – Current 'I_{IN}' still increases linearly and is equally divided through the commutation cells. Additionally, all the rectifier diodes are reverse biased. The current through T2a and T2c remains null. This stage ends when S4 is turned off.

Third Stage [$t_2 – t_3$] – This stage begins when S4 is turned off, causing the current to flow through the anti-parallel diode of S3, allowing the turn on in ZVS mode. At this moment, S2 is already turned on. The current flowing through the input inductor 'I_{IN}' decreases linearly, while the currents through T1a and T1b increase and decrease linearly, respectively. The current in the primary side T2a decreases linearly, while the current through T2c increases linearly. This stage ends when S4 is turned on and S3 is turned off.

Fourth Stage [$t_3 – t_4$] – This stage begins when S4 is turned on. When S2 is turned on, the input current 'I_{IN}' increases linearly, and so do the currents through T1a and T1b. Also, the current through S4 increases and has flows in the opposite direction. The current through T2a linearly increases, while the one through T2c decreases. This stage ends when the currents in T2a and T2c reach zero, and the current through S2 is equal to the one in S4.

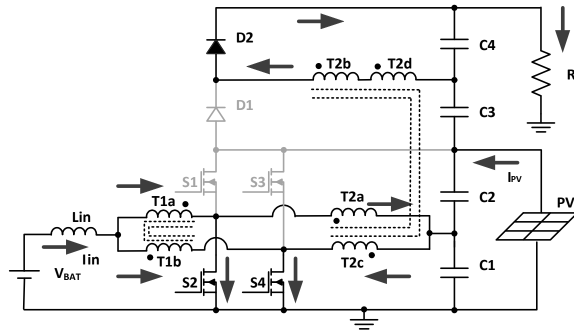

Figure 3. First Stage.

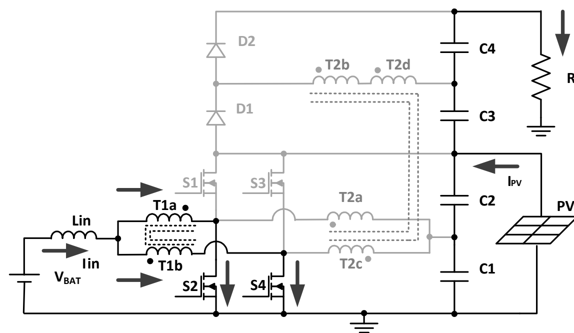

Figure 4. Second Stage.

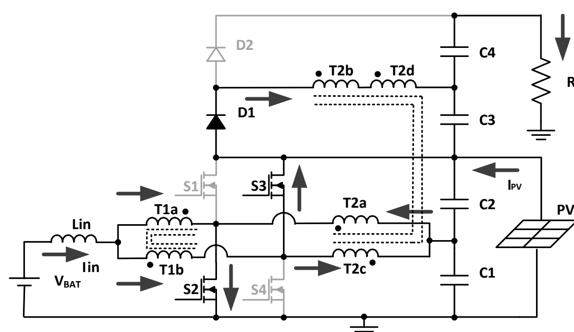

Figure 5. Third Stage.

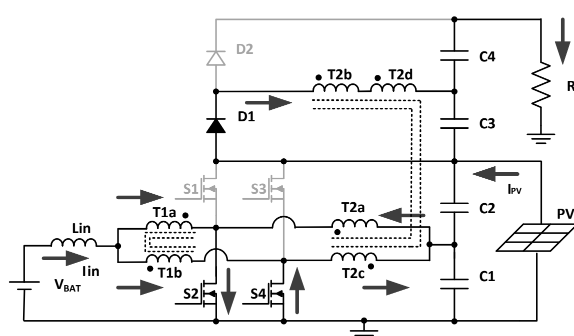

Figure 6. Fourth Stage.

Fifth Stage [t_4 – t_5] – This stage is similar to the second one. In this stage, 'I_{IN}' is still increases linearly and is equally divided between the commutation cells. Besides, all the rectifier diodes are reverse biased. The current through T2a and T2c remain null. This stage ends when S2 is turned off.

Sixth Stage [t_5 – t_6] – This stage begins when S2 is turned off, causing a current flow through the anti-parallel diode of S1, allowing its turn on in ZVS mode. At this moment, S3 is already turned off and S4 is turned on. The current flowing through the input inductor 'I_{IN}' decreases linearly. The current in the primary side T2a increases linearly, while the current through T2c decreases linearly. This stage ends when the currents through T2a and T2c become null, and the current through S2 is equal to the one through S4. After this stage, a new switching cycle begins from the first stage.

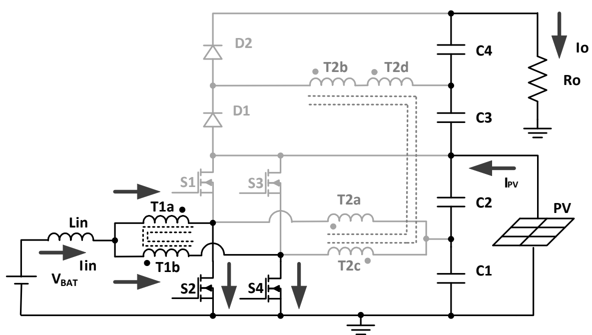

Figure 7. Fifth Stage.

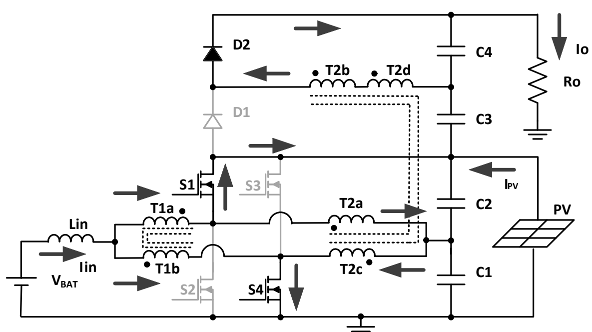

Figure 8. Sixth Stage.

C. STATIC GAIN

Considering that the duty cycle is applied to the lower switches, there are two possible operation modes. For D>50%, there is an overlapping period for the lower switches, which remain turned on simultaneously during a certain time interval. On the other hand, for D<50%, there is an overlapping period of the upper switches.

Static Gain for D>50%

The equivalent circuits from which were derived equations are shown in Figure 10.

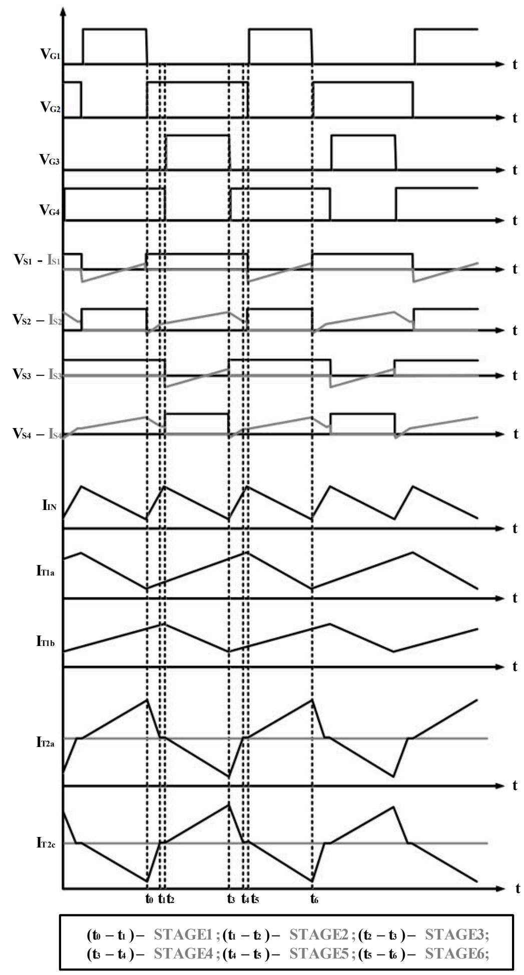

Figure 9. Main theoretical waveforms.

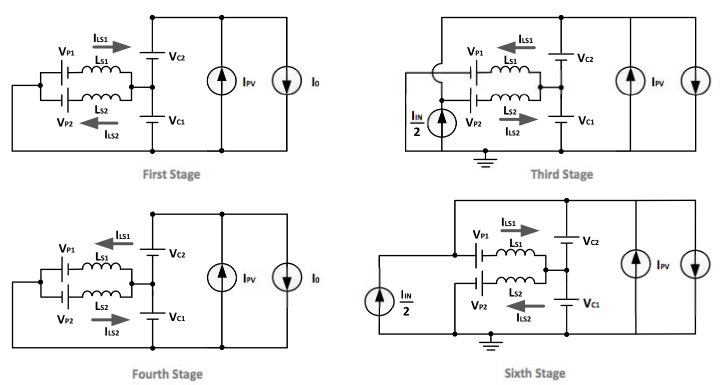

Figure 10. Equivalent circuits used to detarminate static gain for D>50%.

The output voltage can be obtained as:

$$V_0 = V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{1}$$

Where:

$$V_{C3} = V_{C4} = n.(V_{P1} + V_{P2})$$

V_{P1} and V_{P2} represent the transformer secondary voltage reflexed on primary side.

Since the voltage across the capacitor C1 is equal to the voltage across the battery bank, V_{C1} and V_{C2} can be obtained as:

$$V_{C1} = V_{BAT} \tag{2}$$

$$V_{C2} = \frac{D.V_{BAT}}{1-D} \tag{3}$$

From the equations of the currents through the inductors L_{S1} and L_{S2} on the first stage (4), second stage (5), third stage (6) and from the time interval equations given in (7), the voltage across capacitors C3 and C4 can be obtained as (8).

$$\begin{cases} I_{LS1}(t) = I(0) - \left(\dfrac{V_{C1}+V_{P1}}{L_S}\right).t \\ I_{LS2}(t) = -I(0) + \left(\dfrac{V_{C1}-V_{P2}}{L_S}\right).t \end{cases} \tag{4}$$

$$I_{LS1}(t) = I_{LS2}(t) = 0 \tag{5}$$

$$\begin{cases} I_{LS1}(t) = \left(\dfrac{V_{C1}-V_{P1}}{L_S}\right).t \\ I_{LS2}(t) = \left(\dfrac{V_{C2}-V_{P2}}{L_S}\right).t \end{cases} \tag{6}$$

$$\begin{cases} \Delta_{t1} = \Delta_{t4} = \dfrac{\left[(1-D).Ts.(n.V_{C1} - V_{C4} + n.V_{C2})\right]}{V_{C4}} \\ \Delta_{t2} = \Delta_{t5} = -\dfrac{\left[Ts.(2.V_{C1}.n.(1-D) - V_{C4} + 2.V_{C2}.n.(1-D)\right]}{2.V_{C4}} \\ \Delta_{t3} = \Delta_{t6} = (1-D).Ts \end{cases} \tag{7}$$

$$V_{C3} = V_{C4} = \frac{n.Ts.V_{BAT}^2}{(1-D).Ts.V_{BAT} + 4.I_0.L_S.n} \tag{8}$$

From the previous equations, the static gain can be obtained as:

$$G_{D>50\%} = \frac{V_0}{V_{BAT}} = \frac{1}{(1-D)} + \frac{2.n}{\left[(1-D)+\alpha\right]} \tag{9}$$

The static gain depends exclusively on the duty cycle 'D', the transformer turns ratio 'n', and the normalized load current 'α'.

$$\alpha = \frac{4.n.I_0.L_S}{V_{BAT}.Ts} \tag{10}$$

Static Gain for D<50%

The equivalent circuits from which were derived equations are shown in Figure 11.

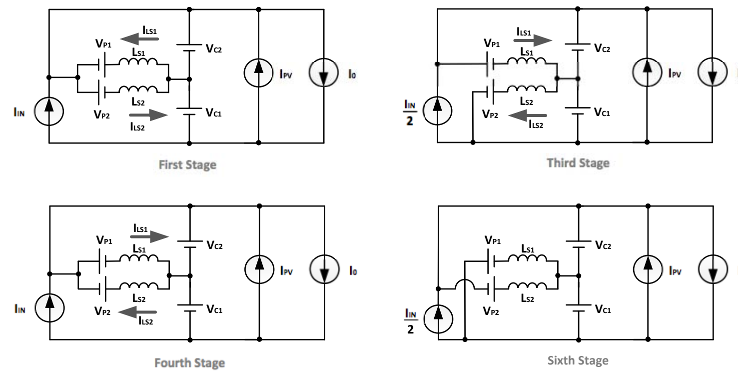

Figure 11. Equivalent circuits used to detarminate static gain for D<50%.

The voltages across capacitors C1 and C2 are given by (2) and (3), but the voltages across capacitors C3 and C4 for D<50% are given by (11).

$$V_{C3} = V_{C4} = \frac{\left[2.I_0.n - \dfrac{D^2.Ts.[V_{C3}.(D-1) + n.V_{C1}]^2}{2.L_S.V_{C3}.n.(D-1)^2}\right].V_{C1}}{2.I_0.(1-D)} \tag{11}$$

Therefore, the static gain for D<50% is given by (12).

$$G_{D<50\%} = \frac{V_0}{V_{BAT}} = \frac{1}{(1-D)} \cdot \left[\frac{2.n.D^2}{D^2 + \alpha.(1-D)} + 1\right] \tag{12}$$

Figure 12 presents the curves of the static gain (G) as a function of the duty cycle (D) for different values of (n). Figure 13 presents the curves where the static gain (G) varied with the normalized load current (α) for different values of (D).

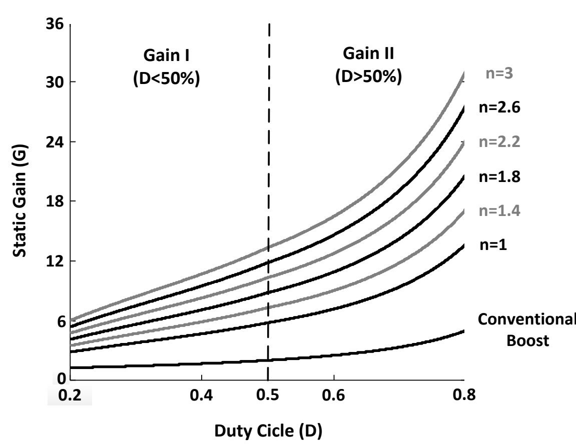

Figure 12. G versus D for different values of 'n'.

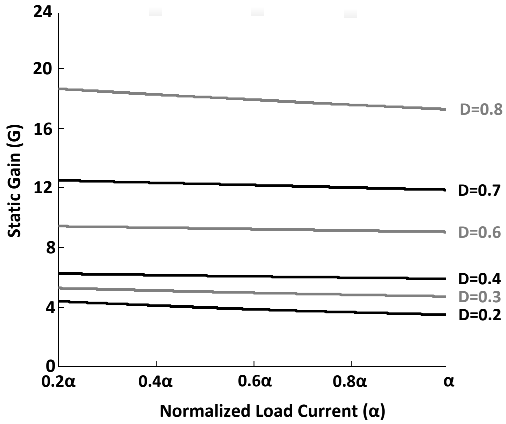

Figure 13. G versus α for different values of 'D'.

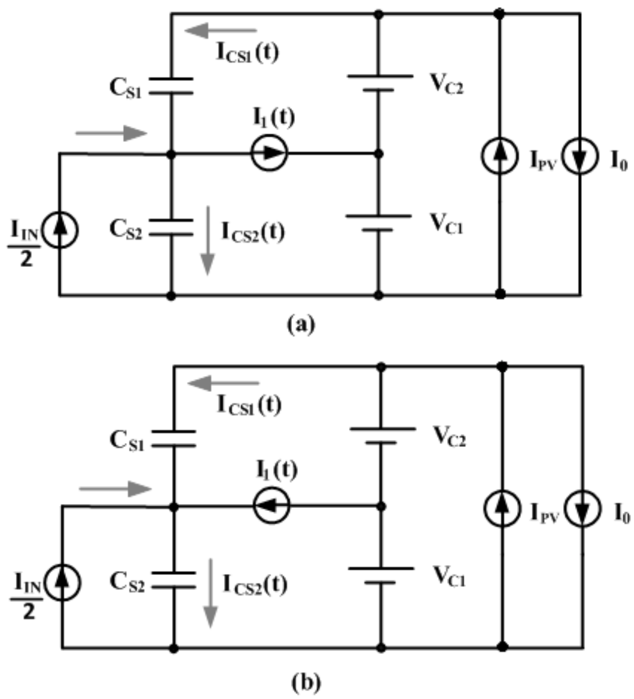

Figure 14. Equivalent circuits used for the commutation analysis of topology III.

D. SOFT-SWITCHING CONDITION

This section presents the analysis of minimum and maximum dead times necessary to obtain the soft-switching condition for the switches. In order to obtain soft switching, the leakage inductance of the transformer and the intrinsic capacitance of the switches are considered. Then, Figure. 14a presents the equivalent circuit during the turn off time of switch S1 and Figure 14b corresponds to the equivalent circuit during the turn off time of switch S2.

Considering the peak current value during stage 6 and the voltage across the primary winding (V_{P1}) in the first stage, the minimum dead time for the lower switches S2 and S4 can be obtained as (13).

$$td_{MIN\_S_{INF}} = -\frac{\frac{I_{IN}}{2} - \left[\frac{\alpha.D.Ts}{2.L_S.(D+\alpha)}\right] + \sqrt{\left(\frac{I_{IN}}{2}\right)^2 - 2.\frac{I_{IN}}{2}.\left[\frac{\alpha.D.Ts}{2.L_S.(D+\alpha)}\right] + \left[\frac{\alpha.D.Ts}{2.L_S.(D+\alpha)}\right]^2 - 4.Cs.V_{PV}.\left(\frac{D.V_{PV}}{2.L_S.(D+\alpha)}\right)}}{\frac{D.V_{PV}}{2.L_S.(D+\alpha)}} \tag{13}$$

On the other hand, the maximum dead time that allows soft switching depends on the time interval necessary for the current to become zero during the first stage. Then the maximum dead time can be obtained as (14).

$$td_{MAX\_S_{INF}} = Ts.\alpha - \frac{I_{IN}.L_S.(D+\alpha)}{D.V_{PV}} \tag{14}$$

The commutation analysis for the upper switches can be performed analogously, while expression (15) can be easily derived.

$$td_{MAX\_S_{SUP}} = \frac{\left[\begin{matrix} Ts.V_{IN}.(D-1). \\ (\alpha - D + 1) \end{matrix}\right] . \left[\frac{\begin{matrix}(Ts.V_{IN}.\alpha - \\ 4.I_{PV}.L_S.n + \\ 2.Ts.V_{IN}.n.\alpha)\end{matrix}}{4.n.(D-1)} + \frac{Ts.V_{IN}.\alpha^2}{2.D.(D+\alpha)}\right]}{V_{IN}^2.Ts.\alpha} \tag{15}$$

Figures 15 and 16 show the soft-switching condition for the upper and lower switches by varying with the normalized load current and for different values of duty cycle. From this figure, it can be observed that the duty cycle variation plays a small role in the commutation condition if compared with the switching interval.

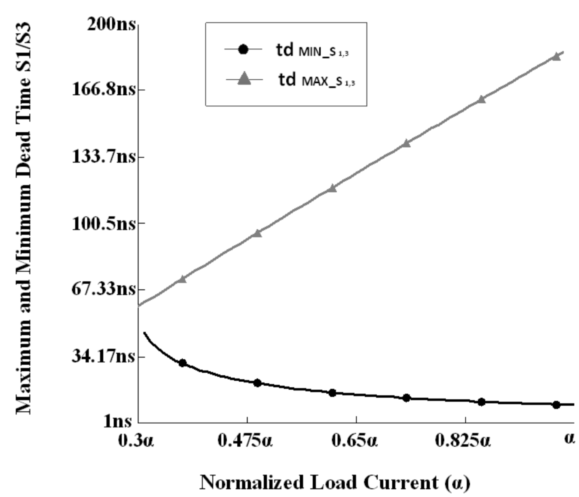

Figure 15. Soft-switching condition for the upper switches.

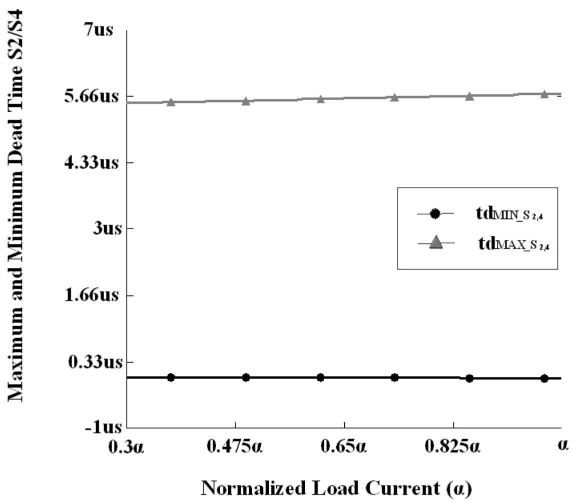

Figure 16. Soft-switching condition for the lower switches.

E. CONTROL STRATEGY

The strategy described in Figure 17 can be used in the proposed converter, where it is necessary to measure only three quantities that are the PV panel voltage (V_{PV}), the PV panel current (I_{PV}), and the voltage across the battery bank (V_{BAT}).

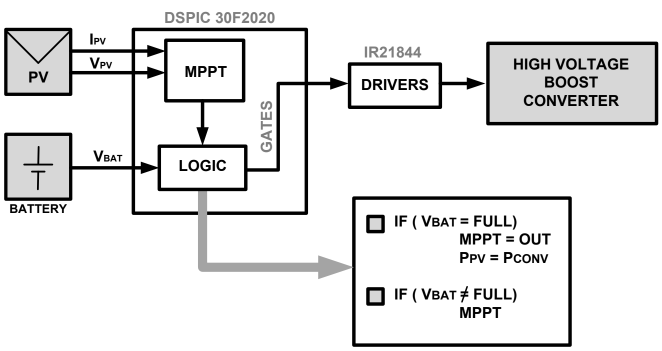

Figure 17. Control strategy.

Let us suppose that constant power is supposed to be injected in the inverter stage. Considering that the battery has low charge, the MPPT can be performed in any radiation and output power condition. The power difference is naturally transferred to or from the battery and the inverter can easily support the resulting dc bus voltage variation. If the battery is fully charged, the MPPT is not performed and the operation point is changed until the current through the battery becomes zero.

III. EXPERIMENTAL RESULTS

This section presents the experimental results obtained from the converter operating in rated power condition. Table I shows the prototype specifications.

Figure 18 presents the voltages across the output capacitors, where it can be seen that the sum of such quantities gives the output voltage. This result also shows good voltage sharing across the output capacitors.

Figure 19 presents the voltages across the diodes D1 and D2, which operate in complementarily way, while the voltages are clamped to approximately 150 V i.e. there is no overvoltage.

Figure 20 presents the behavior of the input current and the currents through the switching cells, where good sharing exist between the currents through T1a and T1b. Consequently, the stresses regarding the active elements are reduced.

TABLE I. PROTOTYPE SPECIFICATIONS

Switching frequency	fs = 25 kHz
Input voltage	V_{IN} = 24V
Output voltage	V_{out} = 200V
Load power	P_0 = 500 W
Input inductance	L_{IN} = 100 uH
Leakage indutance	L_K = 1 uH
Output capacitors	C1, C2, C3 and C4 = 100uF
Turns ratio for the autotransformer of the three-state commutation cell	(1:1)
Transformer turns ratio	(1:1.4)
Switches	MOSFET IRFB4710
Diodes	MBR10200

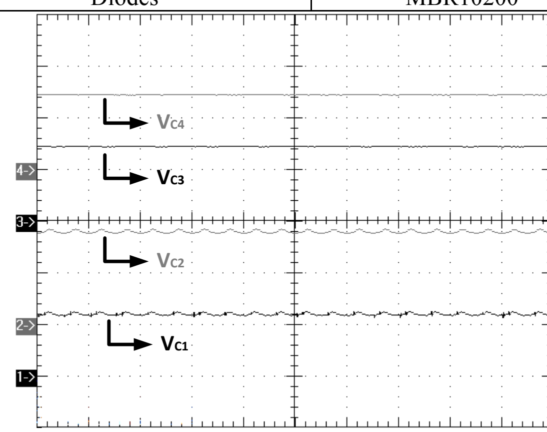

Figure 18. Voltage across the output capacitors (Ch1 20V/div, Ch2 20V/div, Ch3 50V/div, Ch4 50V/div – 20us/div).

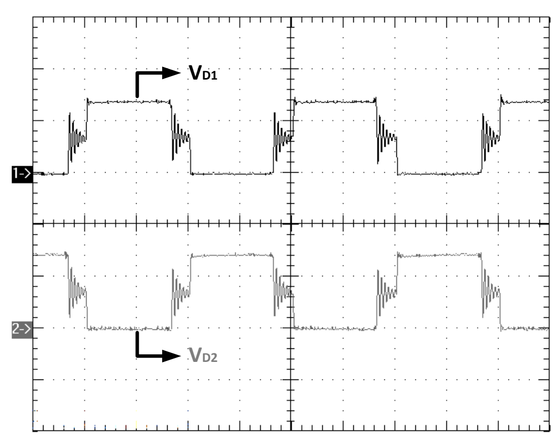

Figure 19. Voltages across D1 and D2 (Ch1 100V/div, Ch2 100V/div – 10us/div).

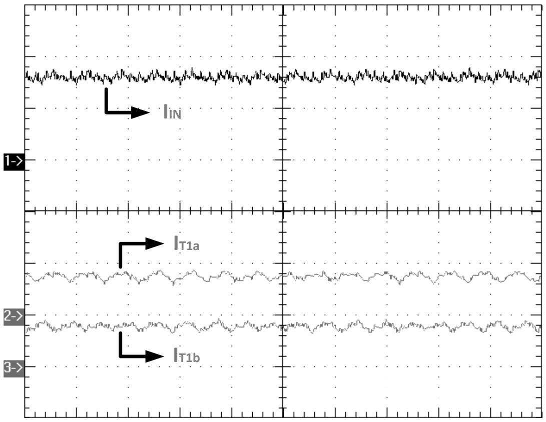

Figure 20. Input current and currents through the switching cells (Ch1 10V/div, Ch2 10A/div, Ch3 10A/div – 50ms/div).

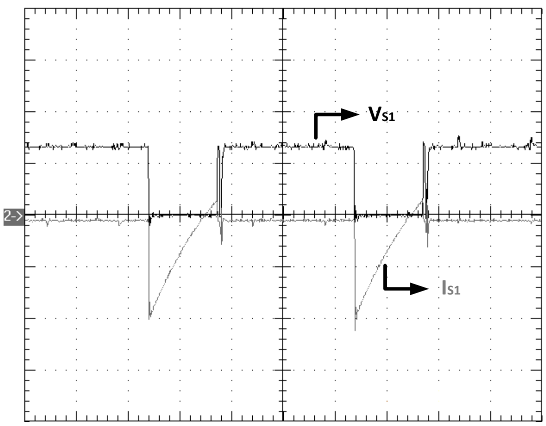

Figure 21. Voltage and current through S1(Ch1 50V/div, Ch2 10A/div – 10us/div).

Figure 21 presents the voltage and the current through S1, where the operation ZVS mode is noticed. As it can be seen the conduction of the body diode can be avoided as S1 and S3 are used as synchronous rectifiers what reduce losses. Switch S3 presents the same behavior, although the waveforms are phase-shifted by 180°.

Figure 22 presents the voltage and the current through S2, whose operation is complementary to S1. It can be seen that S2 operates in ZVS mode. Also, the current at the instant of the turning off is reduced what favors the turning off behaviour.

Figure 23 presents the open loop converter dynamic behavior, where the bidirectional characteristic between the input voltage sources (batteries and photovoltaic panels) becomes evident. From such waveforms, one can be observe the behavior of the currents through the battery, the panel, and the load Ro, as well as the voltages across the panel and the load when a load step is performed.

A current step simulating the insertion of the photovoltaic panel is introduced at 45 ms, while the panel is responsible for supplying most of the energy and charging the batteries, since its current direction is inverted. Then, at approximately 65 ms, a load step of 50% is applied, where a small loss of the output voltage regulation characteristic can be observed.

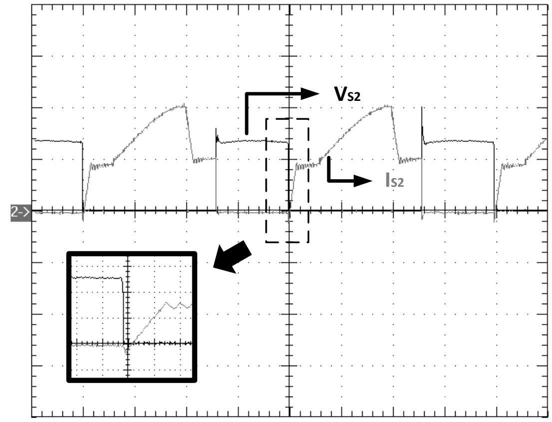

Figure 22. Voltage and current through S2 (Ch1 50V/div, Ch2 10A/div – 10us/div).

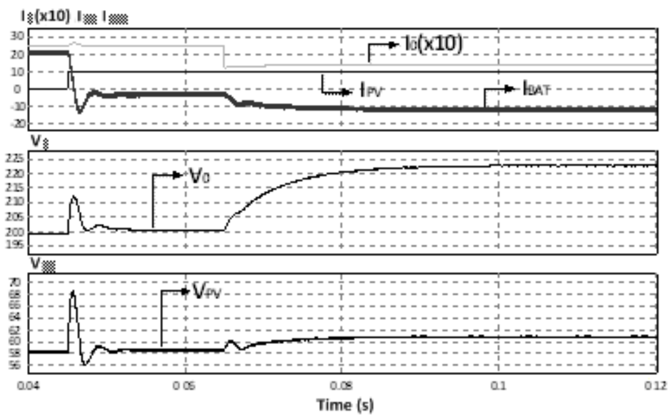

Figure 23. Dynamic behavior of the converter.

Figure 24 presents the efficiency of the proposed converter, as well as the respective curves for topologies I [22] and II [23], where it can be observed that higher efficiency is achieved in lower load condition (97%) and decreases in the rated condition (about 94%). This behavior can be explained since the transformers were designed for low core losses.

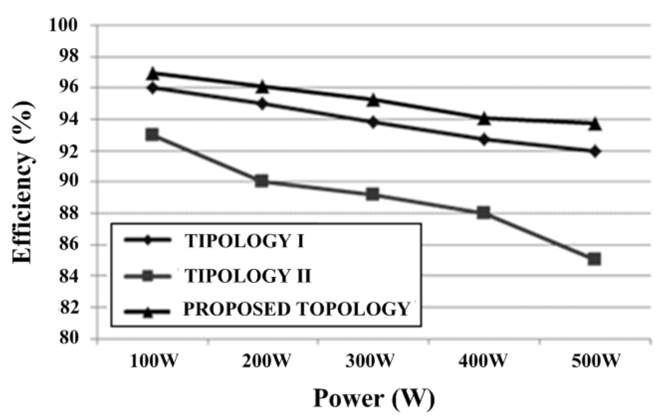

Figure 24. Efficiency as a function of the output power.

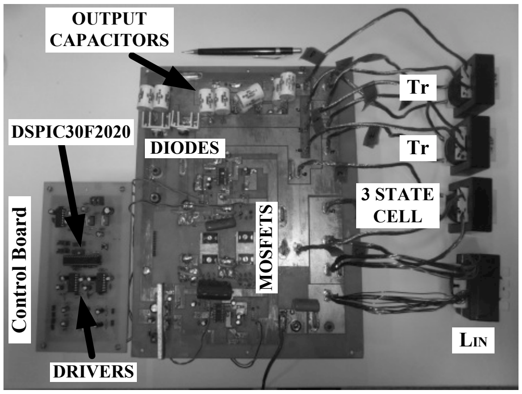

Figure 25. Experimental prototype.

Figure 25 presents the experimental prototype, where transformer Tr is split in two separate cores due to the availability of components.

IV. CONCLUSION

A boost converter with high voltage gain has been presented in this paper. The relevant equations for the design procedure, the operation principle, and the main theoretical waveforms are discussed in detail. The main advantage of the topology is the wide voltage step-up ratio with reduced voltage stress across the main switches, what is important in stand alone or in grid-connected systems based on battery storage, such as renewable energy systems.

Experimental results obtained from a 500 W prototype have validated the concept, with high efficiency over a wide load range and smaller efficiency at the rated condition (94%), confirming the satisfactory performance of the structure. Although such curve is satisfactory for PV applications further optimization can be investigated in order to reduce conduction losses and improve efficiency in the rated condition.

The concept of integrated converters in a single-stage approach seems to be promising, thus leading to the proposal of additional topologies feasible to photovoltaic and fuel cell applications.

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