A New Multilevel Converter Topology With Reduced Number of Power Electronic Components

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***Abstract*—In this paper, a new topology for cascaded multilevel converter based on submultilevel converter units and full-bridge converters is proposed. The proposed topology significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. Also, an algorithm to determine dc voltage sources magnitudes is proposed. To synthesize maximum levels at the output voltage, the proposed topology is optimized for various objectives, such as the minimization of the number of switches, gate driver circuits and capacitors, and blocking voltage on switches. The analytical analyses of the power losses of the proposed converter are also presented. The operation and performance of the proposed multilevel converter have been evaluated with the experimental results of a single-phase 125-level prototype converter.**

***Index Terms*—Bidirectional switch, cascaded multilevel converter, full-bridge converter, multilevel converter, submultilevel converter.**

I. Introduction

THE basic concept of a multilevel converter is to use a series of power semiconductor switches that properly connected to several lower dc voltage sources to synthesize a near sinusoidal staircase voltage waveform. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency.

Numerous multilevel converter topologies and wide variety of control methods have been developed in the recent literature [1]–[4]. Three different basic multilevel converter topologies are the neutral point clamped (NPC) or diode clamped [5], the flying capacitor (FC) or capacitor clamped [6] and the cascaded H-bridge (CHB) [7]. The main drawbacks of NPC topology are their unequal voltage sharing among series connected capacitors that result in dc-link capacitor unbalancing and requiring a great number of clamping diodes for higher level. The FC multilevel converter uses flying capacitor as clamping devices. These topologies have several attractive properties in comparison with the NPC converter, including the advantage of the transformerless operation and redundant phase leg states that allow the switching stresses to be equally distributed between semiconductor switches [8], [9]. But, these converters require an excessive number of storage capacitors for higher voltage steps. The CHB topologies are proper option for high level applications from point of view of modularity and simplicity of control. But, in this topology, a large number of isolated dc voltage sources are required to supply each conversion cell. It increases the converter cost and complexity.

In multilevel converter, the power quality is improved as the number of levels increases at the output voltage. However, it causes to the increasing number of switching devices and other components, and increases the cost and control complexity and tends to reduce the overall reliability and efficiency of the converter. It is noticeable that multilevel converters can sustain the operation in case of internal fault [10]. In the case of internal fault of one cell of FC converter, the maximum output voltage remains constant, but the number of levels decreases. On the other hand, when an internal fault is detected in the CHB converter, and the faulty cell is identified, it can be easily isolated through an external switch and replaced by a new operative cell [11].

Asymmetric and/or hybrid multilevel converters have been presented in [12], [13]. In the asymmetric topologies, the values of dc voltage sources magnitudes are unequal or changed dynamically [14]. These converters reduce the size and cost of the converter and improve the reliability since fewer semiconductors and capacitors are employed [15]. The hybrid multilevel converters are composed of different multilevel topologies with unequal values of dc voltage sources and different modulation techniques and/or semiconductor technologies [12]. With appropriate selection of switching devices, the converter cost is significantly reduced. But, the application of different multilevel topologies result in loss of modularity and produces problems with switching frequency and restrictions on the modulation and control method [16].

The researchers are strived in [17] and [18] to introduce a new topology for multilevel converters with a reduced number of components compared to conventional multilevel converters. This topology is composed of modular submultilevel converters that makes it easily extensible to higher number of output voltage levels without undue increase in the power circuit complexity and reduces controller design cost. By the presented algorithm in [17] and [18], it is not possible to create all levels (odd and even) at the output voltage, and it reduces the flexibility of the converter. Also, to create the output voltage with a constant number of levels, the converter needs many large numbers of bidirectional switches. To overcome these

Manuscript received May 27, 2010; revised September 22, 2010, January 2, 2011, and March 18, 2011; accepted March 28, 2011. Date of publication May 5, 2011; date of current version October 18, 2011. This work was supported by the Iran Renewable Energy Organization (SUNA), Tehran, Iran.

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Digital Object Identifier 10.1109/TIE.2011.2151813

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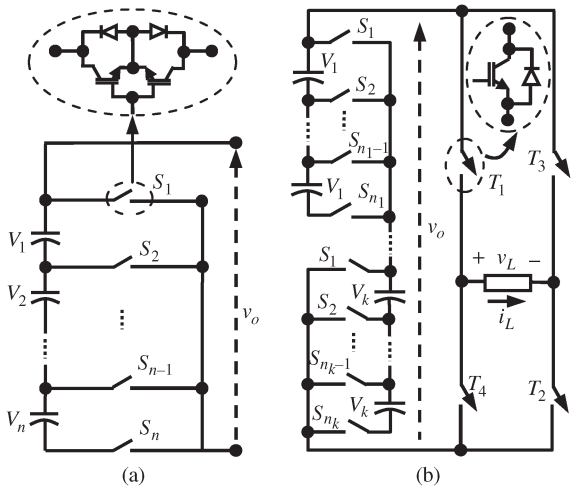

Fig. 1. (a) Basic unit [19] and (b) multilevel converter presented in [19].

disadvantages, [19] has presented a new topology, which has decreased the number of bidirectional switches and dc voltage source compared to [17] and [18] and with the ability of the production of all levels at the output voltage. The main drawback of this topology is the utilization of unidirectional switches that operate in the high output voltage.

The structures, based on similar concepts, have been presented in [20]. In these topologies, the dc source is formed by connecting a number of half-bridge cells, diode-clamped phase leg or capacitor-clamped phase leg. Also, in [21], the topology has been obtained from the mixture of the FC and CHB inverter. These structures provide a high number of output levels using low number of components. But, the main drawback of these topologies is the utilization a full-bridge converter, which operates in the high output voltage. Also, these designs are not flexible.

This paper proposes a new modular and simple topology for cascaded multilevel converter that produces a high number of levels with the application of a low number of power electronic components. Then, a procedure for calculating the values of required dc voltage sources is also proposed. In addition, the structure of the proposed topology is optimized for various aims. Finally, a design example of the proposed multilevel converter is included.

II. Multilevel Converter With Reduced Number of Switches

The basic unit of the submultilevel converter, presented in [19], is illustrated in Fig. 1(a). It consists of several capacitors (with dc voltages) and bidirectional switches. If n capacitors are used, $n+1$ different values can be obtained for v_o, by $n+1$ bidirectional switches. The output voltage of this submultilevel converter has zero or positive values. The presented unit requires bidirectional switches with the capability of blocking voltage and conducting current in both directions. Several arrangements can be used to create bidirectional switches considering of insulated gate bipolar transistors (IGBTs) and diodes. The proper configuration of bidirectional switches is arranged by a common emitter connection of two IGBTs, which each one of IGBTs has an antiparallel diode. Because the emitters of two IGBTs are common, the base voltage of each IGBT can be measured versus its common emitter. Therefore, a bidirectional switch requires a gate driver circuit in this configuration. This configuration of bidirectional switch is used in this paper, to make it comparable with one presented in [19].

The cascaded connection of these submultilevel converters increase the possible value of v_o, effectively. But, it can only generate the positive output voltages. To generate both positive and negative voltages, a full-bridge converter is connected to the output terminal of the cascaded connection of submultilevel converters. But, the unidirectional switches in the full-bridge converter and some bidirectional switches, such as S_1, must operate at the high output voltage and need higher voltage blocking. As a result, the cost and losses will be increased and its industrial applications will be limited. Fig. 1(b) shows k submultilevel converters in series, where the structure of the first till kth submultilevel converters has $n_1, n_2, \ldots, n_k$ bidirectional switches, respectively. In this case, only one switch of each submultilevel converter turns on in different operation modes of the converter. The number of output voltage levels (N_{level}) and IGBTs (N_{IGBT}) are given by the following equations, respectively:

$$N_{level} = 2\left(\prod_{i=1}^{k} n_i\right) - 1 = 2(n_1 \times n_2 \times \ldots \times n_k) - 1 \quad (1)$$

$$N_{IGBT} = 2\left(\sum_{i=1}^{k} n_i\right) + 4 = 2(n_1 + n_2 + \ldots + n_k) + 4. \quad (2)$$

The maximum value of the output voltage $(V_{o\max})$ can be obtained, as follows:

$$V_{o\max} = \sum_{i=1}^{k} (n_i - 1) V_i. \quad (3)$$

III. Proposed Topology

Fig. 2(a) shows the proposed topology for a submultilevel converter, hereafter called multilevel module (MLM), which is used for the implementation of the proposed multilevel converter topology. It consists of n dc voltage sources and n bidirectional switches. A MLM produces a staircase voltage waveform with positive polarity. It is connected to a single-phase full-bridge converter, which particularly alternates the input voltage polarity and provides positive or negative staircase waveform at the output. The full-bridge converter has four unidirectional switches, which consists of an IGBT and an antiparallel fast recovery diode. The typical output waveforms of v_o' and v_o are shown in Fig. 2(b). It is noticeable that only one switch turns on in different operation modes of the MLM and also, both switches T_1 and T_4 (or T_2 and T_3) cannot be simultaneously turned on (expect state 1 in Table I) because of a short circuit occurrence across dc voltage sources and then the voltage v_o would be produced. Table I summarizes the values of the output voltage of a MLM and corresponding full-bridge converter for different state of switches $S_1, S_2, \ldots, S_n, T_1, \ldots, T_4$. State conditions 1 and 0 means that

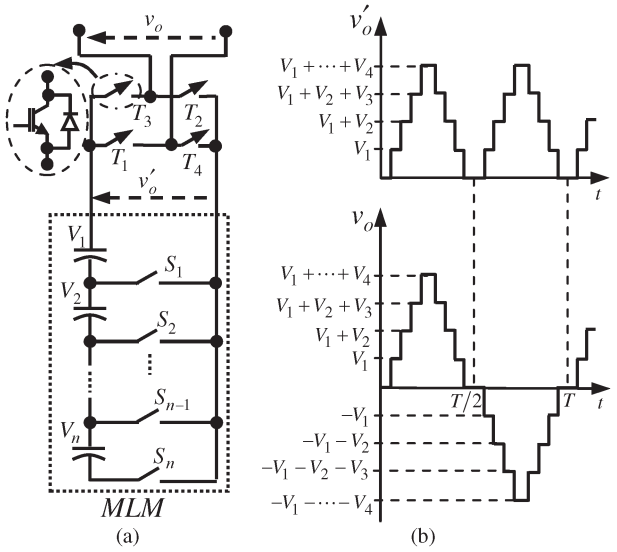

Fig. 2. (a) Proposed submultilevel topology and (b) typical output waveform of v_o.

TABLE I
VALUES OF v_o FOR DIFFERENT STATES OF SWITCHES IN SUBMULTILEVEL CONVERTER

State	Switches states								v_o'	v_o
	S_1	S_2	…	S_n	T_1	T_2	T_3	T_4		
1	0	0	…	0	1	0	1	0	0	0
	0	0	…	0	0	1	0	1		
2	1	0	…	0	0	0	1	1	V_1	V_1
3	1	0	…	0	1	1	0	0	V_1	$-V_1$
4	0	1	…	0	0	0	1	1	V_1+V_2	V_1+V_2
5	0	1	…	0	1	1	0	0	V_1+V_2	$-V_1-V_2$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$2n$	0	0	…	1	0	0	1	1	$\sum_{i=1}^{n} V_i$	$\sum_{i=1}^{n} V_i$
$2n+1$	0	0	…	1	1	1	0	0	$\sum_{i=1}^{n} V_i$	$-\sum_{i=1}^{n} V_i$

the switch is on and off, respectively. For simplicity, the on-state voltage drops of switches have been neglected. As it can be seen, $2n+1$ different values can be obtained for v_o.

The proposed multilevel converter topology, which is based on the combination of MLMs and full-bridges converters, is shown in Fig. 3. The structure of the first till kth MLM has $n_1, n_2, \ldots, n_k$ bidirectional switches, respectively. Each MLM can generate a stepped voltage waveform with positive polarity. The full-bridge converters provide positive and negative stepped voltage waveforms in their output.

The different output voltage levels can be determined by the combination of switching states of MLMs. It is obvious that only one switch of each MLM turns on in different operation modes of the converter without considering the zero voltage state of MLMs. If the proper values for dc voltage sources are selected, then, the output voltage of the converter will be obtained between $-\sum_{i=1}^{k}\sum_{j=1}^{n_i} V_{ij}$ and $+\sum_{i=1}^{k}\sum_{j=1}^{n_i} V_{ij}$. Table II shows the output voltage of the proposed topology for different switching states. It is noticeable that there are two

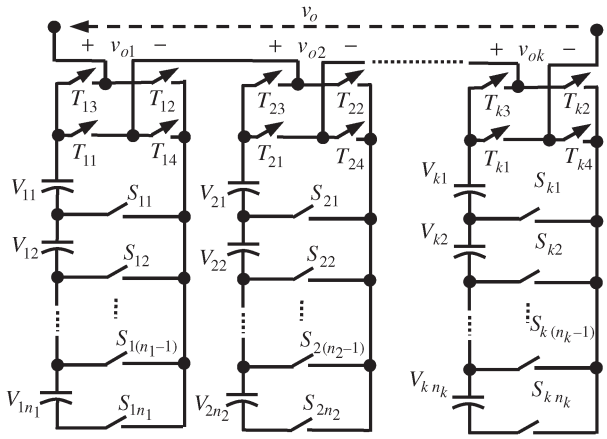

Fig. 3. Proposed multilevel converter topology.

TABLE II
VALUES OF v_o FOR DIFFERENT STATES OF SWITCHES IN PROPOSED TOPOLOGY

State	On switches							v_o
1	-	T_{11}	T_{13}	…	-	T_{k1}	T_{k3}	0
2	S_{11}	T_{13}	T_{14}	…	-	T_{k1}	T_{k3}	$+V_{11}$
3	S_{11}	T_{11}	T_{12}	…	-	T_{k1}	T_{k3}	$-V_{11}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$2n_1$	S_{1n_1}	T_{13}	T_{14}	…	-	T_{k1}	T_{k3}	$+\sum_{i=1}^{n_1} V_{1i}$
$2n_1+1$	S_{1n_1}	T_{11}	T_{12}	…	-	T_{k1}	T_{k3}	$-\sum_{i=1}^{n_1} V_{1i}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$\prod_{i=1}^{k}(2n_i+1)-3$	S_{1n_1}	T_{13}	T_{14}	…	S_{kn_k}	T_{k1}	T_{k2}	$+\sum_{i=1}^{n_k} V_{ki}+\sum_{i=1}^{k-1}\sum_{i=1}^{n_i} V_{1i}$
$\prod_{i=1}^{k}(2n_i+1)-2$	S_{1n_1}	T_{11}	T_{12}	…	S_{kn_k}	T_{k1}	T_{k2}	$+\sum_{i=1}^{n_k} V_{ki}-\sum_{i=1}^{k-1}\sum_{i=1}^{n_i} V_{1i}$
$\prod_{i=1}^{k}(2n_i+1)-1$	S_{1n_1}	T_{13}	T_{14}	…	S_{kn_k}	T_{k1}	T_{k2}	$-\sum_{i=1}^{n_k} V_{ki}+\sum_{i=1}^{k-1}\sum_{i=1}^{n_i} V_{1i}$
$\prod_{i=1}^{k}(2n_i+1)$	S_{1n_1}	T_{11}	T_{12}	…	S_{kn_k}	T_{k1}	T_{k2}	$-\sum_{i=1}^{n_k} V_{ki}-\sum_{i=1}^{k-1}\sum_{i=1}^{n_i} V_{1i}$

switching states for producing the zero voltage level and in the Table II, only one of them is presented.

It should be noted that the capacitors can be replaced with the dc voltage sources in the proposed topology. Although this topology requires multiple dc voltage sources, but they may be available in some systems through renewable energy sources, such as photovoltaic panels or fuel cells, or with energy storage devices, such as capacitors or batteries. When ac voltage is already available, then, multiple dc sources can be generated using isolated transformers and rectifiers, too [19].

If the voltage sources are changed during the converter operation, the voltage balancing should be done. For example, the output voltages of fuel cells are variable. Therefore, if they are used at dc-link, the quality of output voltage of the converter will be reduced. The hardware proposed method to

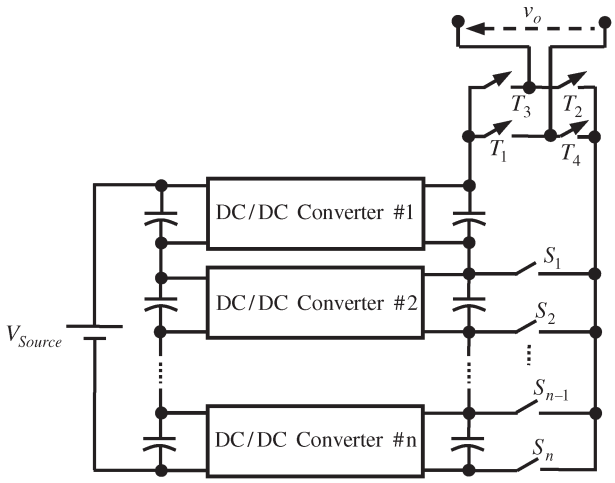

Fig. 4. DC-link voltage balancing.

dc-link balancing is shown in Fig. 4. The capacitor voltages are controlled with the DC/DC converters.

If the dc voltage sources are considered to be equal in MLMs, the structure of the proposed topology will be symmetrical. In the asymmetrical structure of the proposed topology, similar to the asymmetrical cascaded multilevel converter, there is only one switching state for each output voltage level (except the zero level) to produce unequal values for v_o. In this paper, to reduce the number of components, the asymmetrical structure has been studied. It is noticeable that the asymmetrical structure has circulating energy problems. Therefore, if diode-based rectifiers are used for dc voltage sources, their dc-link voltages can increase their values dangerously [12].

Considering the first dc voltage source (V_{11}) as the base value of the per-unit system, i.e.,

$$V_{base} = V_{11} = V_{dc} \tag{4}$$

then, the normalized values of the dc voltage sources for producing all levels (odd and even) in the output must be chosen using the following algorithm.

For module 1

$$V_{11} = V_{dc} \tag{5}$$

$$V_{1i} = V_{11} = V_{dc}, \quad i = 2, \ldots, n_1. \tag{6}$$

For module 2

$$V_{21} = V_{11} + 2\sum_{i=1}^{n_1} V_{1i} = (2n_1 + 1)V_{dc} \tag{7}$$

$$V_{2i} = V_{21} = (2n_1 + 1)V_{dc}, \quad i = 2, \ldots, n_2. \tag{8}$$

For module 3

$$V_{31} = V_{11} + 2\sum_{i=1}^{n_1} V_{1i} + 2\sum_{i=1}^{n_2} V_{2i} = (2n_1 + 1)(2n_2 + 1)V_{dc} \tag{9}$$

$$V_{3i} = V_{31} = (2n_1 + 1)(2n_2 + 1)V_{dc}, \ \ i = 2, \ldots, n_3. \tag{10}$$

In general, for the mth module

$$V_{m1} = V_{11} + 2\sum_{i=1}^{m-1}\sum_{j=1}^{n_i} V_{ij} = \prod_{i=1}^{m-1}(2n_i + 1)V_{dc} \tag{11}$$

$$V_{mi} = V_{m1} = \prod_{i=1}^{m-1}(2n_i + 1)V_{dc}, \quad i = 2, \ldots, n_m. \tag{12}$$

By using the proposed algorithm, the maximum value of the output voltage $(V_{o\max})$ is obtained, as follows:

$$V_{o\max} = \sum_{i=1}^{k}\sum_{j=1}^{n_i} V_{ij} = \sum_{i=1}^{k}(n_i \times V_{i1}). \tag{13}$$

The number of output voltage levels can be determined by the following equation:

$$N_{level} = \prod_{i=1}^{k}(2n_i + 1) = (2n_1 + 1) \times (2n_2 + 1) \times \ldots \times (2n_k + 1). \tag{14}$$

Considering the selected common emitter configuration for bidirectional switches, the number of power IGBTs in the proposed topology can be obtained as follows:

$$N_{IGBT} = 2(n_1 + n_2 + \ldots + n_k) + 4k. \tag{15}$$

It is important to note that the number of IGBTs and main diodes are the same.

IV. Optimal Structures

A. Maximum Number of Voltage Levels With Constant Number of IGBTs

The desirable object in a multilevel converter is maximizing the number of levels using the minimum number of IGBTs. The question concerning the proposed structure is that for the constant number of IGBTs, which topology can provide a maximum number of output voltage levels?

The product of numbers, whose summation is constant, will be maximum, when all are equal. Then considering (14) and (15) we have

$$n_1 = n_2 = \ldots = n_k = n. \tag{16}$$

Using (15) and (16), we have

$$k = \frac{N_{IGBT}}{2n + 4}. \tag{17}$$

Now, the value of n must be determined. Considering (14) and (16), the maximum number of voltage levels will be determined

$$N_{level} = (2n + 1)^k. \tag{18}$$

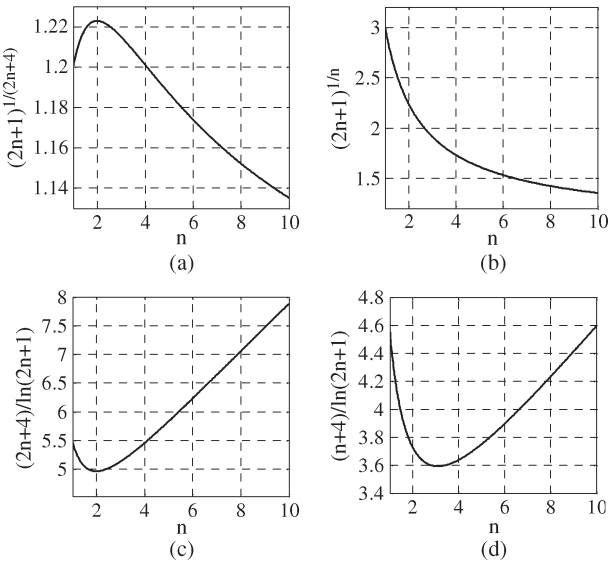

Fig. 5. (a) Variation of $(2n+1)^{1/(2n+4)}$, (b) $(2n+1)^{1/n}$, (c) $(2n+4)/\ln(2n+1)$ and (d) $(n+4)/\ln(2n+1)$ versus n.

Considering (17) and (18), we have

$$N_{level} = \left[(2n+1)^{1/(2n+4)}\right]^{N_{IGBT}}. \tag{19}$$

Fig. 5(a) shows the variation of $(2n+1)^{1/(2n+4)}$ versus n. It is clear that the maximum number of voltage levels is obtained for $n=2$. Thus, a structure consisting of two bidirectional switches (i.e., two dc voltage sources) in each MLM can provide the maximum voltage levels for v_o with using minimum numbers of IGBTs.

It is necessary to notice that the number of components is an integer. Thus, if an integer number is not obtained, the nearest integer number should be selected.

B. Maximum Number of Voltage Levels With Constant Number of Capacitors

Suppose the number of capacitors (dc voltage sources) is constant and equal to $(N_{capacitor})$, the question in this section is, which topology provides the maximum number of voltage levels?

Suppose the proposed topology consists of a series of k MLMs and each of them consists of n_i capacitors $(i = 1, 2, \ldots, k)$. Thus

$$N_{capacitor} = \sum_{i=1}^{k} n_i = n_1 + n_2 + \ldots + n_k. \tag{20}$$

Considering (16), the number of capacitors can be written as follows:

$$N_{capacitor} = n \times k. \tag{21}$$

Using (18), the maximum number of voltage levels can be determined

$$N_{level} = \left[(2n+1)^{1/n}\right]^{N_{capacitor}}. \tag{22}$$

Fig. 5(b) shows the variation of $(2n+1)^{1/n}$ versus n. It is clear that the maximum number of voltage levels is obtained for $n=1$. Thus, a structure consisting of MLMs with one capacitor (dc voltage source) can provide maximum voltage levels for v_o with minimum numbers of capacitors. It is necessary to note that the proposed topology is converted in this case to the conventional cascaded multilevel converter.

C. Minimum Number of IGBTs With Constant Number of Voltage Levels

In this section, the question is that if N_{level} is the number of voltage levels considered for the voltage v_o, which topology with a minimum number of IGBTs can produce it?

It can be proven that the maximum number of voltage levels may be obtained for equal bidirectional switches. Thus, if the number of switches in each MLM is assumed to be equal to n, then the total numbers of IGBTs (N_{IGBT}) can be obtained, considering (15) and (18), as follows:

$$N_{IGBT} = (2n+4)k = \ln(N_{level}) \times \frac{(2n+4)}{\ln(2n+1)}. \tag{23}$$

Since N_{level} is constant, N_{IGBT} will be minimized, when $(2n+4)/\ln(2n+1)$ tends to be minimum. Fig. 5(c) shows that the minimum number of IGBTs to realize N_{level} values for the output voltage is possible for $n=2$.

D. Minimum Number of Gate Driver Circuits With Constant Number of Voltage Levels

In the proposed topology, each bidirectional switch is composed of two IGBTs and two anti-parallel diodes. Also, each unidirectional switch used in full-bridge converter is composed of an IGBT and an anti-parallel diode. Each bidirectional and unidirectional switch in the converter requires an isolated driver circuit. The isolation can be provided using either pulse transformers or optoisolators. The optoisolators can work in a wide range of input signal pulsewidths, but a separate isolated power supply is required for each switching device.

To reduce the number of components, the objective is to determine the topology, which can provide v_o with the minimum number of gate driver circuits.

If the number of switches in each MLM is assumed to be equal to n, then, the total numbers of gate drive circuits (N_{driver}) can be obtained, as follows:

$$N_{driver} = (n+4)k = \ln(N_{level}) \times \frac{(n+4)}{\ln(2n+1)}. \tag{24}$$

Since N_{level} is constant, N_{driver} will be minimized, when $(n+4)/\ln(2n+1)$ tends to be minimum. Fig. 5(d) shows that the minimum number of gate drive circuits to realize N_{step} values for voltage v_o is realizable for $n=3$.

E. Minimum Blocking Voltage of Switches With Constant Number of Voltage Levels

The voltage and current ratings of switches in a multilevel converter play important role in the cost and realization of multilevel converters. In all topologies, currents of all switches are equal to the rated current of the load. But, this is not the case for the voltage. The objective is to determine the topology with the minimum blocking voltage, which can provide constant number of voltage levels v_o.

Suppose that the peak value of the blocking voltage of switches (V_{switch}) is represented by the following equation:

$$\begin{aligned} V_{switch} &= V_{switch,M} + V_{switch,B} \\ &= \sum_{j=1}^{k} V_{switch,m,j} + \sum_{j=1}^{k} V_{switch,b,j}. \end{aligned} \tag{25}$$

In this equation, $V_{switch,M}$ and $V_{switch,B}$ are the peak value of the blocking voltage of the bidirectional and unidirectional switches, respectively. Also, $V_{switch,m,j}$ and $V_{switch,b,j}$ represent the peak value of the blocking voltage of bidirectional switches in the jth MLM and unidirectional switches in the jth full-bridge converter, respectively. Therefore, (25) can be considered as a criterion to compare different topologies from the viewpoint of the maximum voltage on the switches [19]. The lower value of the criterion indicates that a smaller voltage is applied to the terminal of the switches. According to Fig. 3, the following equations can be obtained:

$$V_{switch,m,j} = P \times V_j, \quad j = 1, \ldots, k. \tag{26}$$

Therefore, the peak value of the blocking voltage of MLM switches can be written, as follows:

$$V_{switch,M} = P \times (V_{11} + V_{21} + \ldots + V_{k1}). \tag{27}$$

In these equations, P is calculated by the following equation:

$$\begin{aligned} P &= 2\left[(n-1) + (n-2) + \ldots + \left(n - \frac{n-2}{2}\right)\right] + \frac{n}{2} + n \\ &= \frac{3n^2}{4} \qquad \text{(if } n \text{ is an even number)} \\ P &= 2\left[(n-1) + (n-2) + \ldots + \left(n - \frac{n-1}{2}\right)\right] + n \\ &= \frac{3n^2+1}{4} \qquad \text{(if } n \text{ is an odd number)}. \end{aligned} \tag{28}$$

According to (4)–(12), (16) and (28), (27) can be simplified, as follows:

$$\begin{aligned} V_{switch,M} &= P \times \left[1 + (2n+1) + \ldots + (2n+1)^{k-1}\right] \times V_{dc} \\ &= \frac{P}{2n} \times (N_{level} - 1) \times V_{dc}. \end{aligned} \tag{29}$$

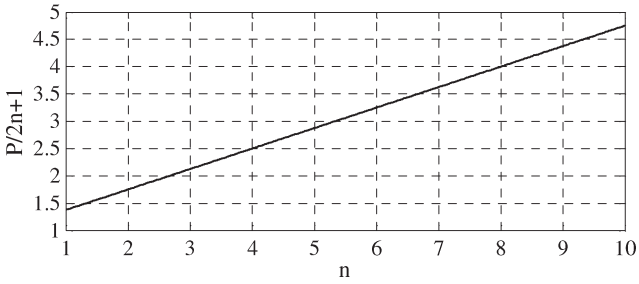

Fig. 6. Variation of $(P/2n) + 1$ voltage versus n.

The peak value of the blocking voltage of switches in the jth full-bridge converters can be calculated, as follows:

$$V_{switch,b,j} = 2 \times \sum_{i=1}^{n} V_{ji} = 2n \times (2n+1)^{j-1} \times V_{dc}. \tag{30}$$

The peak value of the blocking voltage of full-bridges switches $(V_{switch,B})$ can be calculated, as follows:

$$\begin{aligned} V_{switch,B} &= \sum_{j=1}^{k} V_{switch,b,j} = V_{dc} \times \left[(2n+1)^k - 1\right] \\ &= V_{dc} \times (N_{level} - 1). \end{aligned} \tag{31}$$

Therefore, the peak value of the blocking voltage of all switches can be written, as follows:

$$\begin{aligned} V_{switch} &= V_{switch,M} + V_{switch,B} \\ &= V_{dc} \times \left(\frac{P}{2n} + 1\right) \times (N_{level} - 1). \end{aligned} \tag{32}$$

The variation of $P/2n + 1$ versus n is shown in Fig. 6. As illustrated in this figure, V_{switch} is minimum for $n = 1$. Thus, the optimal structure, from the point of view of the minimum blocking voltage of switches, is a classic full-bridge cell with one dc voltage source and in this case, the proposed topology is converted to the conventional cascaded multilevel converter. Here, the dc voltage sources of H-bridges have been scaled by the factor of three.

V. Losses in Proposed Topology

The total losses of switches are the conduction and switching losses. The blocking state losses have been neglected, because they are much smaller than the conduction losses [22].

A. Calculation of Conduction Losses

The conduction losses are the losses that occur while the power device is in the on-state and conducting current. Therefore, power dissipation during the conduction is computed by multiplying the on-state voltage drop by the current that flows through device [23], i.e.,

$$p(t) = V_{on}(t).I(t) \tag{33}$$

where, V_{on} is the on-state saturation voltage and I is the power device current. The saturation voltage is a function

of the junction temperature and the current flowing through the device. The saturation voltage of a bidirectional switch, shown in Fig. 1(a), is the sum of saturation voltage of a diode, approximated by a linear function, and an IGBT, obtained from the manufacturers. Therefore, we have

$$\begin{aligned} V_{on} &= V_{on,IGBT} + V_{on,Diode} \\ &= (V_T + R_T.I^{\beta}) + (V_d + R_d.I) \end{aligned} \tag{34}$$

where, V_T and V_d are the threshold voltages of power devices and R_T and R_d are the equivalent resistances of the voltage drop across the power devices and β is a constant. At a particular temperature, the semiconductor specifications (from the manufacturer) can be used to approximate semiconductor losses [22].

If the inverter generates a high number of levels, the output current can be assumed to be sinusoidal. Therefore, the instantaneous conduction losses in the bidirectional switch can be written by using (33) and (34), as follows:

$$\begin{aligned} p(t) = (V_T + V_d)I_p \sin(\omega t) + R_d I_p^2 \sin^2(\omega t) \\ + R_T I_p^{\beta+1} \sin^{\beta+1}(\omega t) \end{aligned} \tag{35}$$

where, I_p is the peak value of the output current. It is obvious that one switch is turned on in different operation modes of the MLM (except for the zero voltage level). Therefore, assuming the application of same bidirectional switches in mth MLM, the conduction losses of bidirectional switches of mth MLM can be calculated, as follows:

$$\begin{aligned} P_{M_m cond} &= \frac{1}{\pi} \int_0^{\pi} p_m(t)\, d\omega t \\ &= \frac{2I_p}{\pi} \left(V_{T_m} + V_{d_m}\right) + \frac{I_p^2}{2} R_{d_m} \\ &\quad + \frac{I_p^{\beta_m+1}}{\frac{\pi}{\omega}} R_{T_m} \int_0^{\frac{\pi}{\omega}} \sin^{\beta_m+1}(\omega t)\, dt. \end{aligned} \tag{36}$$

In the H-bridge inverter, two diodes for half cycle conduct in φ rad. and two IGBTs conduct for $(\pi - \varphi)$ rad., when φ is the power factor angle. Therefore, the instantaneous conduction losses in the diodes of the mth H-bridge are, as follows:

$$p_{D_m}(t) = 2V_{d_m} I_p \sin(\omega t) + 2R_{d_m} I_p^2 \sin^2(\omega t). \tag{37}$$

The conduction losses of diodes of the mth H-bridge can be calculated, as follows:

$$\begin{aligned} P_{D_m} &= \frac{1}{\pi} \int_0^{\varphi} p_{D_m}(t)\, d\omega t \\ &= \frac{2}{\pi} \left[V_{d_m} I_p (1 - \cos\varphi) \right. \\ &\quad \left. + \frac{R_{d_m} I_p^2}{4} \left(2\varphi - \sin(2\varphi)\right) \right]. \end{aligned} \tag{38}$$

Also, the instantaneous conduction losses in the IGBTs are, as follows:

$$p_T(t) = 2V_T I_p \sin(\omega t) + 2R_T I_p^{\beta+1} \sin^{\beta+1}(\omega t). \tag{39}$$

The conduction losses of IGBTs of the mth H-bridge can be calculated by the following equation:

$$\begin{aligned} P_{T_m} &= \frac{1}{\pi} \int_{\varphi}^{\pi} p_{T_m}(t)\, d\omega t \\ &= \frac{2}{\pi} \left[V_{T_m} I_p (1 + \cos\varphi) \right. \\ &\quad \left. + R_{T_m} I_p^{\beta_m+1} \int_{\varphi}^{\pi} \sin^{\beta_m+1}(\omega t)\, d\omega t \right]. \end{aligned} \tag{40}$$

The total conduction losses of the mth H-bridge are, as follows:

$$P_{H_m cond} = P_{D_m} + P_{T_m}. \tag{41}$$

The total conduction losses of the proposed topology can be expressed by the following equation:

$$P_{cond} = \sum_{m=1}^{k} \left(P_{M_m cond} + P_{H_m cond}\right). \tag{42}$$

B. Calculation of Switching Losses

The switching losses are the power dissipation during turn-on and turn-off switching transitions. These losses are due to the imperfect switching of devices. The switching losses can be obtained by integrating the product of the voltage and the current waveforms on the switching period.

In the proposed topology, to have a safe operation of a MLM, all the switches should not turned off at the same time, since the MLM does not have a freewheeling path and therefore, severe voltages will appear across the devices. That is, when a switch turned off, another switch should be turned on (except the case of the zero voltage level). In the other hand, more than one switch cannot be on, because a short circuit would be occurred across dc voltage sources. As a result, a delay is considered between the bidirectional switches to avoid simultaneous conduction of two or more switches. However, since all the devices are turned off during this delay time and there is not any freewheeling path, again severe voltages will occur on the switching elements. Therefore, a turn-off R-C snubber is used across each bidirectional switch [24].

1) Turn-Off Losses: To calculate the turn-off losses, consider a bidirectional switch as shown in Fig. 3. Before turning off, this switch carries the output current I. At the end of this period, the output current is carried by n snubber circuits of the MLM and therefore, the voltage across this switch, is IR/n, since the snubber capacitor was initially discharged. Assuming that the device current changes linearly during turn-off period [24], the switching waveforms shown in Fig. 7 can be used.

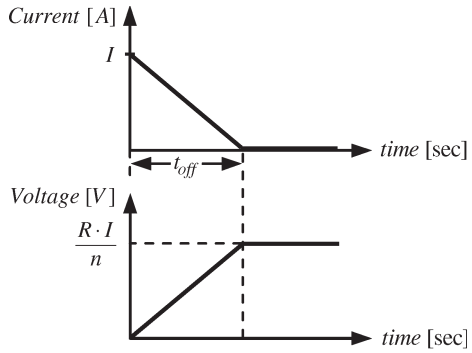

Fig. 7. Current and voltage waveforms of device during turn-off period.

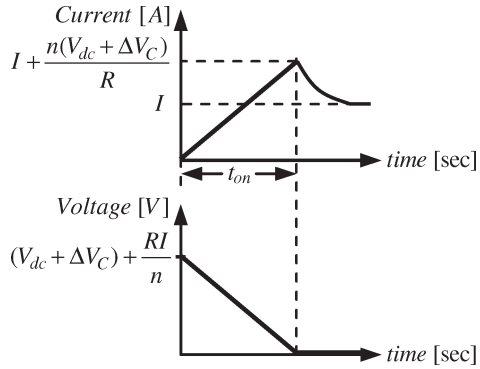

Fig. 8. Current and voltage waveforms of device during turn-on period.

The energy losses can be obtained by integrating the product of the voltage and current waveforms on the switching period, as follows:

$$E_{off} = \frac{I^2 R t_{off}}{6n} \tag{43}$$

where R is the snubber resistor and t_{off} is the fall time of the device and I is the RMS value of the output current.

In the MLM, each switch (except S_n) turns-off four times in each period of output voltage of corresponding cell. Therefore, the total turn-off energy losses for a MLM during any particular sequence can be expressed by the following equation:

$$\begin{aligned} E_{off\ T} &= (4n-2)E_{off} \\ &= \frac{(2n-1)}{3n} I^2 R t_{off}. \end{aligned} \tag{44}$$

The total power losses of mth MLM during the turn-off period is, as follows:

$$\begin{aligned} P_{offm} &= E_{off\ T} f_m \\ &= \frac{(2n-1)}{3n} I^2 R_m t_{off_m} f_m \end{aligned} \tag{45}$$

where, f_m is the output voltage frequency of mth cell and can be obtain, as follows:

$$f_m = (2n+1)^{k-m} f \tag{46}$$

where, k is the number of MLM and f is the output voltage frequency of the proposed topology. Using (45) and (46), the total turn-off losses of MLMs in the proposed topology can be calculated, as follows:

$$\begin{aligned} P_{off\ M} &= \sum_{m=1}^{k} P_{off\ m} \\ &= \sum_{m=1}^{k} \frac{(2n-1)(2n+1)^{k-m}}{3n} I^2 R_m t_{off_m} f. \end{aligned} \tag{47}$$

The unidirectional switches of the H-bridges do not require the snubber circuits. At the end of the turn-off period, the voltage across a unidirectional switch is equal to the sum of dc voltages of related MLM. Assuming that the device current changes linearly during the turn-off period, the total turn-off losses of hth H-bridge can be calculated, as follows:

$$P_{off\ h} = \frac{2}{3} n V_{dch} I f_h t_{off_h}. \tag{48}$$

The total turn-off losses of H-bridges are obtained, as follows:

$$\begin{aligned} P_{off\ H} &= \sum_{h=1}^{k} P_{off\ h} \\ &= \frac{2}{3} n V_{dc} I f \sum_{h=1}^{k} (2n+1)^{h-1} (4n)^{k-h} t_{off_h}. \end{aligned} \tag{49}$$

Then, the total turn-off losses of the proposed topology can be expressed by the following equation:

$$P_{off} = P_{off\ M} + P_{off\ H}. \tag{50}$$

2) Turn-On Losses: To determine the turn-on losses, consider the bidirectional switch shown in Fig. 3. Before the turn-on, the output current is flowing through n snubber circuits in parallel and the snubber capacitor associated with this switch is charged to $(V_{dc} + \Delta V_C)$, where V_{dc} is the dc voltage of the MLM. Therefore, the switch voltage is the sum of the capacitor voltage $(V_{dc} + \Delta V_C)$ and the voltage drop across the snubber resistor, RI/n. At the end of the turn-on period, the sum of the load current (I) and the peak snubber discharge current $(n(V_{dc} + \Delta V_C)/R)$ flow through the switch. Assuming again that the device current changes is linear during turn-on period [24], then the waveforms shown in Fig. 8 can be used. The energy losses are calculated in this switch during the turn-on period, as follows:

$$E_{on} = \left(V_{dc} + \Delta V_C + \frac{RI}{n}\right) \left(I + \frac{n(V_{dc} + \Delta V_C)}{R}\right) \frac{t_{on}}{6} \tag{51}$$

where, t_{on} is the rise time of the IGBT device and ΔV_C is equal to $I\tau/nC$. C is the snubber capacitor and τ is the delay time considered among drive signals of IGBTs to provide the safe commutation of switches.

In the MLM, each switch (except S_n) turns-on four times in each period. Therefore, the total power losses of mth MLM

during turn-on period are, as follows:

$$P_{on\ m} = E_{on\ m} \times 4n \times f_m = \frac{2}{3} t_{on\ m} f_m \left[\frac{n^2}{R_m} V_{dc\ m}^2 + 2n \left(1 + \frac{\tau_m}{R_m C_m} \right) I V_{dc\ m} + \left(R_m + \frac{2\tau_m}{C_m} + \frac{\tau_m^2}{n R_m C_m^2} \right) I^2 \right] \quad (52)$$

where, V_{dcm} is dc voltage source of mth MLM.

Using (46) and (52), the total turn-on losses of MLMs in the proposed topology can be calculated, as follows:

$$P_{on\ M} = \sum_{m=1}^{k} P_{on\ m}. \quad (53)$$

Using the same analysis of the turn-off state for H-bridges switches, the total turn-on losses of H-bridges in the proposed topology can be obtained, as follows:

$$P_{on\ H} = \sum_{h=1}^{k} P_{on\ h} = \frac{2}{3} n V_{dc} I f \sum_{h=1}^{k} (2n+1)^{h-1} (4n)^{k-h} t_{on_h}. \quad (54)$$

Then, the total turn-on losses of the proposed topology are the sum of MLMs and H-bridges turn-on losses, i.e.,

$$P_{on} = P_{on\ M} + P_{on\ H}. \quad (55)$$

Now, the total switching losses can be calculated as follows:

$$P_{sw} = P_{on} + P_{off}. \quad (56)$$

VI. Comparison of Proposed Topology With Topology Suggested in [19]

To compare with existing topologies, the number of bidirectional switches of MLMs in the proposed topology and blocks in the topology presented in [19] have been considered to be equal to two and three, respectively. Therefore, the maximum number of voltage levels will be produced. The proposed topology has an asymmetrical converter, then, the results are compared with the well-known asymmetrical cascaded multilevel converter. The most common type has dc voltage sources that scaled by the factor of three, hereafter called trinary configuration. The trinary configuration provides the maximum number of voltage levels with constant number of IGBTs.

Fig. 9 compares the number of IGBTs (N_{IGBT}) versus the number of output voltage levels (N_{level}) in the proposed topology, the topology presented in [19] and the trinary configuration. This comparison shows that the proposed topology needs fewer IGBTs than the topology presented in [19] for realizing N_{level} for v_o. It is important to note that the number of IGBTs and main diodes are the same. Although the trinary configuration produces high number of levels with less number of switches, but, less diversity for dc voltage sources is necessary in the proposed topology. In the next section, this subject will be discussed in detail. Fig. 10 shows the total blocking voltage on bidirectional switches. In the proposed topology is

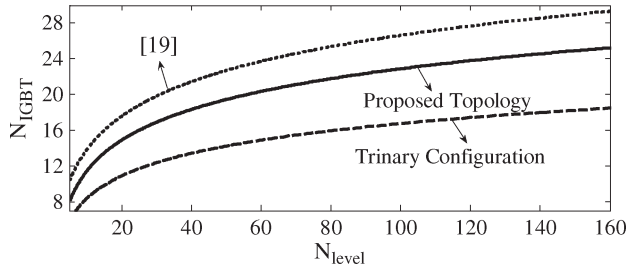

Fig. 9. Required number of IGBTs to realize N_{level} voltages in different topologies.

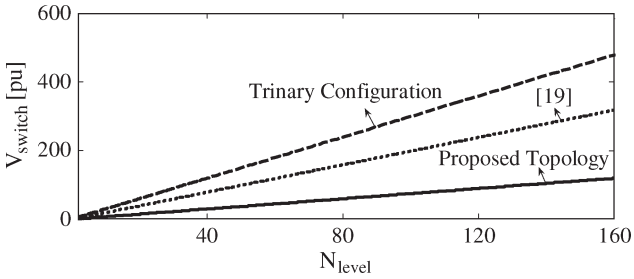

Fig. 10. Blocking voltages on bidirectional switches to realize N_{level} voltage levels in different topologies.

less than that recommended in [19] and trinary configuration for realizing N_{level} for v_o. In this figure, the structure of the proposed topology consists of two bidirectional switches in each MLM to provide maximum voltage levels. The blocking voltage on unidirectional switches in the proposed topology and [19] is equal. In the proposed topology, the blocking voltage on unidirectional switches in the full-bridge converters are proportional to maximum output voltage of adjoining MLM. But, in [19], it is proportional to maximum output voltage of the converter that restricts the industrial applications of the converter.

The maximum blocking voltage of switches in the proposed topology, topology presented in [19] and trinary configuration are shown in Fig. 11. In the optimized proposed topology, the MLMs have two bidirectional switches. So, the maximum blocking voltage is related to S_{k2} and equal to $2 \times 5^{k-1}$ (i.e., $N_{level}/2.5$). This figure shows that this voltage is less than the equivalent voltage of [19] and has a minor difference with trinary configuration. That is, if the optimized proposed topology is utilized, the voltage stress of the switches is not much more than the common asymmetric cascaded multilevel converters. Anyway, the major demerit of these topologies is the increase of the stress with increasing the number of levels. There are other topologies in the literatures that do not have this problem, such as symmetric cascaded multilevel converter and HVDC plus [25], formed by the cascaded connection of full bridges and half-bridges, respectively. In these topologies, the voltage stress of switches is equal to dc voltage of bridges and does not change with increasing the voltage levels. But, in comparison with the proposed topology, they use higher number of IGBTs, gate drivers and dc voltage sources. In the other hand, if the optimum proposed topology is used as symmetric one (equal dc voltage source in MLMs), the maximum voltage stress of

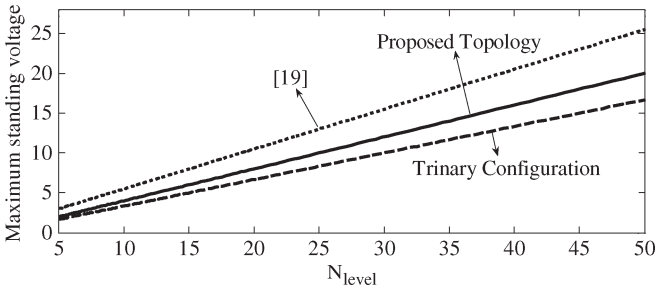

Fig. 11. Maximum blocking voltage of switches for different N_{level} in different topologies.

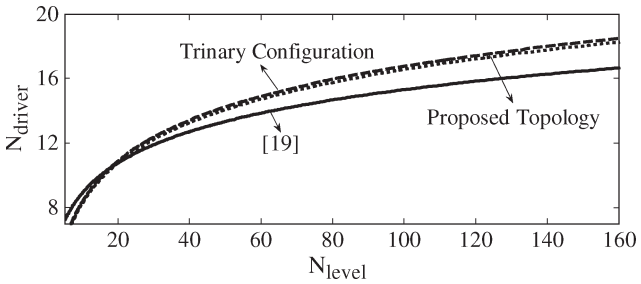

Fig. 12. Required number of gate driver circuits to realize N_{level} voltage levels in different topologies.

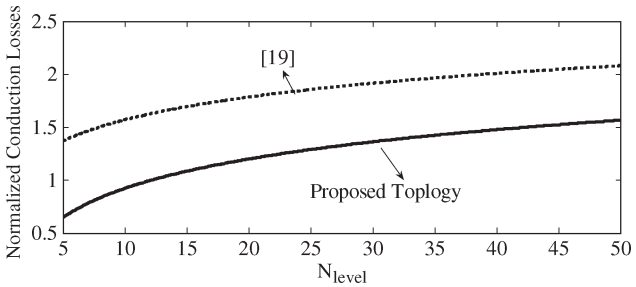

Fig. 13. Normalized conduction losses of switches versus N_{level}.

switches is equal to $2V_{dc}$, that is, comparable with the common symmetric topologies.

Fig. 12 shows the required number of gate driver circuits for realizing N_{level} of voltages for v_o in the proposed topology, topology presented in [19] and trinary configuration. This figure shows that the proposed topology required less number of gate driver circuits than [19] for N_{level} less than 20. For higher levels, the number of gate driver circuits increases. But, it is noticeable that the gate driver circuits are the electronic part of the circuit and has lower cost in comparison with power electronic components of the converter. Therefore, increasing the number of gate driver circuits is not a considerable deficiency. The proposed topology not only has lower number of switches and components in comparison with [19], but also its full-bridge converters operate in the lower voltage. Considering (31), the overall peak value of the blocking voltage of full-bridge converters in the proposed topology and [19] are the same, but in the topology presented in [19], this voltage is related to only one full-bridge converter.

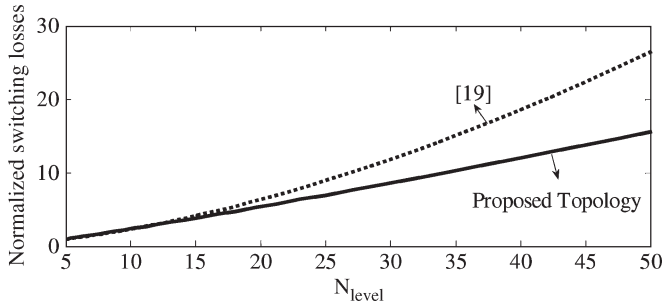

Fig. 14. Normalized switching losses of switches versus N_{level}.

Figs. 13 and 14 show the normalized conduction and switching losses, respectively, versus the number of output voltage levels for the proposed topology and the topology presented in [19]. To calculate the losses and possibility to compare proposed topology with other topology, it assumed that the switches used in all MLM and H-bridges of two topologies are the same. These comparisons show that the proposed topology has less conduction and switching losses than the others, especially for higher number of voltage levels.

VII. Design of Multilevel Converter Based on Proposed Topology

In this section, a typical single-phase multilevel converter with a minimum of 120 voltage levels and a peak value of 400V should be designed. The on-state voltage drops of the switches have been neglected. The optimal multilevel structure is presented in Fig. 15(a) for the minimum number of used switches. As shown in this figure, the number of IGBTs and capacitors are 24 and 6, respectively. In this design, the number of voltage levels is 125. The optimal structure based on the minimum number of capacitors is similar to Fig. 15(a). The optimal structure based on the minimum number of gate driver circuits is shown in Fig. 15(b). In this structure, the number of gate driver circuits is 21 and the number of voltage levels is 343.

The structure of optimal multilevel with minimum used switches based on the recommended topology of [19] is presented in Fig. 16(a). The number of IGBTs and capacitors are 28 and 8, respectively, and the number of voltage levels is 161. The optimal multilevel structure with minimum used gate driver circuits based on the topology presented in [19] is presented in Fig. 16(b). The number of IGBTs and capacitors are 28 and 6, respectively, and the number of voltage levels is 127. The number of gate driver circuits is 16.

The design example by a trinary configuration of cascaded multilevel inverter with five series-connected cells is possible using 20 IGBTs. In this case, the number of voltage levels is 243. In trinary configuration, five dc voltage sources with different amplitudes should be used. But, three different dc voltage sources is need in the proposed topology.

The blocking voltages of the bidirectional and unidirectional switches in Fig. 15(a) are 604.5 V and 806 V, respectively. These are 917.7 V and 786.6 V in Fig. 15(b). The blocking

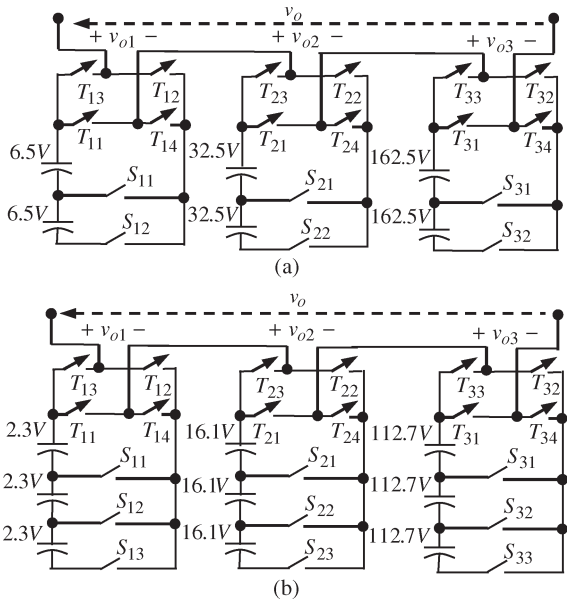

Fig. 15. Optimal multilevel structure with minimum used (a) switches (b) gate driver circuits.

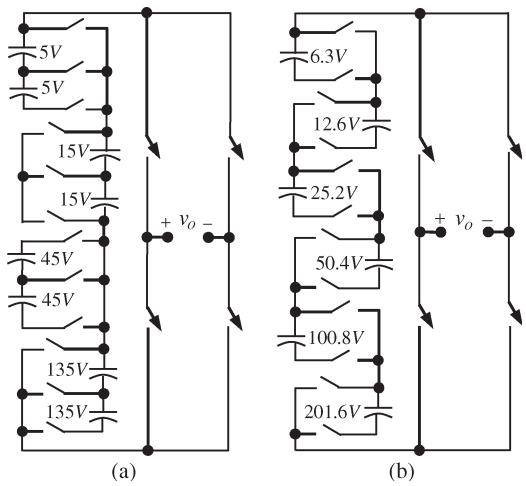

Fig. 16. Optimal multilevel structure with minimum (a) used switches and (b) gate driver circuits based on topology of [19].

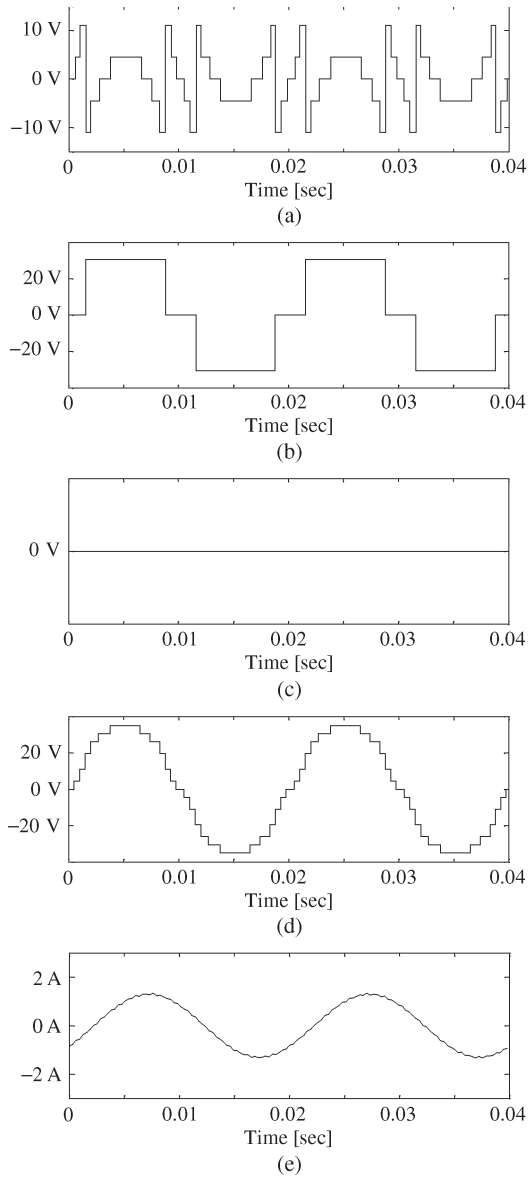

Fig. 17. Experimental results; (a) output voltage of first full-bridge (v_{o1}); (b) output voltage of second full-bridge (v_{o2}); (c) output voltage of third full-bridge (v_{o3}); (d) converter output voltage (v_o); and (e) converter current.

voltages of the bidirectional and unidirectional switches in Fig. 16(a) are 1000 V and 800 V, respectively. These are 793.8 V and 793.8 V in Fig. 16(b).

VIII. Experimental Results

To evaluate the performance of the proposed multilevel converter in the generation of a desired output voltage waveform, a single-phase 125-level multilevel converter prototype is implemented based on the proposed topology shown in Fig. 15(a). The IGBTs are BUP306D with internal anti-parallel diodes. The 89C52 microcontroller of ATMEL Company has been used to generate the switching patterns. The required dc voltage sources have been provided by cascaded connection of dc power supplies. There are several modulation techniques for multilevel converters [26]–[30]. In this paper, the fundamental frequency switching technique has been used. The main object of the control strategy is to synthesis the output voltage that minimizes the error with respect to the reference voltage. It is important to note that the calculation of optimal switching angles for the elimination of the selected harmonics or the minimization of the total harmonic distortion (THD) is not the objective of this work.

In the experimental case, the waveforms of the output voltages, produced by different full-bridges, and the output current have been studied. In this regard, the converter has been adjusted to produce a 50 Hz, 13-level staircase waveform. In this test, the load is a series R-L load ($R = 20\ \Omega$ and $L = 55$ mH). The result of this test is shown in Fig. 17. As shown in this figure, the ac output of each full-bridge is connected in series such that the synthesized voltage waveform is the sum of the outputs of the full-bridge. Considering the output voltage and

current waveforms, it is obvious that there is a phase difference between voltage and current waveforms, due to the inductive behavior of the load. The Fourier series expansion of the stepped output voltage waveform of the multilevel converter, as shown in Fig. 17(d), have a fundamental frequency and an infinite number of odd harmonics [28]. It can be seen that the output current is almost sinusoidal. Since the load of the converter (R-L) behaves as a low-pass filter. In this case, the THDs of the output voltage and current based on simulation results (using PSCAD/EMTDC software) are %5.9 and %0.64, respectively. To generate a desired output with best quality of the waveform, the number of the voltage steps should be increased or another appropriate switching technique should be used.

IX. Conclusion

A new basic multilevel module (MLM) for the multilevel converter has been proposed. The proposed topology is a combination of MLMs and full-bridges converter. The proposed topology extends the design flexibility and the possibilities to optimize the converter for various objectives. It has been shown that the structure, consisting of MLMs with two switches has the minimum number of switches for a given number of voltage levels. The proposed topology has been compared with other topology. It has been shown that the proposed topology provides 125 levels on the output voltage with a peak of 400 V, using 24 IGBTs and the blocking voltage of 604.5 V on bidirectional switches. But, the other topology produces 161 voltage levels using 28 IGBTs and a blocking voltage of 1000 V. The proposed topology not only has lower switches and components in comparison with other one, but also its full-bridge converters operate in the lower voltage. The operation and performance of the proposed topology has been experimentally verified on a single-phase 125-level multilevel converter prototype. Reduction of the power losses of the proposed topology in comparison other topology is another advantage of the proposed converter. The proposed topology can be a good solution for applications that require high power quality, or applications that have considerable numbers of dc voltage sources.

References

[1] J. Rodriguez, B. Wu, S. Bernet, J. Pontt, and S. Kouro, "Multilevel voltage source converter topologies for industrial medium voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium voltage multilevel converters—State of the art, challenges and requirements in industrial applications," *IEEE Trans. Ind. Electron*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[3] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *J. Energy Convers. Manag.*, vol. 50, no. 11, pp. 2761–2767, Nov. 2009.

[4] E. Babaei and M. S. Moeinian, "Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem," *J. Energy Convers. Manag.*, vol. 51, no. 11, pp. 2272–2278, Nov. 2010.

[5] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[6] T. A. Meynard and H. Foch, "Multi-level choppers for high voltage applications," in *Proc. Eur. Conf. Power Electron. Appl.*, 1992, vol. 2, pp. 45–50.

[7] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non conventional power converter for plasma stabilization," in *Proc. Power Electron. Spec. Conf.*, 1988, pp. 122–129.

[8] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, Jul./Aug. 2007.

[9] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 543–550, Mar. 2008.

[10] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos, and F. Richardeau, "Survey on fault operation on multilevel inverters," *IEEE Trans. Ind. Electron*, vol. 57, no. 7, pp. 2207–2218, Jul. 2010.

[11] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1517–1526, Jun. 2010.

[12] C. Rech and J. R. Pinheiro, "Hybrid multilevel converters: Unified analysis and design considerations," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 1092–1104, Apr. 2007.

[13] C. Rech and J. R. Pinheiro, "Line current harmonics reduction in multipulse connection of asymmetrically loaded rectifiers," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 640–652, Jun. 2005.

[14] S. Lu, S. Marieethoz, and K. A. Corzine, "Asymmetrical cascade multilevel converters with noninteger or dynamically changing dc voltage ratios: Concepts and modulation techniques," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2411–2418, Jul. 2010.

[15] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[16] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[17] M. T. Haque, "Series sub-multilevel voltage source inverters (MLVSIs) as a high quality MLVSI," in *Proc. SPEEDAM*, 2004, pp. F1B-1–F1B-4.

[18] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of DC voltage sources and switches in asymmetrical multilevel converters using a novel topology," *J. Elect. Power Syst. Res.*, vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[19] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[20] G. Su, "Multilevel dc-link inverter," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 848–854, May/Jun. 2005.

[21] P. Lezana and J. Rodriguez, "Mixed multicell cascaded multilevel inverter," in *Proc. ISIE*, 2007, pp. 509–514.

[22] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.

[23] T. J. Kim, D. W. Kang, Y. H. Lee, and D. S. Hyun, "The analysis of conduction and switching losses in multi-level inverter system," in *Proc. Power Eletron. Spec. Conf.*, 2001, pp. 1363–1368.

[24] S. Sunter and H. Altun, "A method for calculating semiconductor losses in the matrix converter," in *Proc. MELECON*, 1998, pp. 1260–1264.

[25] K. Friedrich, "Modern HVDC PLUS application of VSC in modular multilevel converter topology," in *Proc. ISIE*, 2010, pp. 3807–3810.

[26] Y. Liu, H. Hong, and A. Q. Huang, "Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2249–2258, Jun. 2009.

[27] J. I. Leon, S. Vazquez, S. Kouro, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Unidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2981–2986, Aug. 2009.

[28] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded H-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2691–2699, Aug. 2010.

[29] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[30] D. C. Ludois, J. K. Reed, and G. Venkataramanan, "Hierarchical control of bridge-of-bridge multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2679–2690, Aug. 2010.

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