A New Interleaved Three-Phase Single-Stage PFC AC-DC Converter

M. Narimani, *Student Member, IEEE,* G. Moschopoulos, *Senior Member, IEEE*

***Abstract*— A new interleaved single-stage ac-dc converter is proposed in this paper to reduce line current harmonics while achieving power factor correction. The proposed rectifier can produce input currents that do not have deadband regions with high power factor correction, continuous output current and minimize the input EMI filter size. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with experimental results obtained from a prototype.**

***Index Terms*— AC–DC power conversion, three-phase, single-stage power factor correction (SSPFC), three-level converters.**

I. INTRODUCTION

Power factor correction (PFC) is needed in ac-dc power supplies for them to comply with harmonic standards such as IEC 1000-3-2 [1]-[3]. Although it is possible to satisfy these standards by adding passive filter elements to the traditional passive diode rectifier/LC filter input combination, the resulting converter would be very bulky and heavy due to the size of the low-frequency inductors and capacitors. The most common approach to PFC is to use two-stage power conversion schemes. These two-stage schemes use a front-end ac-dc converter stage to perform ac-dc conversion with PFC with the output of the front-end converter fed to a back-end dc–dc converter stage that produces the desired isolated dc output voltage [4]. Using two converter stages in this manner, however, increases the cost, size, and complexity of the overall ac-dc converter and this has led to the emergence of single-stage power-factor-corrected (SSPFC) converters.

In order to reduce the cost, size, and complexity associated with two-stage ac-dc power conversion and PFC researchers have tried to propose single-stage converters that integrate the functions of PFC and isolated dc-dc conversion in a single power converter. Several single-phase [5]-[11] and three-phase [12]-[25] converters have been proposed in the literature, with three-phase converters being preferred over single-phase converters for higher power applications.

Previously proposed three-phase single-stage ac-dc converters, however, have at least one of the following drawbacks that have limited their widespread use:

- They are implemented with three separate ac-dc single-stage modules [13]-[15].
- The converter components are exposed to very dc bus high voltages so that switches and bulk capacitors with very high voltage ratings are required [17], [18], [22], [23].
- The input currents are distorted and contain a significant amount of low frequency harmonics because the converter has difficulty performing PFC and dc-dc conversion simultaneously [16].
- The converter must be controlled using very sophisticated techniques and/or non-standard techniques [5]-[11]. This is especially true of resonant type converter that need variable switching frequency control methods to operate.
- The output inductor must be very low, which makes the output current to be discontinuous. This results in a very high output ripple so that secondary diodes with high peak current ratings and large output capacitors to filter the ripple are needed [13]-[20].
- Most of them are DCM at input and need to have a large input filter to filter out large high-frequency harmonics [13]-[15], [17], [18],[22]-[25].

The authors proposed a three-phase, single-stage three-level converter to mitigate these drawbacks in [25], which was published in the Transactions on Industrial Electronics. Although the converter proposed in that paper was an advance over previously proposed three-phase single-stage converters, it still suffered from the need to have a discontinuous output inductor current at light load conditions to keep the DC bus capacitor voltage < 450V and it needed to operate with discontinuous input current, which resulted in high component current stress and the need for significant input filtering due to the large amount of ripple.

This paper presents a new interleaved three-phase, single-stage rectifier that does not have any of these drawbacks. The work presented in this paper can be considered to be follow-up work in relation to what was presented in [25]. In comparison to the converter presented in [25], the converter presented in this paper has an interleaved structure, requires two fewer diodes in the dc bus, has an output current which is continuous for all load ranges, has a dc bus voltage that is less than 450 for all load conditions and has a much better input current

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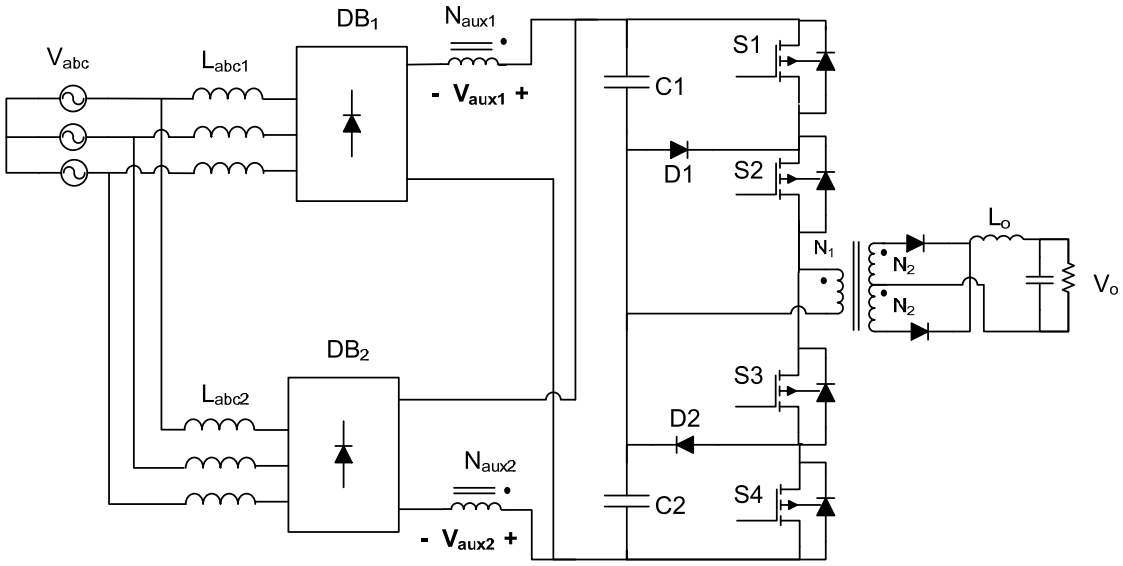


Fig. 1. Proposed interleaved three-phase three-level converter.

harmonic content. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with experimental results obtained from a prototype.

II. Converter Operation

The proposed converter and its key waveforms are shown in Fig. 1 and 2. The proposed converter uses auxiliary windings that are taken from the converter transformer to act as "magnetic switches" to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. When the primary voltage of the main transformer is positive, Auxiliary Winding 1 ($N_{aux1}/N1=2$) cancels out the dc bus voltage so that the output voltage of Diode Bridge 1 (DB_1) is zero and the currents in input inductors L_{a1}, L_{b1}, and L_{c1} rise. When the primary voltage of the main transformer is negative, Auxiliary Winding 2 ($N_{aux2}/N1=2$) cancels out the dc bus voltage so that the output voltage of Diode Bridge 2 (DB_2) is zero and the currents in input inductors L_{a2}, L_{b2}, and L_{c2} rise. When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridges and the input currents falls since this voltage is greater than the input voltage. If the input currents are discontinuous, the envelope of the input current will be sinusoidal and in phase with the input voltages.

The converters modes of operation are explained in this section. Typical converter waveforms are shown in Fig. 2. The equivalent circuit in each stage is shown in Fig. 3.The converter goes through the following modes of operation:

Mode 1 ($t_0 < t < t_1$) (Fig. 3(a)):

During this interval, switches S_1 and S_2 are ON. In this mode, energy from dc bus capacitor C_1 flows to the output load. Due to magnetic coupling, a voltage appears across Auxiliary Winding 1 which is equal to dc bus voltage but has opposite

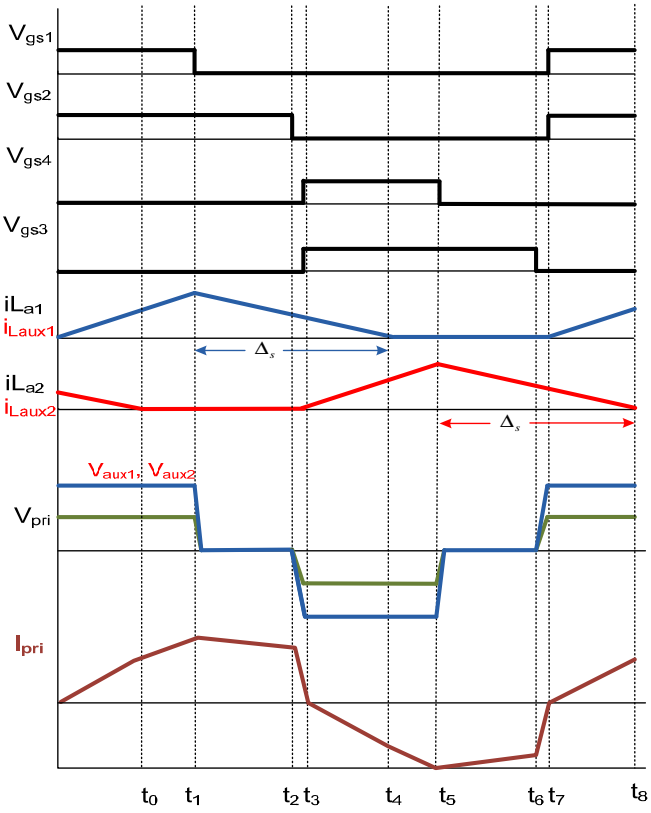
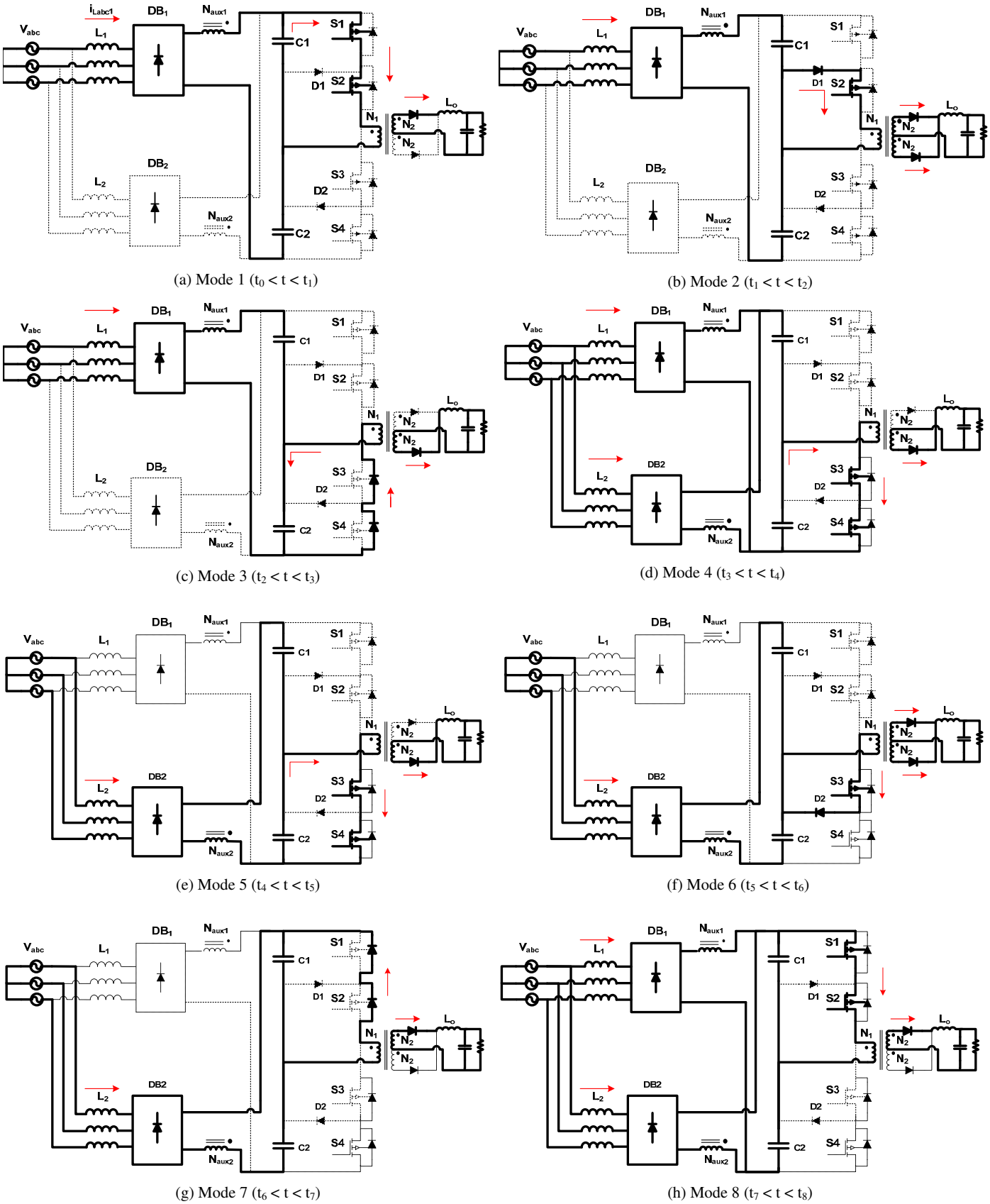


Fig. 2. Typical waveforms describing the modes of operation.

polarity and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero and the input currents in L_{a1}, L_{b1}, and L_{c1} rise.



(a) Mode 1 ($t_0 < t < t_1$)

(b) Mode 2 ($t_1 < t < t_2$)

(c) Mode 3 ($t_2 < t < t_3$)

(d) Mode 4 ($t_3 < t < t_4$)

(e) Mode 5 ($t_4 < t < t_5$)

(f) Mode 6 ($t_5 < t < t_6$)

(g) Mode 7 ($t_6 < t < t_7$)

(h) Mode 8 ($t_7 < t < t_8$)

Fig. 3. Modes of operation.

Mode 2 ($t_1 < t < t_2$) (Fig. 3(b)):
In this mode, S_1 is OFF and S_2 remains ON. The energy stored in L_1 ($L_1 = L_{abc1}$) during the previous mode starts to transfer into the dc bus capacitors. The voltage appears across Auxiliary Winding 1 is zero. The primary current of the main transformer circulates through D_1 and S_2. With respect to the converter's output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to $-V_L$.

Mode 3 ($t_2 < t < t_3$) (Fig. 3(c)):
In this mode, S_1 and S_2 are OFF. The energy stored in L_1 still is transferring into the dc bus capacitor. The primary current of the transformer charges C_2 through the body diodes of S_3 and S_4. Switches S_3 and S_4 are switched ON at the end of this mode.

Mode 4 ($t_3 < t < t_4$) (Fig. 3(d)):
In this mode, S_3 and S_4 are ON and energy flows from the capacitor C_2 into the load. The voltage appears across Auxiliary Winding 2 which is equal to dc bus voltage but acts like a magnetic switch and cancels out the dc bus voltage. The voltage across the boost inductors L_2 ($L_2 = L_{abc2}$) becomes only the rectified supply voltage of each phase and the current flowing through each inductor increases. This mode ends when the energy stored in L_1 completely transfers into the dc bus capacitor. For the remainder of the switching cycle, the converter goes through Modes 1 to 4, but with S_3 and S_4 ON instead of S_1 and S_2 and DB_2 instead of DB_1.

Mode 5($t_4 < t < t_5$) (Fig. 3(e)):
In this mode, S_3 and S_4 are ON and a symmetrical period begins. In this mode, energy flows from the capacitor C_2 into the load. The voltage across the boost inductors L_2 becomes only the rectified supply voltage of each phase and the current flowing through each inductor increases.

Mode 6 ($t_5 < t < t_6$) (Fig. 3(f)):
In this mode, S_3 is ON and S_4 is OFF and the primary current of the main transformer circulates through the diode D_2 and S_3. The energy stored in the boost inductors L_2 during the previous mode starts transferring into the dc bus capacitor. The output inductor current also freewheels in the secondary of the transformer during this mode.

Mode 7 ($t_6 < t < t_7$) (Fig. 3(g)):
In this mode, S_3 and S_4 are OFF and the primary current of the transformer charges the capacitor C_1 through the body diodes of S_1 and S_2. The energy stored in the boost inductors L_2 transfers into the dc bus capacitor.

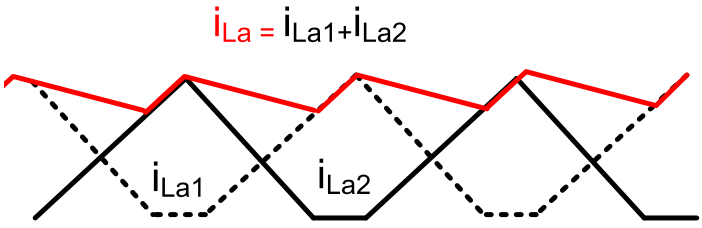


Fig.4. Interleaving between two input inductor currents.

Mode 8 ($t_7 < t < t_8$) (Fig. 3(h)):
In this mode, S_1 and S_2 are ON. In this mode, energy from dc bus capacitor C_1 flows to the output load. This mode ends when energy in inductors L_2 completely transfer into the dc bus. Time t_8 is the end of the switching cycle and another switching cycle begins with the same modes.

It should be noted that input current is summation of inductor currents i_{L1} and i_{L2} which are both discontinuous. However, by selecting appropriate values for L_1 ($= L_{a1} = L_{b1} = L_{c1}$) and L_2 ($= L_{a2} = L_{b2} = L_{c2}$) in such a way that two inductor currents such as i_{La1} and i_{La2} have to overlap each other, the input current can be made continuous as shown in Fig. 4; thus reducing the size of input filter significantly. There is a naturally 180^o phase difference between the currents in L_1 and the currents in L_2 as one set of currents rises when the transformer primary is impressed with a positive voltage and the other set rises when the transformer primary is impressed with a negative voltage – these two events occur 180^o apart during a switching cycle.

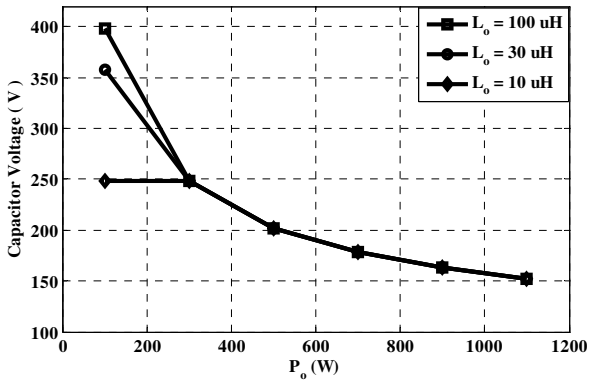
III. Converter Analysis and Design

The analysis and the design of the proposed interleaved converter are almost identical to that presented in [25] and therefore are not presented here. Readers are referred to [25] for details. In this paper, only differences in the analysis and the design are presented.

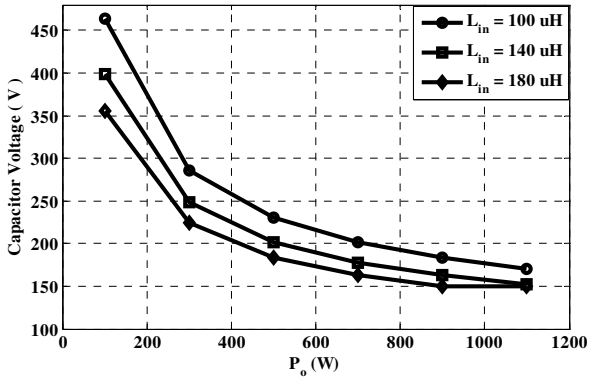
With respect to analysis, steady-state operating points are identified using a computer program such as the one presented in [25]. The only difference between the analysis of the proposed converter and the one in [25] is the analysis and design of the input inductors. In the proposed interleaved converter, there are two set of inductors (L_1 and L_2) at the input side, with each set conducting half the current. The analysis needs to consider the current in both these sets instead of just one.

The value for L_1 and L_2 should be low enough to ensure that their currents are fully discontinuous under all operating conditions, but not so low as to result in excessively high peak currents. The worst-case to be considered is the case when the converter operates with minimum input voltage and maximum load since if the input current in each set of inductor is discontinuous under these conditions, it will be discontinuous for all other operating conditions and thus an excellent power factor will be achieved.

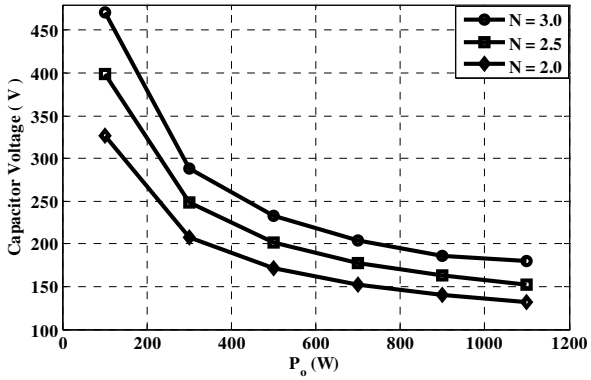
Based on the results of the analysis, graphs of steady-state characteristics, such as the ones shown in Fig. 5 can be drawn and then used as part of a design procedure, just like what was presented in [25]. Although the design procedure of the two converters is the same, what should be noted when comparing graphs of steady-state characteristics for the two converters is that it is much easier to design the converter in such as way that the DC bus voltage is not excessive (< 800 V). It is the fact that the DC bus voltage is not excessive that allows for greater flexibility in the design of the converter such as a greater output inductor, which results in less output current ripple.



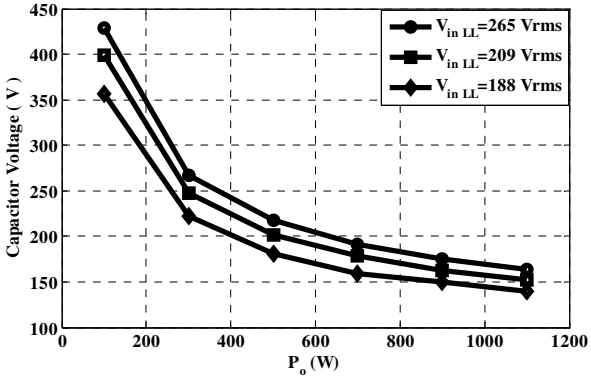
a. Effect of output inductor value L_o on dc bus voltage



b. Effect of input Inductor value L_{in} on dc Bus Voltage



c. Effect of transformer ratio value N on dc bus voltage



d. Effect of input voltage v_{in} on dc bus voltage

Fig.5. Steady-State characteristic curves (V_{in}=208V_{rms}, Vo=48V, f_{sw}=100kHz).

IV. Experimental Results and Converter Comparison

An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications:

Input voltage V_{in} = 208±10% Vrms (line-line),
Output voltage V_o = 48 V,
Output power P_o = 1.1kW,
Switching frequency f_{sw} = 100 kHz.

Typical converter waveforms are shown in Fig. 6. It can be seen that the proposed converter can operate with nearly sinusoidal input currents with no deadband regions. It is a multilevel full-bridge converter that the switch stresses is half the dc bus voltage; it also can operate with a continuous output current, unlike most other converters of the same type.

Experimental results obtained for the proposed converter

Table I: Comparison of elements for non-interleaved and interleaved converters

Components	Converters	
	Non-interleaved three-level PFC converter	**Interleaved** three-level PFC converter
S_1-S_4	4 * FDL100N50F - 500V	
Clamp diodes	2 * MUR 860	
Rectifire diodes	DSSK60-02A	
Auxiliary rectifire diodes	DSI45-16A	-
Diode bridge	2 * SC50VB80-G	SC50VB80-G
Bus Capaciotrs	2 * 2200 uF	
Input boost indutor	80 µH	2 * 140 µH
Input filter inductor	3 * 20 µH	-
Input filter capacitor	3 * 1 µF	-
Output filter inductor	15 µH	100 µH
Output filter capacitor	450µF	450µF
Transformer turns ratio	25:10:10	25:10:10

Table II: Comparison of features for non-interleaved and interleaved converters

Parameters	Converters	
	Non-interleaved three-level PFC converter	**Interleaved** three-level PFC converter
ΔV_o(pk-pk)	1.2 V	0.06 V
ΔI_o(pk-pk)	7.5 A	0.8 A
D_{max}	0.61	0.77
$V_{bus,max}$	533	302
THD of input current	2.9 %	0.8 %

are compared to the converter proposed in [25], as shown in Tables I and II. The converter in [25] is a single-stage three-level PFC converter and is non-interleaved version of the proposed converter with just one set of input inductors instead of two. The output inductor current in [25] was designed to be continuous for heavy loads and discontinuous for light loads to keep the dc bus voltage less than 450V.

Compared to the non-interleaved converter that was presented in [25], the interleaved converter that is proposed in this paper has several advantages in addition to reduced input current ripple. The proposed converter can operate with continuous current at the output from 10% of full load to full load, which makes the output current have less ripple. This is because, the proposed converter has an interleaved structure that results in a change of energy equilibrium at the dc bus (the net equivalent inductance at the input is larger in the proposed converter), which makes the dc bus small enough to permit the output inductor to be sufficiently large.

A larger output inductor means that there is considerably less ripple in the output inductor current of the interleaved converter than there is in the non-interleaved converter proposed in [25]. This helps reduce secondary component stresses and filtering. It should be noted that the converter has been implemented with an output inductor that is larger than necessary to show that the proposed converter can operate with continuous output current and a primary-side dc bus voltage that is not excessive.

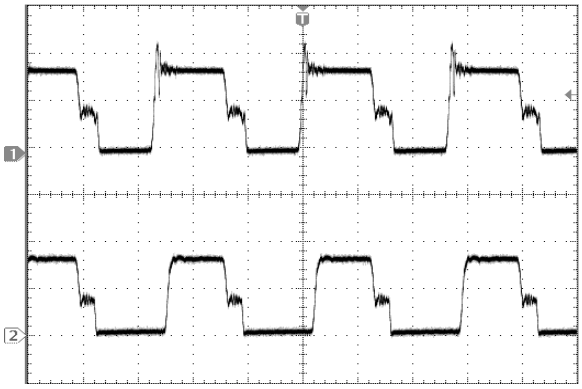
It should also be noted that no additional input filtering was used for the proposed interleaved converter and the input current waveform shown in Fig. 6(c) is just the summation of an input phase current of Diode Bridge 1 and the corresponding phase current of Diode Bridge 2.

Fig. 7 shows efficiency of the proposed converter at various output power. It should be noted that the proposed converter has a higher efficiency than the converter proposed in [25]. This is because it does not have any diode in the DC link whereas the converter proposed in [25] must have. It is also due to the fact that the switch voltage turn-on losses have been reduced considerably as there is much less voltage across the switch, it is because the proposed converter has much less dc bus voltage in compare to [25] (Table II).

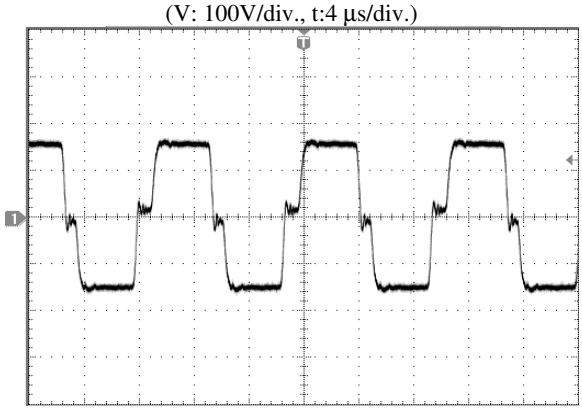
Fig. 8 and 9 show the input current harmonics a P_o =1.1kW and P_o =550 W and V_{in} = 220 $V_{l\text{-}l}$rms. It can be seen that the converter's harmonics are below the harmonic levels that are specified by the IEC 1000-3-2 standard.

V. CONCLUSION

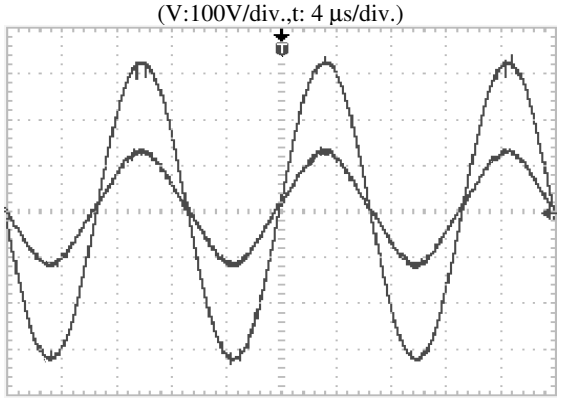
A new three-phase, three-level, single-stage power-factor-corrected ac/dc converter with interleaved input was proposed in this paper. The converter operates with a single controller to regulate the output voltage and uses auxiliary windings taken from its power transformer as magnetic switches to cancel the dc bus voltage so that the input section operates like a boost converter. The proposed converter has the following features:



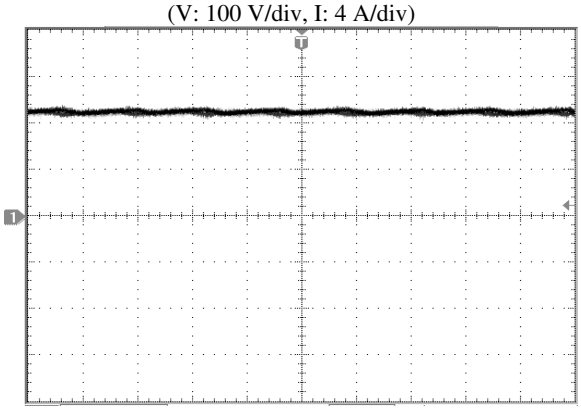
(a) Top switch voltages V_{ds1} and V_{ds2}
(V: 100V/div., t:4 μs/div.)



(b) Primary voltage of the main transformer
(V:100V/div.,t: 4 μs/div.)



(c) Input current and voltage
(V: 100 V/div, I: 4 A/div)



(d) Output inductor current
(I:10A/div., t: 4 μs/div.)

Fig. 6. Experimental results.

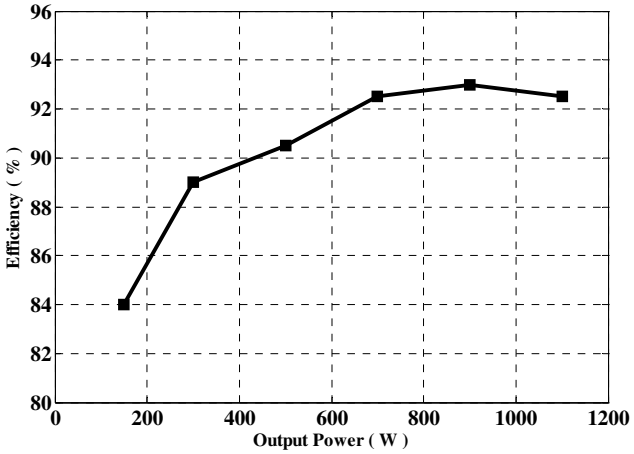


Fig.7. Efficiency of the proposed converter at various output power

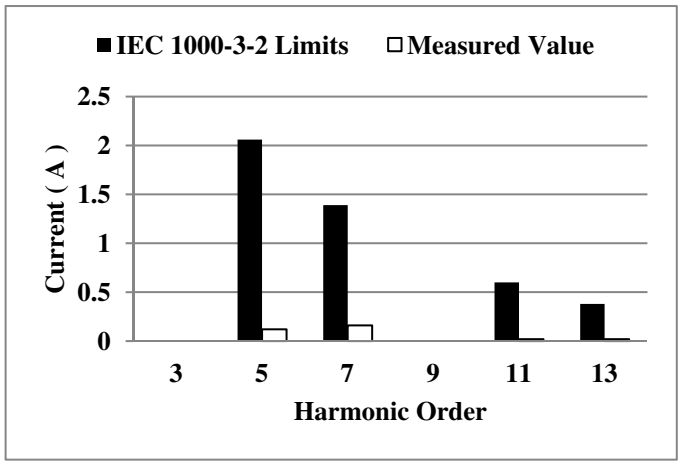


Fig.8. Input current harmonic at V_{in} = 220V_{rms}(l-l) , P_o=1.1 KW compared to IEC1000-3-2 standard.

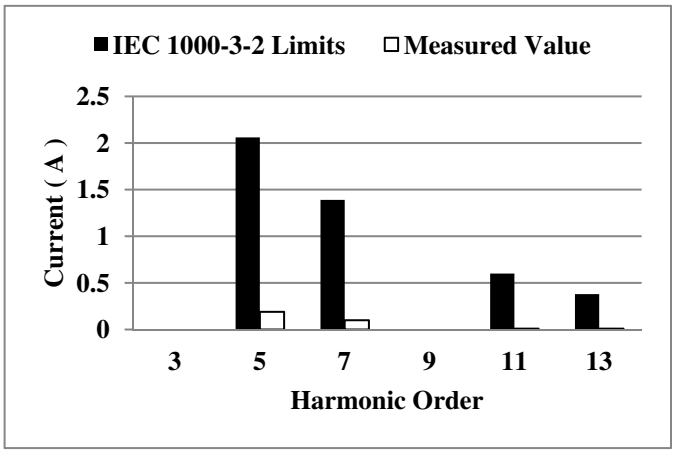


Fig.9. Input current harmonic at V_{in} = 220V_{rms}(l-l) , P_o=0.55 KW compared to IEC1000-3-2 standard.

- The proposed converter can operate with lower peak voltage stresses across its switches and the dc bus capacitors as it is a three-level converter. This allows for greater flexibility in the design of the converter and ultimately improved performance.
- The proposed converter can operate with an input current harmonic content that meets the EN61000-3-2 Class A standard with reduced input filter due to the interleaved structure.
- The output inductor of the proposed converter can be designed to work in CCM mode over a wide range of load variation and input voltage. This results in a lower output inductor current ripple than that found in previously proposed converters which helps reduce secondary component stresses and filtering.
- The above features are all an improvement on the original non-interleaved converter that was presented in [25]. Moreover, the proposed interleaved converter operates with greater efficiency than the converter proposed in [25] because it has fewer diodes in the dc bus and it has less turn-on losses.

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Mehdi Narimani (S'09) received the B.S. and M.S degrees from Isfahan University of Technology (IUT) in Isfahan, Iran in 1999 and 2002 respectively, all in electrical engineering. From 2002 to 2009 he was a lecturer in Isfahan University of Technology, Isfahan, Iran. He is currently a Ph.D. student in the Department of Electrical and Computer Engineering at the University of Western Ontario in London, Ontario, Canada.

Gerry Moschopoulos (S'90–M'96-SM'09) received the B.Eng., M.A.Sc., and Ph.D. degrees from Concordia University, Montreal, QC, Canada, in 1989, 1992, and 1997, respectively, all in electrical engineering. From 1996 to 1998, he was a Design Engineer in the Advanced Power Systems Division, Nortel Networks, Lachine, Canada. From 1998 to 2000, he was a Postdoctoral Fellow at Concordia University, where he was engaged in research in the area of power electronics for telecommunications applications. He joined the Department of Electrical and Computer Engineering at the University of Western Ontario, London, ON, Canada in 2000 and is currently an Associate Professor there. Dr. Moschopoulos is a Registered Professional Engineer in the province of Ontario.