Modular Multilevel Inverter with New Modulation Method and Its Application to Photovoltaic Grid-Connected Generator

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***Abstract*—This paper proposed an improved Phase Disposition Pulse Width Modulation (PDPWM) for Modular Multilevel Inverter which is used for PV grid-connection. This new modulation method is based on Selective Virtual Loop Mapping (SVLM), to achieve dynamic capacitor voltage balance without the help of an extra compensation signal. The concept of virtual sub-module is first established, and by changing the loop mapping relationships between the virtual sub-modules and the real sub-modules, the voltages of the upper/lower arm capacitors can be well balanced. This method does not requiring sorting voltages from highest to lowest, and just selectively take out the corresponding MIN and MAX capacitor voltage's index which makes it suitable for MMC with a large number of sub-modules in one arm. Compared to Carrier Phase-shifted PWM (CPSPWM), this method is more easily to be realized in FPGA and has much stronger dynamic regulation ability, and is conducive to the control of circulating current. Its feasibility and validity have been verified by simulations and experiments.**

***Index Terms*—Modular Multilevel Converter (MMC), Phase Disposition PWM (PDPWM), Selective Virtual Loop Mapping (SVLM), dynamic voltage balance, PV Grid-Connected.**

I. Introduction

In recent years, with the development of large-scale PV power plant system, as well as smart grid and multi-level technologies, higher requirements in voltage level, modular structure, flexibility and reliability of the next generation large-scale PV grid-connected inverter have been put forward [1]. The features include: 1) Power peaking capacity. PV systems should be able to store the electrical energy which is issued by itself as needed during a load trough; meanwhile, this part of the electrical energy would be released again for the load when the load is at the peak. As a result, the peak power of the grid and the reliability of power supply can be improved. 2) Fault ride-through capacity. Large-scale PV system has been required to have the ability to withstand short periods of voltage abnormality, such as the voltage short-term drop caused by short-circuit fault. PV system should maintain the link of the inverter and the grid as well as provide support to the grid [2]. 3) Power quality control. More stable power supply performance could be achieved by introducing suitable inverter control strategy including voltage stability, phase regulation, and active filter [3], etc. 4) Higher redundancy and error correction capacity. PV system should have the capacity to work efficiently when the failure occurs in some of the modules of the inverter system and "smart" enough to correct the situation.

The aforementioned requirements drive the research and development of next generation PV inverter[1], and the topologies of utility PV inverters are moving towards multilevel structure[4] -[5], which could provide better harmonic spectra and reduces the weight of the filtering components. In many of the multilevel structures, Modular Multilevel Converter (MMC) has attracted many researchers recently. By now, MMC-related application research has mostly concentrated on high-voltage direct current transmission [6], high-power motor drives [7], integrated energy storage [8], and medium-voltage STATCOM [9]. Modular multilevel converter used in PV grid-connected system is just mentioned in [10] - [11]. The reasons of this situation are: 1) MMC related research is mostly in theoretical research stage [12]-[13]; 2) The particularity of the photovoltaic power generation. PV panels are intermittent sources and their output voltages would be varied all the time, the DC link's voltage has to be regulated to keep them working in Maximum Power Point Tracking (MPPT) status. 3) The dynamic voltage balance has to be considered in multilevel PWM modulation, while, the system's stability would be damaged by adding improper signals to the reference voltage [14]. 4) The unique circulating current of MMC will increase the system losses and is not conducive to improving the efficiency of the inverter output [15]-[16], and the most important thing is that the uncontrolled circulating current is a big threaten to the security of MMC.

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Among them, the first two points seem not big problems, because as a new modular converter for medium and high voltage applications, MMC has been tested and works well in back-to-back structure and has much better four-quadrant performance. So the third and fourth points are the key to MMC's utility in PV inverter. Many papers have discussed MMC modulation methods. The Amplitude Modulation [17] –[18] has been widely used in HVDC system, its core idea is to first calculate how many sub-modules should be put into action, and the capacitors' voltage sorting and the final working sequence should be determined by the direction of the arm current. The method is simple and practical, but there are frequent sorting issues with the capacitor voltage which would be a burden to the controller if the number of sub-modules is large [19]. Phase Shifted PWM (PSPWM) is a more in-depth method and also studied in the field of MMC modulation [20]-[21]. In order to balance the capacitor voltage, an extra signal generated by a PI regulator of each sub-module has to be added to both the upper arm and lower arm modulation signals. It means a specialized balance controller has to be designed and with the increase of levels, the difficulty of control will increase and bring the risk of instability. At the same time, some new PWM methods have been proposed with different purposes, for example, the Fundamental Switching Frequency Modulation[22] and the Improved Sub module Unified Pulse Width Modulation (SUPWM)[23].

This paper proposes a new Selective Virtual Loop Mapping method (SVLM) based on Phase Disposition PWM (PDPWM) which has voltage balance capability. The concept of Virtual Sub-Module (VSM) is established, and by changing the mapping routines between the VSM and the Real Sub-Module (RSM) with SVLM, the capacitor voltages of the upper and lower arm can be balanced even if the inverter loses its symmetry. The method has been designed to consider the following situations: 1) no extra signal should be added to the reference voltage to provide a good basis for the suppression of the circulating current; 2) the possibility of large number of sub-modules in one arm; 3) retain the equivalent switching frequency of the PDPWM; 4) it could be easy to be realized in FPGA for large scale converter which has a large number of sub-modules. The method is verified through simulations and experiments.

II. Modular Multilevel PV Inverter

A. Modulation Principles

Fig. 1 shows the single phase equivalent circuit of MMC, which has two arms including the upper arm and the lower arm, with each arm having *N* Sub-Modules (SM) and one buffer inductor *L* and equivalent resistor *R*. The DC Link of MMC is floated or connected to high-voltage sources depending on the working purpose of the converter. The output of the converter is the connection point of the upper and lower arm. L_s is the AC Link Inductor and Z_0 is the equivalent impedance of the AC side.

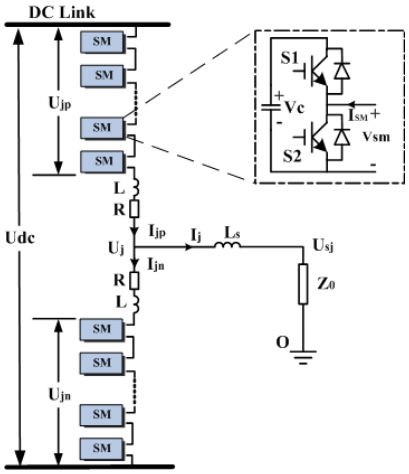

Fig. 1. Single phase equivalent circuit of multi-level converter.

The working states of SM are shown in Table I. Each SM has two states ("on" and "off"), and the corresponding output voltage (U_{sm}) of the SM are *Vc* or 0. The capacitor will charge or discharge during the period of the "on" state of the SM depending on the direction of Ism. For example, if *Ism*>0, capacitor would be charged, and for *Ism*<0, the capacitor would be discharged. The capacitor voltage will be kept while the SM is "off".

TABLE I

HALF-BRIDGE SUB-MODULE WORKING STATES

mode	S1	S2	Usm	Ism	state	capacitor
1	1	0	Vc	>0	on	Charging
2	1	0	Vc	<0	on	discharging
3	0	1	0	>0	off	Unchanged
4	0	1	0	<0	off	Unchanged

Seen from Fig. 1, the *j* phase output voltage U_j can be expressed as: (*j=a, b, c*)

$$U_j = \frac{1}{2}\left[U_{jn} + L\frac{dI_{jn}}{dt} + I_{jn}R\right] - \frac{1}{2}\left[U_{jp} + L\frac{dI_{jp}}{dt} + I_{jp}R\right] \quad (1)$$

where U_{jp} represents the sum of the upper arm's capacitor voltage while U_{jn} is the sum of the lower arm's capacitor voltage. I_{jp} and I_{jn} is the upper arm current and the lower arm current respectively. *L* and *R* are the buffer inductor and resistor of the arm.

$$2U_j = \left(U_{jn} - U_{jp}\right) + L\frac{d\left(I_{jn} - I_{jp}\right)}{dt} + R\left(I_{jn} - I_{jp}\right) \quad (2)$$

$$I_j = I_{jp} - I_{jn} \quad (3)$$

$$I_{circj} = \frac{I_{jp} + I_{jn}}{2} \quad (4)$$

Where I_{circj} is the circulating current of one leg, and I_j is j phase output current.

$$2U_j = \left(U_{jn} - U_{jp}\right) - L\frac{dI_j}{dt} - RI_j \tag{5}$$

$$\begin{aligned} U_{dc} &= \left(U_{jn} + L\frac{dI_{jn}}{dt} + RI_{jn}\right) + \left(U_{jp} + L\frac{dI_{jp}}{dt} + RI_{jp}\right) \\ &= \left(U_{jn} + U_{jp}\right) + L\frac{d\left(I_{jn} + I_{jp}\right)}{dt} + R\left(I_{jn} + I_{jp}\right) \\ &= \left(U_{jn} + U_{jp}\right) + 2L\frac{dI_{circj}}{dt} + 2RI_{circj} \end{aligned} \tag{6}$$

$$L\frac{dI_{circj}}{dt} + RI_{circj} = \frac{1}{2}\left(U_{dc} - U_{jp} - U_{jn}\right) \tag{7}$$

Defining two variables e and U_{circj} as the following equations:

$$e = \frac{1}{2}\left(U_{jn} - U_{jp}\right) \tag{8}$$

$$\begin{aligned} U_{circj} &= L\frac{dI_{circj}}{dt} + RI_{circj} \\ &= \frac{1}{2}\left(U_{dc} - U_{jp} - U_{jn}\right) \end{aligned} \tag{9}$$

From (8) and (9), the reference signals of upper and lower arms can be expressed by (10).

$$\begin{cases} U_{jp} = \frac{1}{2}U_{dc} - e - U_{circj} \\ U_{jn} = \frac{1}{2}U_{dc} + e - U_{circj} \end{cases} \tag{10}$$

Where the U_{circj} can be used to suppress the circulating current.

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B. Basic Structure and Control

There are two structures which can be used in medium and high voltage PV grid-connected inverter with MMC: single-stage and two-stage. The series-connected PV modules of single-stage access to the DC link directly, while two-stage is different, PV panels could be connected to the DC link by cascaded DC/DC circuits[24]-[25]. The differences are that voltage ripples of the single-stage are bigger than two-stage, and two-stage has more complex control [26].

Fig. 2 is the control block diagram of a modular multilevel PV inverter.

Where U_{dcref} is the reference of the DC link voltage, and U_{dc} is the real DC link voltage, they compare with each other to produce the active reference current i_{dref} after the PI controller. i_{qref} is the reactive reference current. *Us (a,b,c)* is the AC side grid voltage, and *I (a,b,c)* is the output current of the MMC. S_j (1…2N, j=*a*,*b*,*c*) are the PWM signals of the MMC.

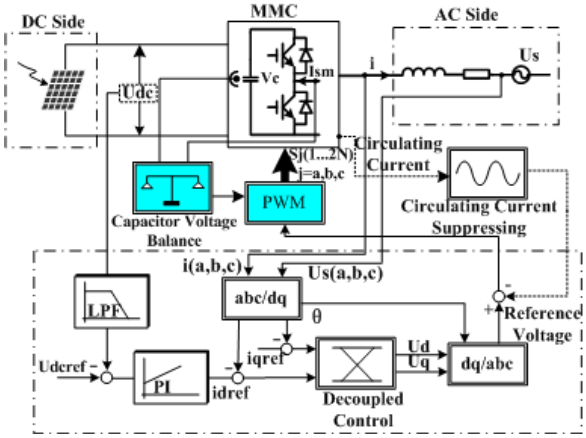


Fig. 2. Modular multi-level PV inverter overall control block diagram.

It can be seen that, the reference voltage can be acquired by decoupled control, and the circulating current suppression compensation signal should be added to it. Meanwhile, the dynamic balance of the system capacitor voltage is no longer by generating the appropriate balance compensation signal, but solely by adjustment of the PWM modulation method. This approach has the advantage not only to avoid excessive compensation signal mutual interference, which increases system stability, but also provides a good basis for circulating current suppression and promotes high DC voltage utilization ratio.

III. Phase Disposition PWM Modulation Method

As an important modulation method, Carrier Disposition (CD) PWM has been widely used in multi-level modulation, and it can be divided into three types: Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD). For simplicity, this paper will focus on the PDPWM to discuss MMC modulation. PDPWM has been studied for MMC modulation [27]-[28], in order to balance capacitor voltages, rotating carrier waves was used, but it seems that it can only work in symmetric condition.

For convenience, it is assumed that the number of the Real Sub-Modules (RSM) of the upper and lower arm is 4 (N=4). And the real Sub-modules are numbered from 1 to 8 (from top to bottom).

To improve the PDPWM, the concept of Virtual Sub-Module (VSM) can be first established, which means the VSMs are not the Real Sub-Modules (RSM), and the PWM output gained by comparison of the modulation signals and the carriers will be transferred to the VSM at first, and VSM are numbered by 1’ to 2N’. The transfer relationships are illustrated as Fig. 3 and 4.

According to Fig. 3 and Fig. 4, 2N+1 level modulation truth table can be shown as Table II. 1’ to 4’ are for the upper arm VSMs, while 5’ to 8’ represent the lower arm VSMs. Here “1” means the corresponding VSM is on while “0” means off. P1-P4 are the comparison results of the carriers and the modulation signals. Range of Normalized Voltage corresponds to the Region I - IV. In each Region, each VSM has different PWM

modulation signal. For example, when the modulation signal Umu in the Region II, P2 and P6 will be transferred to VSM 2' and 6', at the same time, "1" will be output to VSM 1'and 5', "0" will be output to VSM 3', 4', 7' and 8'. Other regions can also be analyzed like this.

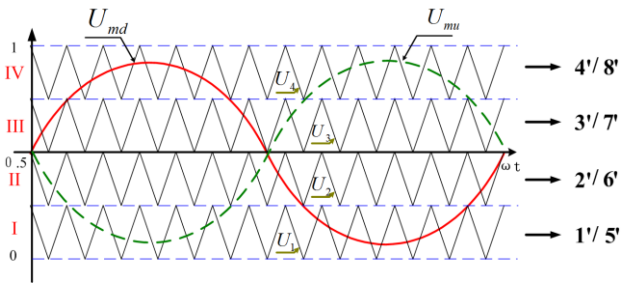


Fig. 3. Transfer relationships of VSM.

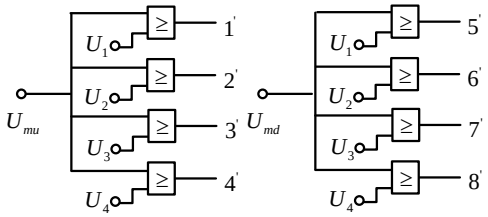


Fig. 4. VSM's input.

TABLE II

SWITCH COMBINATIONS OF VSM (2N+1 LEVEL)

Region	1'	2'	3'	4'	5'	6'	7'	8'	Range of Normalized Voltage
I	P1	0	0	0	P5	0	0	0	0 ~ 0.25
II	1	P2	0	0	1	P6	0	0	0.25 ~ 0.5
III	1	1	P3	0	1	1	P7	0	0.5~ 0.75
IV	1	1	1	P4	1	1	1	P8	0.75 ~ 1

P1~P8 is the corresponding PWM signal of each VSM's input

Table III is N+1 level modulation, compared with Table II; the driving signals of the lower arm VSMs are complementary to the upper arm.

Because the 2N+1 level modulation has bigger DC link voltage ripple, this paper finally chooses the N+1 level modulation as the PV grid-connected inverter's modulation method.

TABLE III

SWITCH COMBINATIONS OF VSM (N+1 LEVEL)

Region	1'	2'	3'	4'	5'	6'	7'	8'	Range of Normalized Voltage
I	P1	0	0	0	P5	1	1	1	0 ~ 0.25
II	1	P2	0	0	0	P6	1	1	0.25 ~ 0.5
III	1	1	P3	0	0	0	P7	1	0.5~ 0.75
IV	1	1	1	P4	0	0	0	P8	0.75 ~ 1

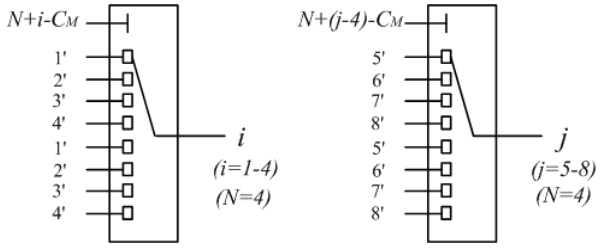
P5~P8 is the corresponding negated PWM signal of P1~P4 respectively

The driving signals of VSMs would be transferred to the Real Sub-Module (RSM) finally by the following mapping rules described in the next section.

IV. CAPACITOR VOLTAGE VIRTUAL LOOP MAPPING BALANCE CONTROL

To solve the sub-module capacitor voltage balance control problems, there are two mechanisms: the Virtual Loop Mapping (VLM) method and the enhanced Selective Virtual Loop Mapping (SVLM) based on the capacitor voltage MIN and MAX values comparison.

The VLM's principle is using a count-up counter "C_M" to control the mapping relationships between the VSMs and the RSMs. The C_M's working frequency can be set equal to the carrier frequency or less, and its counting range is 0- (N-1). Different counter number means different mappings. The VLM can be realized easily by using multiplexer with single pass transistor in FPGA like Fig. 6 (N=4); the Double Input Buffer (DIB) structure is also used here.



（a）Upper arm's mapping (b) Lower arm's mapping

Fig. 5. VLM's mapping relationship.

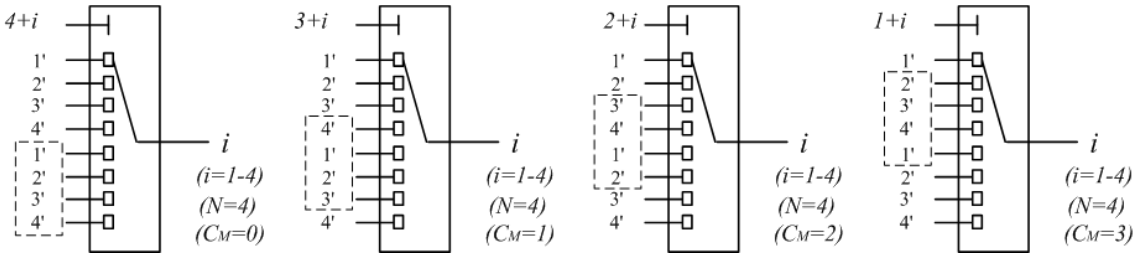
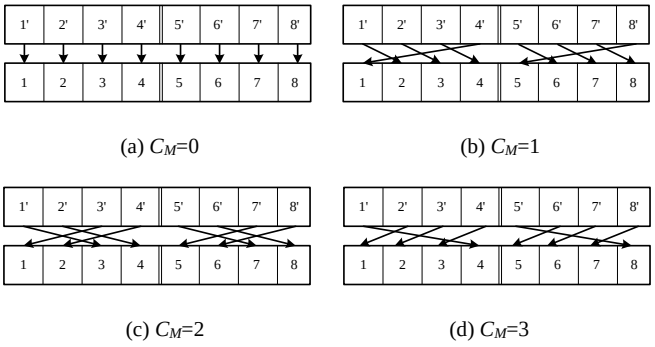


Fig. 6. Upper arm VLM procedures

The *i* and *j* in Fig. 5 is the index number of the RSM respectively, which work with the counter to realize the mapping between the VSMs and the RSMs. For example, if C_M=0, $N+i-C_M=4+i-0=4+i$, VSM 1'-2'-3'- 4' would be mapped to RSM 1-2-3-4 as shown in Fig. 6 (a); likely, if C_M=1, $N+i-C_M=4+i-1=3+i$, VSM 4'-1'-2'-3' would be mapped to RSM 1-2-3-4 (Fig. 6(b)), and so on.

The VLM's final results of both arms are illustrated as the following:



(a) C_M=0 (b) C_M=1

(c) C_M=2 (d) C_M=3

Fig. 7. Virtual loop mapping final results.

This method can achieve capacitor voltage balance in case of system symmetry.

V. Capacitor Voltage Selective Virtual Loop Mapping Balance Control

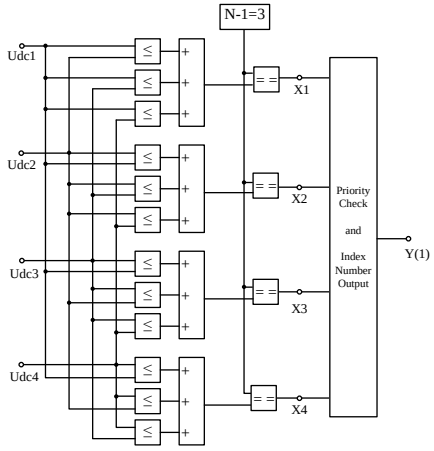
A practical modulation method should be not only be effective in a symmetrical system, but also have the ability to regulate dynamically and provide some error correction capabilities to ensure the system works well in some conditions of error accumulation and device parameter deviation. For example, commonly used Phase-Shift PWM, by changing the modulation signals of the upper and lower arm to get the dynamic balance adjustment capacity of the capacitor voltage, but will bring more harmonics to the arm current, change the circulating current characteristics, and may cause instability. Therefore, changing the modulation signals to achieve the dynamic adjustment capability would be valid only to a certain extent.

The new method is mainly through the Selective Virtual Loop Mapping (SVLM) to achieve the effect of dynamic regulation ability; here "Selective" means just taking out the capacitor voltage of MIN and MAX values and their corresponding index selectively. Before introducing the SVLM rules, note there are four interesting SM in Table III, they are 1', 4', 5' and 8'. VSM 1' and 8' output PWM in region I and IV respectively, while output "1" in other regions. Likewise, VSM 4' and 5' output PWM in region IV and I, output "0" in other regions. Table I shows that if some capacitor voltage of the leg is less than the others (means needing more charge and less discharge), it would be right to map the SM 1' and 8' to this sub-module when the corresponding current ISM is positive and mapping the SM 4' and 5' to it when ISM is negative.

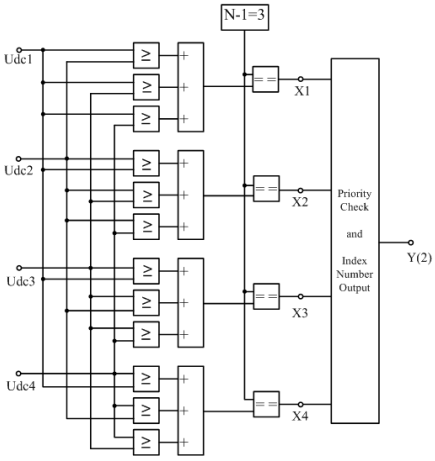
To achieve the SVLM, it needs to sort the capacitor voltage as [29]-[30] described, but frequent sorting is very time-consuming, and requires more hardware resources, which would be a large burden especially for high voltage applications needing more sub-modules. Other disadvantages of sorting are a reduction in system equivalent frequency and an increase in switching losses. Therefore, the actual method of selective mapping in this paper is just picking the MIN and MAX capacitor voltage and their corresponding index directly and make sure it can be easily implemented in FPGA.

The rules of the SVLM are as follows (just taking the upper arm as an example):

1) First, all of the individual capacitor voltages are compared, and obtain the corresponding RSM indexes of the maximum voltage and minimum voltage. The MIN index block diagram is shown in Fig. 8(a). (*N*=4). Y is an array, and *Y(1)* is the first element.



(a) MIN block diagram



(b) MAX block diagram

Fig. 8. Index acquirement method of the MIN and MAX voltage.

U_{dc1}-U_{dc4} are the SM's capacitor voltage of the upper arm separately and they are compared to each other at the same time which means the time is limited. *Y(1)* would be equal to the capacitor index having the minimum voltage, for example, if the voltage of U_{dc3} is the minimum, *Y(1)* would be equal to 3. Priority check is just for the case of more than one input of X_1 -X_4 equal to 1, so X_1 could be setup to the highest priority in the MIN check, while X_4 has the lowest priority. For the MAX check, the "≤" would be replaced by "≥", while, *Y(2)* provides

the corresponding index of the maximum capacitor voltage(Fig. 8(b)), and X_4 should have the highest priority and X_1 have the lowest priority.

2) The corresponding truth table of the priority check and index number output function for *Y(1)* has been shown in Table IV. *Y(2)* can be acquired by the same method (Table V).

TABLE IV

PRIORITY CHECK AND INDEX NUMBER OUTPUT TRUTH TABLE OF Y(1)

X1	X2	X3	X4	Y(1)
1	x	x	x	1
0	1	x	x	2
0	0	1	x	3
0	0	0	1	4

x means any state

TABLE V

PRIORITY CHECK AND INDEX NUMBER OUTPUT TRUTH TABLE OF Y(2)

X1	X2	X3	X4	Y(2)
x	x	x	1	4
x	x	1	0	3
x	1	0	0	2
1	0	0	0	1

x means any state

3) The other SMs' indexes except the minimum and maximum capacitor voltage would also be assigned to the Y array by sequence after *Y(2)*. For example, if SM 3 has the lowest voltage and SM 2 has the highest voltage, the Y array would be assigned like this:

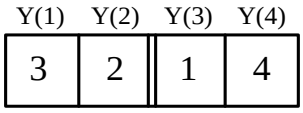
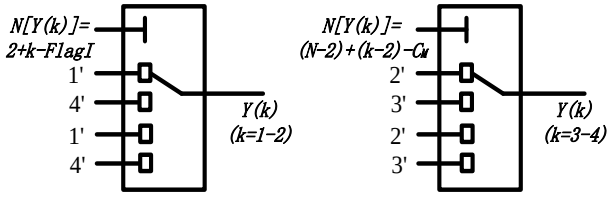


Fig. 9. Assignment of the Y array.

4) Change the Mapping Route as shown in Fig. 10, *N[Y(i)]* is the multiport switch selector array, its index is *Y(i)* (*i*=1-4). *FlagI* is the symbol of the arm current direction. If the upper arm current is positive (I_{jp} >0), *FlagI*=0; the *N[Y(1)]* would be equal to 3, which means VSM 1' would be mapped to RSM 3. At the same time, the *N[Y(2)]* would be equal to 4, and VSM 4' be mapped to RSM 2. In contrast, if I_{jp}<0, *FlagI*=1, the *N[Y(1)]* is assigned with 2, and VSM 4' is mapped to RSM 3, while VSM 1' is mapped to RSM 2. The rest of the mappings follow the aforementioned VLM, and can be seen in Fig. 10(b).



(a) (b)

Fig. 10. Mapping route control of each RSM.

Just take Fig. 9 as an example:

If I_{jp}>0,

$$N\left[Y(1)\right]=N[3]=3$$

$$N\left[Y(2)\right]=N[2]=4$$

If I_{jp}<0,

$$N\left[Y(1)\right]=N[3]=2$$

$$N\left[Y(2)\right]=N[2]=3$$

At the same time, the rest of the RSMs would still follow the previously described VLM rule. But the maximum counter range of the C_M would be set equal to *N*-2.

If C_M=0,

$$N\left[Y(3)\right]=N[1]=3$$

$$N\left[Y(4)\right]=N[4]=4$$

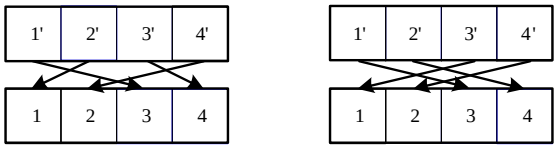
If C_M=1,

$$N\left[Y(3)\right]=N[1]=2$$

$$N\left[Y(4)\right]=N[4]=3$$

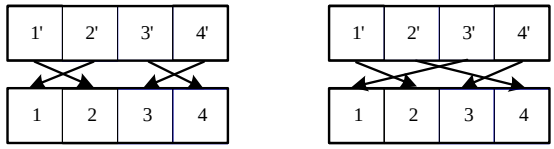
5) The final mapping route would be like the following:

I_{jp} > 0 (j=a, b, c), SVLM is:



(a) C_M=0 (b) C_M=1

I_{jp} < 0 (j=a, b, c), SVLM is:



(c) C_M=2 (d) C_M=3

Fig. 11. Selective virtual loop mapping.

6) In order to minimize the delay of the PWM signal, a synchronous sampling control should be adopted to the SVLM as shown in Fig. 12. U_{mu} is the reference voltage, and *Y* array is sampled at the intersection point of two triangular carriers. From Fig. 12, it is obvious that the whole processing time of the SVLM is made up of three parts: Δt1 is corresponding to the processing time of step 1 and 2 of the SVLM while *Y(1)* and *Y(2)*

are acquired, and because all the comparisons are taking place in parallel, the delay would be limited and has no relationships to the number of SMs in one arm. Δt2 is the forming time of Y array which length depends on the modules in each arm (*N*), and Δt3 is the transmission delay of the mapping. It can be seen that the delay of Δt3 is limited which mainly depends on the hardware, while Δt1 and Δt2 have almost no impact to the real modulation process.

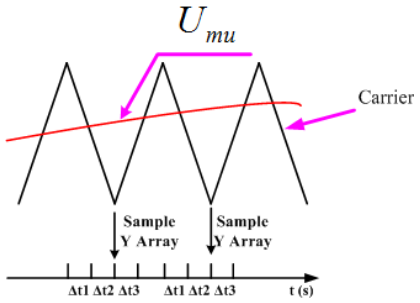


Fig. 12. Synchronous sampling control

VI. Simulation and Experiments

A. Simulation

In order to verify the validity of the modulation method, a five-level MMC PV single phase grid-connected simulation model reference to the experimental system was built, while the SVLM would be put into action at 0.5 s. In order to break the symmetry of the system, a resistor of 100 Ω was paralleled to the capacitor of the SM 1, the relative simulation and experiment parameters are shown in Table VI. The PV panel is modeled according to the specification of the commercial PV panel from Sanyo, HIP-195BA19.

The control scheme can be designed as shown in Fig. 13.

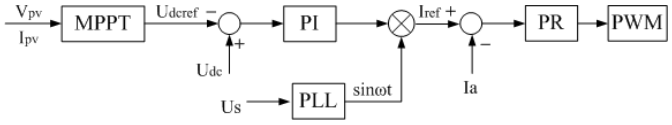


Fig. 13. Control scheme of the single phase PV grid-connected inverter.

Simulation system for a 5-level output waveform is shown in Fig. 14, and it was assumed that all the PV panels had the same working conditions: irradiance S = 1000 W/m2, ambient temperature 25 ℃. Fig. 14 (a) shows the system voltage U_{sa} of the grid, and the inverter output current Ia, which should be synchronous to the grid voltage. Fig. 14 (b) is the output voltage U_a of the modular multilevel inverter. It is clear that the output voltage's ripples were reduced after 0.5s when the SVLM was on.

Fig. 15 is the corresponding capacitor voltages of the upper and lower arm. Since a 100 Ω resistor was paralleled to the capacitor #1 of the SM 1, its voltage was the lowest one before 0.5s. From Fig. 15 (b) and (c), the capacitor voltages of the upper and lower arm quickly balance since the SVLM was in operation at 0.5s.

TABLE VI

Simulation and Experiment Parameters

Parameters	Values
No. of PV panels	4
No. of Sub-modules in each arm	4
Sub-module Capacitor C	2200 uF
Arm Inductor L	2 mH
Arm Equivalent Resistance	0.1 Ω
AC Link Inductor L_S	5 mH
Carrier frequency	2400 Hz
AC system voltage Us (rms)	115 V
Power frequency	60 Hz
Transformer ratio	600 V/ 240 V

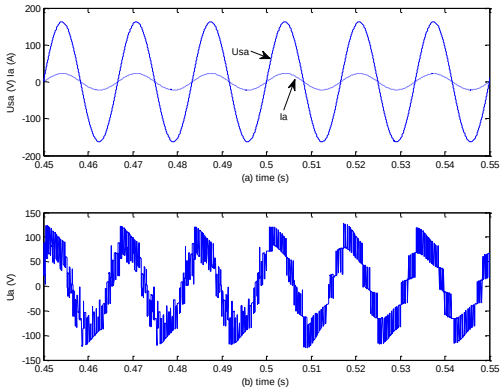


Fig. 14. Modular multilevel inverter output waveforms. (a) system voltage Us and output current Ia; (b) inverter output voltage Ua.

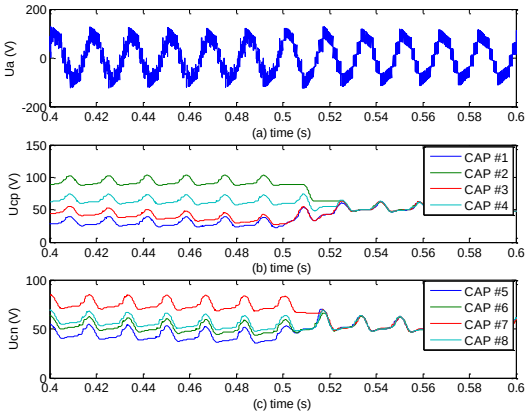


Fig. 15. Simulation showing balance of the upper and lower arm capacitor voltage with the SVLM off and turned on at 0.5s. (a) inverter output voltage; (b) the upper arm capacitor voltages; (c) the lower arm capacitor voltages.

Fig. 16 (a) and (b) show the upper/ lower arm current, and the corresponding circulating current is shown in (c). Obviously, the circulating current of the *N*+1 level modulation is mainly consisting of DC and second harmonic. The spectrum of the

circulating current before and after the SVLM is on could be seen in Fig. 17, and the high frequency components of the circulating current could be reduced with SVLM.

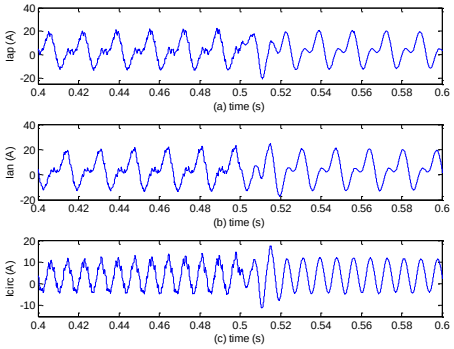
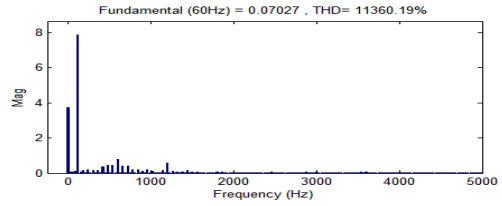
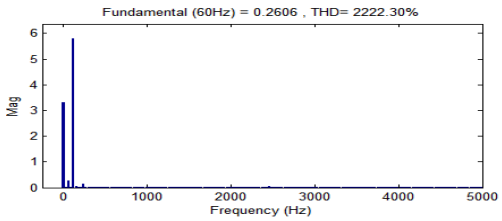


Fig. 16. Simulation showing the upper and lower arm currents and the circulating current of the leg with the SVLM off and turned on at 0.5s. (a) the upper arm current; (b) the lower arm current; (c) the circulating current of the leg.



(a) SVLM is off



(b) SVLM is on

Fig. 17. Harmonics of the circulating current shown in Fig. 16 (c)

From these simulation results, it is obvious that the SVLM can work well to achieve the capacitor voltage balance. The difference of the capacitor voltage can be greatly reduced, and the system output voltage and current waveforms are improved. Since no additional signals are added to the reference voltage, the overall characteristics of the MMC do not need to be changed, such as the internal circulating current, which can be observed within Fig. 16 (c). This characteristic provides a good basis to eliminate the circulating current further.

B. Experiment

To test the performance of the SVLM, experiments are carried out on a MMC. Fig. 18 shows the experimental PV modular multilevel inverter which has component values listed in Table VI.

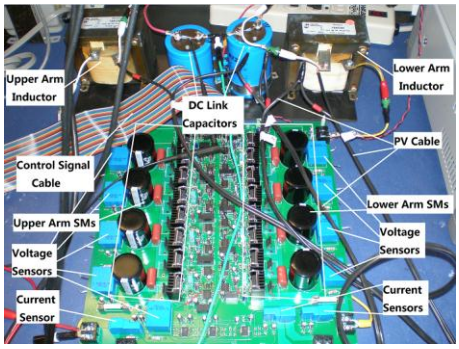


Fig. 18. Photos of the experimental system.

To test the system balance ability with the new modulation method, a 160 ohm resistor was shunted to the sub-module 3 capacitor. The MMC first worked at this unbalanced condition and turned on the SVLM to balance the capacitor voltage in process. The output voltage and current of inductor and resistor load can be seen in Fig.19; after the SVLM is turned on, the voltage output waveform becomes flat, and the unbalance situation was corrected.

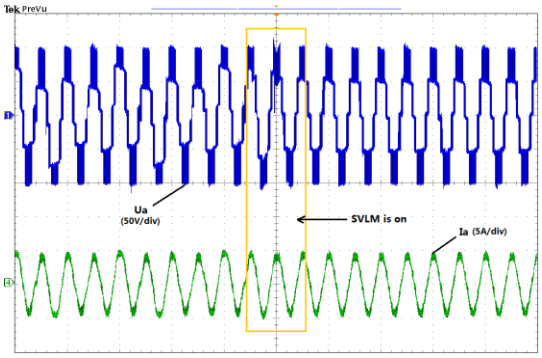


Fig. 19. Experimental output voltage and current of the converter with the SVLM off and on (Load is inductor and resistor).

The variation of the CAP #1 and CAP #3 voltages are shown in Fig. 20. Obviously, both of them are close to each other after the SVLM is on. The same situation also happens to the lower arm capacitors which can be seen in Fig. 21. The corresponding variations of the upper and lower arm currents are also shown in Fig. 20.

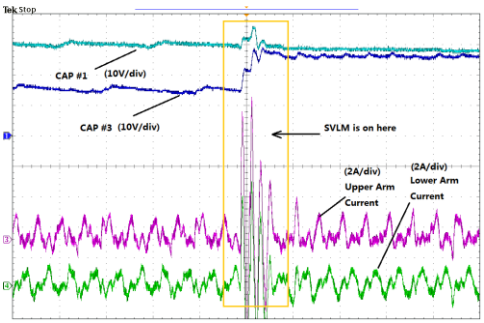


Fig. 20. Experimental capacitor voltage (CAP #1 and CAP #3), and the upper / lower arm current with SVLM off and on.

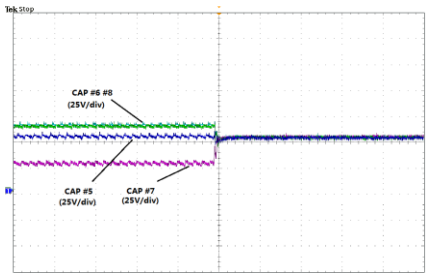


Fig. 21. Experimental capacitor voltage(CAP #5 to #8) with SVLM off and on.

Finally, the new modulation method was used in PV grid-connected inverter, and the corresponding parameters are the same with the Table V. Fig. 22 shows the DC link voltage U_{dc}, the output voltage Ua and the output current *Ia* of the inverter.

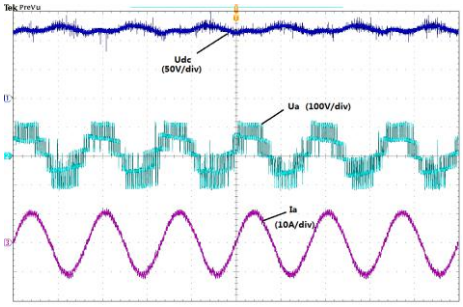


Fig. 22. DC link voltage, output voltage, and output current of the experimental inverter.

The experimental results also show that the grid current has the same frequency and phase as the grid voltage and has unity power factor, as shown in Fig. 23.

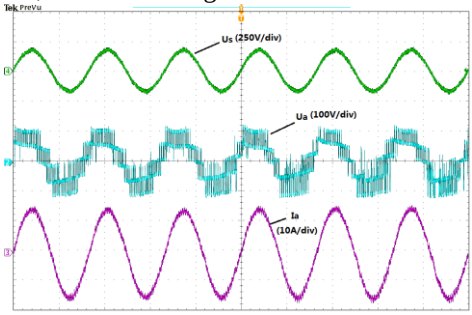


Fig. 23. Grid voltage, output voltage, and output current of the experimental inverter.

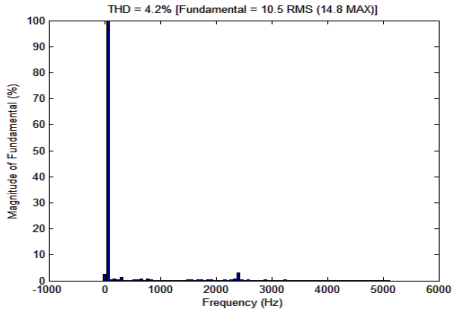


Fig. 24. Harmonic of the output current. Shown in Fig. 23.

The THD of the grid current in Fig. 23 is 4.2%, as shown in Fig. 24, which is less than 5% and meets the power quality standards, like IEEE1547 in the US and IEC61727 in Europe.

VII. Conclusion

This article first discussed the possibilities of MMC being used as an interface between the grid and PV panels, and proposed an improved Selective Virtual Loop Mapping method based on the Phase Disposition PWM. This method can produce $2N$+1 and N+1 level output in MMC, and achieve sub-module capacitor voltage dynamic balance compensation control while not changing the reference signal. The whole mapping rules are presented and it is easy to be implemented in FPGA. Simulation and experiments were carried out under the conditions of load and grid, the effectiveness of the method was proved well.

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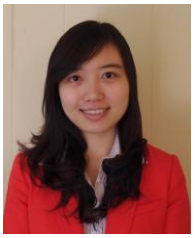

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