Flying Capacitors Reduction in an Improved Double Flying Capacitor Multicell Converter Controlled by a Modified Modulation Method

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***Abstract*—This paper proposes an improved configuration of double flying capacitor multicell (DFCM) converter. The main advantages of the proposed converter, compared to the conventional DFCM converter, are the doubling of the number of output voltage levels and improvement of the output voltage frequency spectrum. This progress is achieved by adding only two low-power switches and one dc voltage source, whose voltage rating is a small fraction of the main dc-link voltage rating, to the conventional configuration of the DFCM converter. However, the number and voltage rating of high-frequency switches and capacitors and the number of high-frequency switchings during a full cycle are kept constant. The doubling of the number of output voltage levels in the proposed converter makes it possible to decrease the number of cells, the number of flying capacitors, as well as their voltage rating and the amount of stored energy in flying capacitors. Moreover, a modulation method based on phase-shifted carrier pulsewidth modulation is proposed to control the new converter. Simulation and measured experimental results are presented to illustrate the performance of the proposed configuration and its control strategy.**

***Index Terms*—Double flying capacitor multicell (DFCM) converter, flying capacitor multicell (FCM) converter, flying capacitors, natural self-balancing, phase-shifted carrier pulsewidth modulation (PSC-PWM).**

NOMENCLATURE

FCM	Flying capacitor multicell.
SM	Stacked multicell.
DFCM	Double flying capacitor multicell.
I-DFCM	Improved double flying capacitor multicell.
PSC-PWM	Phase-shifted carrier pulsewidth modulation.
IGBT	Insulated gate bipolar transistor.
V_{ref}	Output reference voltage of converter.
$V_{\mathrm{ref\text{-}mdf}}$	Modified output reference voltage of converter.
$V_{\mathrm{ref\text{-}DFCM}}$	Output reference voltage of DFCM converter.
PCB	Printed circuit board.

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I. INTRODUCTION

HIGH-POWER industrial applications of converters have been revolutionized in recent decades by the advent of multilevel converters [1]. The logic behind multilevel converters lays in connecting medium-voltage semiconductor switches in series to attain high-power ranges [2], [3]. The most noteworthy advantages of multilevel converters in comparison with their conventional two-level counterparts are synthesizing an output voltage waveform from several steps of voltage with significantly improved harmonic content, reduction of output dv/dt, electromagnetic interference, filter inductance, etc. [1]–[3]. These appreciable features have motivated researchers to focus their studies on improvement of topology and control methodology of multilevel converters in recent years [4]–[18].

Multilevel converters are categorized, based on their topologies, into three major groups which are diode-clamped converters, cascade multicell converters with multiple isolated dc voltage sources, and flying-capacitor-based multicell converters [19]–[21]. The diode-clamped multilevel converter suffers from drawbacks such as imbalance issue of dc-link capacitors voltages and its excessive use of clamping diodes, especially when the number of levels is high, which have constrained its application. Promising alternatives for diode-clamped multilevel converters are multicell structures [20]–[23]. Cascade multicell converters, despite their disadvantage of requiring multiple isolated dc voltage sources, are being successfully utilized in high-power applications. However, there are other significant topologies of multicell converters such as flying capacitor multicell (FCM) and its subtopology stacked multicell converters [21], [24]. The FCM converters consist of ladder connection of cells while each cell in FCM is made up of a flying capacitor and a pair of semiconductor switches with a complimentary state. The commutation between adjacent cells with their associated flying capacitors charged to the specific values generates different levels of chopped input voltage at the output side of converter [21]–[25].

The voltage balancing of flying capacitors which guarantees the safe operation of the converter is a crucial subject in these topologies [22], [23]. It is well demonstrated via precise mathematical modeling of FCM converters that the capacitors voltage balancing which is called self-balancing occurs

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if phase-shifted carrier pulsewidth modulation (PSC-PWM) technique is applied to the converter control pattern [26]–[31]. Flying-capacitor-based converters have many attractive properties for medium voltage applications including natural self-balancing, transformerless operation, and equal distribution of voltage stress between semiconductor switches. Consequently, many research studies have been dedicated to enchance the topology and control procedure in these promising converters [4], [32]–[34].

Besides the previously mentioned advantages of flying-capacitor-based converters such as FCM and SM converters, their bulky and costly flying capacitors are the main problems of these converters especially when the number of cells increases [35], [36]. Sadigh *et al*. in [4] proposed a configuration called double flying capacitor multicell (DFCM) converter in which the number of flying capacitors and their voltage rating are reduced significantly. In this paper, the improved configuration of a DFCM converter, called I-DFCM, is proposed to reduce the number of flying capacitors and as a result, decrease the size and cost of the converter in comparison with conventional DFCM. The remainder of this paper is organized as follows. In Section II, configuration of the I-DFCM converter and its new control strategy based on the PSC-PWM technique are presented. The advantage of the proposed topology in comparison with the conventional DFCM converter is that the number of output voltage levels is doubled by adding only two low-power switches and one dc voltage source whose voltage rating is a fraction of voltage rating of main dc voltage source. Simulation and experimental results are presented in Sections III and IV, respectively, for proposed single phase I-DFCM converter to validate the effectiveness and advantages of the proposed configuration and its control strategy. Size and cost comparison of DFCM and I-DFCM are also presented in Section V.

II. Improved Configuration of a Double Flying Capacitor Multicell Converter

The main advantages of the DFCM converter, versus FCM and SM converters, are doubling the rms of output voltage and the number of output voltage levels and canceling the midpoint of dc voltage source. This has been achieved by adding only two low-frequency switches to the configuration of an FCM converter while the number of high-frequency switches and capacitors, voltage ratings of capacitors and switches, and the number of high-frequency switchings during a full cycle are kept constant [4]. In addition, the frequency spectrum of output voltage is improved and its total harmonic distortion (THD) is reduced significantly because of the doubling of the number of output voltage levels [4]. In other words, the superiority of the DFCM converter over FCM and SM converters in producing the same voltage is the reduction of the number of switches and especially the number of bulky and costly flying capacitors by 50% [4]. These achievements reduce the size and cost of the converter effectively. However, any effort and improvement to reduce the number and voltage rating of flying capacitors make these types of converters more practical and cost effective.

Fig. 1. Two-cell 11-level proposed I-DFCM converter's configuration, control strategy, switches states, and output voltage.

In this paper, the improved configuration of a DFCM converter is proposed to reduce the number and voltage rating of flying capacitors and as a result, decrease the size and cost of the converter. Fig. 1 shows the proposed 11-level I-DFCM converter which only uses one flying capacitor, while it is required to use nine, eight, and four flying capacitors, respectively, to produce the same number of levels utilizing FCM, SM, and DFCM converters. Moreover, the total voltage rating of flying capacitors and dc-link capacitors to produce the single-phase 11-level output voltage with the peak-to-peak voltage of $10E$ is $55E$, $30E$, and $15E$ in FCM, SM, and DFCM converters, respectively, while it is $7E$ in the proposed configuration of an I-DFCM converter.

As shown in Fig. 1, which illustrates the operational principles of an I-DFCM converter, one minor dc voltage source with the voltage rating of $E/4$ (equal to half of the voltage rating of the smallest and the most right flying capacitor) and two

complimentary low-power high-frequency switches are added to the most left part of the DFCM converter. The main duty of added minor dc voltage source as well as two switches of K and $\overline{K}$ is to produce the minor voltage levels, i.e., odd levels, between the major voltage levels, i.e., even levels, produced by DFCM converter. Two added switches of K and $\overline{K}$ make it possible that the minor dc voltage source to be connected in series with the major dc voltage source and therefore, produces the small steps and increases the number of output voltage levels. As a result, the minor converter which includes the minor dc voltage source and two low-power switches produces only the minor levels of -1, 0, and $+1$ in series with the main DFCM converter which produces -4, -2, 0, $+2$, and $+4$, i.e., even levels; thus, the proposed I-DFCM converter, as sum of minor and major converters, in total produces 11 levels from -5 to $+5$ in one-unit steps.

The switching procedure of an 11-level two-cell I-DFCM converter is as follows. As shown in Fig. 1, $V_{\mathrm{ref,abs}}$, which is the absolute value of output reference voltage V_{ref}, is intersected and compared with five phase-shifted carriers. As seen, the output of comparator #*Y* is 1 when the $V_{\mathrm{ref,abs}}$ is higher than the carrier #*Y* and is 0 when the $V_{\mathrm{ref,abs}}$ is lower than the carrier #*Y*. Then, the output of comparators are added together to generate the output reference voltage in a staircase waveform $V_{\mathrm{ref,abs,s}}$. The notation of abs and s refer to absolute value and staircase waveform, respectively. Afterward, the modified output reference voltage (called $V_{\mathrm{ref\text{-}mdf}}$) can be generated as follows:

$$V_{\mathrm{ref,mdf}} = V_{\mathrm{ref,abs,s}} \cdot \mathrm{sgn}\left(V_{\mathrm{ref}}\right) + \frac{\left(1 - \mathrm{sgn}\left(V_{\mathrm{ref}}\right)\right)}{2} \cdot 5 \quad (1)$$

where $\mathrm{sgn}\,(x)$is the signum function and equals $+1$ when the signal x is positive and equals -1 when the signal x is negative. According to the modified output reference voltage $V_{\mathrm{ref\text{-}mdf}}$, the reference of a DFCM converter $V_{\mathrm{ref\text{-}DFCM}}$ is calculated to produce the major levels of 0, $+2$, and $+4$, i.e., even levels. In other words, $V_{\mathrm{ref\text{-}DFCM}}$ can be expressed as

$$V_{\mathrm{ref\text{-}DFCM}} = 2 \cdot \left\lfloor \frac{\left(V_{\mathrm{ref\text{-}mdf}}\right)}{2} \right\rfloor \quad (2)$$

where, $\lfloor\rfloor$ indicates the floor function and $\lfloor x \rfloor$ is the integer part of x. After this calculation, the reference of a DFCM converter $V_{\mathrm{ref\text{-}DFCM}}$ is intersected with two phase-shifted carriers to determine the states of DFCM converter's switches, i.e., *J*, S_2, and S_1. In the next step, as shown in Fig. 1, $V_{\mathrm{ref\text{-}DFCM}}$ is subtracted from $V_{\mathrm{ref\text{-}mdf}}$ to calculate the status of switch *K*. If the result of subtraction is 1, the switch *K* is ON and if the result of subtraction is 0, the switch *K* is OFF. It should be noted that switches K and $\bar{K}$ are complimentary. To make the operational principle of an I-DFCM converter much more comprehensible, the switching states of a two-cell-11-level I-DFCM converter are illustrated in Table I. The switch *X* is ON when its state is 1 and is OFF when its state is 0. Moreover, Fig. 2 shows the general configuration of an *n*-cell 4*n*+3-level I-DFCM converter whose control method is as follows. First, the $V_{\mathrm{ref,abs}}$ waveform, absolute value of output reference voltage, is intersected and compared with 2*n*+1 phase-shifted carriers. Then, the output reference voltage in a staircase waveform $V_{\mathrm{ref,abs,s}}$ can be expressed as follows:

TABLE I
SWITCHING STATES OF THE PROPOSED TWO-CELL 11-LEVEL I-DFCM CONVERTER

Output Voltage Level	*J*	State (K, S_2, S_1)	No. of states
$+5\frac{E}{4}$	0	(1,1,1)	1
$+4\frac{E}{4}$	0	(0,1,1)	1
$+\frac{3}{4}E$	0	(1,0,1) , (1,1,0)	2
$+\frac{2}{4}E$	0	(0,0,1) , (0,1,0)	2
$+\frac{1}{4}E$	0	(1,0,0)	1
0	0 1	(0,0,0) (1,1,1)	2
$-\frac{1}{4}E$	1	(0,1,1)	1
$-\frac{2}{4}E$	1	(1,0,1) , (1,1,0)	2
$-\frac{3}{4}E$	1	(0,0,1) , (0,1,0)	2
$+4\frac{E}{4}$	1	(1,0,0)	1
$+5\frac{E}{4}$	1	(0,0,0)	1

$$V_{\mathrm{ref,abs,s}} = \sum_{i=1}^{2n+1} \alpha_i, \quad \alpha_i = \begin{cases} 1 & V_{\mathrm{ref,abs}} \geq \text{carrier}\#i \\ 0 & V_{\mathrm{ref,abs}} < \text{carrier}\#i. \end{cases} \quad (3)$$

Afterward, the modified output reference voltage (called $V_{\mathrm{ref\text{-}mdf}}$) can be generated as follows:

$$V_{\mathrm{ref,mdf}} = V_{\mathrm{ref,abs,s}} \cdot \mathrm{sgn}\left(V_{\mathrm{ref}}\right) + \frac{\left(1 - \mathrm{sgn}\left(V_{\mathrm{ref}}\right)\right)}{2} \cdot (2n+1)\,. \quad (4)$$

According to the modified output reference voltage $V_{\mathrm{ref\text{-}mdf}}$, the reference of a DFCM converter $V_{\mathrm{ref\text{-}DFCM}}$ is calculated by (2), and then the waveform of $V_{\mathrm{ref\text{-}DFCM}}$ is intersected with *n* phase-shifted carriers to determine the states of *n*-cell DFCM converter's switches. In the next step, the state of complimentary switches K and $\overline{K}$ is determined according to the previously explained procedure.

In general, the *n*-cell $4n+3$-level I-DFCM converter, as shown in Fig. 2, is composed of two low-frequency switches, 2*n*+2 high-frequency switches, *n*-commutation cells controlled with equal duty cycles and phase shift of $2\pi/n$ and $n-1$ flying capacitors with the same capacitance due to the similar

Fig. 2. Proposed n-cell $4n+3$-level I-DFCM converter configuration.

TABLE II
COMPARISON BETWEEN THE CONVENTIONAL FLYING-CAPACITOR-BASED CONVERTERS AND PROPOSED I-DFCM CONVERTER IN PRODUCING THE IDENTICAL OUTPUT VOLTAGE (I.E., $4n+3$ LEVELS, $2E$ PEAK TO PEAK)

Type of Multicell Converter	No. of High Frequency Switches ***A***	No. of Cells	No. of Capacitors (dc link and flying capacitors)	No. of DC Sources	Voltage Rating of DC Sources (per unit)	Voltage Rating of High Frequency Switches (per unit) ***B***	Power Rating of High Frequency Switches (per unit)	Voltage Rating of Flying Capacitors (per unit)	No. of unit switches (***A**B***)
FCM	$8n+4$	$4n+2$	$4n+3$	*1*	$4n+2$	*1*	*1*	From *1* to $4n+1$. *(1 unit increase)*	$(8n+4)\times 1 = 8n+4$
SM	$8n+4$	$4n+2$	$4n+2$	*1*	$4n+2$	$4n+2$ *switches are 2 and* $4n+2$ *switches are 1*	$4n+2$ *switches are 2 and* $4n+2$ *switches are 1*	2 series. Each one from *1* to $2n$. *(1 unit increase)*	$(4n+2)\times 2 + (4n+2)\times 1 = 12n+6$
DFCM	$4n+2$	$2n+1$	$2n+1$	*1*	$2n+1$	*1*	*1*	From *1* to $2n$. *(1 unit increase)*	$(4n+2)\times 1 = 4n+2$
Improved DFCM	$2n+2$	n	$n+1$	*2*	*2n & 1*	*2n switches are 2 but 2 switches are 1*	*2*	From *2* to $2n$. *(2 unit increase)*	$2n\times 2 + 2\times 1 = 4n+2$

waveform of current in all flying capacitors, and different dc voltage ratings equal to $E/n, 2E/n, \ldots, (n-1)\,E/n$. As a result, the electrical stress on switches is more equally distributed as each high-frequency switch must withstand E/n volts. The energy stored in the capacitor i (i.e., U_i) of an n-cell I-DFCM converter is

$$U_i = \frac{1}{2}C\left(\frac{iE}{n}\right)^2 \tag{5}$$

where C and E are the capacitance of flying capacitors and the voltage rating of main dc voltage source, respectively [35]. Furthermore, the output voltage of an n-cell I-DFCM converter has $4n+3$ levels and its frequency spectrum has the harmonic groups around the $((2n+1)\times k\times f_{\mathrm{SW}})\,\mathrm{th}$ harmonic where k and f_{SW} are the integer number and switching frequency, respectively [35].

The comparison between the different types of flying-capacitor-based multicell converters, i.e., FCM, SM, DFCM, and the proposed I-DFCM converters, for producing the identical output voltage with equal number of levels ($4n+3$ levels) and equal peak-to-peak output voltage ($2E$) is illustrated in Table II. In addition, according to (6)–(9), Fig. 3 shows the

Fig. 3. Comparison of stored energy in all capacitors used in FCM, SM, DFCM, and proposed I-DFCM converters for producing the identical output voltage.

Fig. 4. Comparison of total voltage rating of all capacitors used in FCM, SM, DFCM, and proposed I-DFCM converters for producing the identical output voltage.

amount of stored energy in all dc-link and flying capacitors and Fig. 4 shows total voltage rating of all dc-link and flying capacitors in FCM, SM, DFCM, and I-DFCM converters. According to (5), the stored energy in, as well as the total voltage rating of, all dc-link and flying capacitors to produce $4n+3$-level output voltage with $2E$ peak-to-peak value in FCM, SM, DFCM, and I-DFCM can be calculated by the following equations:

$$Z_{\mathrm{FCM}} = \sum_{i=1,2,..}^{4n+1} k_1 \cdot (E_{Ci})^{k_2} + 2 \cdot k_1 \cdot (E)^{k_2} = \sum_{i=1,2,..}^{4n+1} k_1 \cdot \left(i \cdot \frac{E}{2n+1}\right)^{k_2} + 2 \cdot k_1 \cdot (E)^{k_2} \quad (6)$$

$$Z_{\mathrm{SM}} = 2 \cdot \sum_{i=1,2,..}^{2n+1} k_1 \cdot (E_{Ci})^{k_2} = 2 \cdot \sum_{i=1,2,..}^{2n+1} k_1 \cdot \left(i \cdot \frac{E}{2n+1}\right)^{k_2} \quad (7)$$

$$Z_{\mathrm{DFCM}} = \sum_{i=1,2,..}^{2n+1} k_1 \cdot (E_{Ci})^{k_2} = \sum_{i=1,2,..}^{2n+1} k_1 \cdot \left(i \cdot \frac{E}{2n+1}\right)^{k_2} \quad (8)$$

$$Z_{\mathrm{I-DFCM}} = \sum_{i=1,2,..}^{n} k_1 \cdot (E_{Ci})^{k_2} + k_1 \cdot \left(\frac{E}{2n+1}\right)^{k_2} = \sum_{i=1,2,..}^{n} k_1 \cdot \left(i \cdot \frac{2E}{2n+1}\right)^{k_2} + k_1 \cdot \left(\frac{E}{2n+1}\right)^{k_2} \quad (9)$$

where Z_X states the amount of stored energy in or the total voltage rating of all capacitors in converter X, k_1 and k_2 are equal to $(1/2)C$ and 2, respectively, in the case of stored energy calculation, while k_1 and k_2 are both equal to 1 in the case of total voltage rating calculation, and C is the capacitance of all capacitors.

As shown in Table II and Figs. 3 and 4, the progress of producing the minor levels between the major levels makes it possible to decrease the number of cells, the number of bulky and costly flying capacitors, the total voltage rating of flying capacitors, and the amount of stored energy in flying capacitors in the proposed I-DFCM converter in comparison with FCM, SM, and DFCM converters producing the identical output voltage. Although the voltage rating of high-frequency switches is doubled in the I-DFCM converter in comparison with the DFCM converter, their number is decreased by 50% in I-DFCM; however, the current rating of high-frequency switches due to the same output voltage and current is same in these converters. This means that the total voltage rating and total power rating of all high-frequency switches are almost the same in DFCM and I-DFCM converters for identical output voltage.

Due to the requirement of an extra small (minor) dc voltage source in the proposed I-DFCM converter which should be isolated from main dc voltage source, I-DFCM needs one extra isolation transformer. Even if the main dc link is made by a diode rectifier directly from power grid without any transformer, one transformer is required to make small (minor) dc voltage source isolated from main dc link. This issue eliminates the possibility of transformerless configuration. However, the power rating of minor dc voltage source is a small fraction of the main converter's power rating which results in a transformer with small size and light weight.

III. Simulation Results

In this section, simulation results are illustrated in two parts. First, simulation results of the proposed 19-level I-DFCM converter are provided to verify its good performance and switching pattern. Then, simulation results of 11-level FCM, DFCM, and I-DFCM converters, possessing the same conditions and specifications, are presented to facilitate their comparison.

Fig. 5. Output voltage and load current (increased by coefficient of 10) of a four-cell 19-level proposed I-DFCM converter.

Fig. 6. Internal flying capacitors' voltages of a four-cell 19-level proposed I-DFCM converter.

Fig. 7. Output voltage frequency spectrum of a four-cell 19-level proposed I-DFCM converter.

TABLE III
MAIN PARAMETERS OF A SIMULATED I-DFCM CONVERTER

System Parameters	Values
Major dc voltage (E)	200 V
Minor dc voltage (E)	25 V
Internal flying capacitors (C)	1000 uF
PSC-PWM carrier frequency	1 kHz
Fundamental output voltage frequency	50 Hz
Resistive-inductive load (R_L- L_L)	15 Ω – 30 mH

A. 19-Level Proposed I-DFCM Converter

The output voltage of the proposed four-cell 19-level I-DFCM converter with THD of 6% and the load current (increased by coefficient of 10) both in the steady state, internal flying capacitors voltages in both transient and steady states, and frequency spectrum of output voltage are shown in Figs. 5–7, respectively. The converter is operated with a modulation index equal to 0.8 ($M = 0.8$) and controlled by the proposed modulation method in which the PSC-PWM frequency is 1 kHz. Fig. 5 illustrates that the major converter (DFCM converter) produces nine major levels, i.e., ± 50, ± 100, ± 150, ± 200 V, and the minor converter adds minor levels, i.e., ± 25 V, between the major levels; thus, the output voltage of an I-DFCM converter is the sum of the major and minor converters' output voltages and has 19 levels with steps of 25 V. Moreover, as illustrated in Fig. 6, flying capacitors reached their desired voltage values without any feedback control due to the operation of I-DFCM based on phase-shifted modulation method. As shown in Fig. 7, which demonstrates the frequency spectrum of output voltage, the output voltage has harmonic groups around the $\left(k \times 9 \times 1^{\mathrm{kHz}}\right)$ th harmonic where k is the integer number and 9 is the number of voltage levels produced in each half-cycle. The main parameters used in the simulations are given in Table III.

B. 11-Level FCM, DFCM, and Proposed I-DFCM Converters

In this section, to compare different types of flying capacitor-based converters with each other in order to highlight the advantage of the proposed converter, simulation results of 11-level FCM, DFCM, and I-DFCM converters possessing the same conditions and specifications are presented. The main parameters used in the simulations are as follows: internal flying capacitors are 1 mF, resistive–inductive load (R_L–L_L) is 15 Ω–30 mH, maximum output voltage is ± 250 V, PSC-PWM frequency is 1 kHz, and LC filter including an inductor of 0.8 mH and a capacitor of 20 μF with cutoff frequency of 1.3 kHz is added at the output of converters. Steady state of output voltage and load current (increased by factor of 10), steady and transient states of internal flying capacitors' voltages, and frequency spectrum of output voltage before LC filter pertaining to FCM, DFCM, and

Fig. 8. Simulation results of an 11-level ten-cell FCM converter. (a) Output voltage and load current (increased ten times). (b) Internal flying capacitors' voltages. (c) Frequency spectrum of output voltage before *LC* filter.

Fig. 9. Simulation results of an 11-level five-cell DFCM converter. (a) Output voltage and load current (increased ten times). (b) Internal flying capacitors' voltages. (c) Frequency spectrum of output voltage before *LC* filter.

I-DFCM converters are shown in Figs. 8–10, respectively. As can be pointed out, the I-DFCM converter has the fastest time response in balancing the voltage of internal flying capacitor, improving the dynamic of converter, while all conditions such as load impedance, load current, the capacitance of flying capacitors, and output *LC* filter are the same in all the aforementioned converters. It is worth mentioning that the time response of the I-DFCM converter (about 0.1 s) is 25 times faster than the time response of the FCM converter (about 2.5 s) and is three times faster than the time response of the DFCM converter (about 0.3 s).

Furthermore, the FCM and DFCM converters need nine and four flying capacitors, respectively, while the I-DFCM converter needs only one flying capacitor. This advantage makes the I-DFCM converter cheaper and smaller in comparison with the FCM and DFCM converters for the same output voltage and same power rating. As shown in Figs. 8(c), 9(c), and 10(c), the harmonic groups of output voltage before *LC* filter are around $\left(k \times m \times 1^{\mathrm{kHz}}\right)$ th harmonic in which k is an integer number and m is the number of carriers which are used in each half cycle of fundamental frequency to be intersected with reference signal. It should be mentioned that in the obtained simulation results of FCM, DFCM, and proposed I- DFCM converters, m equals 10, 5, and 5, respectively. The THD of output voltage before *LC* filter in FCM, DFCM, and I-DFCM converters are 8.5%, 11%, and 11%, respectively. The reason for low THD in an FCM converter is that the PSCAD software can measure THD only up to 255th harmonic; thus, the second harmonic group pertaining to unfiltered output voltage in an FCM converter which is around 400th harmonic cannot be measured by the PSCAD software. In contrast, the second harmonic group of unfiltered output voltage in DFCM and I-DFCM converters falls around 200th harmonic which can be measured by the PSCAD software. Consequently, THD of DFCM and I-DFCM converters is calculated based upon two harmonic groups of unfiltered output voltage, causing higher value of THD. Moreover,

Fig. 10. Simulation results of the proposed 11-level two-cell I-DFCM converter. (a) Output voltage and load current (increased ten times). (b) Internal flying capacitors' voltages. (c) Frequency spectrum of output voltage before *LC* filter.

as shown in Figs. 8–10, the output voltage after *LC* filter in all three converters is almost the same with THD of about %1.

IV. Experimental Results

To verify the feasibility and practicality of the proposed I-DFCM converter and its control scheme, a prototype of a two-cell 11-level converter was built and tested in the laboratory. The converter is implemented with eight BUP-314D 1200 V 42 A IGBTs while the capacitance of flying capacitor (C) is 3.6 mF, major dc bus voltage is 160 V, and minor dc bus voltage is 40 V. The resistive–inductive load is $R_L = 44.3\ \Omega$ and $L_L = 19.4$ mH. The balance booster circuit parameters are $R_b = 90\ \Omega$, $L_b = 7\ \mu$H, and $C_b = 145\ \mu$F. The switching frequency is 5 kHz and modulation index is 0.9. The dsPIC30F4011 microcontroller manufactured by MICROCHIP has been used to control the new converter according to the proposed modulation method. The gate drivers for IGBTs and opto-isolators are IR2111 and 6N136 ICs, respectively. It should be mentioned that an isolated power supply is used for each gate driver. Fig. 11

Fig. 11. Experimental results of the proposed two-cell 11-level I-DFCM converter. (a) V_{AB}. (b) V_{AN}.

shows the measured waveforms of V_{AB} and V_{AN}, and furthermore, the waveforms of output voltage, load current, and the flying capacitor's voltage are illustrated in Fig. 12.

Another experimental test has been conducted for a four-cell 19-level proposed I-DFCM shown in Fig. 13. This converter is built with the 12 aforementioned type IGBTs while the capacitance of flying capacitors C is 1850 μF, major dc bus voltage is 178 V, and minor dc bus voltage is 22 V. The control unit and other circuit parameters are the same as those used in the previous experimental test. Figs. 14 and 15 show the measured waveforms of this converter and the voltage waveforms of flying capacitors, respectively.

V. Cost and Size Comparison of DFCM and I-DFCM

It is obvious that the size and cost of the DFCM converter is much lower than the size and cost of the FCM converter in producing the identical output voltage with the same condition and power rating. The reason is that the number of switches (with the same specification and power rating), the number of flying capacitors, and the number of dc voltage sources in the DFCM converter are half the number of those components in the FCM converter. Therefore, the price of the DFCM converter is much less than the FCM converter in the same power rating. Thus, the proof of reduction of size and cost of I-DFCM converter in comparison with DFCM converter means that the size and cost of the I-DFCM converter is the lowest among the three mentioned converters. A comparison between the main parts,

Fig. 12 Experimental results of the proposed two-cell 11-level I-DFCM converter. (a) Output voltage V_{AO} . (b) Flying capacitor voltage V_{C1} . (c) Load voltage and current. (d) More detailed waveform of load voltage and current.

Fig. 13. Hardware implementation of a four-cell 19-level proposed I-DFCM converter.

i.e., switches, gate drivers, gate drivers' isolated power supply, and flying capacitor of the DFCM and proposed I-DFCM converters is illustrated next. The information about size and cost of the mentioned components are obtained from an online distributer such as NEWARK, DIGIKEY, and MOUSER, or the website of some companies such as IRF and ABB. In this part, any increase or decrease in the I-DFCM converter's size, cost, and components count is compared with the DFCM converter. Also, it is assumed that these converters have the same specifications and operational conditions such as the same load impedance, maximum output voltage, number of voltage levels, output current, and switching frequency.

A. Size and Cost Comparison of Required DC Links

DFCM and I-DFCM converters need one and two dc-link voltage, respectively. However, the current rating of those dc links is almost the same in both converters, due to the same load current, and the voltage rating of one dc link in DFCM is equal to the total voltage rating of two dc links in I-DFCM. If the combination of transformer, diode rectifier, and dc capacitor is used to make the dc link, it is possible to implement the configurations shown in Fig. 16. In these configurations, from the transformer point of view, the number of primary winding's turns, total number of secondary winding's turns, wire thickness in primary and secondary side, total power rating, and core size are the same as shown in Fig. 16(a) and (b). The only difference between Fig. 16(a) and (b), from the transformer point of view, is that Fig. 16(b) needs isolation between two windings at the secondary side. The price of this isolation is not significant in comparison with the price of the whole transformer; as a result, the price of the transformer in Fig. 16(a) and (b) is almost same. Moreover, the total price of diode rectifier and dc capacitor to make the dc link with voltage rating of n p.u. is approximately the same as the total price of two diode rectifiers and two dc capacitors to make two dc links with voltage ratings of $(n-1)$ p.u. and 1 p.u. As a result, it can be concluded that the total price to make the required dc links in I-DFCM and DFCM is nearly the same.

(a)

(b)

(c)

(d)

Fig. 14. Experimental results of the proposed four-cell 19-level I-DFCM converter. (a) V_{AB}. (b) V_{AN}. (c) Output voltage and load current. (d) More detailed waveform of output voltage.

(a)

(b)

(c)

Fig. 15. Experimental results of the proposed four-cell 19-level I-DFCM converter. (a) Flying capacitor voltage of cell-1 V_{C1}. (b) Flying capacitor voltage of cell-2 V_{C2}. (c) Flying capacitor voltage of cell-3 V_{C3}.

(a)

(b)

Fig. 16. Configuration to make required dc links in (a) DFCM converter and (b) proposed I-DFCM converter.

B. Size and Cost Comparison of Switches

According to Table II, the number of high-frequency switches in the proposed I-DFCM converter is almost half the number of high-frequency switches in the DFCM converter to produce the same number of levels. However, the voltage rating of switches in the I-DFCM converter is two times higher than the voltage rating of switches in the DFCM converter to produce the identical output voltage; but the current rating of switches in both converters is the same because it was assumed that the output voltage and current is the same in both converters. The price of switches with 2 p.u. voltage rating and 1 p.u. current rating is around 150–200% of the price of switches with 1 p.u. voltage rating and 1 p.u. current rating (The price of switches with voltage rating up to 1200 V was only available in the aforementioned online distributor or companies). This means that the price of all high-frequency switches in the I-DFCM converter is almost 75% or 100% in the worst case, compared with the DFCM converter. It should be mentioned that the voltage rating unit is different from the current rating unit. In the comparison process, an attempt was made to compare the switches with each other to have almost the same condition such as power dissipation, power loss, total gate charge, and turn-on time. On the other hand, producing the identical output voltage by DFCM and the proposed I-DFCM needs the same high-power low-frequency switches. Thus, it can be pointed out that the ratio of total price of all switches in the I-DFCM converter to the DFCM converter is 1 for the worst case and 0.75 for the best case.

C. Size and Cost Comparison of Switches' Gate Drivers

The price of gate drivers for switches with voltage rating of 2 p.u. is about 100–140% of the price of gate drivers for switches with a voltage rating of 1 p.u. It should be mentioned that the comparison was done between ICs with the same specification such as output current and type of package. Due to the reduction of the number of switches in the I-DFCM converter by 50%, the required number of gate drivers is reduced by 50% in the I-DFCM converter; this issue causes a reduction in the price of all required gate drivers by 50–70%. Moreover, the size of all required gate drivers can then decrease by 50%.

D. Size and Cost Comparison of Gate Drivers' Isolated Power Supplies

Each gate driver needs one isolated power supply to be able to operate while the price and especially the size of the isolated power supply are comparable with the price and size of the gate driver. Due to the reduction of the number of required gate drivers by 50% in the I-DFCM, the number of required isolated power supply is decreased by 50% which results in a significant decrease in the size and cost of all required isolated power supply.

E. Size and Cost Comparison of Flying Capacitors

Flying capacitors are remarkable components from the cost and size point of view in flying-capacitor-based converters. Furthermore, in flying-capacitor-based converters, the price of the dc flying capacitors is much higher (sometimes ten times higher) than the price of switches.

Although, due to the identical output current, the capacitance of flying capacitors is the same in both the I-DFCM and DFCM converters, the number of flying capacitors in the I-DFCM is decreased by more than 50%. For example, a three-cell 15-level I-DFCM converter with maximum voltage of 15 p.u. needs two capacitors with voltage rating of 2 and 4 p.u., while the DFCM converter needs six capacitors with a voltage rating of 1, 2, 3, 4, 5, and 6 p.u. to produce the same output voltage. In general, the I-DFCM converter needs $n-1$ flying capacitors to produce $4n+3$-level output voltage while the DFCM converter needs $2n$ flying capacitors. Even if we assume that the capacitors with different voltage rating have the same price and size, which is not the case, the size and price of the required flying capacitors can be reduced by more than 50%. In practice, it can decrease much more than 50%. Moreover, capacitors have less life time in comparison with other components. As a result, decreasing the number of capacitors makes these converters more reliable.

Moreover, reduction in the size and number of required components causes a decrease in the size of the PCB. In conclusion, the price and size of the proposed I-DFCM converter are significantly less than the price and size of the DFCM converter for the same operational condition and specification.

VI. Conclusion

Even though the flying-capacitor-based converters such as FCM, SM, and DFCM offer remarkable advantages for medium voltage and high-power applications, they unfortunately require bulky and costly flying capacitors. This paper proposes a new configuration called the I-DFCM converter to decrease the number of cells and flying capacitors as well as the flying capacitors' voltage ratings. This results in a reduction of the cost and size of the flying-capacitor-based converters and makes them more practical. These achievements are obtained by adding one cell, including one dc voltage source whose voltage rating is a small fraction of the main dc-link voltage rating, and two low-power high-frequency switches, to the conventional DFCM converter. The added cell produces the minor levels (odd levels) between the major levels (even levels) while the voltage rating and total power rating of the switches are almost the same in both the proposed and the conventional converters. Moreover, a proposed modulation method is implemented to control the new I-DFCM converter while the natural self-balancing property still exists to balance the voltage of flying capacitors in their desired level without any active or feedback control. In addition, the complete comparison between the conventional flying-capacitor-based converters and the proposed one is illustrated regarding the number of devices, voltage rating of devices, and the amount of stored energy in the converters. Moreover, the simulation results of the proposed I-DFCM, FCM, and DFCM converters producing 11-level output voltage are illustrated and compared with each other. The provided simulation results together with the measured experimental results verify the good performance and feasibility of the proposed converter.

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REFERENCES

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[2] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[3] A. K. Sadigh, V. Dargahi, and A. Shoulaie, "Elimination of one dc voltage source in stacked multicell converter," *IET Power Electronics*, doi: 10.1049/iet-pel.2011.0320, to be published.

[4] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulse width modulation," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1517–1526, Jun. 2010.

[5] B. P. McGrath and D. G. Holmes, "Enhanced voltage balancing of a flying capacitor multilevel converter using phase disposition (PD) modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1933–1942, Jul. 2011.

[6] A. K. Sadigh, S. H. Hosseini, S. M. Barakati, and G. B. Gharehpetian, "Flying capacitor multicell converter based dynamic voltage restorer," in *Proc. 41st North Amer. Power Symp.*, Oct. 2009, pp. 1–6.

[7] A. Shukla, A. Ghosh, and A. Joshi, "Natural balancing of flying capacitor voltages in multicell inverter under PD carrier-based PWM," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1682–1693, Jun. 2011.

[8] F. H. Khan, L. M. Tolbert, and W. E. Webb, "Start-up and dynamic modeling of the multilevel modular capacitor-clamped converter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 519–531, Feb. 2010.

[9] A. K. Sadigh, E. Babaei, S. H. Hosseini, and M. Farasat, "Dynamic voltage restorer based on stacked multicell converter," in *Proc. IEEE Symp. Ind. Electron. Appl.*, Kuala Lumpur, Malaysia, Oct. 2009, pp. 1–6.

[10] Y. Zhang and L. Sun, "An efficient control strategy for a five-level inverter comprising flying-capacitor asymmetric H-bridge," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4000–4009, Sep. 2011.

[11] A. Shukla, A. Ghosh, and A. Joshi, "Hysteresis modulation of multilevel inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1396–1409, May 2011.

[12] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[13] J. Wen and K. M. Smedley, "Synthesis of multilevel converters based on single- and/ or three-phase converter building blocks," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1247–1256, May 2008.

[14] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 25–33, Jan. 2009.

[15] J. Wen and K. M. Smedley, "Hexagram rectifier—Active front end of hexagram inverter for medium-voltage variable-speed drives," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 3014–3024, Nov. 2008.

[16] V. Dargahi and A. Shoulaie, "Capacitors voltage balancing modeling in three phase flying capacitor converters with booster," in *Proc. Power Electron. Drive Syst. Technol. Conf.*, Feb. 2012, pp. 1–6.

[17] A. K. Sadigh, S. H. Hosseini, S. M. Barakati, and G. B. Gharehpetian, "Stacked multicell converter based DVR with energy minimized compensation strategy," in *Proc. 41st North Amer. Power Symp.*, Oct. 2009, pp. 1–6.

[18] A. Shukla, A. Ghosh, and A. Joshi, "Improved multilevel hysteresis current regulation and capacitor voltage balancing schemes for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 518– 528, Mar. 2008.

[19] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[20] P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[21] T. A. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *Eur. Power Electron. Drives J.*, vol. 2, no. 1, pp. 45–50, Mar. 1992.

[22] T. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: Basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002.

[23] T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: Derived topologies," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 978–987, Oct. 2002.

[24] G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): Properties and design," in *Proc. IEEE 32nd Annu. Power Electron. Spec. Conf. Meet.*, 2001, pp. 1583–1588.

[25] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, "Multicell converters: Active control and observation of flying capacitor voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 998–1008, Oct. 2002.

[26] S. Mohamadian and A. Shoulaie, "Comprehensive definitions for evaluating harmonic distortion and unbalanced conditions in three and four-wire three-phase systems based on IEEE standard 1459," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 1774–1782, Jul. 2011.

[27] X. Yuang, H. Stemmler, and I. Barbi, "Self-balancing of the clamping capacitor- voltages in the multilevel capacitor-clamping-inverter under sub-harmonic PWM modulation," *IEEE Trans. Power Electron.*, vol. 16, no. 2, pp. 256–263, Mar. 2001.

[28] R. Wilkinson, H. du Mouton, and T. Meynard, "Natural balance of multicell converters: The two-cell case," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1649–1657, Nov. 2006.

[29] R. Wilkinson, H. du Mouton, and T. Meynard, "Natural balance of multicell converters: The general case," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1658–1666, Nov. 2006.

[30] B. P. McGrath and D. G. Holmes, "Analytical modeling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 543–550, Mar. 2008.

[31] B. P. McGrath and D. G. Holmes, "Natural current balancing of multicell current source converters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1239–1246, May 2008.

[32] B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, Mar. 2007.

[33] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted PWM control for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 178–185, Jan. 2007.

[34] A. Shukla, A. Ghosh, and A. Joshi, "Flying-capacitor-based chopper circuit for dc capacitor voltage balancing in diode-clamped multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2249–2261, Jul. 2011.

[35] A. K. Sadigh and S. M. Barakati, *Modeling and Control of Sustainable Power System*. New York: Springer, 2012, ch. 14, pp. 311–340.

[36] A. K. Sadigh, V. Dargahi, and S. M. Barakati, "New asymmetrical cascade multicell converter based on optimized symmetrical modules," in *Proc. Int. Symp. Ind. Electron.*, May 2012, pp. 1–6.

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