Light Load Efficiency Improvement in Buck-derived Single-stage Single-switch PFC Converters

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***Abstract*—Single-stage single-switch ac/dc converters with power factor correction (PFC) generally have higher power losses at light load condition, as compared to that of two-stage approach, due to the sharing of common power transistor such that the PFC stage cannot be switched off separately to save power losses. This letter addresses this problem by using a buck topology for the PFC stage of the single-stage single-switch converters as it can be completely turned off by operating the converter only near the zero crossing of the input voltage, due to the presence of dead angle of input current. Hence the switching and conduction losses to the transistor and diodes, and passive devices are reduced. Also, further improvement is carried out by finding the best combination of dc bus capacitor charging time and discharging time to achieve the lowest power loss. A recently proposed converter topology which combines a buck PFC cell with a buck-boost dc/dc cell is used as an example. Experimental results are reported and confirmed that the proposed light load power loss reduction scheme on the converter can improve power stage efficiency by up to 7% at 1W of output power as compared to that without the proposed scheme.**

***Index Terms*—Power factor correction, light load efficiency, power consumption, single-stage**

I. Introduction

Since the research of single-stage power-factor-corrected (S^2PFC) converters in the early nineties, they have now been adopted for different low power conversion equipment such as power factor correction (PFC) pre-regulators, electronic ballast and ac adaptors. The acceptance of S^2PFC converters is because of their simplified converter structure and controller circuit as compared to the two-stage PFC design. They favour applications where cost and compact design are of prime concern.

In recent years, energy efficient concept is incorporated into switching power supply design due to the enforcement of stringent standards from regulatory bodies such as Energy Star and AU/NZ Minimum Energy Performance Standards (MEPS). There are various approaches to reducing power consumption at light load condition. Adding a small auxiliary power conversion circuit in parallel with the output load improves the overall efficiency, particularly at light load condition [1]. The idea is to optimize both main and auxiliary power conversions by varying the sharing of total output power among the two conversions at different load conditions. Light load frequency modulation is introduced to maintain soft-switching (ZVS) of the converter even at light load condition [2]. In [3], the output load range is divided into several sections and efficiency optimization is achieved through operating the converter at different switching frequencies. Buck PFC front-end has a higher light load efficiency than that of its boost counterpart [4] due to its lower voltage stress on switching devices. At light load, switching loss is more dominant than conduction loss and the voltage stress is the key factor in determining switching loss. By dynamically scaling of gate drive voltage, the switching loss can also be reduced [5]. For two-stage PFC design, turning off the PFC stage has been proven an effective method to reduce power loss [6]. However, in general it is difficult to apply the same method to S^2PFC converters as the PFC stage and dc/dc stage share the same power switch, unless the converter has multiple switches and is constructed differently such that it can control currents from the ac line and intermediate storage capacitor to flow into the converter in separate time slots within a switching period (e.g. [7]).

This letter, however, introduces a possible approach to turning off the PFC stage in single switch S^2PFC converters similar to that in the two-stage approach [6]. The idea takes the advantages of varying input voltage and dead angle of input current characteristic of the ac/dc converter. Buck or buck-derived PFC converter inherently has such characteristic as there are times during a line cycle when the input voltage is smaller than the output voltage and the PFC stage is effectively turned off. The purpose of this letter is hence to explain, analyze and demonstrate this approach through a selected single-stage single-switch buck-derived PFC topology under the light load operation where power consumption of the load is only a few watts or less and to evaluate different switching patterns to search for the lowest power losses under this condition. Experimental results are presented to demonstrate the effectiveness of the proposed light load power losses reduction scheme. Note that the purpose of this letter is not to show the experimental results that are complied with international standard but suggest several possible power saving combinations, which take the advantage of the uniqueness of buck PFC converter operation and different operating regions in each half-line cycle, for light load operation. The authors believe by detailed product design, circuit optimization and selection of low power consumption integrated circuits, the proposed methods can assist the compliance with the standards.

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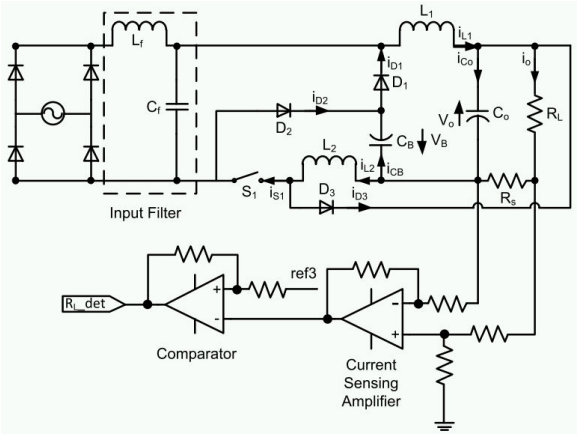


Fig. 1. Proposed converter which combines a buck PFC cell and a buck-boost dc/dc cell.

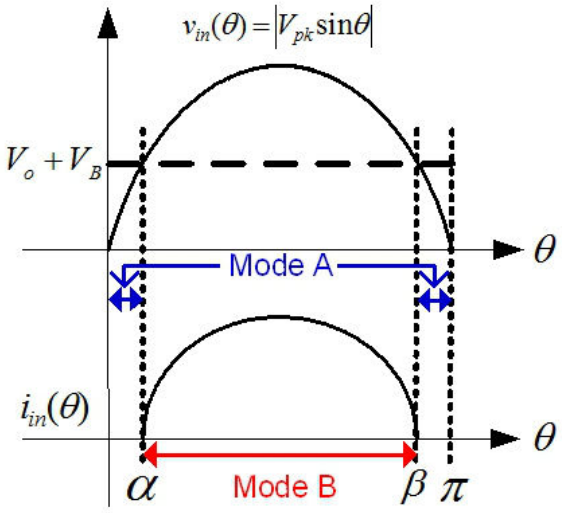


Fig. 2. Definition of Mode A and Mode B for the converter operation during half line cycle.

II. Operation Principle of the Selected Converter

To facilitate the explanation of light load operation in single-stage PFC converters, a recently introduced transformerless high step-down single-stage PFC converter [8] is used as an example. The converter, as shown in Fig. 1, is an integration of a buck PFC cell with a buck-boost dc/dc cell. The buck PFC cell consists of L_1, S_1, D_1, C_o and C_B while the buck-boost dc/dc cell consists of L_2, S_1, D_2, D_3, C_o and C_B. Since the input voltage v_{in} varies between zero and its peak value, and also as the buck converter only operates when input voltage is greater than output voltage, the proposed converter has two operation modes. As detailed explanation has been reported in [8], the operation principle of the converter with the aid of Fig. 2 is only briefly reviewed here:

Mode A occurs when $v_{in} \leq V_B + V_o$ (where V_B is the dc bus capacitor voltage and V_o is the output voltage). The buck PFC cell is inactive and there is no input current flowing into the converter. In this mode only the buck-boost dc/dc cell is active. When the switch S_1 is turned on, L_2 is charged by C_B through D_2. The output voltage is sustained by output capacitor C_o. After a duration of $d_1 T_s$, S_1 is turned off. The energy stored in L_2 is transferred to output via D_3. i_{L2} is completely discharged before the start of next switching cycle.

Mode B occurs when $v_{in} > V_B + V_o$. Both PFC cell and dc/dc cell are active. When S_1 is turned on, both inductors L_1 and L_2 are charged linearly by $v_{in} - V_o - V_B$ and V_B respectively. After a duration of $d_1 T_s$, S_1 is turned off. L_2 releases its energy to output via D_3 while L_1 couples its energy to both output and bus capacitors as $C_o||R_L$ and C_B are in series of the current path of i_{L1}. Both i_{L1} and i_{L2} are completely discharged before the start of next switching cycle.

III. Implementation of Light Load Power Management

A. Concept

Switching loss of power semiconductors is the major cause of low efficiency of single-stage PFC converters under light load condition. Due to the dead angle of input current of the buck PFC cell, it is possible to use this duration to turn off the PFC cell to reduce switching loss of power semiconductors and conduction loss of passive devices. This section hence explores the possibility of reducing the switching loss by different PWM patterns while maintaining output voltage (V_o) regulation and dc bus voltage (V_B) control. Note that it is common in single-stage PFC converters that the bus voltage cannot be regulated but only be controlled within a certain range due to the lack of extra control device in the simplified converter structure; the power MOSFET can achieve only one dimensional control which is the output voltage regulation. Although some research has been done using continuous variable frequency control to limit the bus voltage, the wide switching frequency range will incur extra switching losses [9]. This paper uses a similar concept to burst mode control [6], [10]. But instead of having a random pattern of pulses, the proposed light load power management has deterministic patterns of pulses as described as follows.

This paper considers four distinctive PWM patterns to operate the single-stage buck-derived PFC converters under light load condition. In all cases, the output voltage is regulated by a voltage-mode controller.

- The first scheme (M1) does not use any specific switching pattern. The converter operates at fixed switching frequency and the duty cycle reduces when the load decreases. This scheme is used as a reference for comparison of the proposed power management schemes (M2 to M4).
- The second scheme (M2) operates the converter in the zero crossing region of rectified input voltage where the buck PFC cell is inactive (i.e. Mode A in Sec. II). Note that the duration of Mode A is defined by the voltage conversion ratio and is given by $\arcsin[(V_o + V_B)/V_{pk}]$ according to Fig. 2. However, if operating in Mode A only, the dc bus voltage will decrease to zero gradually as the charge is taken away from the bus capacitor by the buck-boost dc/dc cell but there is no input current flowing into the buck PFC cell in order to charge the bus

capacitor. Therefore in order to control the bus voltage, the converter will continue to operate and enter Mode B (defined in Sec. II) for a short duration so that the buck PFC cell is active. Hence the bus capacitor can be recharged to maintain its voltage but at a lower level.

- The third scheme (M3) operates the converter around the peak input voltage only. Both buck PFC cell and buck-boost dc/dc cell are in active states (i.e. Mode B in Sec. II). Apart from the output regulation, with this method, the dc bus voltage is somehow controlled as charging and discharging of bus capacitor occur simultaneously.
- The fourth scheme (M4) combines the two schemes above; the converter operates at both the zero crossing and peak input voltage regions. Unlike scheme M2, however, the converter will not operate just beyond the dead angle of input current except for region around the peak input voltage duration. This method also allows for bus voltage control and output voltage regulation.

Note that schemes M2 to M4 define when the converter operates to generate the burst mode patterns. For every burst duration, fixed-frequency PWM pulses are used.

B. Practical implementation

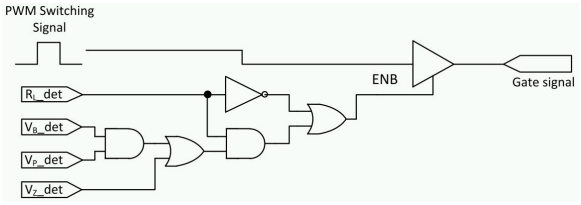
A logic circuit, as shown in Fig. 3(a), is added to the PWM controller to implement the above three light load power management schemes. The truth table of the logic circuit is shown in Fig. 3(b), where X denotes a don't-care option and C1 and C2 denote binary control variables. The light load operations (M2 to M4) will be enabled once R_{L_det} is at level high. The signal R_{L_det} is generated from the current sensing amplifier and the comparator as shown in Fig. 1. The output load current of R_L is sensed via R_s. Once the current in R_s is below a pre-determined level (in this example was equivalent to 3W of output power), R_{L_det} will set to high and enable M2 to M4 light load operation schemes. The full logic function of the proposed three light load power management schemes can be summarized by the following boolean equality:

$$\text{ENB} = \overline{R_{L\_det}} + R_{L\_det}(V_{B\_det} \cdot V_{P\_det} + V_{Z\_det}) \quad (1)$$

where ENB determines when the PWM signal will be sent to the gate of MOSFET, V_{B_det} will go high when the bus voltage is lower than the pre-defined level, V_{P_det} will go high when peak input voltage is close, and V_{Z_det} will go high when the zero crossing region is near.

The logic design for M2 to M4 implementations are described as follows:

- To activate M2 (near zero crossing of input voltage PWM switching), the rectified input voltage is sensed and compared with a voltage reference. Once the rectified input voltage goes lower than the reference voltage, V_{Z_det} is set to high. This reference voltage is set such that it allows the single-stage converter or the buck PFC cell to operate for a short duration in Mode B and charge the bus capacitor. V_{P_det} and V_{B_det} are set to low level at all times in this scheme. With such settings the enable signal ENB is at high level only when V_{Z_det} is at level high, enabling PWM switching to occur.



(a) Logic circuit.

	M1	M2	M3	M4
R_L_det	0	1	1	1
V_B_det	X	0	1	C1
V_P_det	X	0	C1	C1
V_Z_det	X	C1	0	C2
ENB	Always 1	1 when C1=1	1 when C1=1	1 when C1=1 or C2=1

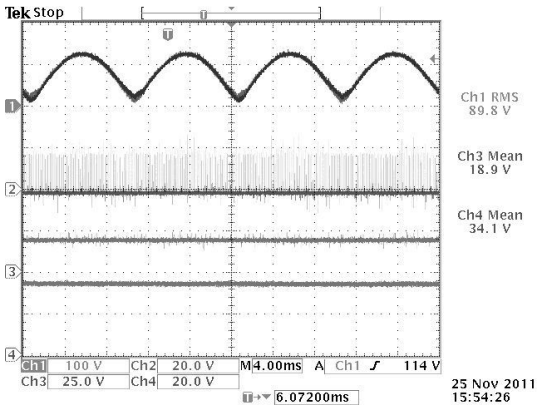
(b) Logic truth table.

Fig. 3. Logic circuit and its truth table for zero crossing discharge and peak voltage charge.

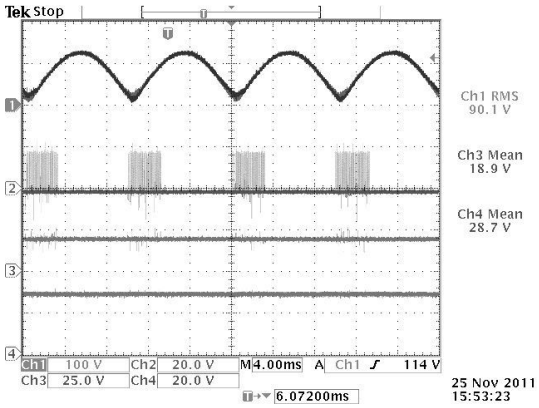
- To activate M3 V_{B_det} is set to high level at all times. V_{P_det} will set to high once the input voltage reaches near the peak input voltage range. V_{Z_det} is set to low level at all times in this scheme. With such settings the enable signal ENB is at high level only when V_{P_det} is at level high, enabling PWM switching to occur.
- To activate M4 V_{B_det} is set to high level once the bus voltage V_B is smaller than the lowest allowable voltage. V_{P_det} and V_{Z_det} will set to high once the input voltage reaches near the peak input voltage range and once it reaches near the zero crossing range respectively. With such settings the enable signal ENB is at high level whenever V_{B_det} and V_{P_det} are both at level high or V_{Z_det} is at level high, enabling PWM switching to occur.

IV. Experimental Verifications and Discussion

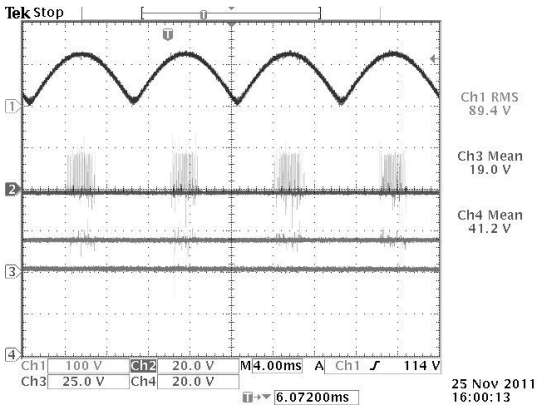
To verify the proposed light load power management schemes, a laboratory hardware prototype of Figs. 1 and 3 is built and tested. The values of key circuit parameters and operation conditions for the converter are shown as follows: L_f = 2mH, C_f = 2μF, L_1 = 106μH, L_2 = 46μH, S_1 = SPW47N60CFD, D_1 to D_3 = MUR3040PT, C_B and C_o = 5mF, PWM controller = TL594, v_{in} = 90Vac, and V_o = 19Vdc. To implement the burst mode control as depicted in Fig. 3(a), an AND gate is used to implement ENB which combines the PWM controller output and the logic output. Then the resultant burst mode signals are fed to an opto-coupler gate driver to drive S_1. The list of equipment for the test is shown as follows: Power analyzer (Voltech PM100), DSO (Tektronix TDS3012), power source (GW INSTEK APS-1102) and electronic Load (TEKPower 3710A). The efficiency measurement does include the voltage and current sensors but does not include the power consumption of the control part which includes PWM IC, comparators and logic gates. For fair comparison, same setting is used for all four modes.



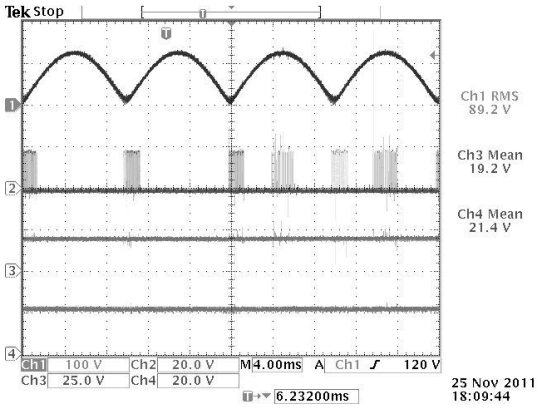
(a) M1: Normal PWM switching



(b) M2: Switching near zero-crossing



(c) M3: Switching near the peak input voltage



(d) M4: Combining M2 and M3

Fig. 4. Switching waveforms of the converter at different stand-by mode power managements. CH1: Rectified input voltage; CH2: Gate signal; CH3: Output voltage V_o; CH4: DC bus voltage V_B. Time base: 4ms/div.

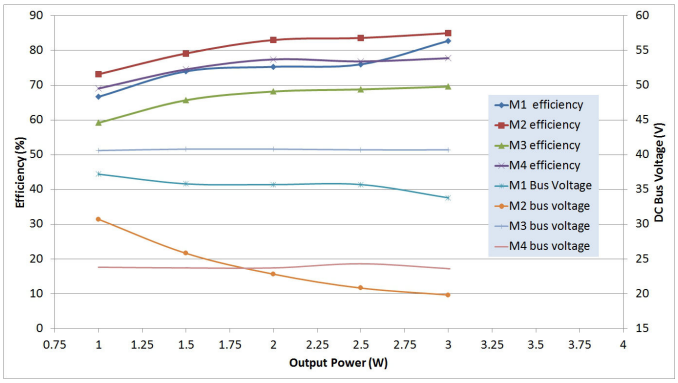


Fig. 5. Comparison of measured efficiencies and dc bus voltages of different light load schemes.

Fig. 4 shows the key experimental waveforms of the four schemes (M1 to M4). The rectified input voltage and gate pulses shown in the figure confirm the designed switching patterns and logic design for the four schemes as discussed in Section III. For all schemes the output voltage is regulated at 19V. It is observed that the dc bus voltage, V_B, in different scheme has different value. A more clear picture for V_B under different load conditions (from 1W to 3W) for all schemes is shown in Fig. 5. For scheme M3, it has the highest V_B among other schemes whilst M4 has lowest V_B at 1W to 1.5W and M2 has lowest V_B from 2W to 3W.

The difference of V_B value can be explained by the occurrence of switching during the varying input voltage. For scheme M3, the switching occurs entirely around the peak input voltage. For scheme M2, the switching occurs mostly at the zero crossing region. Scheme M4 has switching in both regions. According to the equation of V_B against input voltage [8], it is shown that for a given ratio of L_1 to L_2, V_B increases as RMS input voltage increases. Therefore as scheme M3 has the highest effective input voltage, it is expected that V_B is higher in M3 than that in M2 and M4. (Note that it is common in S^2PFC converters that V_B varies proportionally to the input voltage [11]). The effective input voltage varies from scheme to scheme is that although the input ac voltage is the same for all schemes, the converter operates in burst mode (for schemes M2 to schemes M4) and hence the region where the switching takes place causes the converter to operate as if it is operating at different line voltage. For M3 the converter operates as if input voltage is around 120V. For M2 the converter operates as if it is around 15V or so. For M4 it operates mostly at lower voltage region but sometimes near peak input voltage to recharge C_B. The reason for V_B for M2 is higher than that for M4 from 1W to 1.8W is that M2 has extended operation of the converter outside dead angle of input current to operate in Mode B (i.e. PFC cell is active to recharge C_B). The duration in Mode B for M2, however, is fixed in this experiment and therefore as output power increases new equilibrium points on both C_B and duty cycle have to be re-established and hence it is reflected on V_B.

As shown in [12], at light load condition the MOSFET switching loss and diode loss dominant the total losses of a single-ended converter in the absence of a snubber circuit.

The switching losses involves turn-on and turn-off losses. For turn-on losses, it involves the switch capacitance loss and current-rising-voltage-trailing crossed conduction loss. Since the absolute value and the rate of change of current through the MOSFET are limited by the inductor at light load (i.e. $i_{L1} = i_{L2} = 0$ when MOSFET turns on), this turn-on crossed conduction loss is negligible. Switch capacitance loss is then the major switching turn-on loss component. The switch capacitance loss, $P_{sw,cap}$, is determined by the following equation:

$$P_{sw,cap} = \frac{1}{2} f_s C_{oss} v_{DS}^2 \tag{2}$$

where C_{oss} is the switch output capacitance, f_s is the switching frequency and v_{DS} is the drain-to-source voltage of the MOSFET. Since all four schemes use the same MOSFET and similar burst mode frequency (except for M1), v_{DS} becomes the main variable that makes the difference in the turn-on switching loss. v_{DS} referring to Fig. 1 is given by the following conditions:

$$\begin{array}{ll} v_{DS} = V_B & \text{in Mode A (PFC inactive)} \\ v_{DS} = |v_{in}| - V_o & \text{in Mode B (PFC active)} \end{array} \tag{3}$$

Equation (3) here shows status of v_{DS} just before the MOSFET is turned on. Comparing the occurrence of which switching takes place, scheme M3 has the switching only at the peak input voltage where it happens in Mode B and $|v_{in}| - V_o > V_B$ for switching near the peak input voltage and therefore v_{DS} for M3 is the highest amongst others schemes. M4 has switching mainly at the zero crossing and partly at the peak input voltage while M2 only switches at the zero crossing. Therefore from the turn-on switching loss perspective, the turn-on switching loss in descending order is M3 $>$ M4 $>$ M2.

Regarding the turn-off switching loss, it mainly depends on the current-trailing-voltage rising crossed conduction loss. As for M2, most of the switching time happens near the zero crossing region and the PFC cell is turned off (i.e. i_{L1} = 0), the current flowing through S1 comes from C_B only. When S1 turns off, only $i_{L2} (= i_{CB})$ intersects with v_{DS}. However, for M3, most of the switching time occurs at the peak input voltage and the PFC cell is turned on, there are currents from input voltage and bus capacitor flowing through S1 simultaneously and therefore when S1 turns off, both i_{L1} and i_{CB} intersect with v_{DS}. In addition, at the turn-off instant v_{DS} has different values in different modes as described by the following equalities

$$\begin{array}{ll} v_{DS} = V_B + V_o & \text{in Mode A (PFC inactive)} \\ v_{DS} = V_B + V_o + |v_{in}| & \text{in Mode B (PFC active)} \end{array} \tag{4}$$

Based on (4), scheme M3 has the highest V_B value among other schemes. As M4 operates in between M2 and M3, it is expected that turn-off loss is in the following descending order: M3 $>$ M4 $>$ M2. Note that when PFC cell is inactive, the converter also saves the power losses by the inductor, bridge-rectifier and input filter. Lastly, in terms of number of diodes that are in conduction at different modes, one can see that for Mode A only D_2 and D_3 are conducting while for Mode B all diodes (D_1 to D_3) are conducting. Based on the above voltage stress and loss analysis, it is clear that scheme M2 has highest conversion efficiency and M3 the lowest. For M1, although the switch capacitance loss appears to be the highest among other three schemes as the converter always operates for every line cycle, it has lower V_B than that of M3. In addition its turn-off switching loss is reduced as the duty cycle is comparatively smaller, leading to lower $i_{L1} + i_{CB}$ when turned-off. But from the trend of V_B it is expected that the higher V_B the converter operates, the lower efficiency it can achieve, particularly at light load condition.

V. Conclusion

This letter proposed and compared three different burst mode operations for buck-derived single-switch single-stage PFC (S^2PFC) converters under light load operation. The experimental results on a buck-derived S^2PFC converter example have confirmed that the power loss is reduced when the burst mode switching happens around the zero crossing of input voltage and when the dc bus voltage is lowered. Among the proposed schemes, the scheme allowing switching only around the zero crossing of input voltage achieves the highest efficiency as the PFC cell is effectively switched off due to the dead angle of input current and hence power loss is reduced. Compared to the operation without the burst mode switching arrangement, the zero-crossing switching scheme has the highest efficiency gain of 7% at 1W output. Not only this idea can be applied to other buck-derived S^2PFC converters such as full-bridge S^2PFC converter [13] but also to other PFC converters which have small dead angle of input current. An example is the S^2PFC converter with bus voltage feedback which has a coupled-inductor winding inserted in series with the boost inductor path [14], [15]. Note that this solution is suitable for single-stage PFC converters only. For conventional buck PFC rectifier, a two-stage approach will be used. To improve light load efficiency the buck PFC rectifier can simply turn off completely by opening the power switch. Since the single-stage PFC converters have more than one power processing stage, it is expected that its efficiency will be lower than a conventional buck PFC rectifier. An example is shown in [16] where a two-stage design (a buck PFC rectifier and a half-bridge dc/dc converter) has around 4% lower efficiency than that of a buck PFC rectifier alone.

References

[1] Y. Jang and M. M. Jovanovic, "Light-load efficiency optimization method," *IEEE Transactions on Power Electronics*, vol. 25, no. 1, pp. 67–74, Jan. 2010.

[2] H.-W. Seong, H.-S. Kim, K.-B. Park, G. W. Moon, and M.-J. Youn, "High step-up dc-dc converters using zero-voltage switching boost integration technique and light-load frequency modulation control," *IEEE Transactions on Power Electronics*, vol. 27, pp. 1383–1400, Mar. 2012.

[3] R. Yu, B. M. H. Pong, B. W.-K. Ling, and J. Lam, "Two-stage optimization method for efcient power converter design including light load operation," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1327–1337, Mar. 2012.

[4] L. Huber, L. Gang, and M. Jovanović, "Design-oriented analysis and performance evaluation of buck pfc front-end," in *Proceedings, IEEE Applied Power Electronics Conf. (APEC)*, Feb. 2008, pp. 1170–1176.

[5] M. D. Mulligan, B. Broach, and T. H. Lee, "A constant-frequency method for improving light-load efciency in synchronous buck converters," *IEEE Power Electronics Letters*, vol. 3, no. 1, pp. 24–29, Mar. 2005.

[6] Y.-K. Lo, S.-C. Yen, and C.-Y. Lin, "A high-efficiency ac-to-dc adaptor with a low standby power consumption," *IEEE Transactions on Industrial Electronics,*, vol. 55, no. 2, pp. 963 –965, Feb. 2008.

[7] D. D.-C. L. Lu, H. H.-C. Iu, and V. Pjevalica, "A single-stage ac/dc converter with high power factor, regulated bus voltage and output voltage," *IEEE Transactions on Power Electronics*, vol. 23, pp. 218–228, Jan. 2008.

[8] S.-K. Ki and D. D.-C. Lu, "A transformerless single-stage ac/dc converter with low output voltage," in *Proceedings, IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2011, pp. 3458 –3465.

[9] M. Jovanovic, D. Tsang, and F. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable-frequency control," in *Proceedings, Ninth Annual IEEE Applied Power Electronics Conference and Exposition, APEC '94*, vol. 2, Feb. 1994, pp. 569 –575.

[10] B.-C. Kim, K.-B. Park, and G.-W. Moon, "Sawtooth burst mode control with minimum peak current in stand-by operation of power supply," in *Proceedings, 8th IEEE International Conference on Power Electronics - ECCE Asia*, May-June 2011, pp. 474–479.

[11] R. Redl, L. Balogh, and N. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage," in *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, jun 1994, pp. 1137 –1144 vol.2.

[12] D. Murthy-Bellur and M. K. Kazimierczuk, "Two-switch flyback pwm dc-dc converter in continuous-conduction mode," *International Journal of Circuit Theory and Applications*, vol. 39, no. 11, pp. 1145–1160, 2011. [Online]. Available: http://dx.doi.org/10.1002/cta.690

[13] H. Ribeiro and B. Borges, "New optimized full-bridge single-stage ac/dc converters," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2397 –2409, june 2011.

[14] Q. Zhao, F. C. Lee, and F. sheng Tsai, "Voltage and current stress reduction in single-stage power factor correction ac/dc converters with bulk capacitor voltage feedback," *IEEE Transactions on Power Electronics*, vol. 17, no. 4, pp. 477–484, Jul. 2002.

[15] Y.-M. Liu and L.-K. Chang, "Single-stage soft-switching ac-;dc converter with input-current shaping for universal line applications," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 467 –479, feb. 2009.

[16] Y. Jang and M. M. Jovanović, "Bridgeless high-power-factor buck converter," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 602–611, Feb 2011.