ECE 230L - LAB 6

BASIC DIGITAL CIRCUITS

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1 Objectives of this Laboratory

The objectives of this laboratory session are as follows:

- Measure the static and switching characteristics of discrete (transistors, resistors, and capacitors) MOS inverter circuits,
- Determine experimentally the truth tables of CMOS integrated-circuit gates,
- Measure the static voltage-transfer characteristics of CMOS NOR and NAND gates, and
- Measure the switching characteristics of CMOS NOR and NAND gates

2 Discrete Diode Logic OR and AND Gates

Diodes can be used to significantly reduce circuit cost, complexity, and save precious board space. By implementing discrete-device logic instead of using OR and AND gates, whole integrated circuits (ICs) can be replaced in a circuit. In general, ICs with 50% or fewer gates being used stand to gain by being replaced by discrete components. Diode logic takes advantage of the diode properties to build useful circuits that can reduce component count and simplify circuits. A few simpler components can be inserted to perform the same function of large integrated circuits more cheaply and more directly. Often, it is more convenient to build a logic gate then use a pre-manufactured chip. When more than a few inputs are desired, building your own logic gates can be the only way to get the desired number. For instance, a 7-input OR gate is easily implemented just by adding more diodes to a basic 2-input gate. You may not always have the ICs that you need available, and ordering them and then waiting for the delivery takes time. You will always have resistors and diodes, and this is another reason for using logic gates made from discrete components.

2.1 Diode OR Gate

Consider the diode as a simple switch. It is closed (ON) when the voltage on the anode or p-side is higher than that on the cathode or n-side. Current flows in the direction of the arrow in the diode's schematic symbol. The logic symbol of an OR gate and its discrete diode implementation are shown in Figure 1. In an OR gate, the output is '1' if either of the inputs are '1'. In other words, if either of the inputs has a high voltage, its diode will conduct and current will flow to the output. A high voltage will appear across the resistor, equal to the input voltage minus a voltage drop across the silicon diode. If both of the inputs are '0', then neither of the diodes will conduct and the gate?s output voltage will be zero.

☐ Wire the diode OR gate using 1N4148 Si diodes on a breadboard and verify its truth table by applying 0 and 5 V (4 combinations) to the inputs A and B. Measure the value of the output voltage. Note the diode voltage drop and its effect on the output voltage.

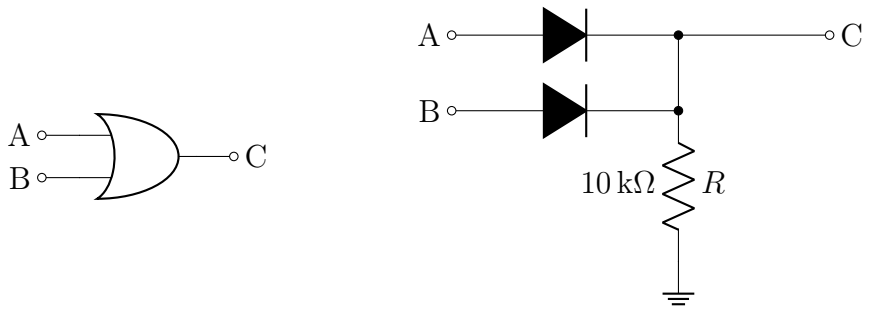

Figure 1: OR Gate Symbol and Discrete Diode Implementation

Note that '+' is used to represent the OR operation. Hence, in Figure 1 we have

$$C = A + B. \tag{1}$$

2.2 Diode AND Gate

Consider the diode AND gate shown in Figure 2. Its circuit is similar to the OR-gate circuit except that the diode connections (anodes and cathodes) are switched, and the resistor is connected to a power supply of 5.0 V, instead of ground. The output of an AND gate is '1' only if both inputs are '1'. In the diode implementation, if either input is '0', then the diode will conduct and the output voltage will be effectively shorted (through the diode) to ground. If both inputs are '1' , then neither of the diodes will be conducting and the output voltage will be 5.0 V (logical '1') because nearly all the voltage drops across the 10 MΩ resistor. This operation yields the desired result. Note that again, due to the voltage drop across a conducting silicon PN-junction diode, the actual 'low' output voltage is higher than the 'low' voltage of 0 V applied at the input of the gate.

☐ Wire the diode AND gate using 1N4148 Si diodes on a breadboard and verify its truth table by applying 0 and 5 V (4 combinations) to the inputs A and B. Measure the output voltage. Note the diode voltage drop and its effect on the output voltage.

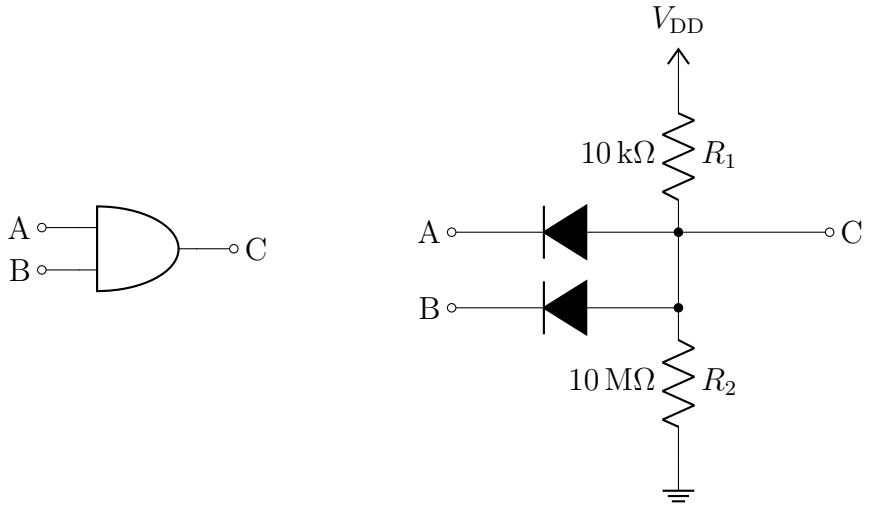

Figure 2: AND Gate Symbol and Discrete Diode Implementation

Note that '·' is used to represent the AND operation. Hence, in Figure 2 we have

$$C = A \cdot B. \tag{2}$$

3 Discrete MOS Inverter Circuit

An inverting function cannot be implemented with diodes and resistors alone. A transistor is needed to provide the inverting action. In this lab, you will use the BS170 N-type Metal Oxide Semiconductor Field Effect Transistor (NMOSFET). If the voltage present at the gate of the transistor is above 0.7 V (high), the transistor will conduct, reducing the output voltage to logical '0'. If the input voltage is logical '0' (low), then the transistor does not conduct, and zero voltage drops across the load resistor which results in the output voltage being '1'. A current-limiting resistor at the gate is always needed, otherwise excessive gate current might destroy the transistor. The circuit used in the electrical characterization of the MOS inverter with a resistive load is shown in Figure 3. Digital integrated circuits are circuits based on the principles of Boolean algebra. The binary logic variables in this algebra can assume only one of two possible values which are called the logical '0' and '1' levels. In the electronic circuit implementation of Boolean algebra, these variables correspond to the values designated by the voltages V_{OL} and V_{OH}.

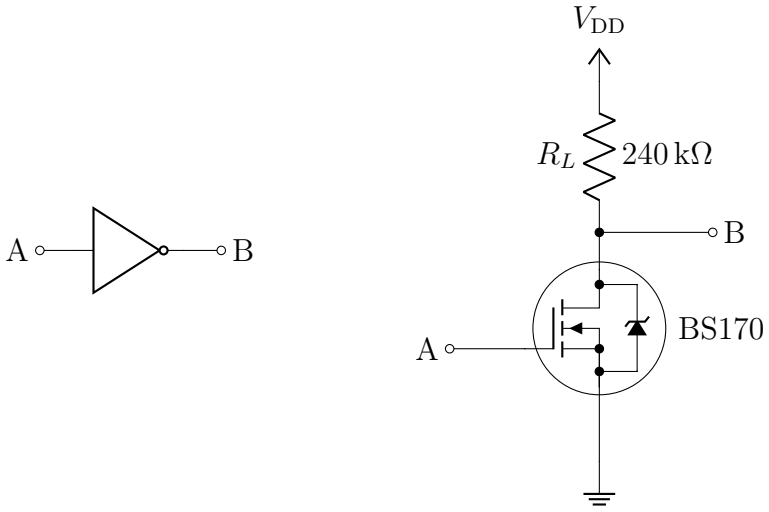

Figure 3: Inverter Gate Symbol and Discrete Diode Implementation

We usually denote negation with a bar above a character. Hence, in Figure 3 we have

$$B = \overline{A} \tag{3}$$

The static voltage and switching characteristics of an inverter can be characterized and serve as a measure of the inverter's overall performance. The voltages V_{OL} and V_{OH} are always between 0 and V_{DD}. The static voltage characteristics of an inverter is shown in Figure **??**. The switching characteristics of an inverter is shown in Figure **??**.

1. Wire the diode Inverter gate using a BS170 MOSFET on a breadboard and verify its truth table by applying 0 and 5 V (2 combinations) to the input A. Measure the value of the output voltage. Note the voltage drops across the inverter circuit and their effect on the output voltage.

2. Using LabVIEW, measure the static voltage-transfer characteristics (SVTC) VOUT(VIN) for this inverter implemented with the NMOSFET BS170, RL = 240 k?, and VDD = 5 V. Determine VOL and VOH.

3. Measure the static power-supply-current IDD (VIN) when VIN = VOL and when VIN = VOH (both for RL = 240k) (2 cases). Calculate the static power dissipation in this inverter for VIN = VOL and VIN = VOH. (2 cases) (Hint: P = IV.)

4. Measure the output-voltage waveform vOU T (t) for a square-wave input-voltage waveform with VPP = 5V and f = 1 kHz obtained from the function generator. Observe the input and output waveforms on the oscilloscope simultaneously. Determine the high-to-low transition time (tp.HL) and the low-to-high transition time (tp.LH). Turn up the input frequency of the square wave keeping the maximum input voltage equal to VPP = 5V. At what frequency does the output waveform begin to degrade? Be as quantitative as possible.

4 Exploration

In this exploration, you will use what you have learned about discrete logic circuits to complete the following:

1. Build a NAND gate from the combination of discrete AND gates using diodes and Inverter gates using NMOSFET transistors.
2. One very useful application of an Inverter gate is the Inverter Ring Oscillator shown in Figure 5. You will build a self-sustaining Ring Oscillator and measure its output square-wave frequency. (A similar circuit can be built using NAND gates chained together. You have all the knowledge you need to build this circuit, too. Hint: to build a Ring Oscillator with NAND gates, one of the two inputs needs be set to Ground. Most designers choose either the A or B input to be grounded for each NAND gate in the chain in this application.)
3. (Optional) Another very useful implementation of NAND gates is the Debounced Switch or SR Latch. A Debounce Switch prevents pushbutton switching events from triggering more than On/Off occurrence in a circuit. Deboucing inputs is critical in many logic circuit applications. A Debounce Swtich or SR Latch can be completely constructed using discrete NAND gate logic when wired as shown in Figure 6. This exercise is left as an optional activity.

4.1 Discrete NAND Gate

Using a combination of the AND and NOT gates built above, build a discrete NAND gate. Draw a circuit diagram of the circuit you designed and verify the NAND gate truth table.

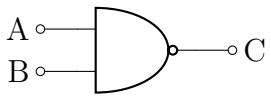

Figure 4: NAND Gate Symbol

4.2 Ring Oscillator

The propagation delay of a switching circuit is a measure of the maximum speed or minimum time for an input change to pass to the device?s output. Measurements in this mode are made by setting up an odd number of inverters or inverting gates in a ring, that is, with the output of one inverter connected to the input of the next inverter. In this mode, a logic steady-state cannot be reached. The results is a passing along of the logic mismatch?a form of oscillation. To measure the propagation delay of the discrete inverter built above, arrange an odd number of inverters (at least 3) in series. No input excitation at the first inverter is needed; the circuit should oscillate when the inverters are on (i.e. when VDD is applied to each discrete MOSFET inverter). The output of the Ring Oscillator should be a square wave of amplitude 0 to VDD.

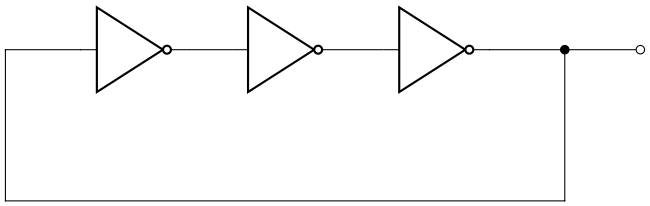

Figure 5: Ring Oscillator Using 3 Inverters

1. Build the Ring Oscillator in Figure 5 using an odd number of the discrete NMOSFET BS170 Inverters shown in Figure 3. Observe the output waveform. Notice that no input excitation at the first inverter is needed; the circuit should oscillate at a high frequency when the inverters are on (i.e. when VDD is applied to each discrete MOSFET inverter). Zoom out to view at least 4 periods of the ring oscillator output when determining its period of oscillation.
2. Measure the period of the ring oscillator output square wave. This period is the time required for the logic transition to propagate around all three devices.
3. The transition or propagation time for one gate in this ring oscillator is one-third of the observed period when 3 inverters are used. Determine the transition time of one of the inverters built by dividing the total transition time by 3. (More accurate transition times can be obtained by using additional odd numbers of inverters for this measurement.)

4.3 (Optional) Debounce Switch or SR Latch

In many applications, especially in digital circuits, you need a manual switch to set the logic state at some point in the circuit. The issue is that switch can often ?bounce? upon actuation. A bouncy switch is one that produces multiple switching operations in a single button press. This leads to a rapid series of alternating logic states for a few milliseconds while the switch contact is stabilizing. The bounce is due to inductive ringing rather than mechanical toggling. We use an SR latch to debounce the switch in hardware by latching the state of the switch as a digital signal. Once the ringing stops, we can safely assume that the signal has been latched successfully.

1. Place a double-pole single-throw switch on a breadboard.
2. Construct the circuit shown in Figure **??** and power it with +5 V.
3. Observe the switch output on an oscilloscope when the input switch is toggled "On." Capture an occurrence of the switch bouncing phenomenon on the oscilloscope screen and save it.

The issue of switch bounce can be corrected through the use of a pair of NAND gates.

1. Using the NAND gate you built above with discrete AND and Inverter gates, build the circuit shown in Figure **??**.
2. Verify its operation. Compare its output to that of the ordinary switch. Capture an occurrence of the switching phenomenon for this circuit on the ?scope screen and save it.

5 IC CMOS NOT, NOR, and NAND Gates

The discrete component logic gates built in this laboratory form the building blocks of all semiconductor logic circuits built and used in industry. Because logic functions are so common, specific Integrated Circuits (ICs) have been built to the highest tolerances to perform on/off functions which are used in electronic devices. There exist common equivalents to the OR, AND, and NOT gates built in this laboratory in individual commercially available IC packages. It is most common to find the NOT versions of the OR and AND functions as ICs (in fact, the OR and AND functions themselves are usually created using a NOT plus OR gate or a NOT plus AND gate in an IC package). The common equivalent devices available commercially are as follows:

- CD4069 CMOS Inverter
- CD4001 CMOS NOR gate
- CD4011 CMOS NAND gate

As you can imagine, because these ICs are specifically built for the purpose they serve, their static voltage-transfer characteristics, static noise margins, static power-supply-current characteristics, and static power consumption are much better than the discrete version equivalents. In addition, their transient switching characteristics (measured by observing their response to a square-wave input-voltage waveform) are much faster than the discrete equivalents. For this reason, and due to the low cost of such integrated circuit devices, they are usually used in application specific integrated circuit (ASIC) designs.

The latch is the most basic memory element in digital electronics, but it is seldom used by itself. Instead, digital designers generally prefer flip-flops (clocked latches) as primitive memory elements because they are less susceptible to glitches. Below is the schematic of an SR flip-flop, which is an SR latch with a gated clock input. The clock signal synchronizes any changes to occur only when the clock is high (An alternative is to use a D flip-flop, which is synchronized to a near-instantaneous clock edge.) The main point is that reducing the duration in which the memory element is transparent to changes reduces the likelihood of a glitch being incorrectly recorded into it.

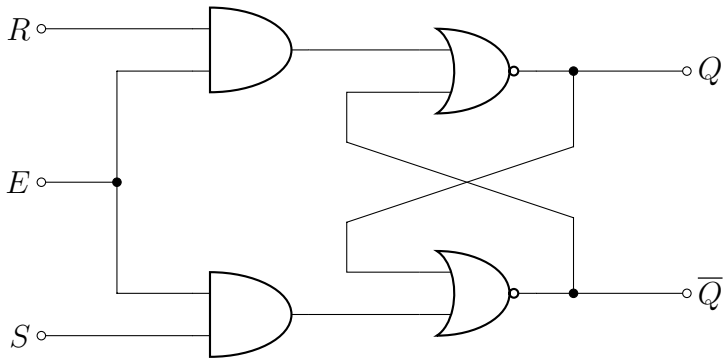

Figure 6: Gate-Level Diagram of a Clocked NAND-Gate SR Flip-flop

Table 1: ECE 230L Laboratory 3 Grading Rubric

Criteria	Points Possible
Diode OR Gate	**10**
Circuit Diagram	1
Truth Table Verified	3
Variable diode drop values given for different diodes	3
Justification of whether circuit is "better"	3
Diode AND Gate	**8**
Circuit Diagram	2
Truth Table Verified	3
Diode Drop Value Noted	3
Discrete MOS Inverter Circuit	**65**
Circuit Diagram	2
Truth Table Verified	3
Voltage Lost Across Circuit	3
V_{OL} from V-V `singleloop.vi` graph	5
V_{OH} from V-V `singleloop.vi` graph	5
$I_{\mathrm{DD}}(V_{\mathrm{in}} = V_{\mathrm{OL}})$	3
$I_{\mathrm{DD}}(V_{\mathrm{in}} = V_{\mathrm{OH}})$	3
$P(V_{\mathrm{in}} = V_{\mathrm{OL}})$	2
$P(V_{\mathrm{in}} = V_{\mathrm{OH}})$	2
Image of V_{out} when square wave is applied	3
Degraded image of V_{out} when square wave is applied	3
High-to-Low Transition Time ($t_{\mathrm{p\cdot HL}}$)	3
Low-to-high transition time ($t_{\mathrm{p\cdot LH}}$)	3
Degradation frequency with explanation	3
Discrete NAND gate circuit diagram	3
NAND Truth Table verified	4
Exploration: Discrete NAND Gate w/ Applications	**12**
NAND Gate Truth Table Verified	3
Ring Oscillator Circuit Diagram	3
Period of oscillator for N inverters	3
Period of oscillator for 1 inverter	3
Quality of thought/analysis	**5**
Total	**100**