ECE 230L - LAB 8

DEVICE NON-IDEALITIES

Contents

| 1 | Obj | ectives of this Laboratory | 2 |
|--------------|------------------------|--|----|
| 2 | Exp | perimental Exploration Format | 2 |
| 3 | $\mathbf{E}\mathbf{x}$ | perimental Explorations | 3 |
| | 3.1 | Thermal Effects on PN-Junction Diode & MOSFET | 3 |
| | 3.2 | MOSFET Amplifier Gain and Load Limits | 5 |
| | 3.3 | MOSFET Input and Output Resistance | 7 |
| | 3.4 | MOSFET Inverter Maximum Clock Frequency | 9 |
| | 3.5 | Zener Diode (Reverse breakdown) | 10 |
| | | | |
| \mathbf{L} | ist | of Figures | |
| | 1 | PN-Junction Diode Test Circuit | 3 |
| | 2 | Circuit Used to Characterize an NMOSFET | 4 |
| | 3 | Circuit Used to Characterize MOSFET Amplifier Gain and Load Limits | 5 |
| | 4 | Circuit Used to Characterize MOSFET Amplifier Gain and Load Limits | 6 |
| | 5 | Inverter Gate Symbol and Discrete Diode Implementation | 7 |
| | 6 | Discrete Diode Implementation Of Inverter Circuit | 9 |
| | 7 | Zener Diode Circuit | 10 |

1 Objectives of this Laboratory

The objectives of this laboratory session are as follows:

• To gain understanding of some of the less than ideal behavior of devices and circuits explored in previous laboratories.

- To explore methods for measuring these non-idealities in a less structured lab environment using the tools presented during the course of the semester.
- To work with a group in the course to explore these methods.
- To present group findings to fellow students in the course in a lab presentation.

2 Experimental Exploration Format

- This lab will be conducted in groups of two or three.
- Each group will be assigned an exploration
- Complete the exploration and form a brief presentation to share with the lab section you have one hour
- Each group will present their findings to the entire lab

3.1 Thermal Effects on PN-Junction Diode & MOSFET

Conducted in groups of 2 or 3 students each.

PN-Junction Diode

Purpose

The purpose of this experiment is to observe the effects on MOSFET characteristics due to thermal variations.

Procedure

1. Construct the circuit shown in Fig. 1 on a breadboard.

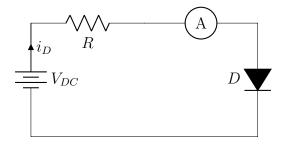


Figure 1: PN-Junction Diode Test Circuit

- 2. Run the singleloop.vi script from 0 to 6 V with 100 steps. This produces $I_D(V_D)$.
- 3. Repeat the above, but with a voltmeter over the diode, to measure V_{PN} . Combine the results to produce the graph $I_D(V_{PN})$.
- 4. Now, obtain thermal paste from your TA and apply it to the diode. Obtain a soldering iron and heat it to its lowest setting. Apply the soldering iron to the diode to allow it to heat it.
- 5. Repeat steps (2) and (3) and compare the results.

MOSFET

Purpose

The purpose of this experiment is to measure the gain of a MOSFET amplifier with varying resistive and capacitive loads.

Procedure

1. Construct the circuit shown in Fig. 2 on a breadboard.

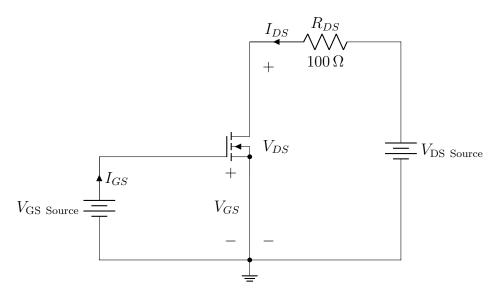


Figure 2: Circuit Used to Characterize an NMOSFET

- 2. Run the doubleloop.vi script with an inner voltage $V_{\rm DS~Source}$ from 0 to 6 V with 50 steps and outer voltage $V_{\rm GS~Source}$ from 2.0 to 3.0 V with 5 steps. This produces $I_D(V_{\rm DS~Source})$.
- 3. Obtain thermal paste from your TA and apply to the face of the NMOSFET. Heat the NMOSFET with a soldering iron on its lowest heat setting. Then, repeat step (2).
- 4. Analyze the results.

Present your findings for both the PN junction diode and the MOSFET under temperature to the class.

3.2 MOSFET Amplifier Gain and Load Limits

Conducted in groups of 2 or 3 students each.

Procedure

1. Construct the circuit shown in Fig. 3 on a breadboard.

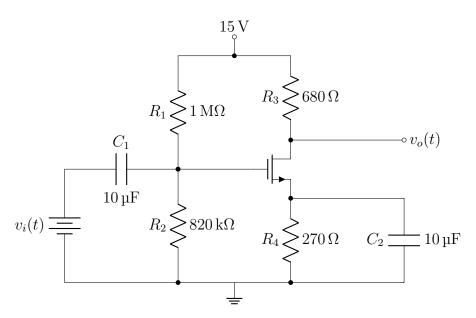


Figure 3: Circuit Used to Characterize MOSFET Amplifier Gain and Load Limits

- 2. Set $v_i(t)$ to be a 100 mV_{pp}, 50 kHz sinusoid.
- 3. Carefully measure and record $v_o(t)$ (both AC and DC components).
- 4. Based on this measurement only, determine the AC voltage gain of this amplifier.
- 5. Now attach a load as shown in Fig. 4 to the amplifier output. C_L should be $1 \mu \text{F}$ and and R_L should be 100Ω . Carefully measure and record the total output voltage $v_o(t)$. Carefully measure and record the total output voltage $v_o(t)$.
- 6. Based on this measurement only, determine the voltage gain Vout/Vin with this output load applied.
- 7. Now increase the magnitude of input Vin until Vout is severely distorted (i.e. both the top and bottom of the sinewave are clipped). Carefully measure and record the output Vout (both AC and DC components).
- 8. Repeat iv-vii for C_L and R_L equals $10\,\mu\text{F}$ and $680\,\Omega$, and for C_L and R_L equals $47\,\mu\text{F}$ and $10\,\mathrm{k}\Omega$, respectively.

At what voltage values did the output signal clip, and why?

Comment on the effect of a capacitive load on this circuit.

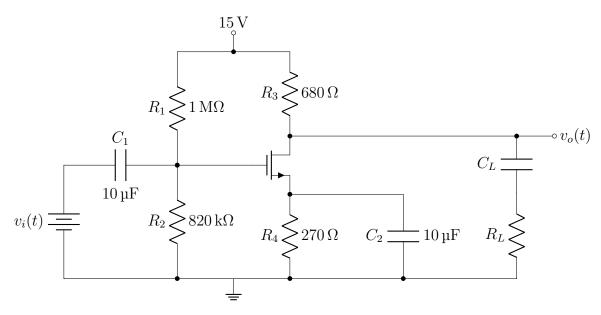


Figure 4: Circuit Used to Characterize MOSFET Amplifier Gain and Load Limits

Comment on the effect of increasing the magnitude of the input voltage on the circuit.

Comment on the effect of increasing the capacitive load values.

Present your findings to the class.

3.3 MOSFET Input and Output Resistance

Conducted in groups of 2 students each.

Purpose

To measure the input and output resistances of a discrete MOSFET inverter device.

Procedure

The Inverter circuit show in Fig. 5 from the Discrete Digital Circuits laboratory is often referred to as a Buffer circuit. One of the benefits of using a MOSFET between stages of a system is that the MOSFET has a very high input resistance and a very low output resistance. A high input resistance means that not much current enters into the device; a low output resistance means that the device does not affect the loading of the system it is attached to. A MOSFET Buffer, as in Lab 6, has both of these advantages. Hence, in a system, it can "buffer" the stages from one other so that the stages acts more or less independently of one another.

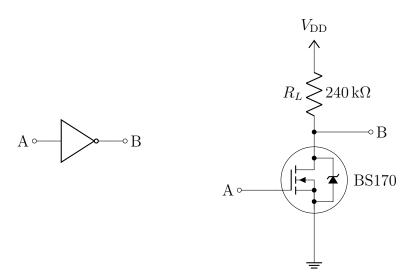


Figure 5: Inverter Gate Symbol and Discrete Diode Implementation

- 1. For the MOSFET Inverter shown in Fig. 5, devise a way to determine the input resistance and the output resistance of the circuit (note that the input and output resistances can be modeled as the Thévenin equivalent resistances at the input and output terminals, respectively).
- 2. Conduct your experiment by measuring input and output voltages and currents, respectively. (Hint: Apply Ohm's Law to determine resistance from current and voltage measurements.)

What is the input resistance of the MOSFET buffer?

What is the output resistance?

3. Now, explore what might change the input and output resistance values the most in this MOSFET Inverter circuit. What you explore as a group is up to you. As suggestions, the source resistor value might be changed, or the voltage supplied to the Inverter circuit could be changed, perhaps what effect adding a load resistor from source to ground has on the input and output.

4. Repeat steps (1) - (3) in PSpice.

Present your findings to the class.

3.4 MOSFET Inverter Maximum Clock Frequency

Conducted in groups of 2 or 3 students each.

Purpose

The purpose of this experiment is to determine the effect of capacitance at the output on the maximum achievable inverter clock frequency.

Procedure

1. Build the inverter circuit shown in Fig. 6 from the Discrete Digital Circuits laboratory.

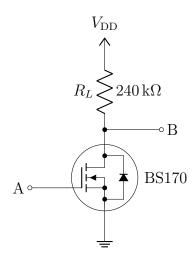


Figure 6: Discrete Diode Implementation Of Inverter Circuit

- 2. Input a slow $100\,\mathrm{Hz}$, $2\,\mathrm{V_{pp}}$ square wave at the gate of the MOSFET and observe the output. It should look square and should be inverted from the input waveform.
- 3. Increase the input square wave frequency until the output waveform is degraded. (Justify how you define a degraded square wave output. Consider whether a digital switching circuit could use the output waveform as a reliable input source.)
- 4. Add a small capacitance (10 nF) to the inverter output from the drain to the ground and repeat step (2).
- 5. Now, continue to replace capacitors at the output and repeat step (2), above. Repeat with $0.1\,\mu\text{F}$, $1\,\mu\text{F}$, $10\,\mu\text{F}$, and $47\,\mu\text{F}$.
- 6. Plot the frequency of the input waveform where the output was considered to be degraded (this is the maximum output frequency f_{max}) vs. capacitance.

What can you conclude from your plot?

How does maximum clock frequency relate to load capacitance? Why might this be important in applications?

Present your results to the class.

3.5 Zener Diode (Reverse breakdown)

Conducted in groups of 2 or 3 students each.

Purpose

The purpose of this experiment is to showcase the use of Reverse breakdown in a practical circuits and to show a circuit using the Zener diode to demonstrate voltage clamping.

Procedure

One of the parameters that was not measured in Lab 2 was the reverse breakdown voltage of a diode. This is because most diodes have very large reverse bias breakdown voltages, on the order of 100's of Volts. However, some diodes are specifically manufactured to be used in the reverse bias breakdown region. These diodes are called Zener diodes.

Warning: Diodes can get hot when supplying a forward bias to them.

1. Simulate the following circuit in PSpice using a $5.5\,\mathrm{V}$ Zener diode found in the standard PSpice parts library, a $6\,\mathrm{V}$ DC source, and a $100\,\Omega$ resistor.

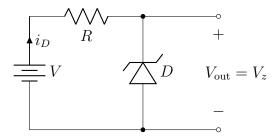


Figure 7: Zener Diode Circuit

- 2. Verify in simulation that the output voltage, V_{out} is 5.5 V. Where is the remaining 0.5 V voltage drop going?
- 3. Verify the current, i_D , through the resistor. Is this value what you expect? Why?
- 4. Build the circuit in Figure 7 on a breadboard. There are Zener diodes in the parts bin.
- 5. Attach the 6 V output source to the circuit. Supply 0 V and measure V_{out} .
- 6. Now, increase the DC voltage up to 6 V.
- 7. Measure the output voltage again.
- 8. Repeat steps (2) (4), but measure current.

 What can you conclude about the Zener diode? How might this be of practical use in an application?
- 9. Now, using the singleloop.vi script, create a plot of the Zener diode V-I curve. Be sure to take both forward biased and negative biased measurements of the Zener diode to show turn-on voltage, V-I characteristics, and reverse breakdown.

What differences do you notice about the Zener diode as compared to the PN junction diode observed in Lab 2?

Present your findings to the class.