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CURSO: ESPECIALIZAÇÃO EM MICROELETRÔNICA
PERÍODO: 1

Resultado da tarefa prática em sala de aula

Polo: Campina Grande -PB -UFCG
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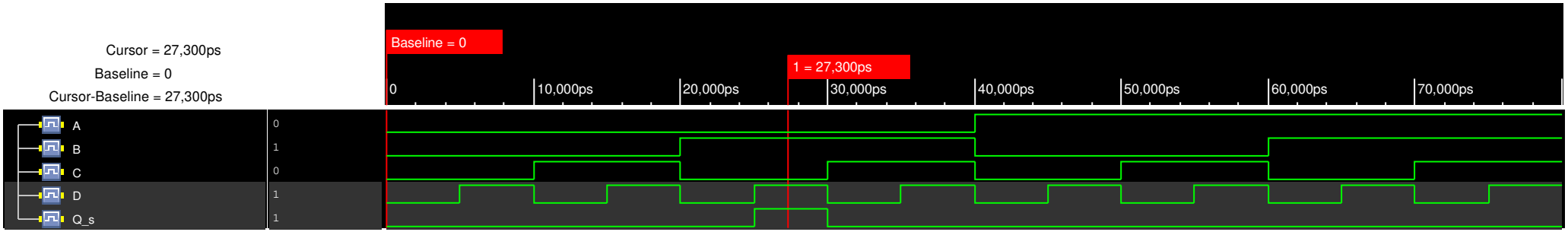
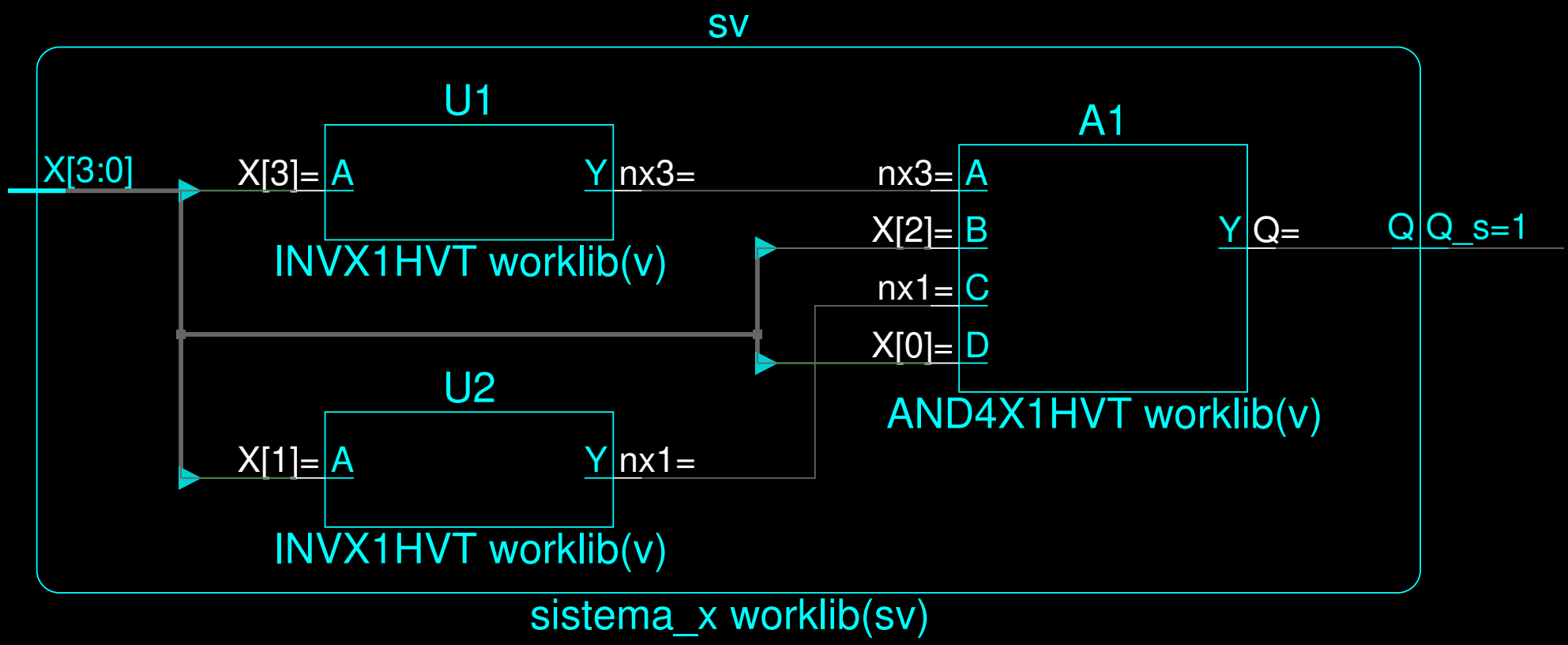
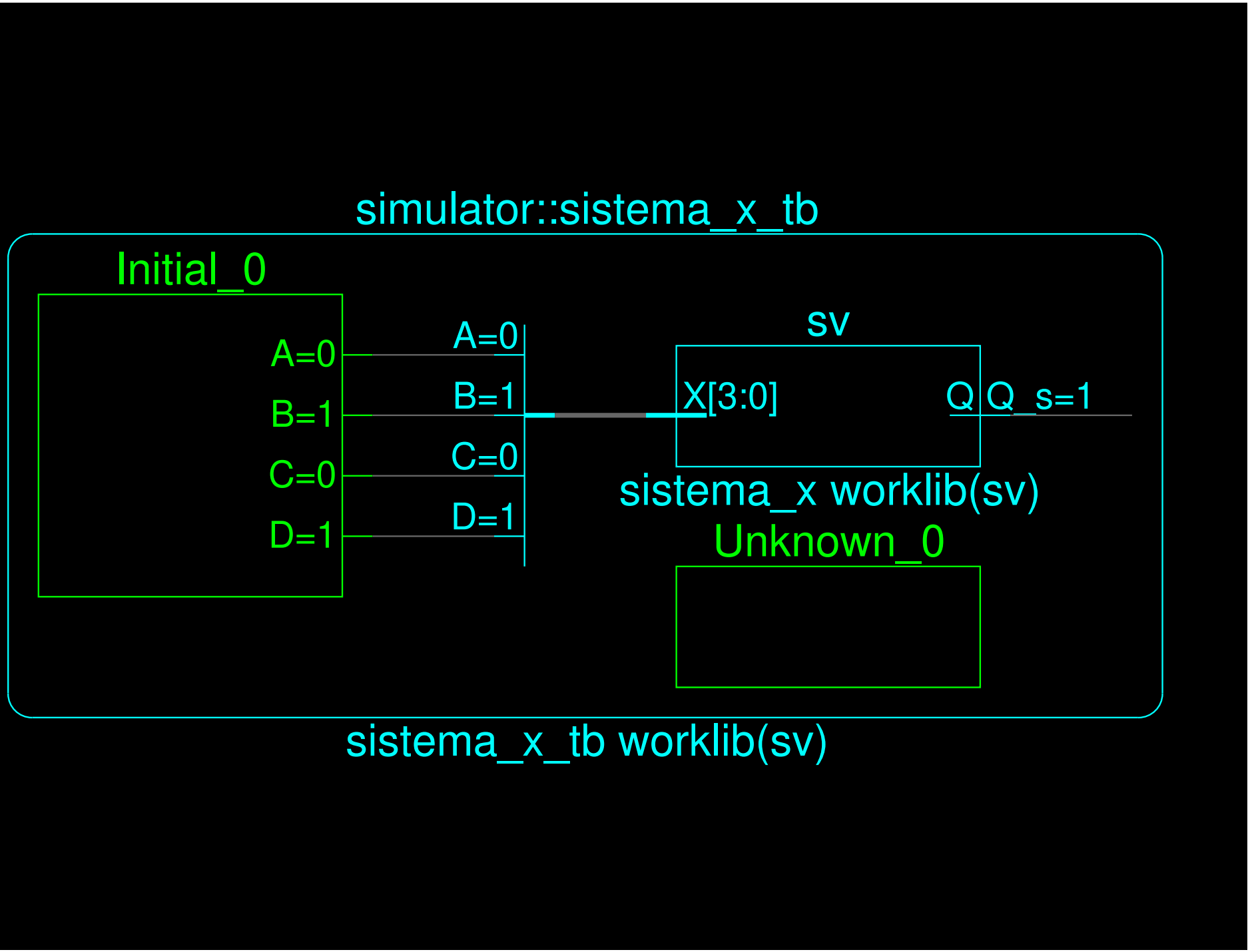
```
//Tarefa prática 2 lógica digital

`timescale 1ns/10ps
`celldefine

module sistema_x(

            input [3:0] X,
            output Q
);
            wire nx3, nx2, nx1, nx0;

            INVX1HVT U1 (nx3, X[3]);
            INVX1HVT U2 (nx1, X[1]);
            AND4X1HVT A1 (Q, nx3, X[2], nx1, X[0]);


endmodule
```

```
`timescale 1ns/10ps

module sistema_x_tb();

            reg A, B, C, D;
            wire Q_s;


initial
begin
            for(int i=0; i < 16; i++ ) begin
                        {A, B, C,D} = i;
                        #5;
            end
        $finish;
end

            sistema_x sv(.X({A,B,C,D}), .Q(Q_s));

initial
begin
            $display("                          Tempo  A B C D   Q");
        $display("                          ===== =========  ==");
            $monitor($time,"                    %b %b %b %b   %b", A,B,C,D, Q_s);

end

endmodule
```

Waveform 3 - SimVision




sv
U1
X[3:0]
X[3]=
A
Y
nx3=
INVX1HVT worklib(v)
A1
nx3=
A
X[2]=
B
nx1=
C
X[0]=
D
Y
Q=
Q
Q_s=1
AND4X1HVT worklib(v)
U2
X[1]=
A
Y
nx1=
INVX1HVT worklib(v)
sistema_x worklib(sv)


simulator::sistema_x_tb
Initial_0
A=0
B=1
C=0
D=1
A=0
B=1
C=0
D=1
sv
X[3:0]
Q
Q_s=1
sistema_x worklib(sv)
Unknown_0
sistema_x_tb worklib(sv)