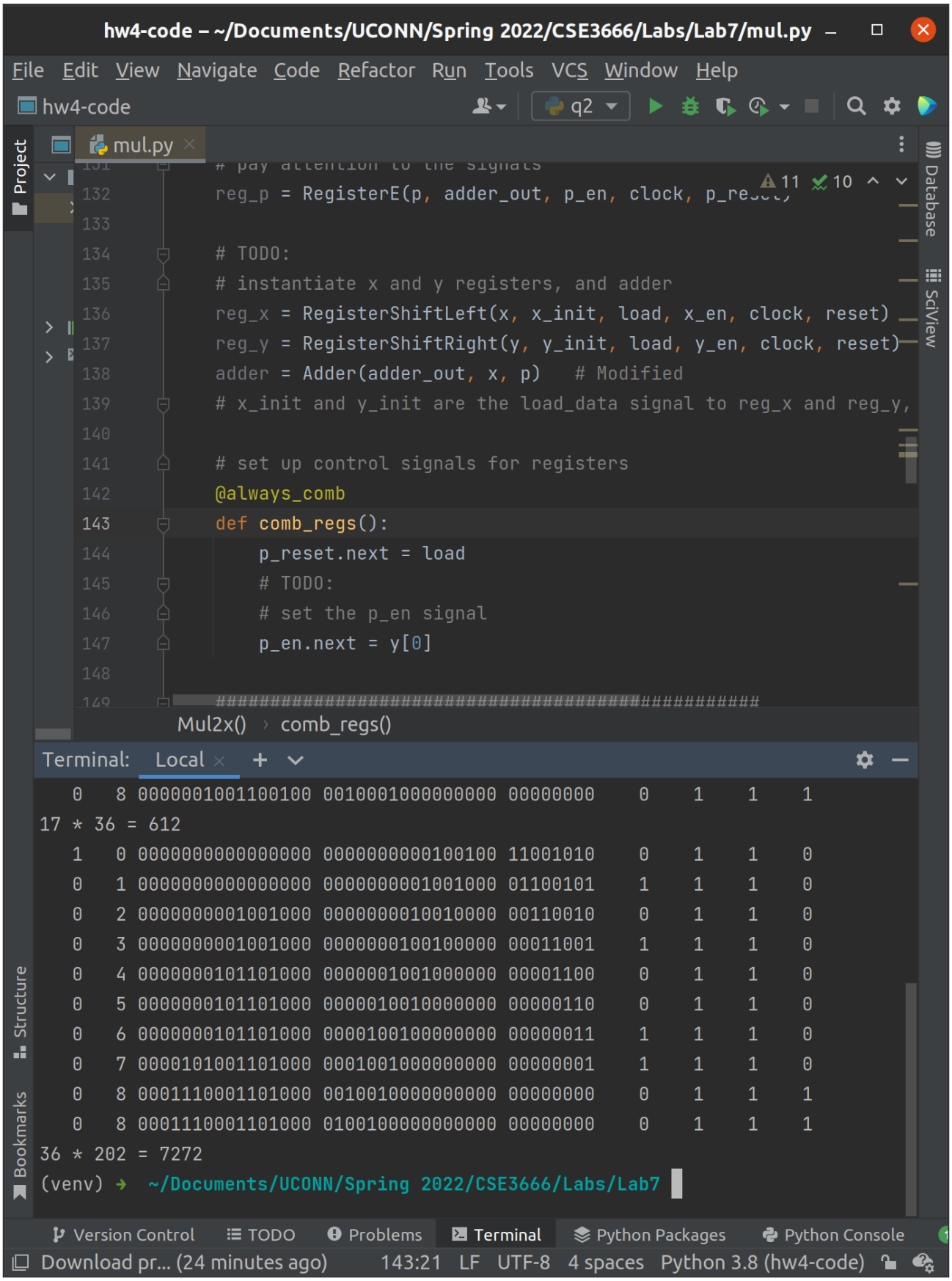
# Lab 7

## Work for Each Step

- Instantiate registers holding the multiplicant and multiplier with shift left and shift right
- Instantiate the adder
- set the next p_enabled signal to be the first item in the list stored in y

## Testing/Screenshots


hw4-code – ~/Documents/UCONN/Spring 2022/CSE3666/Labs/Lab7/mul.py
File Edit View Navigate Code Refactor Run Tools VCS Window Help
hw4-code
q2
mul.py
reg_p = RegisterE(p, adder_out, p_en, clock, p_reset)
# TODO:
# instantiate x and y registers, and adder
reg_x = RegisterShiftLeft(x, x_init, load, x_en, clock, reset)
reg_y = RegisterShiftRight(y, y_init, load, y_en, clock, reset)
adder = Adder(adder_out, x, p)  # Modified
# x_init and y_init are the load_data signal to reg_x and reg_y,
# set up control signals for registers
@always_comb
def comb_regs():
p_reset.next = load
# TODO:
# set the p_en signal
p_en.next = y[0]
Mul2x() › comb_regs()
Terminal: Local
0 8 0000001001100100 0010001000000000 00000000 0 1 1 1
17 * 36 = 612
1 0 0000000000000000 0000000000100100 11001010 0 1 1 0
0 1 0000000000000000 0000000001001000 01100101 1 1 1 0
0 2 0000000001001000 0000000010010000 00110010 0 1 1 0
0 3 0000000001001000 0000000100100000 00011001 1 1 1 0
0 4 0000000101101000 0000001001000000 00001100 0 1 1 0
0 5 0000000101101000 0000010010000000 00000110 0 1 1 0
0 6 0000000101101000 0000100100000000 00000011 1 1 1 0
0 7 0000101001101000 0001001000000000 00000001 1 1 1 0
0 8 0001110001101000 0010010000000000 00000000 0 1 1 1
0 8 0001110001101000 0100100000000000 00000000 0 1 1 1
36 * 202 = 7272
(venv) ➜ ~/Documents/UCONN/Spring 2022/CSE3666/Labs/Lab7
Version Control TODO Problems Terminal Python Packages Python Console
Download pr... (24 minutes ago) 143:21 LF UTF-8 4 spaces Python 3.8 (hw4-code)
Project Database SciView Structure Bookmarks

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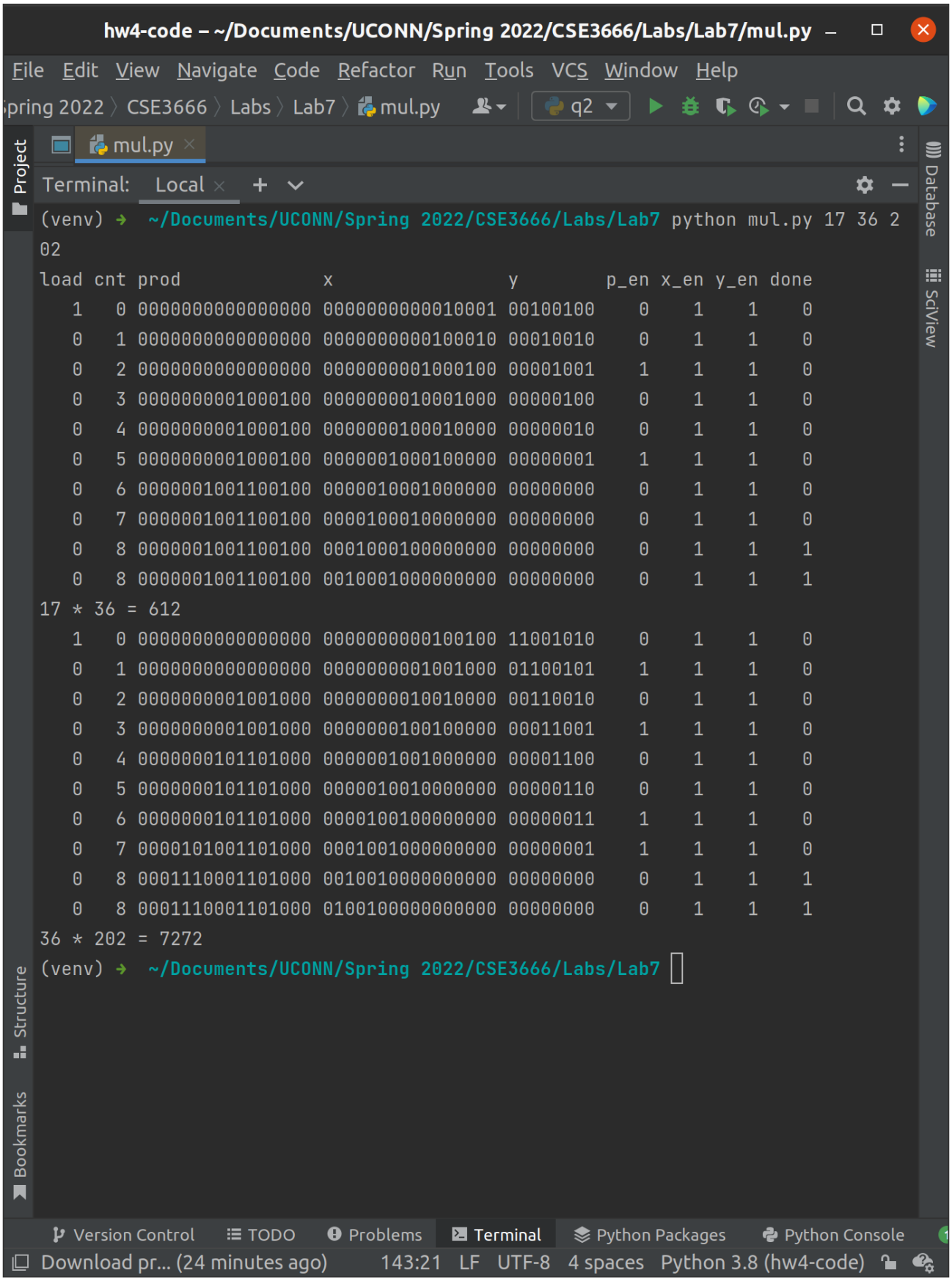
hw4-code – ~/Documents/UCONN/Spring 2022/CSE3666/Labs/Lab7/mul.py
File Edit View Navigate Code Refactor Run Tools VCS Window Help
Spring 2022 〉 CSE3666 〉 Labs 〉 Lab7 〉 mul.py
q2
Project
mul.py
Terminal: Local
(venv) ➜ ~/Documents/UCONN/Spring 2022/CSE3666/Labs/Lab7 python mul.py 17 36 202
load cnt prod x y p_en x_en y_en done
1 0 0000000000000000 0000000000010001 00100100 0 1 1 0
0 1 0000000000000000 0000000000100010 00010010 0 1 1 0
0 2 0000000000000000 0000000001000100 00001001 1 1 1 0
0 3 0000000001000100 0000000010001000 00000100 0 1 1 0
0 4 0000000001000100 0000000100010000 00000010 0 1 1 0
0 5 0000000001000100 0000001000100000 00000001 1 1 1 0
0 6 0000001001100100 0000010001000000 00000000 0 1 1 0
0 7 0000001001100100 0000100010000000 00000000 0 1 1 0
0 8 0000001001100100 0001000100000000 00000000 0 1 1 1
0 8 0000001001100100 0010001000000000 00000000 0 1 1 1
17 * 36 = 612
1 0 0000000000000000 0000000000100100 11001010 0 1 1 0
0 1 0000000000000000 0000000001001000 01100101 1 1 1 0
0 2 0000000001001000 0000000010010000 00110010 0 1 1 0
0 3 0000000001001000 0000000100100000 00011001 1 1 1 0
0 4 0000000101101000 0000001001000000 00001100 0 1 1 0
0 5 0000000101101000 0000010010000000 00000110 0 1 1 0
0 6 0000000101101000 0000100100000000 00000011 1 1 1 0
0 7 0000101001101000 0001001000000000 00000001 1 1 1 0
0 8 0001110001101000 0010010000000000 00000000 0 1 1 1
0 8 0001110001101000 0100100000000000 00000000 0 1 1 1
36 * 202 = 7272
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