CSE3666

Homework 6 (100 points)

Due Date: By the end of Friday, 4/8/2022.

Check answers to Problem 1 and Problem 2c. in HW6-Test.

Submit your answers to Problem 2a and 2b in a PDF file on HuskyCT. The diagrams must be clean. It is highly recommended to draw the diagrams in software.

Figure 4.21 can be downloaded in HuskyCT. Note that **the figure is copyrighted**. We use it in this course for educational purposes. Do not distribute it further.

1. Assume the single-cycle RISC-V processor, as shown in Figure 4.21. Find the following signal values when the processor executes the instruction 0xFE542023 located at 0x00400200.

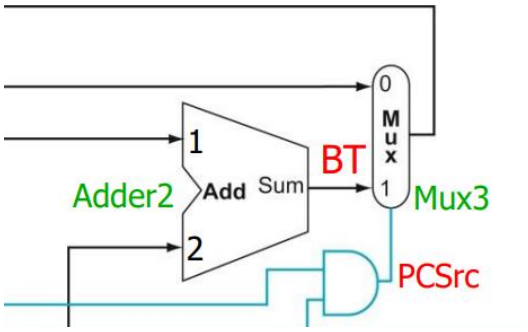
   All signals generated by the main control
   rs1
   rs2
   rd
   Immediate
   ALU operation
   BranchTarget
   PCSrc
   NextPC

2. In this problem, we improve the processor in Figure 4.21 to support JAL and JALR instructions. Assume the following two components have already been revised.

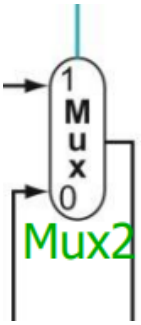
   - The main control. It has two additional outputs J and JR. J is 1 if and only if the instruction is either JAL or JALR. JR is 1 if and only if the instruction is JALR. The two signals can be generated from the opcode.
   - ImmGen. ImmGen can generate correct immediate for all types of instructions.

   Tasks:

   a) We first change part of diagram shown in the following figure. The goal is to set the correct next PC value at the output of Mux3. We will need a new Mux. We call it Mux4. The output of Mux4 is PCRef (the reference PC). In addition, we need to change how the select signal of Mux3 is generated. Let us call the new select signal PCSrcJ. **Include the following in your submission. Your diagram must be clean.**
      - Write the logic expression that generates PCSrcJ from signals from the (main) control and ALU.
      - Draw a new diagram that includes Mux4 and new logic that generates PCSrcJ. Label every signal in your diagram. The figure below has only two signals labeled (BT and PCSrc).



b) We then change part of diagram shown in the following figure. The goal is to set the correct value on Write Data. We will need to add a Mux. Let us call it Mux 5. The output of Mux5, ExResult, is connected to input 0 of Mux2. Mux5 is controlled by an existing signal (i.e., there is no need to add logic to generate the select signal of Mux5). **Draw a new diagram that includes Mux5. Label every signal in your diagram. Your diagram must be clean.**



c) Specify the value of control signals for JAL and JALR. Enter your signal values in HW6-Test. Concatenate the values in a row to form one string, for example, `0000x111`.

Inst.	ALU Src	Memto Reg	Reg Write	Mem Read	Mem Write	Branch	J	JR
JAL								
JALR								

Extra

Explain how JAL and JALR instructions are executed. How is the target address calculated for each instruction? How is PC4 saved? You do not need to submit your explanations.