CSE3666

# Homework 7

**Due Date:** By the end of Friday, 4/22/2022. Submit your answers in HW7-test.

There is no need to submit any files in HuskyCT. However, please compare your steps with the solutions later. Pay attention to details.

**Total Points:** 140

An Excel file is provided for writing pipeline diagram. The Excel file has multiple sheets, one for each pipeline diagram question. Pay attention to the sheet names.

We study two processors in this homework assignment.

**Processor A** is a RISC-V processor with a 5-stage pipeline that does **NOT** have any forwarding paths. The branch is resolved in the MEM stage and the correct instruction is fetched in the WB stage of the branch instruction. The pipeline stalls until the branch is resolved. The instruction following the branch is flushed. It is fetched again if the branch is not taken.

**Processor B** is a RISC-V processor with a 5-stage pipeline that has all necessary forwarding paths. The branch is resolved in the MEM stage and the correct instruction is fetched in the WB stage of the branch instruction. The implementation also uses a static branch predictor that always predicts not taken.

## 1 Hazards on Processor A.

Assume we use processor A. Complete the pipeline diagram for the instruction sequences in the spreadsheet.

## 2 Hazards on Processor B.

Assume we use processor B. Complete the pipeline diagram for the instruction sequences in the spreadsheet. In addition, show the forwarding path (`EX/MEM->EX`, `MEM/WB->EX`, `MEM/WB->MEM`, or `EX/MEM->ID`), if any, used to obtain registers rs1 and rs2 in an instruction. Leave the cell blank if the register value is not forwarded.

## 3 Loop on Processor A.

Assume we use processor A.

The following code adds integers in two arrays (whose address is in s0 and s1, respectively) and stores the results back into the first array. s2 is initialized to 0. s3 is a large number.

```
I1:        lw         t0, 0(s0)
I2:        lw         t1, 0(s1)
I3:        add        t0, t0, t1
I4:        sw         t0, 0(s0)
I5:        addi       s0, s0, 4
I6:        addi       s1, s1, 4
I7:        addi       s2, s2, 1
I8:        bne        s2, s3, I1
I9:
```

a. Write the pipeline diagram of running the loop, from the IF stage of I1 to the IF stage of I1 in the next iteration.
b. What is the number of cycles required for each iteration? This number is the difference of cycle times where the same instruction is fetched. For example, if the first instruction in a loop is fetched in cycle 1 and fetched again in cycle 11 in the following iteration, each iteration takes 10 cycles. How many stall cycles are due to data hazards and how many are due to control hazards?
c. Scheduling instructions can remove some hazards that cannot be handled by hardware. Schedule the instructions to minimize pipeline stalls. Do not change any instructions. What is the number of cycles required for each iteration in the scheduled code?
d. What is the speedup achieved on the loop by scheduling the instructions?

## 4 Loop on Processor B.

We study the loop in Problem 3 on processor B.
Repeat all the questions in Problem 3.

## 5 Performance.

We study the performance of an application on processors B. Suppose the instructions executed in the application break down into the following categories.

| Type | Percentage |
|---|---|
| Arithmetic and Logic | 30% |
| Load | 30% |
| Store | 15% |
| Branch | 25% |

The ideal CPI is 1. However, the actual CPI is higher because of hazards. 10% of the load instructions cause 1 cycle stall because of the load-use hazards. 60% of the executed branches are taken.

a. What is the CPI overhead from data hazards?
b. What is the CPI overhead from control hazards?
c. What is the average CPI of this application on Processor B?

## 6 Performance.

We study the performance of an operation Processor B. The two instructions below perform the **operation**: increment register x11 by 1 if and only if x10 is non-zero (not necessarily 1).

```
        beq   x10, x0, skip
        addi  x11, x11, 1
skip:
```

a. How many cycles does the operation take if x10 is 0?
b. How many cycles does the operation take if x10 is not 0?
c. If x10 is 0 80% of the times when the operation is performed, how many cycles does the operation take on average?