CSE 3666 Exam II Topics

Arithmetic for Computers

- operations on integers
  - addition and subtraction;
  - multiplication and division; multiplication/division algorithm and hardware;
  - RISC-V Multiplication Instructions (Not appear in essay Question)
- floating-point and real numbers
  - Binary to decimal; Decimal to binary
  - Normalized numbers. $1.xx \times 2^e$
  - Encode Floating Point Numbers with Bits
  - IEEE Std 754-1985: Single precision; double precision (one essay)
  - Denormal Numbers; meaning. (Not essay)
  - FP Support in RISC-V (Not essay)

Introduction to Digital Design

- use Boolean algebra to describe circuits
  - Boolean operations: AND, OR, NAND, NOR, XOR, NOT
  - use of truth tables to describe functionality
  - Boolean algebra
  - deriving Boolean expressions from truth tables
- two types of circuits:
  - combinational
  - sequential
- decoder
  - N inputs, 2^N outputs
  - one and only one output specified by input is asserted
- multiplexor
  - Selector: output is one of the inputs, selected by a control.
- 1-bit ALU
  - use Nx1 mux to select desired operation
  - operations:
    - add, sub, AND, OR, NOR, etc. with individual gates
    - addition with full adder
    - subtraction with full adder and two's complement trick
- 32-bit ALU

logic expression
truth Table
Hardware Diagram

Not essay (set)

Sequential Circuits

- Clock cycle, clock rate
- Bistable element, Memory Elements, Flip-Flops and Latches
- Triggering: falling edge and rising edge
- Registers: clock, input, output, control
  - Shift Register
- Register Files

Performance

- CPU Execution Time and Throughput; Relative Performance
- ~~CPU Time= CPU Clock Cycles* Clock Cycle Time= CPU Clock Cycles/Clock rate~~
- CPU Time= Instruction Count *CPI Clock* Cycle Time
  - Instruction Count and CPI
  - average CPI
- How to improve the performance of a computer/CPU? Amdahl's Law

Datapath Design

- general concepts
  - tasks of ``executing an instruction'' into stages
  - create the entire datapath for R/I type instruction.
- typical stages
  - instruction fetch (IF) - all
  - instruction decode (ID) / register fetch - all
  - execution (EX/EXE) - varies based on different instruction
  - memory access (MEM) - load and store only
  - register write (WB) - ALU and load only
- standard components
  - register file
  - PC
  - ``add 4'' unit, i.e., PC+4
  - sign-extention
  - instruction memory
  - data memory
  - ALU and its functions; ALU Control
  - multiplexors
- implementation choices
  - single-cycle: perform all tasks in a single clock cycle
  - multi-cycle/pipeline: use a clock cycle for each stage

Control Implementation

- single cycle control unit
  - used for directing operations of datapath blocks
  - generated based on opcode, function code (e.g., func 3 and func 7)
  - figure out what control signals need to be activated for different R/I/S-type instructions.

Pipelining

- basic concepts
- simple 5-stage pipeline
- pipeline registers
- pipeline control units

Essay Questions

Pipelining Hazard

- Structural hazard
  - Add more resources (IM, DM)
  - Share Resource (Reg)

Essay Questions