CS 2420 Lab 2 Solution

This lab does not need require the measuring probes.
Be sure to remind your students NOT to give the chips more than 5V. You can easily fry the entire chip or an individual gate within them. When using the chips the nitch at the top of the diagram represents the top of the chip so you can know the orientation of the pin layout. Every chip has one of these and the students need to make sure the chip is facing the right direction before using it.

T1:

This part requires the use of the digital writer (DigOut) and the digital reader (DigIn). The digital writer is like an on off switch for a constant +5v supply. The digital reader is simply an LED but on the computer. However, the digital reader and digital writer cannot be set to read/write over the same group of channels. For example, write to channels 0-7 and read from channels 8-15. If you try to read and write from channels 0-7 you will get an error when trying to run both the DigOut and DigIn. Which is another thing, you have to run both programs in order for this to work. Just in case people get confused, when the light is on that means the read channel is hi. The truth table should like the one below because it is a direct relationship from the write channels to the read channels.

Input		Output (lo/hi)	
Manual DIO 1	Manual DIO 0	DIO 9	DIO 8
Lo	Lo	Lo	Lo
Lo	Hi	Lo	Hi
Hi	Lo	Hi	Lo
Hi	Hi	Hi	Hi

T2:

The 7432 chip is a quad 2-input (4 gates each with 2 inputs) OR gate chip. The students don't know that yet. So basically a wire will be run from DIO 0 to pin 1, DIO 1 to pin 2 and then pin 2 to DIO 8 to be measured. These are, again, in addition to the wires that were already run for the power and ground pins for each chip. The OR gate truth tables are below. There are two truth tables to show the usual 0's and 1's from the hi/lo's from the digital reader/writer.

Manual DIO 1	Manual DIO 0	DIO 8 $_{(lo/hi)}$
lo	lo	lo
lo	hi	hi
hi	lo	hi
hi	hi	hi

X	Y	Out$_{(0/1)}$
0	0	0
0	1	1
1	0	1
1	1	1

T3:
The 7408 chip is a quad 2-input AND gate chip. The setup is the same as T2. Truth tables below.

Manual DIO 1	Manual DIO 0	DIO 8 (lo/hi)
lo	lo	lo
lo	hi	lo
hi	lo	lo
hi	hi	hi

X	Y	Out(0/1)
0	0	0
0	1	0
1	0	0
1	1	1

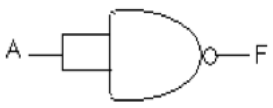
T4:
The 7400 chip is a quad 2-input NAND gate chip. Setup is the same as T2. Truth tables below.

Manual DIO 1	Manual DIO 0	DIO 8 (lo/hi)
lo	lo	hi
lo	hi	hi
hi	lo	hi
hi	hi	lo

X	Y	Out(0/1)
0	0	1
0	1	1
1	0	1
1	1	0

T5:
This section requires the use of some Boolean algebra. DeMorgan's law more specifically. *A'' = A, (x+y)' = x'y', (x+y)'' = (x'y')' = x+y.* Double negation is like saying 5=5+1-1. It doesn't change anything. With that said, if you take the original equation xy' + z and double negate it you get (xy' + z)''. After distributing only one of the two negations you get ((xy')' z')' Breaking it down we have (xy')' which is xy' NANDed together. Then we have (xy')'z')' which is (xy')' NANDed with z'. In order to get an inverted signal, since they are not allowed an inverter chip, is by sending the same signal into both inputs of a NAND gate. See blow. This equation will need all the gates in the 7400 chips. Two gates to invert the y and z signals, and the other two for the (xy')' and the ((xy')'z')' parts. Truth table for the function is below.

X	Y	Z	Output
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



A	F
0	1
1	0