Board I/O

Chapter 6 & 7

Board I/O

- System is a body, board is the head, CPU is the brain, and IO is the eyes, mouth, and limbs.
- Input
  - Bring information from an input device to the processor
- Output
  - Take information out of the processor to an output device
- Topics
  - Interface
  - Performance

I/O Devices

- Networking I/O
  - NICs
- Input
  - Keyboard, mouse, remote, switch
- Graphics
  - Touch screen, printer, LED, LCD
- Storage
  - Hard drive, CD/DVDROM, flash driver
- Debugging and program loading
  - JTAG, UISP, GDB
- Others
  - ADC, DAC

I/O Hardware Model

- Transmission medium
  - Wired or wireless or light or sound
  - Between IO devices and IO ports
- Communication port
  - COM/UART, USB
- Communication interface
  - Between CPU and I/O ports
- I/O Controller
  - Slave I/O processor

I/O Hardware Model

- Simple example,
  - Figure 6-3b
  - Direct connection from CPU to LED
  - No controller, no port
- Complex example
  - Figure 6-3a
  - Monitor display
  - Video control and video port

CPU Control

- No port, no controller
  - Driver and control (API) over the device
  - Data format and transmission with the device
- Have port, but no controller
  - Driver and control (API) over the port
  - Data format and transmission through the port
- Have both port and controller
  - Driver and control (API) over the controller
  - Data format and transmission with the controller

I/O Hardware

- Features
  - Expandability
  - Functionality
  - EM compatibility
  - Power consumption
  - Performance
    - Reliability
    - Throughput
    - Response

Serial I/O

- Communication mode
  - Simplex : Figure 6-4a
    - One direction only
    - Examples ?
  - Half duplex : Figure 6-4b
    - Two direction over time
    - One direction on any particular time point
  - Full duplex : Figure 6-4c
    - Two direction on any time point
  - How about an Ethernet NIC? (UTP vs. Co-axial)

Serial I/O

- Communication type
  - Synchronous
    - One : sender and receiver are using the same clock.
    - Two : sender and receiver are using the same states.
  - Asynchronous
    - One : sender and receiver are using different clocks.
    - Two : sender and receiver are using different states.
  - Example : UART
    - Same clock? Same state?

Serial I/O Protocol

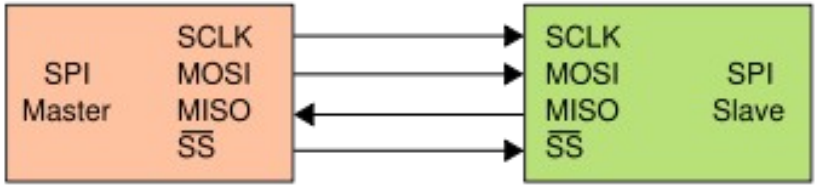
- UART protocol, Figure 6-5
  - Universal Asynchronous Receiver/Transmitter
  - Idle state : voltage ? logic ?
  - Start bit : voltage ? logic ?
  - Stop bits
  - Parity bit
  - Data size
  - Data rate
    - Baud rate : raw data rate, including control and data bits
    - Bit rate : actual data rate, including only data bits
  - Frame vs bits

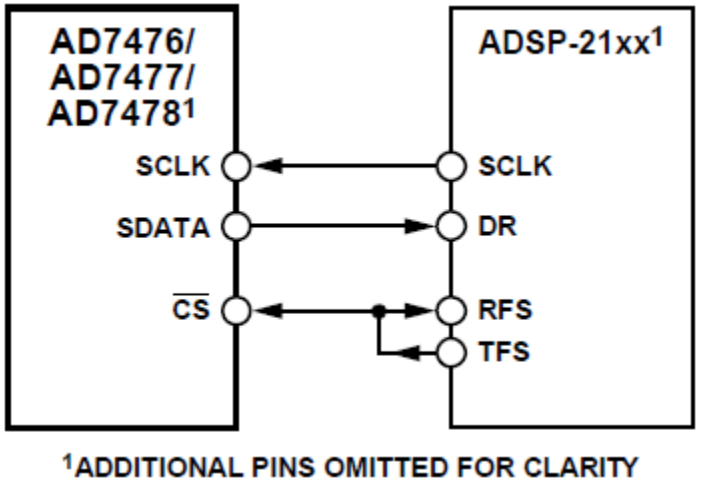
Serial I/O Protocol

- UART protocol
  - If a sender uses a clock of 1MHz
  - If a receiver uses a clock of 1.2MHz, but thinks it is using a clock of 1MHz
  - How can they communicate at 10Kbps?
    - $|t*f_s - t*f_r| < 1 \Rightarrow t < 1/|f_s - f_r|$
    - $frame\_size = t*f_s < f_s/|f_s - f_r|$
  - Generally, what is the allowed difference of their clocks?
    - $frame\_size < f/|\Delta f|$
    - $|\Delta f|/f < 1/frame\_size$

Serial I/O Protocol

- SPI protocol
  - Serial Peripheral Interface
  - Master provides
    - Clock (clock is synced)
    - Slave selection (state is synced)
  - Master output/slave in
  - Slave output/master in
  - Example : AD7476
    - Who is master or slave?





Serial I/O Example

- RS232
  - OSI model
    - Medium (PHY)
    - Interface (control or signalling, PHY and MAC)
    - UART (data format, PHY)
  - DTE (Data Terminal Equipment) : sender
  - DCE (Data Circuit-terminating Equipment) : receiver
  - DB9 connector : at the DTE side, output is italic
    - 1. Carrier Detect (phone), 2. Received Data, *3. Transmitted Data, 4. DTE Ready,* 5. Common Ground, 6. DCE Ready, *7. Request To Send,* 8. Clear To Send, 9. Ring Indicator (modem)

RS232

- Communication process
  - Start from power on (DTE -> DCE) :
  - Simple mode
    - 4->, 6<-, 3->
  - Handshaking mode
    - 4->, 6<-, 7->, 8<-, 3->
  - Data transmission
    - UART
  - What is control logic?

Serial I/O Example

- Small communication range
- 802.15.1 : Bluetooth
- 802.15.4 : Zigbee
  - 10-meter communication range
  - Lower data rate than WiFi : 20, 40, 100, 250 kbps
  - Simpler than Bluetooth
  - 30 channels in 902-928 MHz
  - Point-to-point or star networks
    - Coordinator: full-function device (FFD)
    - Peers: reduced-function devices (RFD)

Another Serial I/O Example

- Ethernet
  - IEEE 802.3/u/z
  - Thick or thin coax : 500 meters or 200 meters
    - 10Base-5 or 10Base-2 : 10Mbps
  - Twisted pair
    - 10Base-T or 100Base-F : 10Mbps or 100Mbps
  - CSMA/CD
  - OSI model and Ethernet controller

Parallel I/O

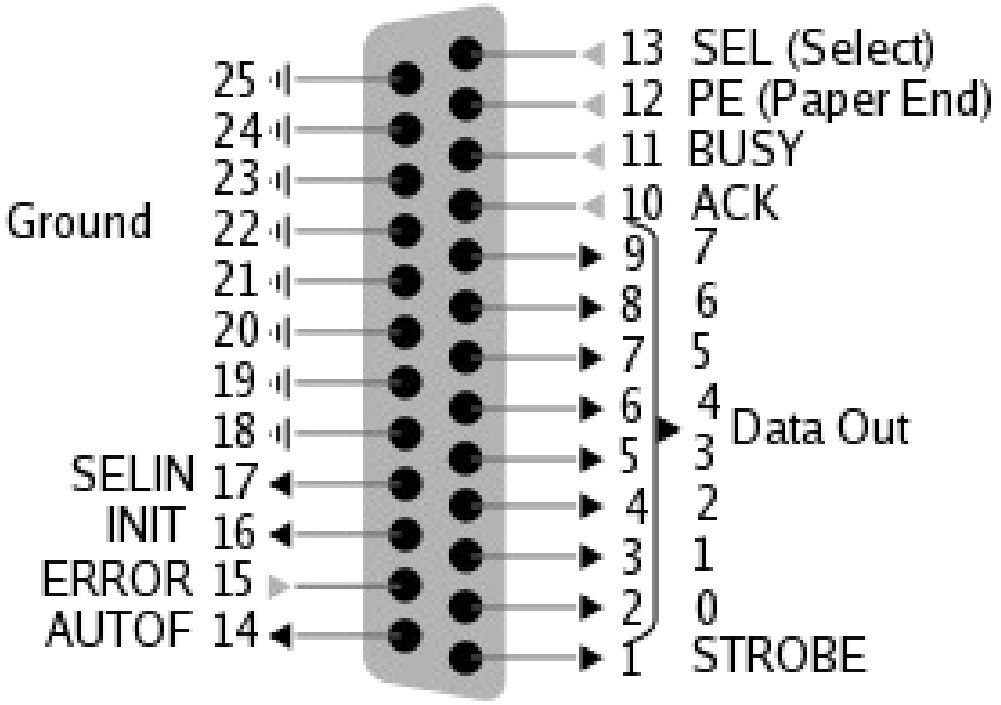
- Transmit multiple-bit data in parallel
- I/O hardware model
  - Transmission medium
  - Communication parallel port
  - Communication parallel interface
  - I/O Controller

Parallel I/O Example

- IEEE 1284
  - LPT (Line Print Terminal) : printers
  - Enhanced Parallel Port (EPP), Extended Capability Port (ECP) : half-duplex, bi-directional
  - Data rate: 2-2.5Mbps
  - Port: DB-25, Micro ribbon (36 pins)
  - 8-bit data pins and other signalling pins

Parallel I/O Example

- Pin schematics



USB

- Replace all types of serial and parallel IOs
- Extended to support multiple devices (physical and logical)
- USB 1.0 : 12Mbps; USB 2.0 : 480Mbps; USB 3.0 : 5.0Gbps
- Pins : 1 VCC, 2 data+, 3 data-, 4 GND
- Cable length : <5meter for 1500ns RTT
- More details are online.

I/O Controller and CPU

- An ability of the master CPU to initialize and monitor the I/O controller
  - Registers in I/O controller
  - Control register for configuration
  - Status register for monitoring
- A way for the master CPU to request I/O
  - Signalling registers
  - Signalling instructions, not data instructions

I/O Controller and CPU

- A way for the I/O controller to contact the master CPU
  - Interrupt
  - Data cache in I/O controller
- A mechanism for both to exchange data
  - Data I/O instructions and data registers
  - Memory-mapped
- Check the manual of I/O controller

I/O Performance

- Performance factors
  - The data rates of the I/O devices
    - Variety of I/O speeds
  - The speed of the master processor
    - Possible application bottleneck in embedded system
  - Communication between them
    - Data loss or hang or interrupt priority ...
- Performance metrics
  - Throughput
  - Processing time
  - Response time

Bus

- Master and slave devices
  - Master : can initiate a bus transaction
  - Slave : can only respond to a master's request
- Buses
  - System bus : specific to CPU and memory
  - Backplane bus : shared with on board components
  - IO bus : extended to external components

Bus

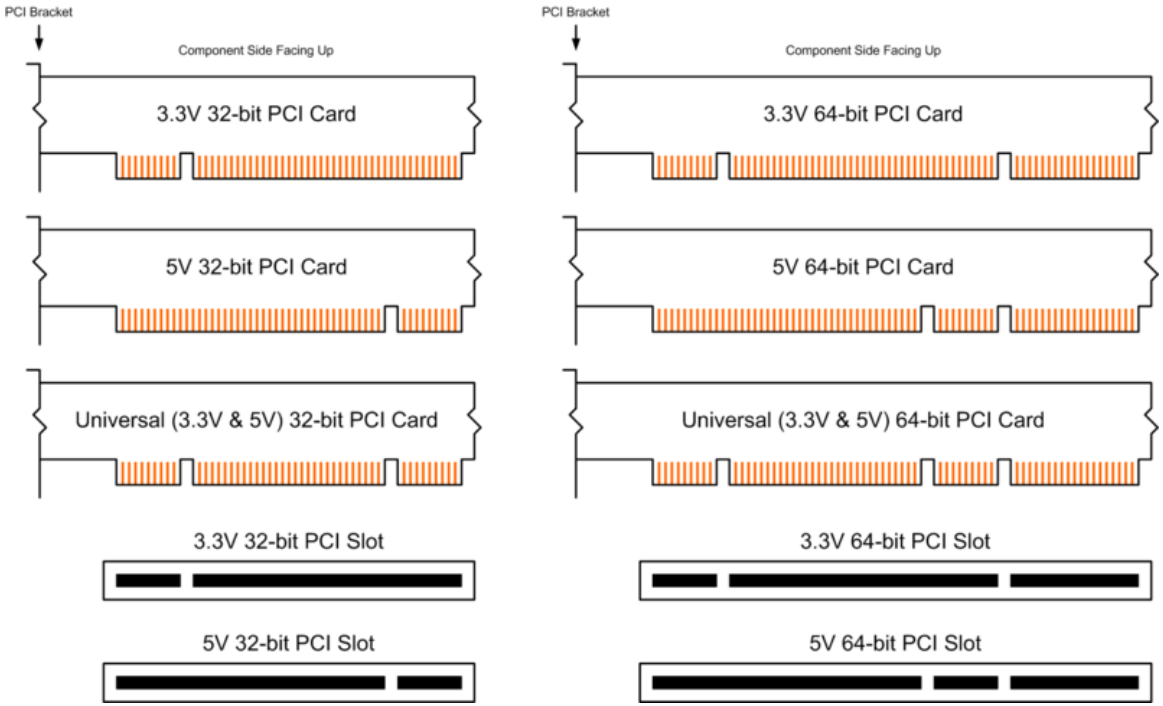
- Bus and bus bridges : north and south
  - Bridge : connection among buses
  - Northbridge : connect faster buses
    - memory controller hub
    - handle communications among CPU, memory, video cards, and southbridge
  - Southbridge : connect slower buses
    - I/O controller Hub
    - handle communications among slower devices (IO) on the motherboard

Bus

- Arbitration
  - Dynamic central parallel, Fig. 7-3a
    - FIFO
    - Priority-based
  - Centralized serial, Fig. 7-4
    - Daisy chain
  - Distributed, Fig. 7-5

Bus Example : PCI

- Peripheral Component Interconnection
  - Data size : 32-bit or 64-bit
  - Data rate : 33MHz or 66 MHz or 133MHz



PCI

- Dynamic centralized parallel arbitration
- Five steps
  - Request to the central arbitrator
  - Be granted
  - Send address and set transfer type
  - Transfer data and set transfer status
  - Terminate