CPU II

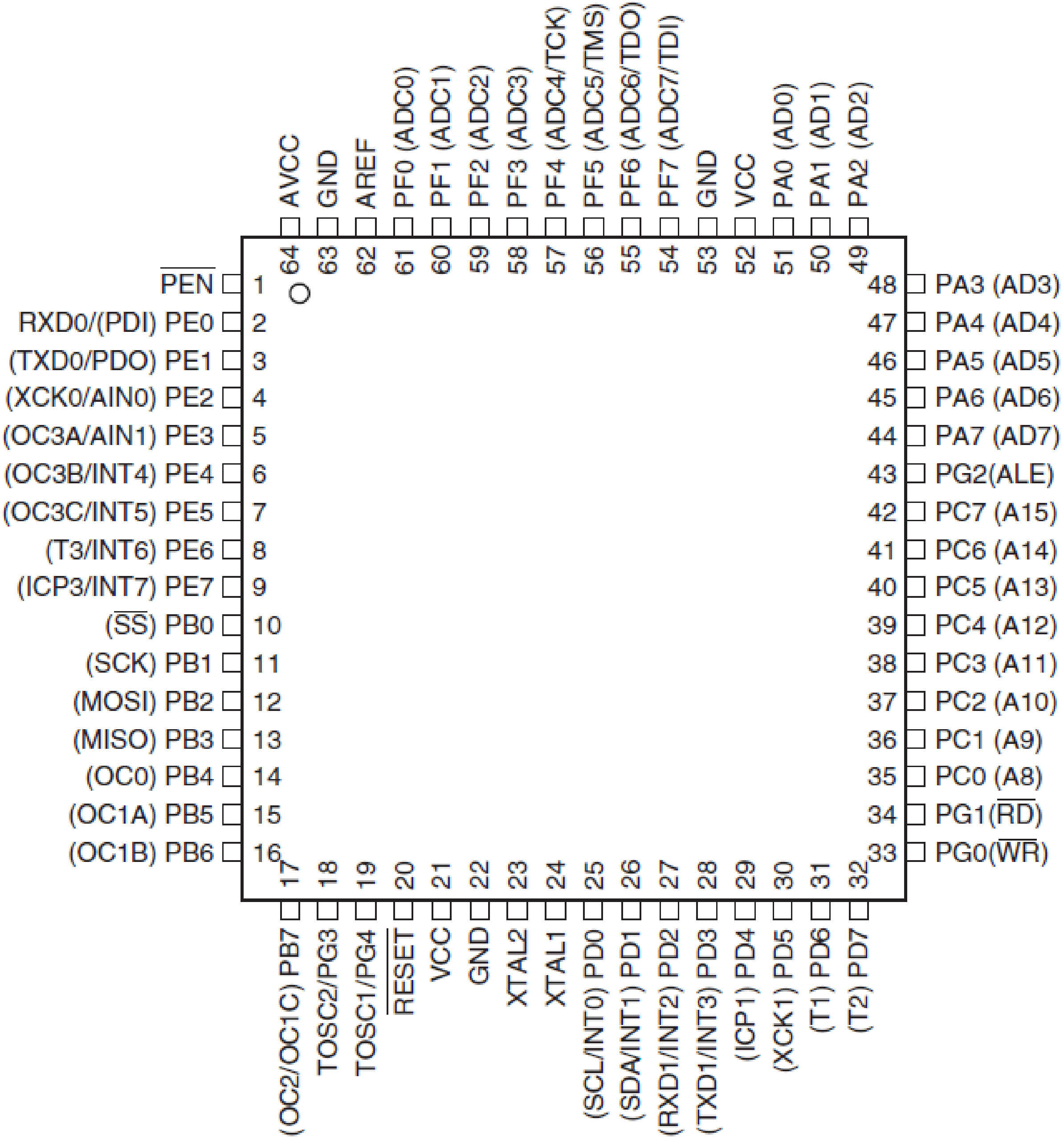
Design

Chapter 4

CPU Model

- Processor pins
  - Power supply
  - Ground
  - Clock
  - Address pins
  - Data pins
  - IO pins
  - Read pin (to memory)
  - Write pin (to memory)
  - Interrupt pins

CPU Model


AVCC 64
GND 63
AREF 62
PF0 (ADC0) 61
PF1 (ADC1) 60
PF2 (ADC2) 59
PF3 (ADC3) 58
PF4 (ADC4/TCK) 57
PF5 (ADC5/TMS) 56
PF6 (ADC6/TDO) 55
PF7 (ADC7/TDI) 54
GND 53
VCC 52
PA0 (AD0) 51
PA1 (AD1) 50
PA2 (AD2) 49
PEN 1
RXD0/(PDI) PE0 2
(TXD0/PDO) PE1 3
(XCK0/AIN0) PE2 4
(OC3A/AIN1) PE3 5
(OC3B/INT4) PE4 6
(OC3C/INT5) PE5 7
(T3/INT6) PE6 8
(ICP3/INT7) PE7 9
(SS) PB0 10
(SCK) PB1 11
(MOSI) PB2 12
(MISO) PB3 13
(OC0) PB4 14
(OC1A) PB5 15
(OC1B) PB6 16
48 PA3 (AD3)
47 PA4 (AD4)
46 PA5 (AD5)
45 PA6 (AD6)
44 PA7 (AD7)
43 PG2(ALE)
42 PC7 (A15)
41 PC6 (A14)
40 PC5 (A13)
39 PC4 (A12)
38 PC3 (A11)
37 PC2 (A10)
36 PC1 (A9)
35 PC0 (A8)
34 PG1(RD)
33 PG0(WR)
17 (OC2/OC1C) PB7
18 TOSC2/PG3
19 TOSC1/PG4
20 RESET
21 VCC
22 GND
23 XTAL2
24 XTAL1
25 (SCL/INT0) PD0
26 (SDA/INT1) PD1
27 (RXD1/INT2) PD2
28 (TXD1/INT3) PD3
29 (ICP1) PD4
30 (XCK1) PD5
31 (T1) PD6
32 (T2) PD7

Execution Cycle

- Determine instruction
- Fetch instruction
- Decode instruction
- Fetch operands
- Execute
- Store result
- ...

Execution Cycle

Figure 6. The Parallel Instruction Fetches and Instruction Executions

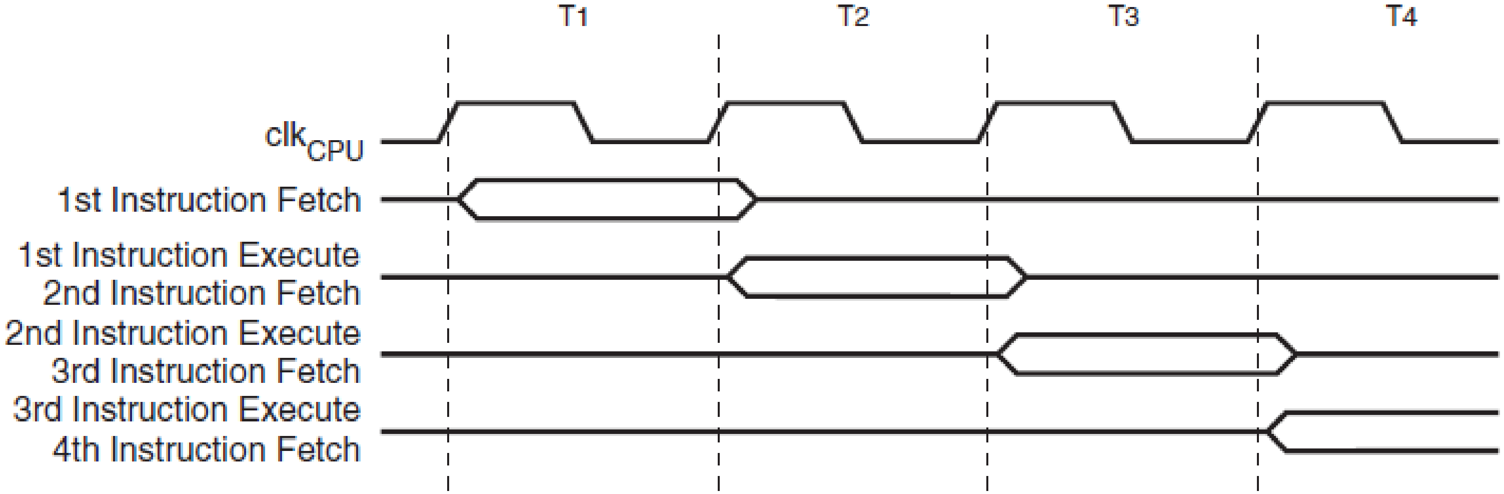
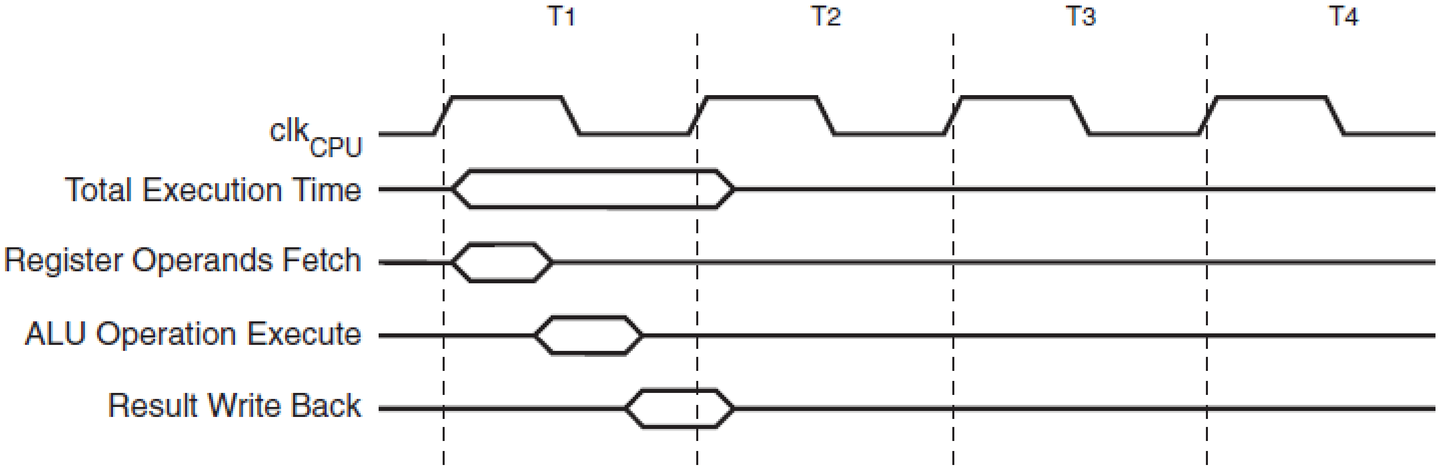


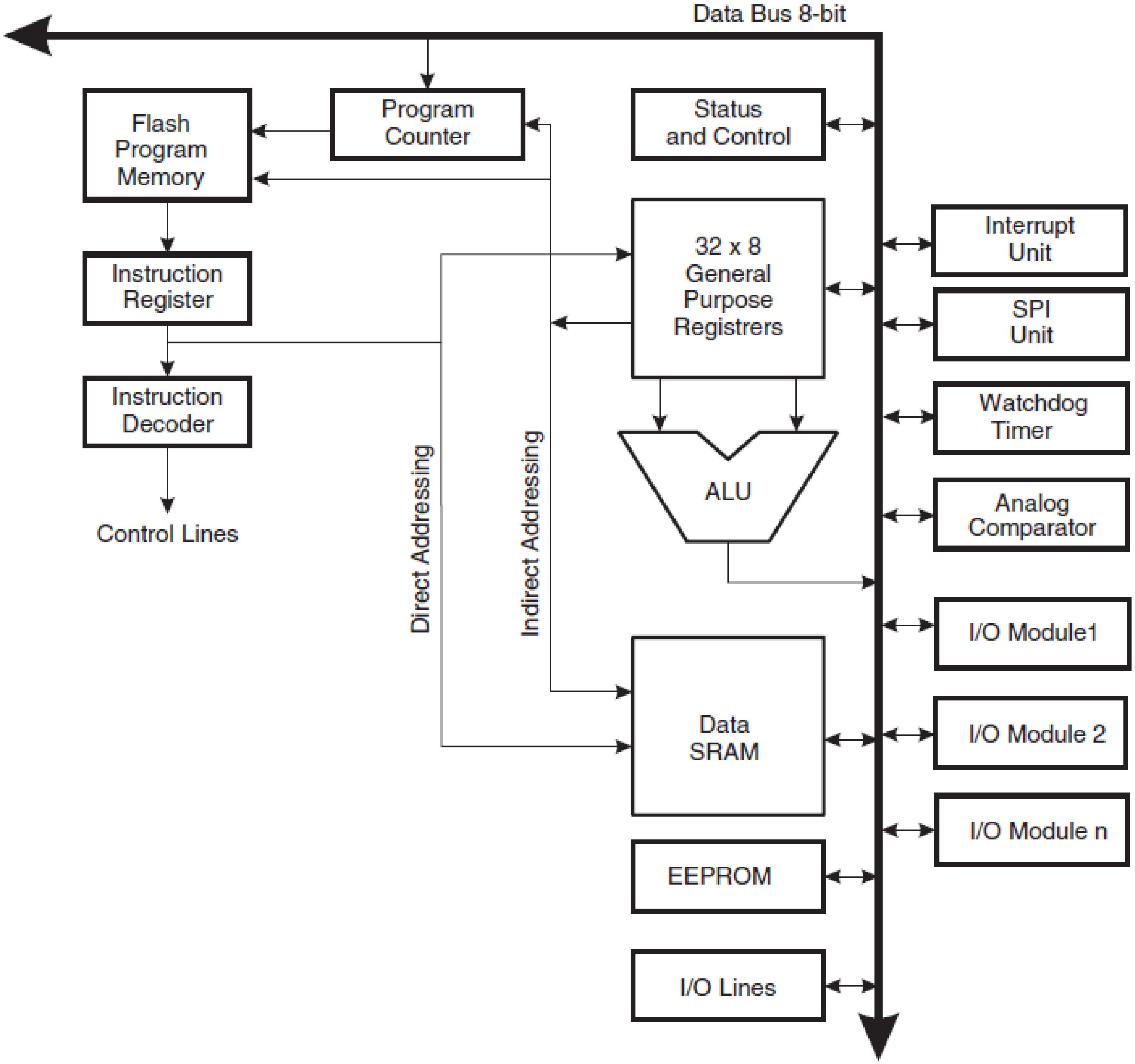
Figure 7. Single Cycle ALU Operation



CPU Core Components

- ALU
  - Computation unit
- Register
  - Fast data storage
- Control unit
  - Management unit
- Internal bus
  - Connect the three components

CPU Core Components



Internal Bus

- Control signals + tri-state gates
- Types
  - Data bus
    - Data mem, registers, IOs
  - Address bus
    - Program counter (to code mem)
    - Registers (to data mem)
  - Control bus
    - Instruction decoder

ALU

- Arithmetic instructions
  - Integer and floating arithmetic computation
  - Signed and unsigned addition and subtraction
  - Multiplication? (*)
  - Division? (/ %)
  - Logarithm, exponentiation, ??
- Logic instructions
  - AND, OR, XOR
  - NOT : 1's and 2's complements

ALU

- Branch instructions
  - Conditional branch
  - Jump : direct, indirect, relative, absolute
  - Call, return : direct, indirect, relative, absolute
- Data transfer instructions
  - Mem to and from reg
  - Reg to reg, mem to mem
  - Mem and reg to and from IO
  - Code mem to and from data mem

ALU

- Bit and bit testing instructions
  - Set, clear
  - Swap, shift
  - Test
- MCU and MMU control instructions
  - NOP
  - Sleep (pause)
  - Soft interrupt
  - Memory control and map

Registers

- Store operands and results
- Made by flip-flop or SRAM
- Storage register vs. shift register
- Special registers
  - Status register
    - State of a processor
  - Timer
  - Program counter

Control Unit

- Fetch instruction
  - Sequential
  - Branch
- Fetch operands
  - Pipeline
- Control execution
  - Select functional unit
  - Signal functional unit

CPU Clock

- External clock
- Internal clocks
  - Generation
    - How? (RC delay)
  - Divide
    - How? (Counter)

On-chip Memory

- Non-volatile memory
  - Data in memory will not disappear
  - Read-only memory (ROM) : Figure 4-39
  - Programmable link/fuse : Figure 4-40
  - Types
    - MROM
    - PROM
    - EPROM
    - EEPROM
    - Flash

Volatile Memory

- Random-access memory (RAM)
- Types
  - SRAM : flip-flop
  - DRAM : capacitor
    - Discharge when read or overtime
    - Need recharge / refresh
    - Refresh is controlled by memory controller

Cache

- Level-1 cache
  - Inside CPU
    - Cache vs. on-chip main memory
  - Snapshot of a part of main memory
  - Directly interact with the CPU
  - Most code only access code and data within a range
  - Cache hit vs. cache miss

Cache

- Data transfer between cache and main memory
  - Consistency
  - Read criteria : high hit rate and low miss rate
  - Write strategies
    - Write through
    - Write back
  - CPU and memory architecture
    - CPU↔cache↔MMU↔memory↔DMA↔HD

On-chip Memory Management

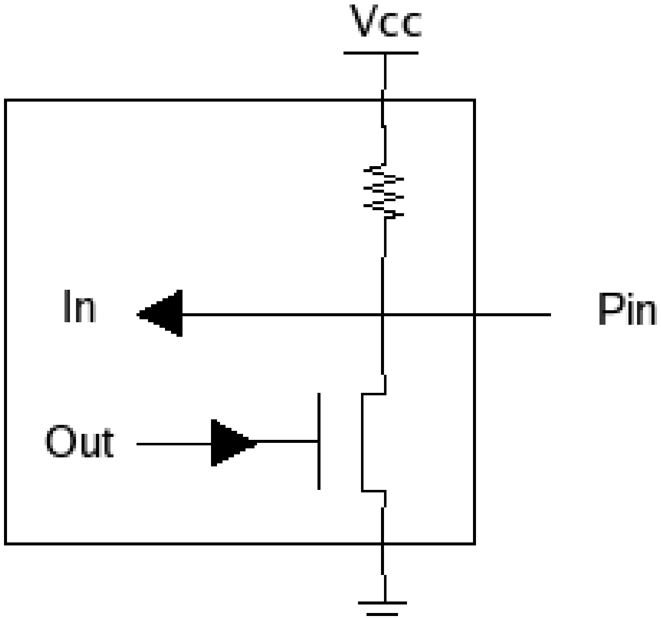
- Functionalities
  - Control multiple physical memories
  - Translate logical address to physical address
  - Handle memory security
  - Control cache
  - Handle bus arbitration between CPU and memory
- Memory organization
  - Code and data memory
  - Memory mapping

Example: Memory and IO Mapping

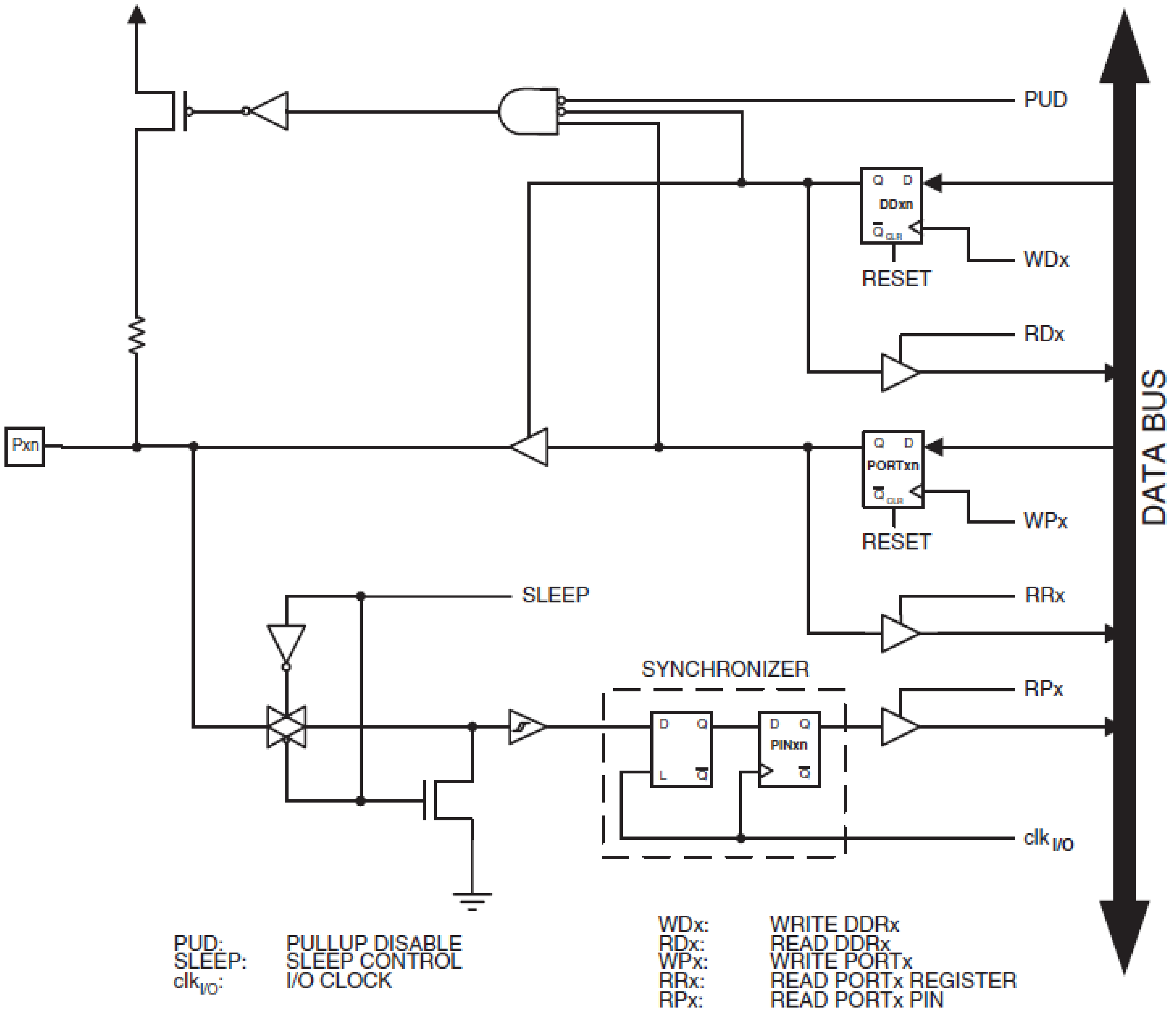
- 256 IOs
- 1 64KB ROM (flash)
- 3 64KB RAMs
- Von-Nueman architecture
- Mapping (20-bit address space)
  - 0x00 - 0xFF IOs (share space with ROM)
  - 0x100 - 0xFFFF code in ROM
  - 0x10000 - 0x3FFFF data in RAMs
  - A selection signal on 0x**000**XX

Processor I/O

- Most concepts are the same as board I/O
  - because the boundary of a board and a processor in an embedded system is not as clear as in a regular computer.
- I/O pin
  - Unidirectional (in or out)
  - Bidirectional (in and out)
  - Programmable



IO Pin Example



PUD:	PULLUP DISABLE
SLEEP:	SLEEP CONTROL
$\text{clk}_{I/O}$:	I/O CLOCK

WDx:	WRITE DDRx
RDx:	READ DDRx
WPx:	WRITE PORTx
RRx:	READ PORTx REGISTER
RPx:	READ PORTx PIN

IO Pin Example

- LEDs
  - Connected to pin set A: 0, 1, 2
  - Two registers control pin set A
    - DDRA ($1A ($3A)) : direction control
      - 0 : input
      - 1 : output
    - PORTA ($1B ($3B)) : data output
    - PINA ($19 ($39)) : data input

Embedded I/O Components

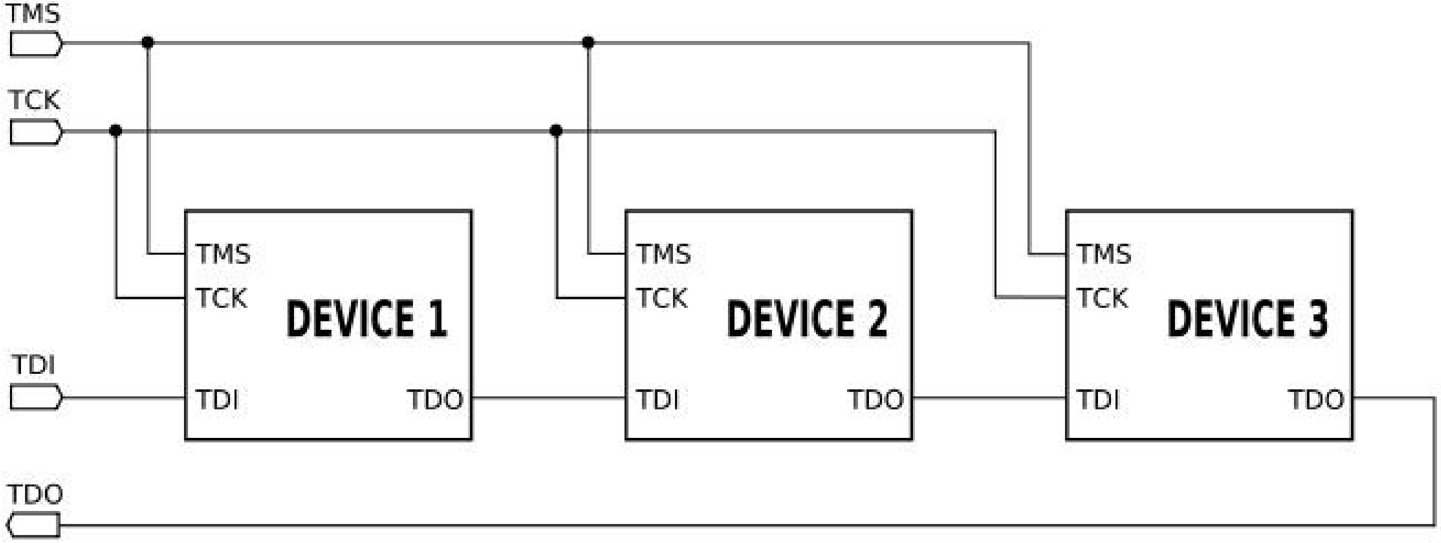
- Serial I/O
  - USART (example in sensor)
    - Universal Synchronous Asynchronous Receiver Transmitter
  - SPI
    - Serial Peripheral Interface
  - JTAG
    - Joint Test Action Group, IEEE 1149.1
    - Diagnose software and hardware of embedded system

JTAG

- Debug support is for many software developers the main reason to be interested in JTAG.
- Debugging architectures built up using JTAG, such as ARM CoreSight, Nexus, ...
- Processors can normally be halted, single stepped, or let run freely.
- Code breakpoints are supported, both for code in RAM and in ROM/flash.
- Data breakpoints are often available, as is bulk data download to RAM.

JTAG

- JTAG pins
  - TDI (Test Data In) : input JTAG instructions
  - TDO (Test Data Out) : obtain scanned data
  - TCK (Test Clock) : clock, SPI
  - TMS (Test Mode Select) : state control
  - TRST (Test Reset) optional



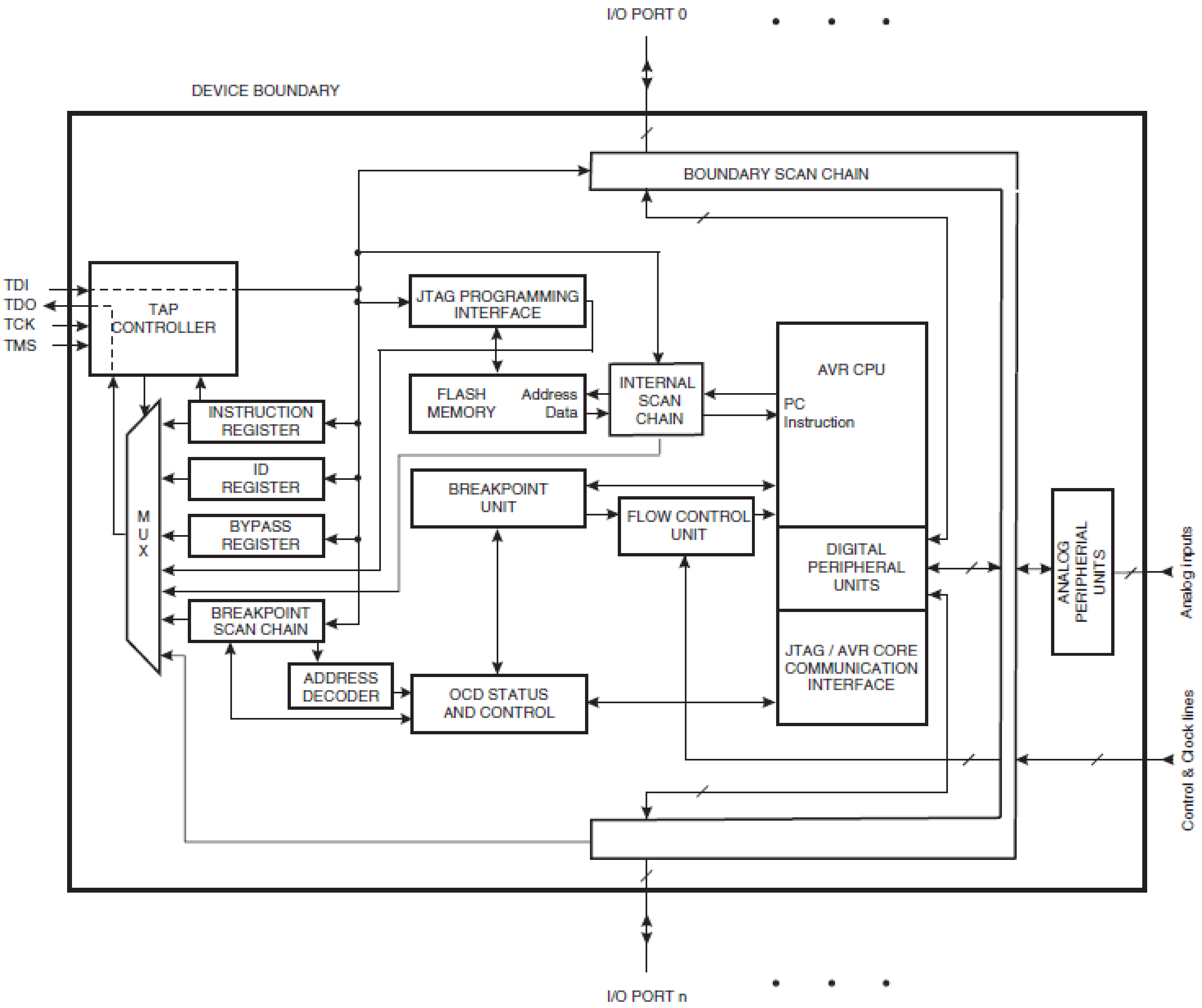
JTAG

- Examples of JTAG instructions
  - EXTEST : for external testing, such as using pins to probe board-level behaviors
  - INTEST : for internal testing, such as using pins to probe on-chip behaviors
  - PRELOAD : loading pin output values before EXTEST
  - SAMPLE : reading pin values into the boundary scan register
  - HIGHZ : deactivates the outputs of all pins
  - RUNBIST : places the chip in a self-test mode
  - SCAN_N : configures a scan path select register (SCREG) affecting the signals to which other boundary scan operations apply
  - USERCODE : returns a user-defined code, for example to identify which FPGA image is active
  - HALT, RESTART : halts or restarts the CPU.

JTAG Example

- Boundary-scan Capabilities
- Debugger Access to:
    - All Internal Peripheral Units
    - Internal and External RAM
    - The Internal Register File
    - Program Counter
    - EEPROM and Flash Memories
- Extensive On-chip Debug Support for Break
    - AVR Break Instruction
    - Break on Change of Program Memory Flow
    - Single Step Break
    - 4 : Program Memory Breakpoints + Data Memory Breakpoints
- Programming of Flash, EEPROM, Fuses, and Lock Bits
- On-chip Debugging Supported by AVR Studio

JTAG Example



Interrupts

- Hardware interrupt
  - Internal
    - Timer, MMU, ADC, operation error, debugging
  - External
    - Hard drive, reset,
- Software interrupt
  - INT instruction
    - Trigger a special routine to change context or mode
- Interrupt vector

Interrupt Service

- Service routine (pseudo-code)
  - When an interrupt is triggered, normally the interrupt flag is cleared to disable other interrupts.
  - Save context
  - Enable other interrupts (optional, set the interrupt flag)
  - Execute the interrupt routine
  - Disable other interrupts (clear the interrupt flag)
  - Restore context
  - Return (normally the interrupt flag is set by the return)
- Example : case8.interrupt

External Interrupt

- Trigger hardware
  - Interrupt pins (IRQs)
  - Interrupt controller
- Trigger mechanism
  - Level-trigger
  - Edge-trigger
- Interrupt controller
  - Slave processor + I/O device

Processor Performance

- Computational performance
  - Throughput : instructions per second (MIPS)
  - Reliability : mean time between two failures
  - Recoverability : mean time from fail to normal
  - Availability : mean time from normal to fail
- Power performance
  - Duty percentage : mean percentage of execution
  - Idle-mode power consumption