DAC and ADC

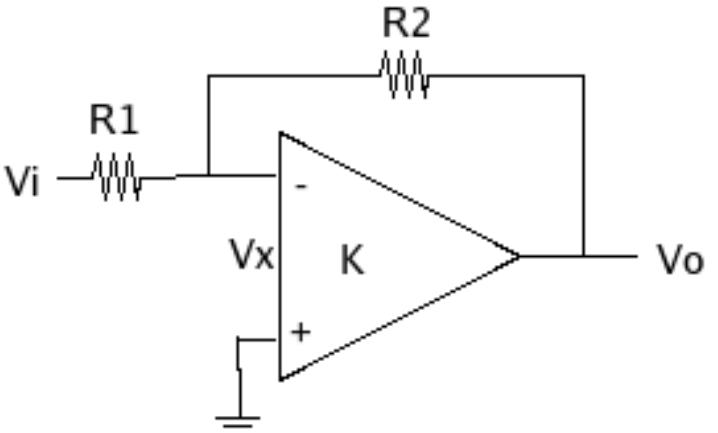
All about data

- Embedded systems
  - Need to process data
    - Sample status of the environment
    - But, raw data is analogous
  - Need to display data
    - Control devices
    - But, control signal is analogous
- Chips
  - Amplifier/Comparator
  - DAC
  - ADC

Circuit model

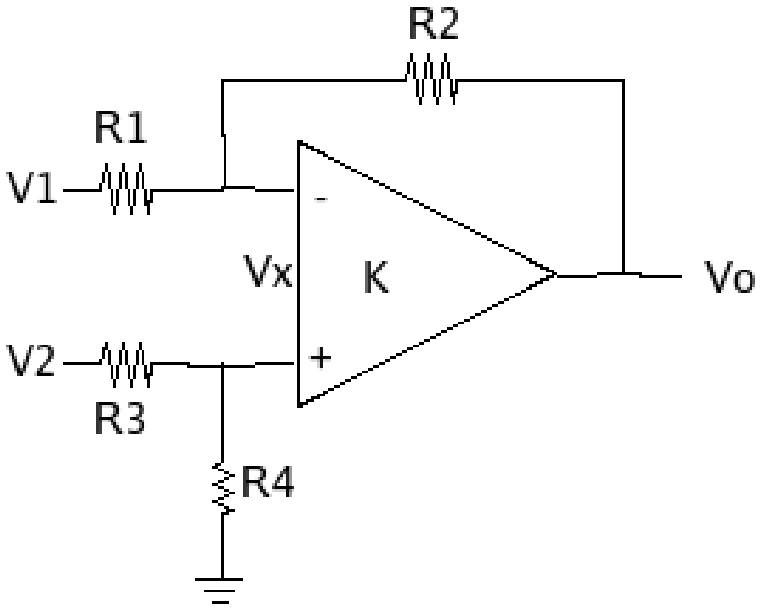
- Amplifier model

$$V_o = -\frac{R2}{R1} V_i$$



- Comparator model

$$V_o = -\frac{R_1}{R_2} V_1 + \frac{(R_1 + R_2) R_4}{R_2 (R_3 + R_4)} V_2$$



Amplifier

- INA2128
  - How to determine gain
  - What is the power supply
  - What is the output range (for sample)
  - What is the input range (for control)
  - How does it respond to input signals with various frequencies (for control)
  - Example circuit: acoustic, temperature, ...

Amplifier/Comparator

- For comparator,
  - If all resistors are the same,

$$V_1 - V_2 = -V_0$$

- Negation and addition circuits
  - Negation?
  - Addition?

DAC

- Digital-to-Analog Converter
- Circuit model
  - Reference voltage
  - Amplifier
  - Analog adder
  - Analog switch

DAC

- Principle
  - Input : 0110
  - Output = 0*8 + 1*4 + 1*2 + 0*1
  - Reference voltage ?
  - Amplifier ?
  - Anolog adder ?
  - Analog switch ?

DAC

- Performance
  - Resolution
    - $2^{number\_of\_bits}$
  - Total harmonic distortion
    - Rectangle output vs. smooth output
  - Noise
  - Dynamic output range

DAC

- Example, AD7304
  - Electrical features
    - Resolution : 8 bits
    - Input resistance : 28KOhm
    - Reference : <5V, from outside
    - Output voltage range : <5V
    - Output current drive : 3mA
    - Logic voltage : 0.8V as low, 2.4V as high
    - Timing : around 50 ns, so safe time is 100ns
    - Operating Temperature Range

DAC (AD7304)

- Example
  - Input
    - Serial :
      - SPI-compatible serial data interface
      - 12-bit data-word format, table 5
      - MSB bits are loaded first
      - Timing
      - How fast is the data rate after all (Bps, not bps)?
    - No parallel

DAC (AD7304)

- Example of control

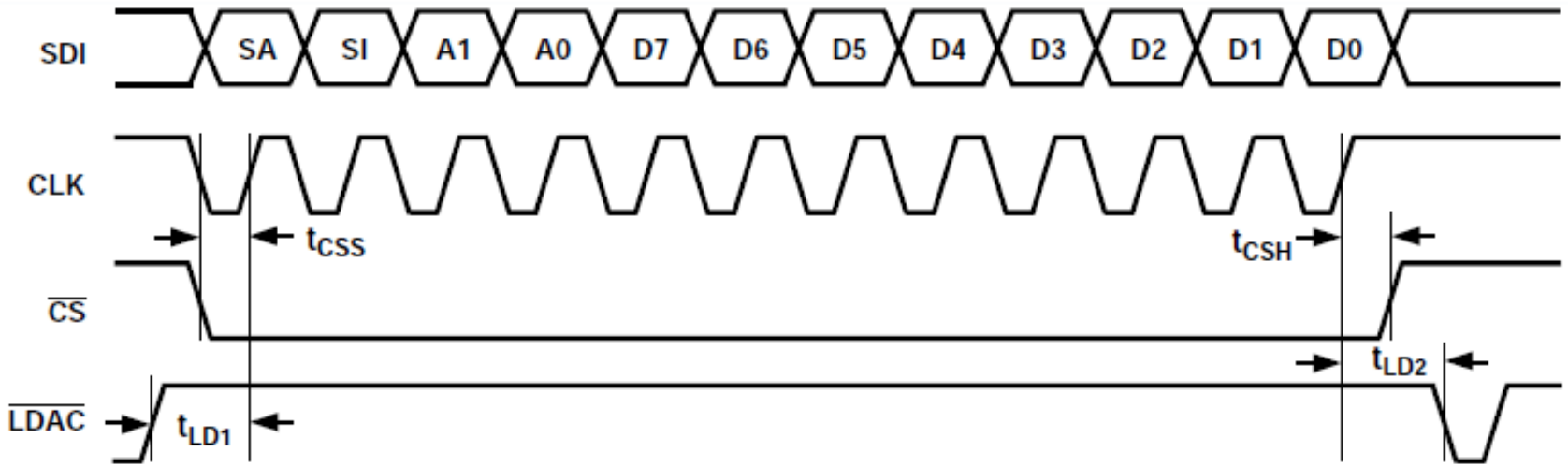


Table 5. AD7304 Serial Input Register Data Format, Data is Loaded in MSB-First Format

	MSB B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	LSB B0
AD7304	SAC	SDC	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

If B11 (SAC), *Shutdown All Channels*, is set to logic low, all DACs are placed in a power shutdown mode, and all output voltages become high resistance. If B10 (SDC), *Shutdown Decoded Channel*, is set to logic low, only the DAC decoded by Address Bits A1 and A0 is placed in shutdown mode.

DAC (AD7304)

- Control by embedded software
  - 1. Configure four IO pins to output
    - SDI, CLK, CS, LDAC
  - 2. Prepare 12-bit data (SDI)
  - 3. Output 1 to the LDAC pin
  - 4. Output 0 to the CS pin
  - 5. Repeat 12 times
    - 5.1. Output the MSB of SDI to the SDI pin
    - 5.2. Output a clock (CLK) to the CLK pin
      - A low and a high
    - 5.3. Left shift SDI
  - 6. Output 1 to the CS pin
  - 7. Output 0 to the LDAC pin

DAC (AD7305)

- Control
  - How many pins
  - Control logic

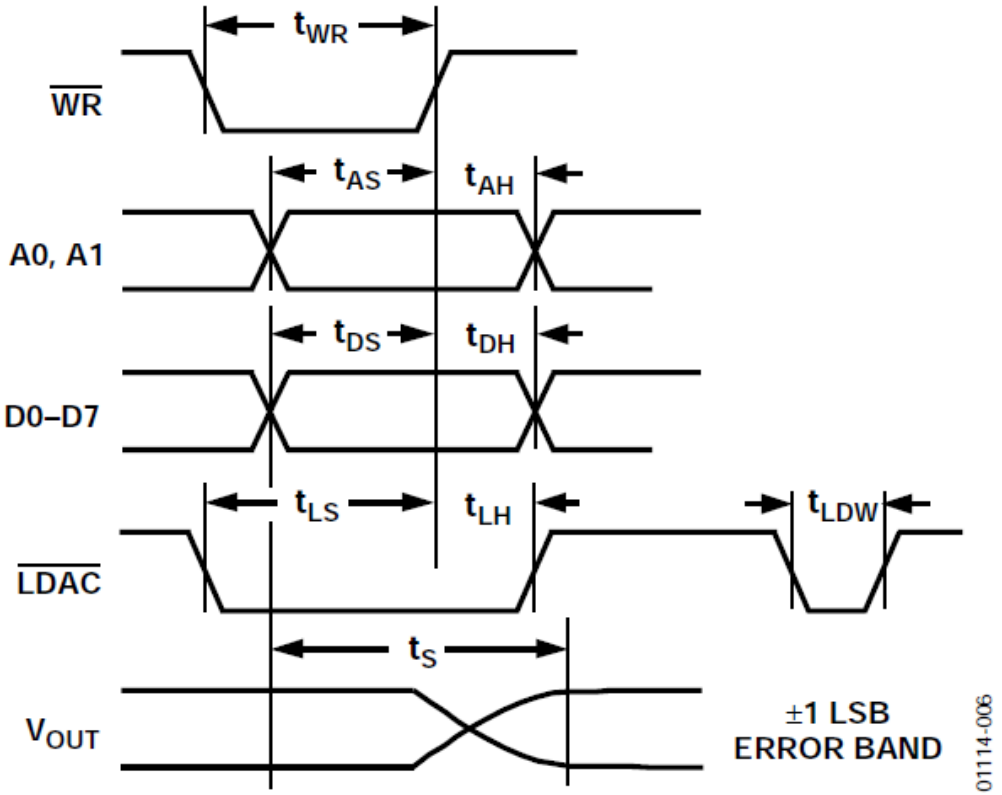


Figure 6. AD7305 General Timing Diagram

ADC

- Analog-to-Digital Converter
- Operation theory
  - Sampling (too low vs too fast)
  - Nyquist theory (proper sampling rate)
    - The sampling rate should at least double the highest frequency of the signal.
  - Sound : 10 Hz to 10KHz
    - Sampling rate? Data rate?
  - Ultrasound for diagnose : 200KHz to 2MHz

ADC

- Performance
  - Resolution
  - Maximum sampling frequency
  - Noise
  - Dynamic input range

ADC

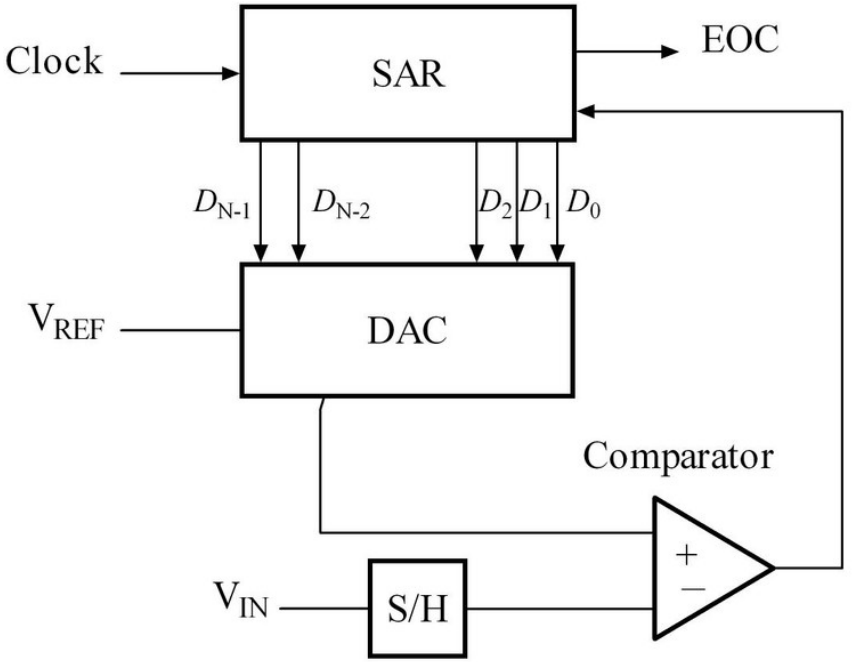
- Type
  - Linear ADC
    - Output = c * Input
    - Distortion = $\sigma^2/2$, where σ is the interval of resolution
  - Non-linear ADC
    - Ouput = c * $\log_2$(input)
    - Distortion = ?

ADC

- Implementation
  - Direct conversion ADC
    - A voltage ladder producing (2^n-1) voltages
    - (2^n-1) comparators
    - An encoder
      - How?
    - Extremely fast, but hard to have a very high resolution
      - 8 bits, OK; 12 bits ?; 16 bits NO
  - Example, a 2-bit ADC

ADC

- Implementation
  - Successive-approximation ADC
    - A comparator
    - A DAC
    - A shift register
    - Procedure
      - MSB 1, all others 0
      - Compare V_{in}>V_{DAC}?
      - Yes, 1->MSB; No, 0->MSB
      - Next bit, ...
    - How fast?



ADC (AD7476)

- Example
  - Electricity features
    - Throughput : 1MSPS
    - f_{SCLK} : 10M or 20M
    - 12 bits
  - Output
    - Serial
    - Timing ?
    - Interface to CPUs ?

ADC (AD7476)

- Control
  - The conversion is initiated on the falling edge of CS as de-scribed in the Serial Interface section.
  - To ensure the part remains fully powered up at all times, CS must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of CS.
  - 16 serial clock cycles are required to complete the conversion and access the complete conversion result.

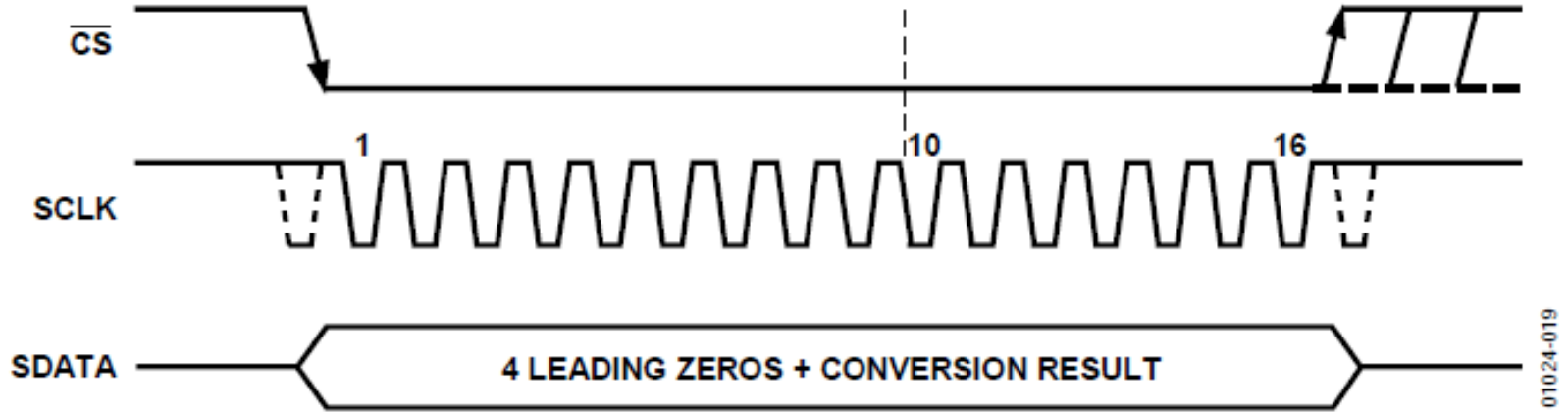
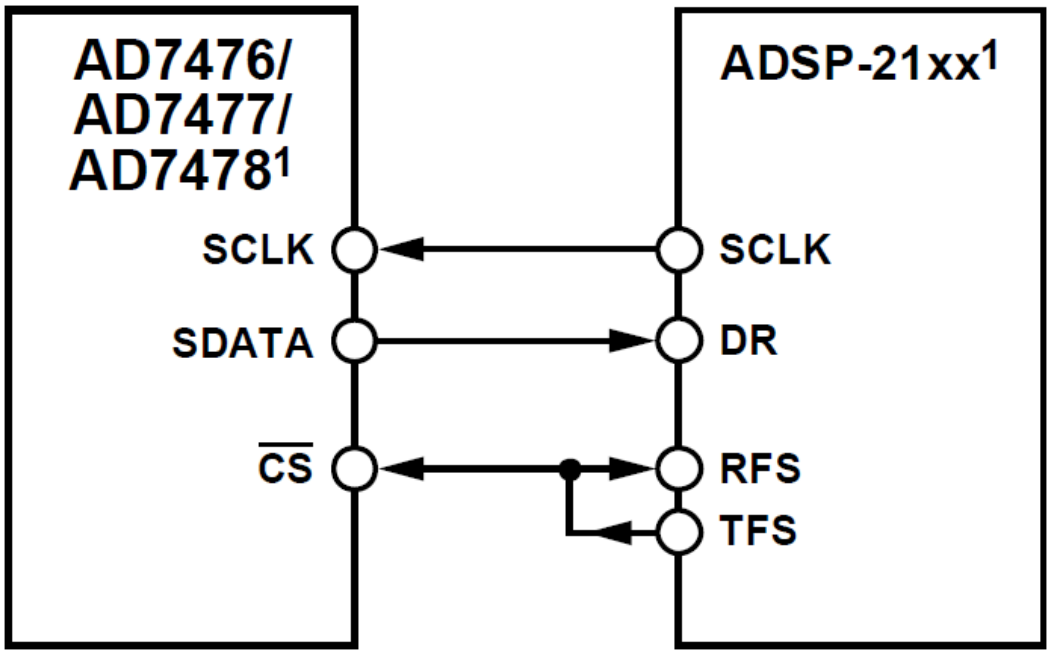


Figure 19. Normal Mode Operation

ADC (AD7476)

- Control logic
  - Output low to CS
  - Output 16 clocks to SCLK
  - Output high to CS
  - Read DR



Design with ADC (AD7476)

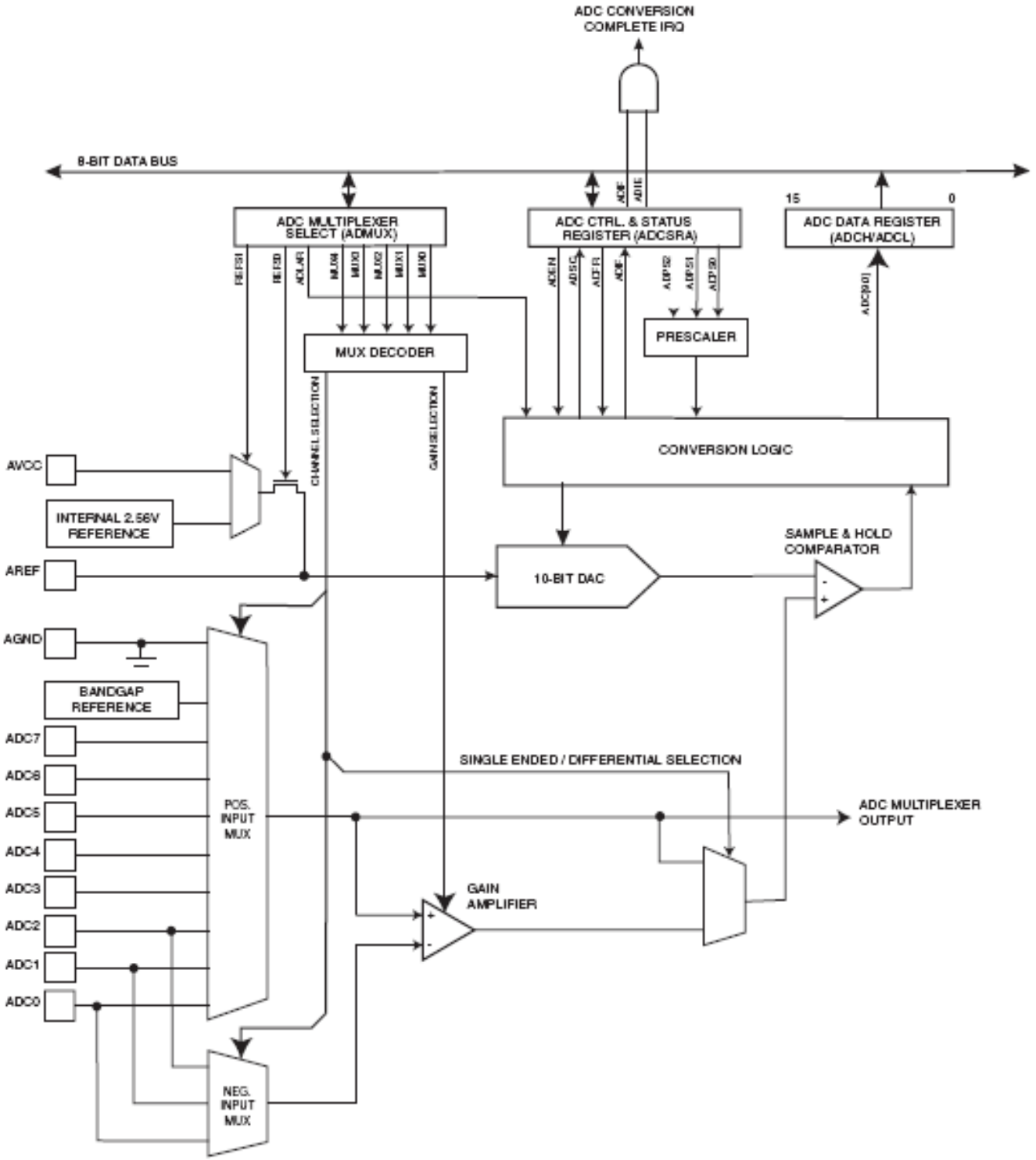
- Sample a signal of 20KHz
  - Can AD7476 work on this?
    - Sample rate?
    - Resolution?
  - Can the CPU ATMega128 (8MHz) work on this?
    - Time for each reading?
    - What is the duty cycle (percentage of working time)?
  - What is the minimum requirement on ADC and CPU for this application?
    - Speed
    - Power

ADC (in chip)

- Example, ATmega128, in chip
  - Electrical features
    - 15KSPS
    - 10 bits
    - 8 input channels (multiplexed single end)
    - Internal adjustable gains
  - Output
    - Parallel
    - 16-bit output register
    - Two configuration registers

- Circuit model

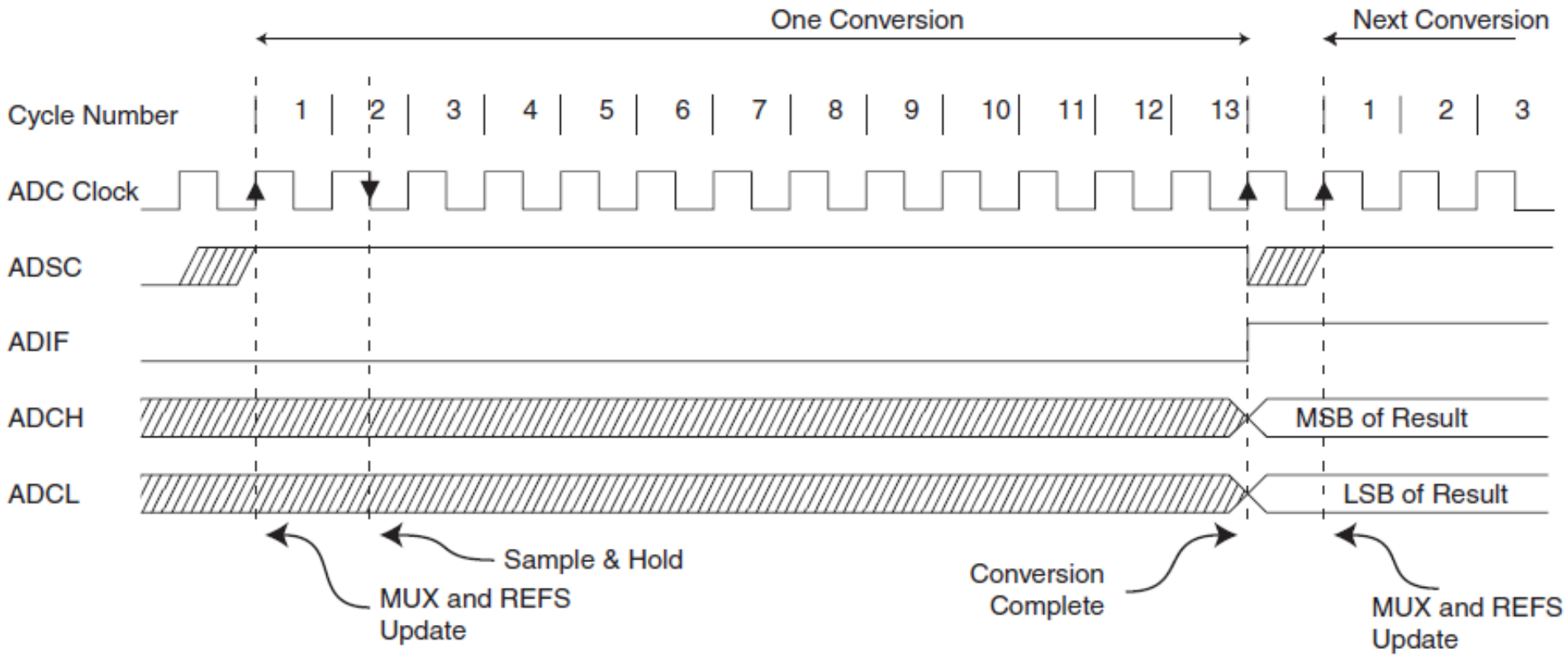
Figure 108. Analog to Digital Converter Block Schematic



ADC (in chip)

- Control

Figure 111. ADC Timing Diagram, Single Conversion



Now,

- We have binary data!