Giga: 1 Billion Micro: 1 Milionth ISA: Instruction Set Architecture false: The Von Neumann architecture allows multiple paths from main memory to the control unit of the CPU. Moore's law is the observation that the number of transistors in a dense integrated circuit (IC) doubles about every two years. Anything that can be done with software can also be done with hardware. System Bus is not part of the Central Processing Unit Which digit determines whether the signed integer number is positive or negative.: The most significant digit or the sign bit.

Convert hex to binary, flip the bits, add one, convert to decimal 0:0000, 1:0001, 2:0010, 3:0011, 4:0100, 5:0101, 6:0110, 7:0111, 8:1000, 9:1001, A:1010, B:1011, C:1100, D:1101, E:1110, F:1111

Reed Solomon: Which Error Detection and Correction Scheme is able to compensate for Burst Errors?, False: ASCII utilizes syndrome's to detect errors. True: Hamming Codes are able to detect and correct errors. False: Parity is able to compensate for multiple bit errors in the same data block. Floating point numbers: 1 sign, 8 exponent, the rest mantissa, exponent-127 = place of decimal point. Past decimal point is 2^1/2 2^1/4 etc. IEEE 754 standard. The purpose of the Control Unit is to Monitor and direct the flow of instructions and data. False: Synchronous busses must use a handshaking protocol. False: Each bit in the computer typically has its own address. If an architecture is byte addressable, and the instruction set architecture word size is larger than 1 byte we must address the issue of byte alignment. In the memory hierarchy, Registers are the fastest. For caching to be effective, we are dependent upon the idea of locality. SRAM is faster. In associative memory, such as cache, information is accessed by its content. In the hexadecimal floating point number 47C69200, the value of it's bias is 16. Amdahl's Law allows you to calculate the speed up of The overall system. The time it takes for sectors to come underneath the read/write heads is called Rotational Delay. False: Raid Level 0 provides for excellent data redundancy. Level 1 RAID gives the best failure protection. False: Programmed I/O uses IRQ lines to notify the CPU of data. For interrupt 11h 1. Multiply 11H by 4 = 44H 2. Lookup in vector table at the address 0000:0040 line over to 0044 3. Read Vector address in backward format 4D F8 00 F0 4. Convert to segment offset address. 5. Correct segment offset address = F000:F84D 6. For 20 bit address add a zero to segment (left) portion of address 7. Add to offset F0000 + F84D 8. Correct 20 bit address = FF84D When the CPU switches between processes, it is called a Context Switch RISC has less instructions than a CISC architecture. True: Compile-time binding requires code to be loaded into the same location each time it is executed. True: Dynamic Link Libraries (DLL's) allow us to share code between several programs without having to include a full copy of external module's code. An Interpreted language processes one source statement at a time when producing a binary stream. SMPP is not one of the possible combinations resulting from Flynn's Taxonomy. A Virtual Machine

allows us to emulate multiple physical computers through the use of a single computer. Embedded systems differ from general-purpose machines in that they carry out a limited set of tasks.