Jared Nay
Lab 3 Writeup
ECE 5780

1) 60 Hz gives us a 16.67 ms period. If we divide the clock by 8000 we will get 1 ms per timer count. We can set the PSC value to 7999 and the AAR value to 17. Since we can't get 16.67ms exactly, doing 17ms counts will suffice.

2) PE3, PA6 - AF1, PC6 - AF0, PB4 - AF1.

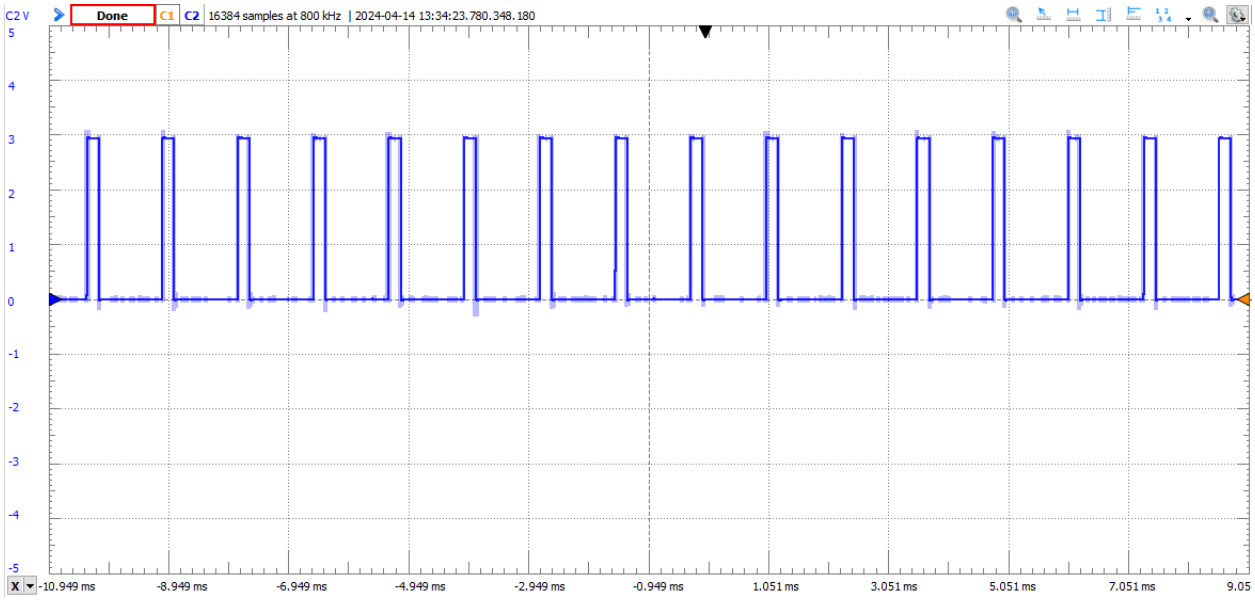
3) 105µs

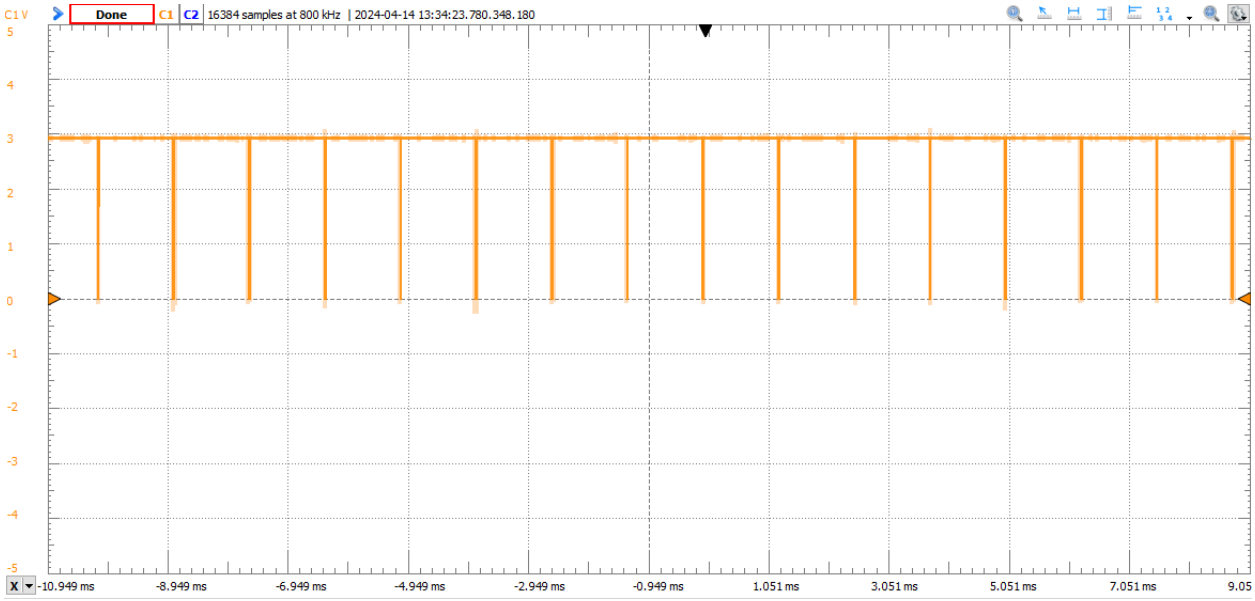
4) When I increased the CCR value the duty cycle increased, spending little time at low voltage.

5) I'm not sure if this is a trick question but I got the same results, the duty cycle increased and I had less time with the voltage high.

6) At the end are two captures from a scope. The first is the blue LED with a low CCR value decreasing the duty cycle. The second is the red LED with a high CCR value increasing the duty cycle. Low duty cycle means dimmer LED.

7) Edge aligned PWM.


C2 V
Done
C1
C2
16384 samples at 800 kHz | 2024-04-14 13:34:23.780.348.180
5
4
3
2
1
0
-1
-2
-3
-4
-5
X
-10.949 ms
-8.949 ms
-6.949 ms
-4.949 ms
-2.949 ms
-0.949 ms
1.051 ms
3.051 ms
5.051 ms
7.051 ms
9.05


C1 V
Done
C1
C2
16384 samples at 800 kHz | 2024-04-14 13:34:23.780.348.180
5
4
3
2
1
0
-1
-2
-3
-4
-5
X
-10.949 ms
-8.949 ms
-6.949 ms
-4.949 ms
-2.949 ms
-0.949 ms
1.051 ms
3.051 ms
5.051 ms
7.051 ms
9.05