

VSD Advanced Physical Design Workshop.

1:

Day 1: QFN - 48

chip vs package x

↳ Quad Flat No-leads.

chip sits @ the center of the package.

Components of a chip:

i ① PADS ② CORE ③ DIE

Usually a chip comprises of:

* SOC * ADC * PLL
* SRAM * DAC * SPI

* SPI

Except SOC → the rest are foundry IPs.

SOC & SPI → Macros

↳ purely digital logic

12: Intro to RISC-V ISA.

High-level → Assembly → Machine-level

RISC-V Architecture → Implementation using HDL → Layout

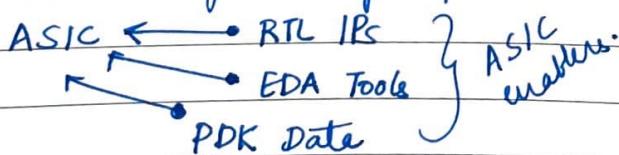
13: from software applications to hardware.

1 Apps → System Software → Hardware

[
OS
Compiler
Assembler]

ISA → Abstract interface b/t high level language & hardware.

14: SOC Design using OpenLANE.

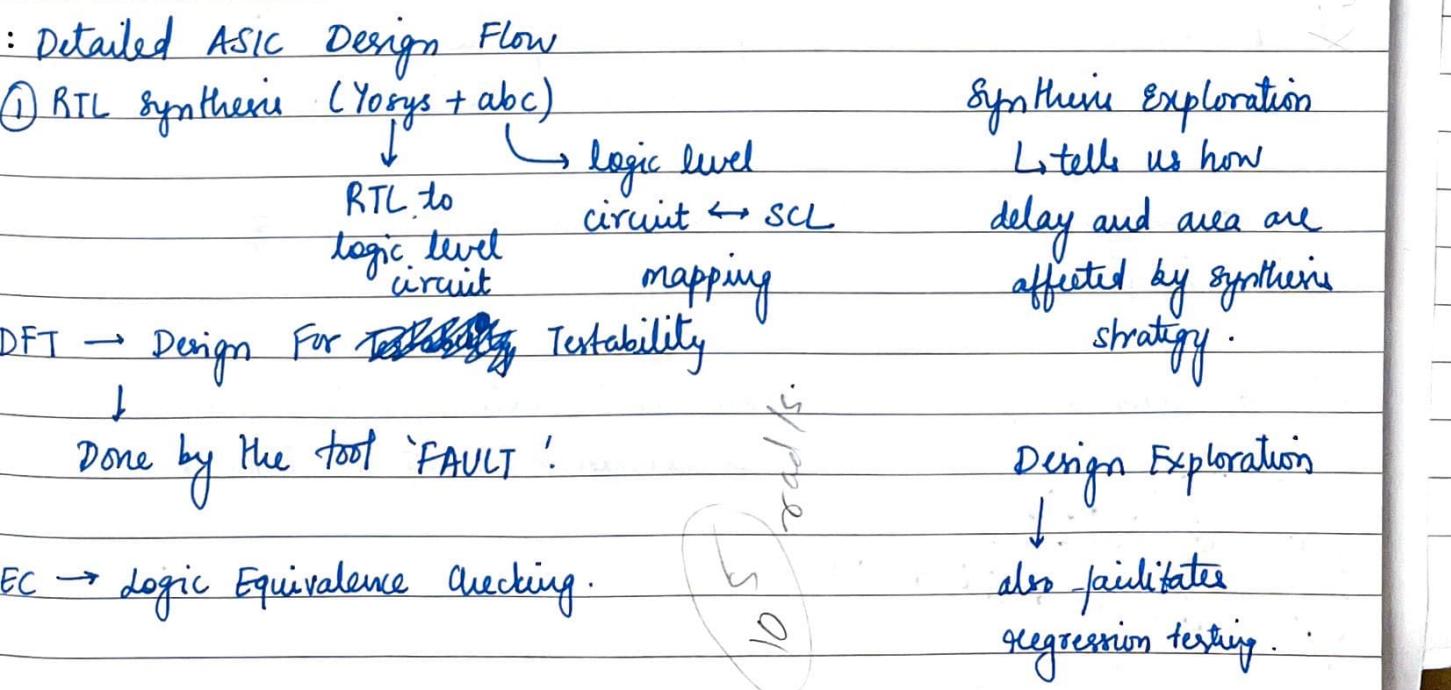
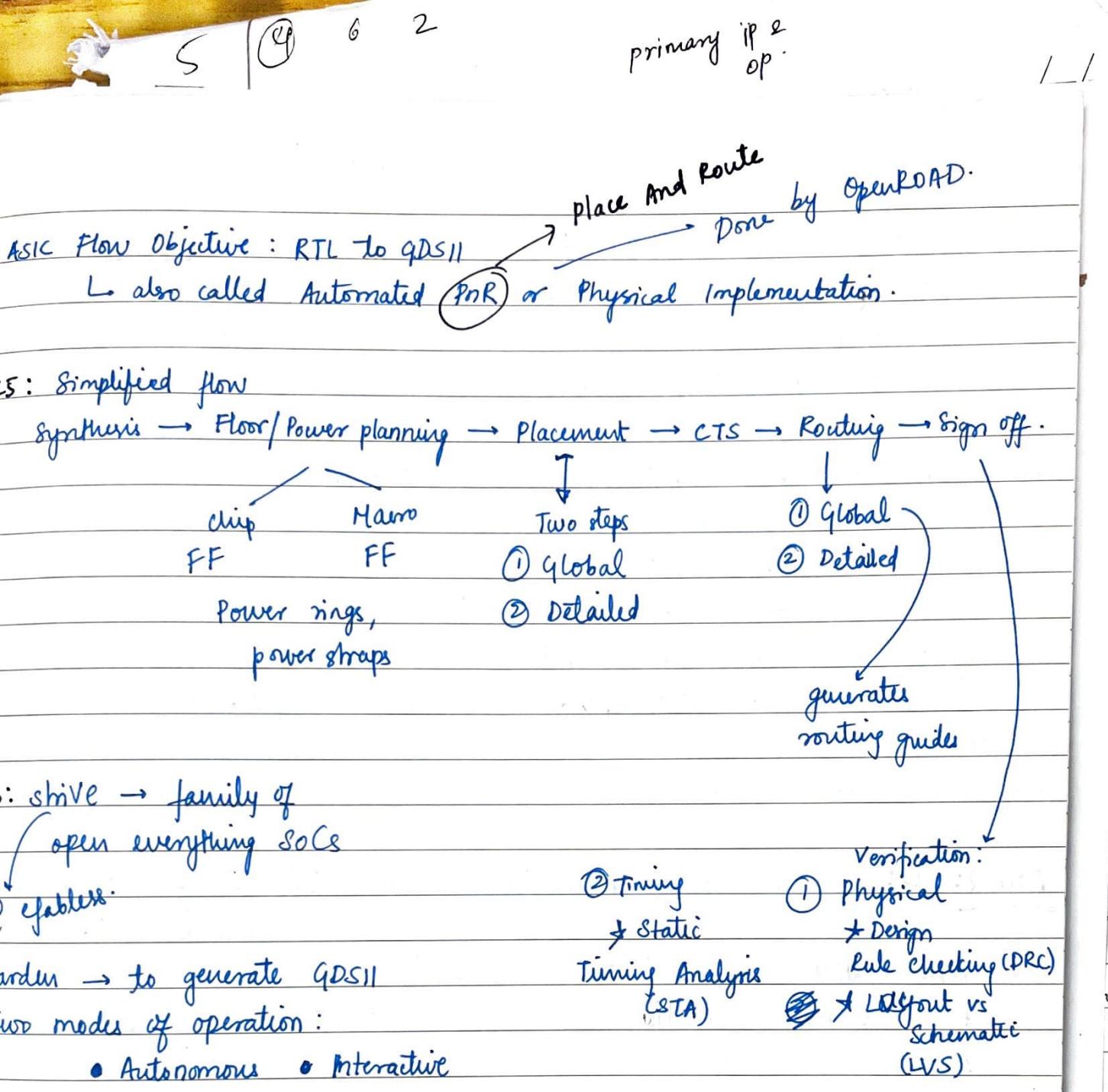


'age of Gods'
Pure Play Fabs
Fabless design companies



PDK → Process Design Kit
↳ interface b/t Fab & designer.

those who controlled physics controlled the creative agenda.



Fake Antenna Diode

Dealing with Antenna Rules Violations

Two solutions:

- * Bridging
- * Add antenna diode

'less' to open & view

files
process & to
exit.

Labs: ① Exploring OpenLANE directory structure.

② Design preparation step.

explore files under design folder.
→ docker
→ flow.tcl - interactive
→ package require openlane 0.9
→ ~~design~~ prep - design picorv32a.

Flop ratio → Task 1.

Day 2: 4: chip floor planning considerations — utilization factor & aspect ratio.

To define width and height of core & die.

* Begin with a netlist

Eg: FF → Combo → FF
logic

* Given H & W of SC,

compute area occupied by each cell

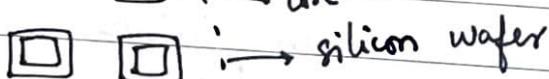
[AND]
[OR]

* logical cells occupies complete area of the

core → 100% utilization.

Core → section of the chip where fundamental logic of the design is placed.

Die → consists of core, a small semiconductor material specimen on which the fundamental circuit is fabricated.



Ideal case: 50% to
60% utilization.

utilization factor = $\frac{\text{area occupied by netlist}}{\text{total area of the core}}$

aspect ratio = $\frac{\text{Height}}{\text{Width}}$

$AR = 1 \rightarrow \text{chip is square shaped.}$

L2: Concept of pre-placed cells.

* Take a complex combinational logic \rightarrow divide it into simpler blocks.

* Extend IO pins * Make the blocks as black boxes
* Separate the black boxes as two different modules.
adv: modules are implemented independently, thus replication becomes easier.

* Arrangement of IP's in a chip \rightarrow Floorplanning

* IP's / blocks \rightarrow user-defined locations

're-used modules'

↓
hence called
pre-placed cells.

placed in chip before automated placement & routing.

L3: Decoupling capacitors.

Location for pre-placed cells are chosen based on the design scenario. Once fixed, it is not modified during automated PnR. & other following cells.

Pre-placed cells should be surrounded with decoupling capacitors.

Why de-coupling capacitors are reqd.?

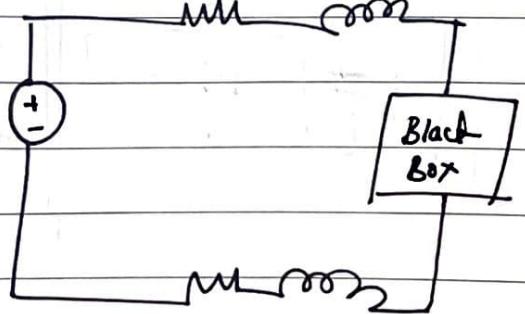
Assume the given circuitry.

Black box distant from the power supply \rightarrow power supply

Wiring introduces C, R & L \rightarrow voltage drop \rightarrow

might not be sufficient to support the noise

Sol: De-coupling cap. margin.



De-coupling capacitor → Huge

↳ charged capacitor → equivalent to V_{DD} (supply)

De-coupling capacitor 'de-couples' the circuit from the intended supply.

Whenever a switching activity occurs in the digital logic, C_D provides the necessary current.

placed
closer to BB
physically.

RL network is used to replenish
the charge into C_D .

4: Power Planning

ground bounce → bump in the ground tap point.

Assume an inverter

ip : 1110010111000110

op : [000] 110 [1000] 111/091

all these capacitors discharge
simultaneously

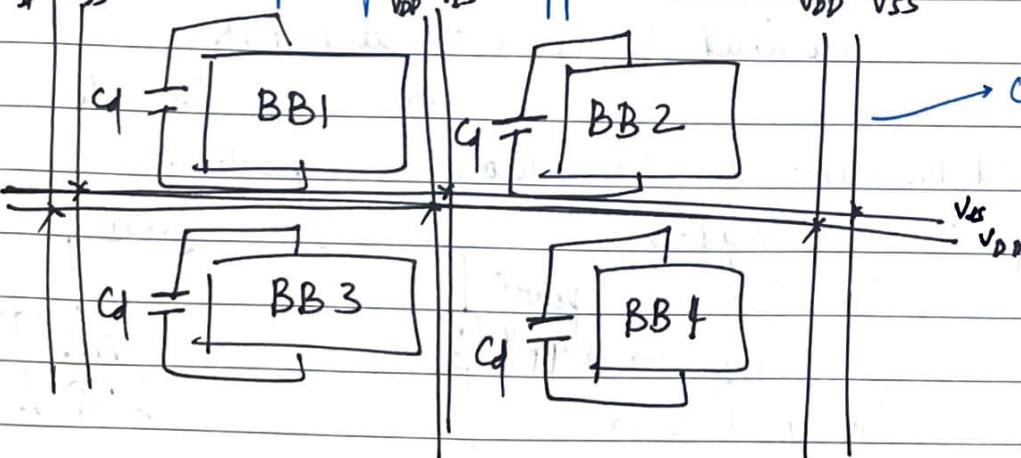
All the
0's will

can cause the busses to enter an undefined state.

charge to 1, demanding current from the same V_{DD} line leading
to 'voltage Droop'.

sol: multiple power supplies

V_{DD} V_{SS}



→ called as the
mesh.

LS : Pin Placement

space b/t core & die → pins.

netlist → connectivity information between the gates coded using verilog/VHDL.

Logical cell placement blockage → to make sure no cells are placed in the area b/t die & core

Lab:

openlane / configuration :

open floorplan.tcl

lowest priority

openlane / designs / pi000v32a.

config.tcl → next priority.

sky130A... → highest priority.

10-METAL → one more than the set value.

run - floorplan.

[magic -T path leg ref] illustrate priority.
def ref }

Review floorplan layout in magic

press Z, then V → to bring layout to center

'S'
↳ to select object

①

Bind netlist with physical cells.

library → a place where all kinds of

cells are found.

↳ basic modules.

also contains the information regarding those cells.

also provides cells with different sizes (various).

decap → endcap
same.

tap cells → to avoid CMOS latch-up.

latch-up.

L7:

② Placement → do a rough placement using the positions of 10 ports.

③ Optimize placement → estimate wire length and capacitance, and based on that, insert repeaters.

↳ to maintain signal integrity.

18: → Final optimization → using setup timing analysis (ideal clock).

19: Flow explanation
Intro to library characterisation & modeling

PDN → post CTS.

Lab: run - placement

congestion aware placement using
REPLACE

(global then detailed)
legalisation: → no overlap b/t cells.
reduces wire length. Half parameter
wire length.

4.0: Cell Design Flow

Inputs

Design steps

* PDKs
* DRC & LVS rules
* SPICE models
* library & user-defined rules.

circuit design

layout design

characterisation

outputs

* CDL
(circuit description language) file

* QDSII
* LEF
* .cir file

Lambda band
design rules.

$\lambda = 42$
 \hookrightarrow minimum
feature size.

Layout Design
Euler's path
stick diagram

extracted
spice netlist

metal layers
supply voltage

Characterisation steps:

GUNA

- ① Read the model
- ② Read .cir file
- ③ Recognize behaviour of the buffer
- ④ To read sub circuits
- ⑤ Attach necessary power sources
- ⑥ Apply stimulus.
- ⑦ Provide necessary op load capacitance
- ⑧ Provide nec. simulation and

Timing characterization :

Timing threshold definitions

- * slew-low-rise-thr → 20% on the lower end
- * slew-high-rise-thr → 20% on the higher end
- * slew-low-fall-thr
- * slew-high-fall-thr
- * in-rise-thr
- * in-fall-thr
- * out-rise-thr
- * out-fall-thr

Propagation delay $= \frac{\text{time}}{\text{out-thr}} - \frac{\text{time}}{\text{(in-thr)}}$ Take 50%.

Transition time : $t(\text{slow-high-rise}) - t(\text{slow-low-rise})$

$t(\text{slow-high-fall}) - t(\text{slow-low-fall})$

Day 3: 10 Place → supports 4 modes.

resetting env. variables can be done on the terminal while using the interactive mode.

4: SPICE deck creation for CMOS inverter

- ↳ connectivity info
 - ↳ ip stimulus decks
 - ↳ tap points for taking op component values.
 - ↳ identify and name nodes.
- supply voltages
usually kept as the multiple of 'L'.

MosFET (M1) Drain gate substrate source model W L

capacitor node1 node2 value.

comments *** ***

Vdd node1 node2 value.

sim under & & &

.op

dc vin 0 0.5 0.05
step size.

and include model file.

.end

Switching threshold V_m → inverter robustness.

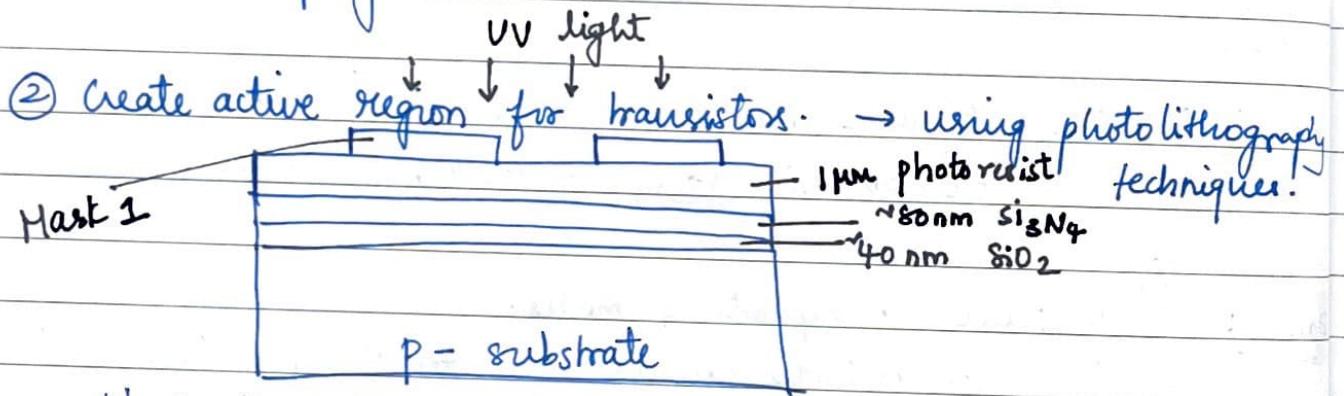
github repo: vslstdcelldesign

copy tech file to this folder.

Inception of layout:

16 - mask CO₂S process.

- ① Selecting a substrate p-type high resistivity ($5 \times 10^{15} \Omega\text{m}$)
★ substrate doping doping level (10^{15} cm^{-3})
should be less than orientation (100)
well doping.



Next step: Remove photoresist

Bird's
beak

* Remove Si_3N_4 (etched)

* Remove resist chemically

* Placed in oxidation furnace. (isolation area is formed)

Field oxide is grown

This process is called as 'LOCOS'.

* Etch out Si_3N_4 using hot phosphoric acid

local oxidation
of silicon.

Phosphorus
doped
n-well
~100 eV.

for PMOS

for N-MOS

- ③ N-well and P-well formation → both cannot be done @ the same time.

* Apply photoresist

* Apply Mask 2

* Apply Boron (P-well)

Ion implantation ~200 keV.

Repeat
same for
N-well
(Mask 3)

$7+5+4+5$
 one shot.
 $3+3+4$ → one shot.

The structure is taken into a high temp furnace (diffusion furnace)

↳ causes drive-in diffusion → depth of the

Process is referred to as : Twin Tub process. well increases (half of substrate)

④ Formation of gate.

2 important terms for gate formation :

$N_A \rightarrow$ doping concentration } controls V_t .

$C_{ox} \rightarrow$ oxide capacitance

gates for PMOS and NMOS are formed separately.

* Photoresist

* Mask 4, UV light

* Introduce boron with low energy (~ 60 keV)

NMOS

* Mask 5, UV light

* Arsenic, low energy. → controls doping concentration.

PMOS

* To fix oxide (damaged C_{ox} of implantation)

etch the oxide using HF solution

re-grown again to give high quality oxide

* $\sim 0.4\ \mu m$ polysilicon layer

* gate should have low resistance, dope with

control oxide capacitance

n-type ion implantation

* Photoresist & Mask 6
(polysilicon)

* remove Mask, remove polysilicon, remove photoresist.

⑤ Lightly Doped Drain (LDD)

N-well: P+, P-, N-

P-well: N+, N-, P+

why? ⑥ Hot electron $\rightarrow E = V/d$

when $d \downarrow$, $E \uparrow \Rightarrow 2$ effects

① Si-Si bonds broken
due to high energy

② 2eV barrier b/w Si

short channel effect

↳ drain field penetrates channel area.

conduction band & SiO_2 band

MASK 7 Phosphorous \rightarrow N- implant

MASK 8 Boron \rightarrow P- implant

Next: $\sim 0.1 \mu\text{m}$ of Si_3N_4 or SiO_2 \rightarrow plasma anisotropic etching
/ \hookrightarrow over the entire structure
side-wall spaces.

⑥ Source and drain formation \rightarrow add a thin layer of ~~screen~~ oxide
 \hookrightarrow to prevent channeling during implants

MASK 9 \rightarrow N+

NMOS \rightarrow Arsenic 75keV energy reqd. then MASK 10

PMOS \rightarrow Boron 50keV "

\hookrightarrow P+

Placed in high temperature furnace \rightarrow \downarrow ?
high temp. annealing

⑦ To form contacts and interconnects (local)

Step 1: Remove screen oxide using HF solution.

2: Deposit titanium on wafer surface using sputtering

3: Wafer heated @ 650-700°C

in N_2 ambient for a minute

fit Ti with Ar^+ (Argon) gas.
Ti molecules vapourize and settle

\downarrow

$\xrightarrow{\quad}$ TiSi_2 \rightarrow low resistant

$\text{TiN} \rightarrow$ only for local communication

4: Mask II \rightarrow sources and one of the drain is coming out.

Unwanted TiN is etched off using RGA cleaning

\hookrightarrow A solution.

5 parts deionised water

1 part NH_4OH

1 part H_2O_2

⑧ Higher level metal formation to reduce temp.

Step 1: 1 μm of SiO_2 doped with phosphorous or boron deposited on wafer surface.

↳ why?

P acts as a protection for the Na ions that are present in SiO_2 .

2: Chemical Mechanical Polishing (CMP)

↳ to planarize the wafer surface.

3: MASK 12 → certain areas protected

→ etch off SiO_2 to drill contacts

4: Remove photoresist. Deposit ~10nm TiN

↳ 2 reasons

5: Deposit blanket Tungsten layer

a) — layer of SiO_2

b: Do CMP.

b) — layer for bottom

7: Deposit Aluminium layer. MASK 13 to protect

interconnects

contacts that is to be taken off out.

Etch off unwanted Al. (plasma etched)

SiO_2 → CMP → MASK 14 to define holes → TiN deposition → Tungsten

MASK 15

/ to define pattern
thicker (for Al)

Bottom → Top
Thickness of metal layers increases.

Top dielectric → Si_3N_4 → to protect the chip

Al.

MASK 16 to bring out contacts.

14:35