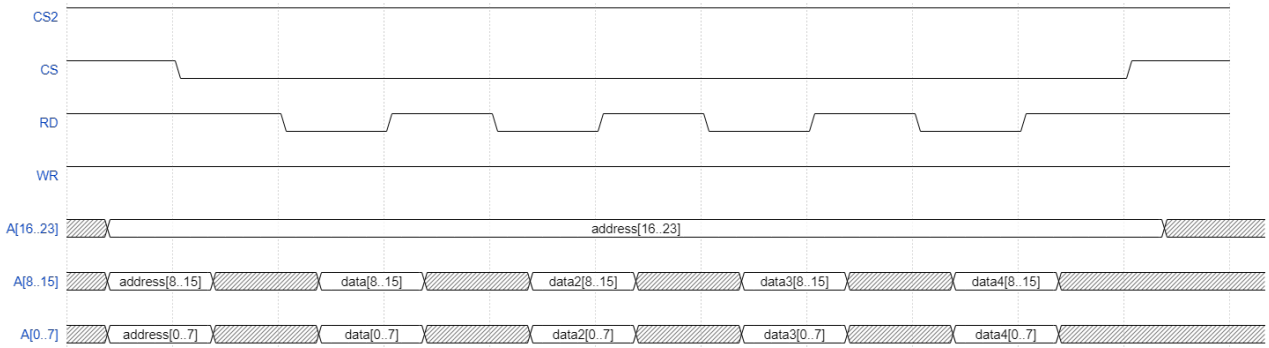
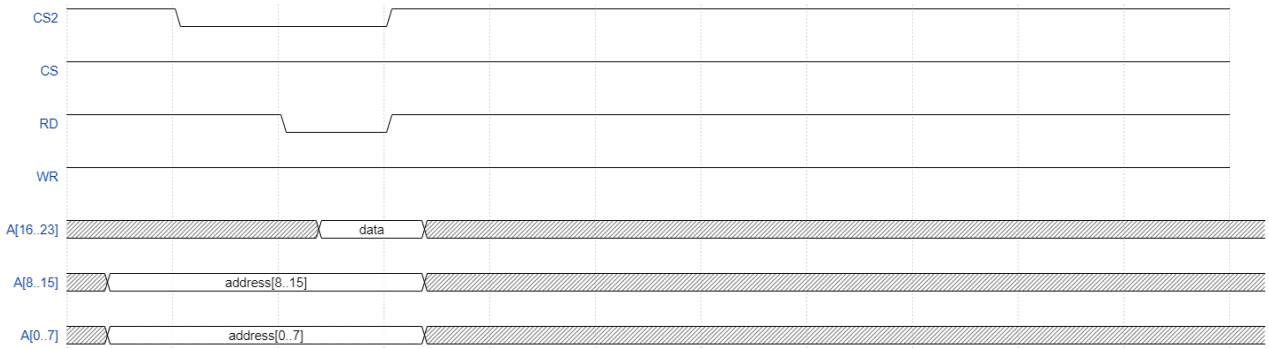
Read ROM

First the two least significant of address have to be latched (CS, falling edge), so the pins A0..15 can be used by the cartridge to send data (RD, falling edge). Any subsequent falling edge of RD (with CS still set to 0) will signal the cartridge to send next 16 bits (the address will be automatically incremented inside). It is important to note that the most significant byte of address should be kept correct at all times by the dumper.



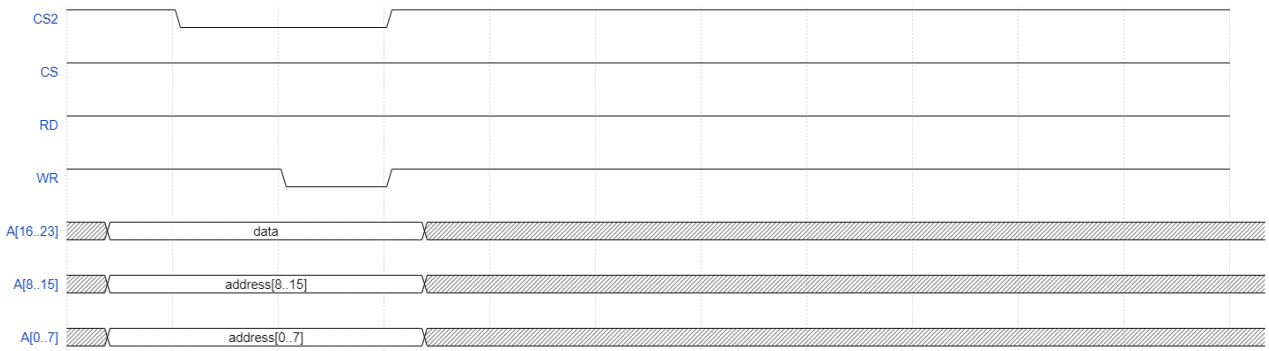
Read RAM

The procedure is very simple, falling edge of CS2 selects RAM. The address should be sent by the dumper via pins A0..15, while pins A16..23 should be in a high impedance state. Falling edge of RD signal the cartridge to sent the data byte (pins A16..23). CS2 should be kept low during the entire process.



Write to RAM (sRAM)/Send a command to RAM (flash)

The data byte and the address should be prepared first on pins A0..23. Then CS2 should be switched to 0 (RAM chip select) and after some time, WR should be lowered as well. The falling edge will send the command to the RAM chip.



RAM commands (flash, from the official MX29L1611 datasheet)

Command Sequence		Read/ Reset	Silicon ID Read	Page/Byte Program	Chip Erase	Sector Erase	Erase Suspend	Erase Resume	Read Status Reg.	Clear Status Reg.
Bus Write Cycles Req'd		4	4	4	6	6	3	3	4	3
First Bus Write Cycle	Addr	5555H	5555H	5555H	5555H	5555H	5555H	5555H	5555H	5555H
	Data	AAH	AAH	AAH	AAH	AAH	AAH	AAH	AAH	AAH
Second Bus Write Cycle	Addr	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH
	Data	55H	55H	55H	55H	55H	55H	55H	55H	55H
Third Bus Write Cycle	Addr	5555H	5555H	5555H	5555H	5555H	5555H	5555H	5555H	5555H
	Data	F0H	90H	A0H	80H	80H	B0H	D0H	70H	50H
Fourth Bus Read/Write Cycle	Addr	RA	00H/01H	PA	5555H	5555H			X	
	Data	RD	C2H/F8H	PD	AAH	AAH			SRD	
Fifth Bus Write Cycle	Addr				2AAAH	2AAAH				
	Data				55H	55H				
Sixth Bus Write Cycle	Addr				5555H	SA				
	Data				10H	30H				

Command Sequence		Sector Protection	Sector Unprotect	Verify Sector Protect	Abort
Bus Write Cycles Req'd		6	6	4	3
First Bus Write Cycle	Addr	5555H	5555H	5555H	5555H
	Data	AAH	AAH	AAH	AAH
Second Bus Write Cycle	Addr	2AAAH	2AAAH	2AAAH	2AAAH
	Data	55H	55H	55H	55H
Third Bus Write Cycle	Addr	5555H	5555H	5555H	5555H
	Data	60H	60H	90H	E0H
Fourth Bus Read/Write Cycle	Addr	5555H	5555H	*	
	Data	AAH	AAH	C2H*	
Fifth Bus Write Cycle	Addr	2AAAH	2AAAH		
	Data	55H	55H		
Sixth Bus Write Cycle	Addr	SA**	SA**		
	Data	20H	40H		