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KEY SKILLS

Embedded programming in C and assembler

- ✓ Expert in low-level C programming.
- ✓ Expert in assembly programming for a number of CPUs.
- ✓ Have worked to MISRA-C standard and can adapt to tighter rule sets and methodologies.
- ✓ Can build test harnesses with C, Python or Matlab as appropriate, on host or on target.
- ✓ Familiar with most Test Driven Development techniques.

Programmable logic design on FPGAs

- ✓ Able to design efficient digital logic and to map that design onto a variety of FPGA architectures using vendor-agnostic VHDL.
- ✓ Alternatively, can develop to the features of a particular device (e.g. Xilinx DSP48 block).
- ✓ Frequent user of Xilinx and Altera synthesis tools.

Programmable logic verification

- ✓ Can devise crafty, effort-effective solutions to verification and testing problems.
- ✓ Will not hesitate to develop custom SW tools when needed, including models for hardware devices.
- ✓ Experienced user of Modelsim for functional simulations.

PERSONAL OPEN-HARDWARE PROJECTS ON FPGA

1. Synthesizable CPU core: Intel 8051 compatible CPU: (*http://opencores.org/project,light52*). *(Finished)*.
    - Smallest practical free 8051 core around, not far behind low-end commercial cores.
    - Dhrystone benchmark score equivalent to a 6-clocker MCS51.

2. Synthesizable CPU core: Intel 8080 compatible CPU: (*http://opencores.org/project,light8080*). *(Finished).*
    - Tested for 100% binary compatibility to original silicon.
    - Tried with original, vintage software – Microsoft's Altair 8080 Basic.

3. Synthesizable CPU core: MIPS-I (R-3000) compatible CPU: (*http://opencores.org/project,ion*). *(Work in progress)*.
    - Best area/performance ratio of any free MIPS core; includes I/D direct-mapped caches.
    - Tried with port of Don Woods' '*Adventure*'. DRAM support missing yet.

- These are the smallest CPU cores in their respective categories. I know how to optimize a logic design for area.
- Made with a minimal expenditure of development effort.
- Co-simulation with SW models of the CPUs – 8051 and MIPS SW simulators included.
- I can supply other samples of my work with FPGAs including some DSP stuff – fixed-point FIR or DDS blocks, small floating point ALU, etc.

RELEVANT EMPLOYMENT HISTORY

Embedded software engineer — Sepsa (Madrid) — Jun/11 - Jun/12

As an embedded programmer my job was to maintain and develop small rail-borne embedded systems.

Projects and roles

1. Maintenance of existing projects.

   I did maintenance work on a number of existing rail-borne systems. These are small boards based on OS-less microcontrollers, usually C166 derivatives.
   I had the opportunity to work with all kind of HW devices: large LED matrix displays, Ethernet PHYs, NMEA GPS interfaces...

2. Firmware for emergency brake controller – critical system, SIL-2 level under EN-50128.

   Built on a XE164 16-bit CPU in plain C with no RTOS, this small system controls an emergency brake interconnected to the main car computer over an RS-485 link using a proprietary protocol.
   I was responsible for 100% of the software, in all stages of development:

   - Drew the SW specs from the system specifications.
   - Designed the SW and implemented it.
   - Defined the SW tests and the SW-HW integration tests.
   - Built an ad-hoc infrastructure for the automation of the tests – repurposed HW controlled by a Python library written by me.
   - Wrote a traffic logger in Python for the propietary RS-485 protocol as a diagnostic tool.
   - Implemented the SW tests in Python, using aforementioned infrastructure.

   Being a SIL-2 level project, all the above tasks entailed extensive documentation.

Embedded SW / FPGA programmer — GCM (Madrid) — Nov/07 - Jul/10

In this small R&D startup I wrote or co-wrote the software for a number of telecomms prototypes: PLC, WDSL and satellite link modems, plus a power line telemetry device. Running on ARM7 and TI DSPs, mostly.
I doubled as FPGA logic designer and made the FPGA-based link layer common to some of the systems.

Projects and roles

1. WDSL2+ modem prototype

   This is a technology demonstrator for an improved WDSL2+ physical layer (and also used in some other related projects) implemented on two Virtex-4 FPGAs and an ARM7 microcontroller running uClinux.

   - I developed the link layer for the modem in VHDL, using Xilinx synthesis tools. Including GMII interface, FEC cores, external CPU interface and IRQ controller, diagnostic logic, etc.
     Plus an automatic test bench in VHDL running on Modelsim.
   - Thanks to the effort spent in verification, the logic needed hardly any on-board debugging.
   - I wrote a custom bootloader, two drivers (character and block) for access to the underlying FPGA hardware and a few small user space applications – for example, a real-time line equalization filter calculator.

2. Power Line Communications modem prototype

   PLC modem implemented in software on a TMS320F28335 DSP.

- I wrote a small signal processing library in assembler, implementing the whole physical layer of the system: Golay correlators, FIR filters, QAM modulator/demodulator, etc.
  The algorithms were tailored to our specific requirements and maximally efficient in execution time – I squeezed every last cycle out of the DSP.

3. Power Line Telemetry device

   The purpose of the device is to estimate the transfer function of a segment of power line and transmit that information periodically to a base station, using PLC techniques.

   The demonstration platform was a TMS320C6748 development board on which the system was implemented entirely in software – about 9KLOC of C (floating point).

   - I built the floating-point, deferred-time signal processing application on a C6748 DSP.
   - Made a hardware abstraction layer for dual-targetting: the code can be run on the real target board and on a regular Linux PC -- this saves lots of development time.
   - Also built a test rig in Matlab for on-host tests: generation of test signals and validation of solutions, all automated.

Senior programmer – Java/JSP web servers Aubay (Málaga) Dec/06 - Oct/07

I did maintenance on a very large Java/JSP web application for Telefónica -- Struts on Oracle.

Programmer – Java/JSP web servers Islanda (Málaga) Mar/05 - Aug/06

Maintenance of web applications for a number of different projects and clients. Mostly Java/JSP on Struts and Hibernate frameworks.
I reached senior programmer level and became inhouse expert for Hibernate.

Development Engineer Dyctel (Madrid) Dec/00 - Sep/02

I contributed to starting a small virtual telephone operator (*reseller*) servicing other companies within the Dragados group. I did all kind of tasks from installation of diallers to embedded programming (in Speed, Kreatel's custom language) or redaction of service manuals.
I left the job (after all technical difficulties had been overcome) in order to finish my studies.

EDUCATION AND TRAINING

BS in Telecommunications Engineering (Esp. Electronic Systems).
Final year project: Hopfield neural network on FPGA (fixed point vectorial numeric computation with sparse matrices on Altera Stratix)

TOEIC English Language certification (score 980).
Plus Official spanish language school title (5 year degree).

Course: Java for web applications (jan/05, 400h).

I regularly attend vendor seminars and workshops, too numerous to list here. The last one was X-Fest Madrid 2012 event (Avnet/Xilinx).