José Antonio Ruiz Domínguez
Pza. Juana de Coello, 5 1A – 28320 Pinto (Madrid, Spain)
ja_rd@hotmail.com / (+34) 645-571-591

RELEVANT EXPERIENCE AND SKILLS

Embedded programming in C and assembler

- Experience with uClinux including custom bootloader, drivers (character and block) and small user space applications – all for a WDSL modem prototype.
- Built a floating-point, deferred-time signal processing application on C6748 DSP – about 9KLOC of plain C, no RTOS. Project can be compiled for real target or for Linux platform for test purposes (dual targetting) and includes Matlab code for test data generation and validation of solutions.
- Specified, designed and programmed the firmware for a small rail-borne subsystem (SIL-2 security level). Including *on-host* and *on-target* test frameworks using C, Python and some custom HW.
- Programmed fixed-point signal processing library for F28027 DSP in assembler (Golay correlators and other uncommon functions not available in vendor libraries).
- Numerous other embedded projects on a variety of 8-, 16- and 32-bit CPUs over a 4 year period.

- ✓ Have worked to MISRA-C standard and can adapt to tighter rule sets and methodologies.
- ✓ Can build test harnesses with C, Python or Matlab as appropriate, on host or on target.
- ✓ Familiar with most Test Driven Development techniques.

Programmable logic design on FPGAs

- Developed link layer for WDSL modem prototype on Virtex-4 FPGA. Including GMII interface, FEC cores, external CPU interface and IRQ controller, diagnostic logic, etc.
- Built a number of synthesizable CPU cores for FPGA as open hardware personal projects.

- ✓ Able to design efficient digital logic and to map that design onto a variety of FPGA architectures using vendor-agnostic VHDL.
- ✓ Alternatively, can develop to the features of a particular device (e.g. Xilinx DSP48 block).
- ✓ Frequent user of Xilinx and Altera synthesis tools.

Programmable logic verification

- Built automatic test bench in VHDL on Modelsim for aforementioned link layer project.
- Developed *co-simulation* test bench for open hardware CPU cores. Including creation and/or modification of CPU software simulators for MIPS-I and 8051 CPUs.

- ✓ Can devise crafty, effort-effective solutions to verification and testing problems.
- ✓ Will not hesitate to develop custom SW tools when needed, including models for hardware devices.
- ✓ Experienced user of Modelsim for functional simulations.

PERSONAL OPEN-HARDWARE PROJECTS ON FPGA

1. Synthesizable CPU core: Intel 8051 compatible CPU: (*http://opencores.org/project,light52*). *(Finished)*.

2. Synthesizable CPU core: Intel 8080 compatible CPU: (*http://opencores.org/project,light8080*). *(Finished).*

3. Synthesizable CPU core: MIPS-I (R-3000) compatible CPU: (*http://opencores.org/project,ion*). *(Work in progress)*.

EDUCATION AND TRAINING

BS in Telecommunications Engineering (Esp. Electronic Systems).

Final year project: Hopfield neural network on FPGA (fixed point vectorial numeric computation with sparse matrices on Altera Stratix)

TOEIC English Language certification (score 980).

Plus Official spanish language school title (5 year degree).

Course: Java for web applications (jan/05, 400h).

I regularly attend vendor seminars and workshops, too numerous to list here. The last one was this year's X-Fest Madrid event (Avnet/Xilinx).

EMPLOYMENT HISTORY

Embedded software engineer — Sepsa (Madrid) — Jun/11 - Jun/12

I maintained several embedded applications in C running on bare-metal C166 processors.
I developed a small application (C on XE164) for which I made the software specification and design, the implementation and the SW test environment. This is a SIL-2 level project involving extensive documentation and testing.

Embedded SW / FPGA programmer — GCM (Madrid) — Nov/07 - Jul/10

In this small R&D startup I wrote the firmware for a number of telecomms prototypes: PLC, WDSL and satellite link modems, plus a power line telemetry device. Running on ARM7 and TI DSPs, mostly.
I doubled as programmable logic designer and made the FPGA-based link layer common to some of the prototypes.

Senior programmer – Java/JSP web servers — Aubay (Málaga) — Dec/06 - Oct/07

I did maintenance on a very large Java/JSP web application for Telefónica -- Struts on Oracle.
A pleasant and very demanding but uneventful job.

Programmer – Java/JSP web servers — Indra (Málaga) — Sep/06 - Nov/06

Hired for a project that was cancelled before starting, before leaving I had time to adapt for our purposes an Eclipse plugin for Java style rule checks. Left for lack of in-house work.

Programmer – Java/JSP web servers — Islanda (Málaga) — Mar/05 - Aug/06

Maintenance of web applications for a number of different projects and clients. Mostly Java/JSP on Struts and Hibernate frameworks.
I reached senior programmer level and became inhouse expert for Hibernate

Development Engineer — Dyctel (Madrid) — Dec/00 - Sep/02

I contributed to starting a small virtual telephone operator (*reseller*) servicing other companies within the Dragados group. I did all kind of tasks from installation of diallers to embedded programming (in Speed, Kreatel's custom language) or redaction of service manuals.
I left the job (after all technical difficulties had been overcome) in order to finish my studies.