FPGA 2018 -project – Zedboard XADC external voltage measurement and serial plotting with laptop

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The idea of the project is to measure an external voltage and plot it in laptop with a serial plotter-program. The project was done as part of master's thesis in company yyy with instrument xxx. Voltage of interest comes from the instrument, after the current has been conversed to voltage and amplified. Project demonstrates how to use Zedboard and laptop as a simple oscilloscope. The system is presented at Figure 1.

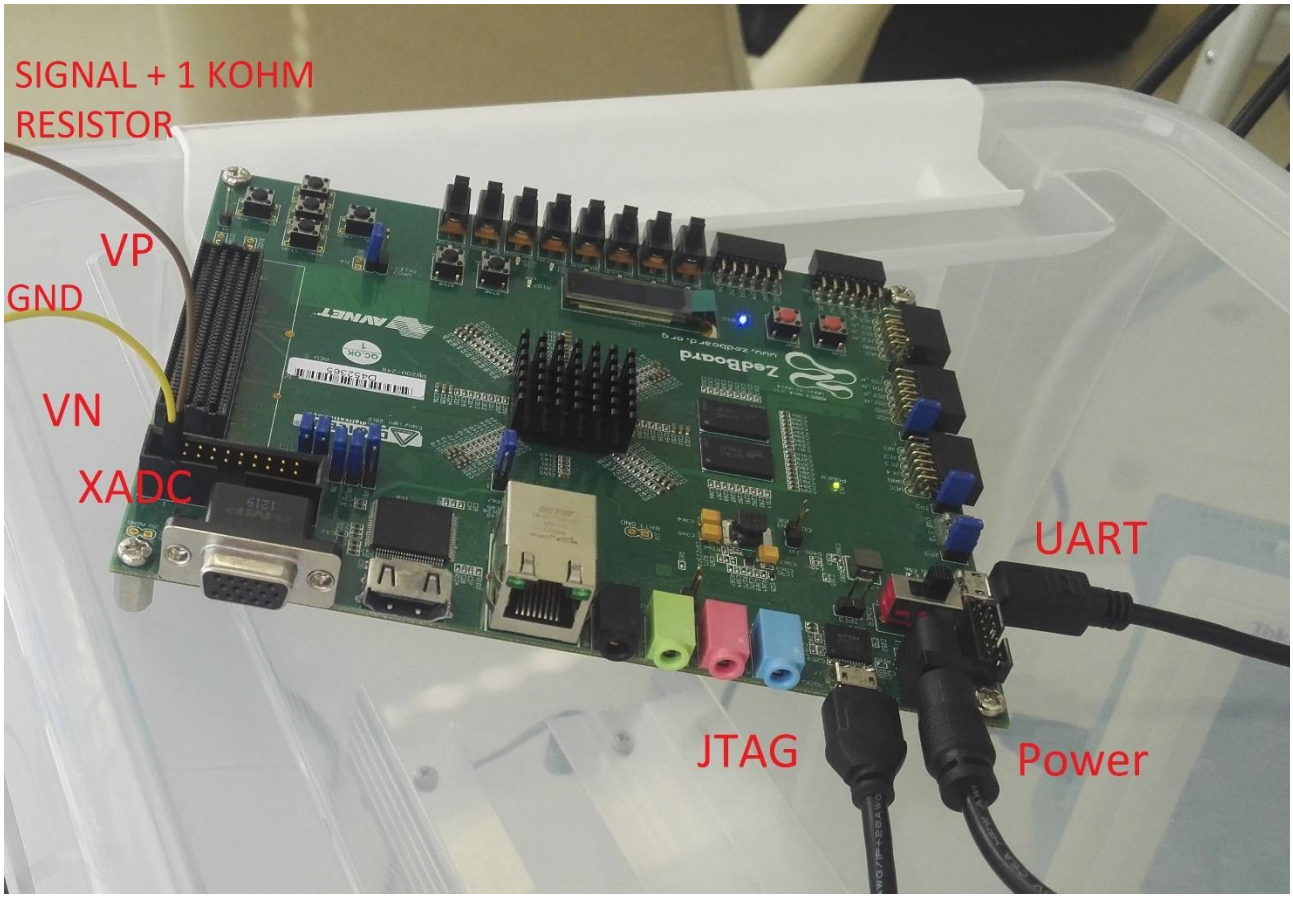

Figure 1 Measurement system. VP pin of XADC is connected to input gate of ADC inside the instrument, through 1 kohm resistor. VN pin of XADC is connected to GND of instrument. FPGA is connected to laptop with UART to transmit the serial signal for plotting. JTAG is used for configuring FPGA.

Project is based on couple of online tutorials:

1) http://zynqhowto.blogspot.com/2014/03/zynq-how-tolab3.html and
2) https://forums.xilinx.com/t5/Xcell-Daily-Blog/Adam-Taylor-s-MicroZed-Chronicles-Part-104-XADC-with-Real-World/ba-p/659668; https://forums.xilinx.com/t5/Xcell-Daily-Blog/Adam-Taylor-s-MicroZed-Chronicles-Part-107-Combining-XADC-and/ba-p/664734

XADC is an analog mixed signal module. It is a hard macro, and has interfaces for JTAG and DRP for accessing the status and control registers in the Xilinx 7-series. It has dual 12-bit 1 MSPS ADCs with effective input signal bandwidth of 500kHz, which were utilized in the design.

XADC's mixed-signal performance is quite good, with a minimum 60-dB signal-to-noise ratio and 70 dB distortion according to data sheet. It also supports used selected averaging. Often, XADC is used for internal system monitoring as it has e.g. multiple auxiliary channels, internal voltage and temperature measurement and alarms. XADC internal structure is presented at Figure 2.

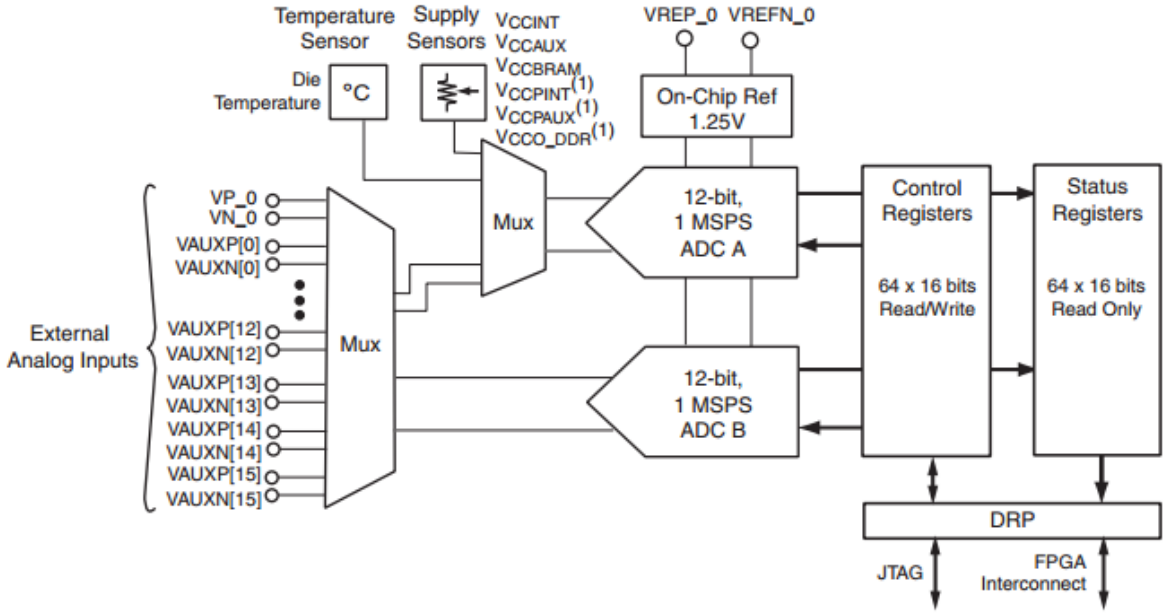

Figure 2 XADC internal structure. VP and VN ports were utilized in the design. XADC communicates through FPGA Interconnect with AXI4-Lite interface.

XADC pin mapping can be found from Figure 3.

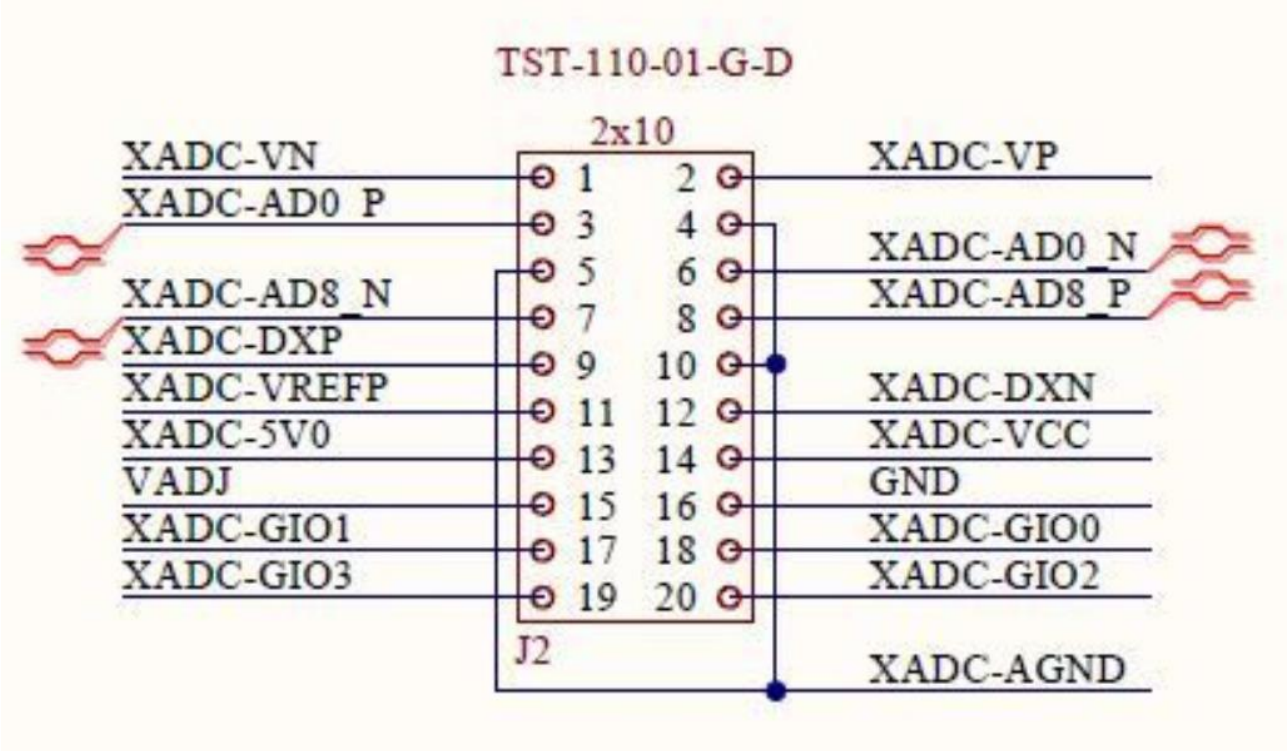

Figure 3 XADC pins

First, a block design was created with Vivado, including XADC wizard -ip block (Figure 3) according to 1) tutorial. It has capability for also auxiliary voltage channels (vaux0 and vaux8) measurements. XADC is connected to Processing subsystem through AXI-interface. AXI-interconnect connects PS to XADC, with PS acting as master for interconnect, and interconnect acting as master for XADC.

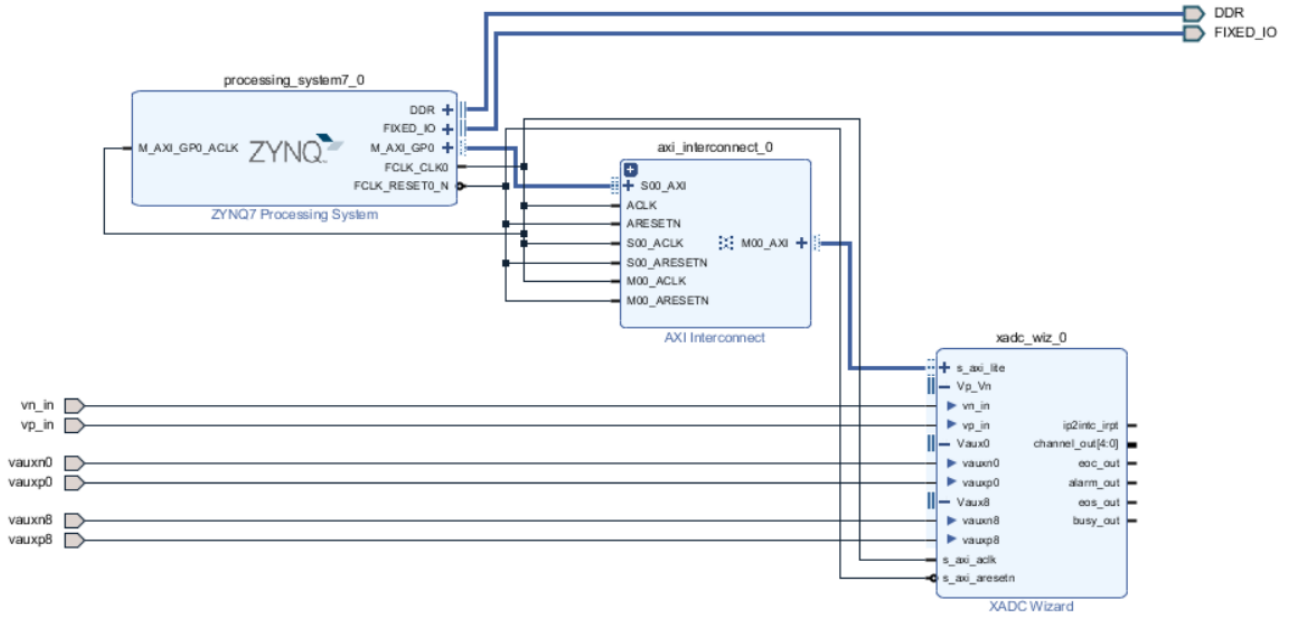

Figure 4 First block design, according to tutorial 1). XADC is connected processing system through AXI-interface.

XADC timing is set to continuous and startup channel selection as channel sequencer. Sequencer mode is set to continuous and channel averaging to 16. Also, ADC, sensor offset and gain calibrations and well calibration averaging are applied. XADC is measuring at unipolar mode at default.

This block design is generated and wrapped to HDL-code, and bitstream is created with Vivado. This bitstream is exported to Xilinx SDK. Already made C-code is used from tutorial 1), with slight modifications. Only VP/VN measurement is used, and there is no sleep time in the continuous loop. Sysmon.h-drivers are used to access the XADC measurements through AXI-interface. This measurement is then printed through serial port UART-USB to laptop, and *Serial-Oscilloscope-v1.5*-program is used to plot the signal.

Second block design utilizing AXI-timer, and XADC interrupts is built latency in mind. This way we can be sure not to miss any XADC-sample. ISR-latency was defined in 2) tutorials, and it was found that there is a significant margin. Timer interrupt is compare to XADC interrupt to be sure of the sufficient margin. Block design is presented at Figure 5.

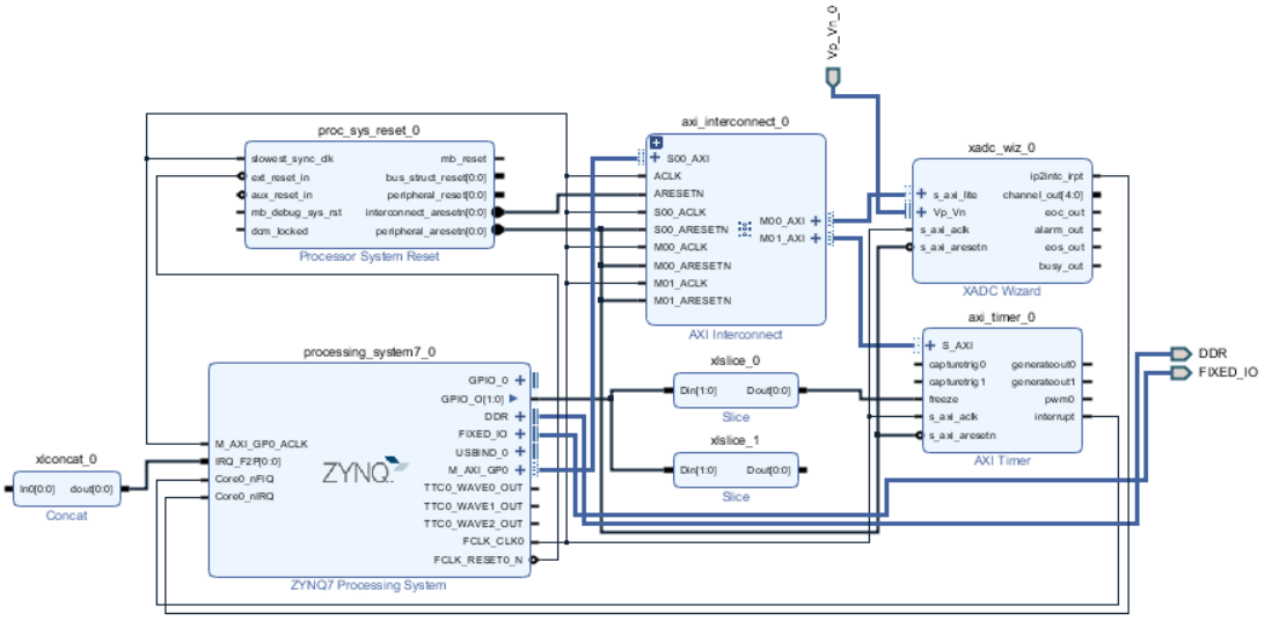

Figure 5 Second block design with timer and synchronous reset included. Interrupts are used for XADC measurements. According to tutorial 2).

This design is also transferred to bitstream and exported to SDK. There is an already made c-code for testing in https://github.com/ATaylorCEngFIET/MicroZed-Chronicles. Again, slight modifications are made for the code to do continuous measurements. Interrupt is not disabled after 64 samples, and the measurements are plotted through UART. XADC-measurement has the same configurations as in first design.

VP/VN has the maximum measurement range of 1 V. It was noticed that instrument generates over 1.5 V spike when it's turned on/off. XADC VP/VN channel has max upper limitation of 1.5 V, so there is possibility that this can cause damage to the Zedboard. This is the reason, a resistor is used in between signal source and VP to mitigate the effect. It was noticed that it's working well to suppress excessive voltage in Figure 6.

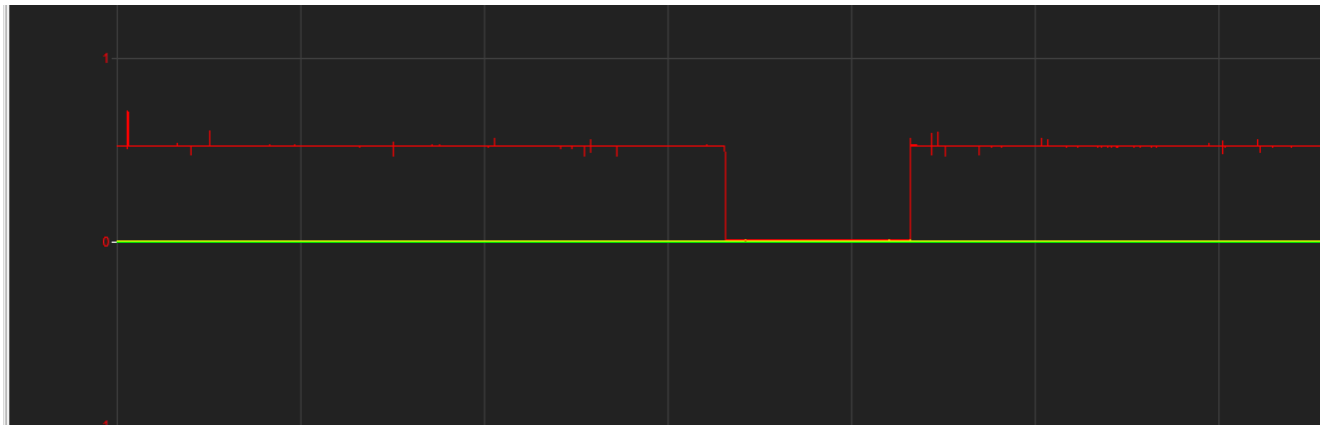

Figure 6 Turning the instrument off and on. The voltage is set to around 500 mV, when instrument in measuring mode. In the picture, it can be easily seen that voltage spike is not dangerous for the XADC.

Serial-Oscilloscope-v1.5 is not the best program to use for plotting the signal, but it is working sufficiently enough to use it as a simple oscilloscope. Background of the signal was plotted also with *SerialPlot*-to acquire better picture of the small oscillation and noise in the signal in Figure 7.

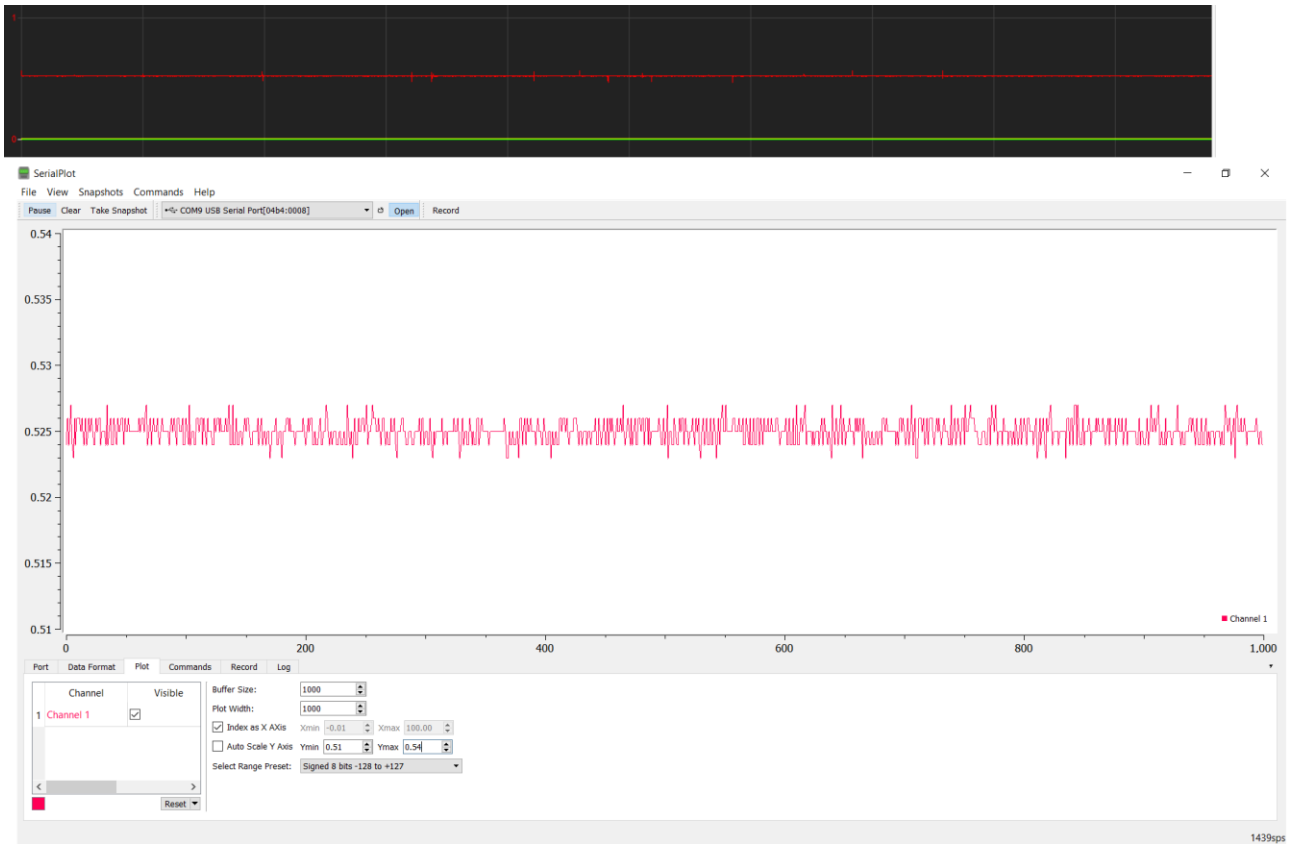

Figure 7 Background of the instrument signal plotted with two serial plotters. Around 5 mV noise in the signal is observed from the picture below. In upper picture, some small spikes can be seen, that are actually individual events measured, that are causing voltage spikes.

An example of the signal coming to ADC in instrument is presented in Figure 8. There can be seen a one spike, that crosses the 1V upper limit of VP/VN XADC measurement. Therefore, it can't

be fully used to specify the signals that individual events cause. Also, this oscilloscope is not functioning as accurately as a dedicated oscilloscope instrument, which can be seen when comparing signals. This may be due to resistor, XADC, FPGA or the serial communication (or everything together), which causes difference compared to straight oscilloscope implementation. However, Zedboard might be a good tool to acquire more information about the noise level in the measurement of instrument. Also, it may be a useful tool to apply signal processing or FFT to build an enhanced oscilloscope.

In Figure 9, there is an idea to develop further. With fir-compiler -ip block and axi-stream interface, some DSP like high-pass filter can be applied to extract elements from the signal. Also, FFT-block could be used. Now, coefficients for high-pass filter were designed with Octave, but the design is not functional.

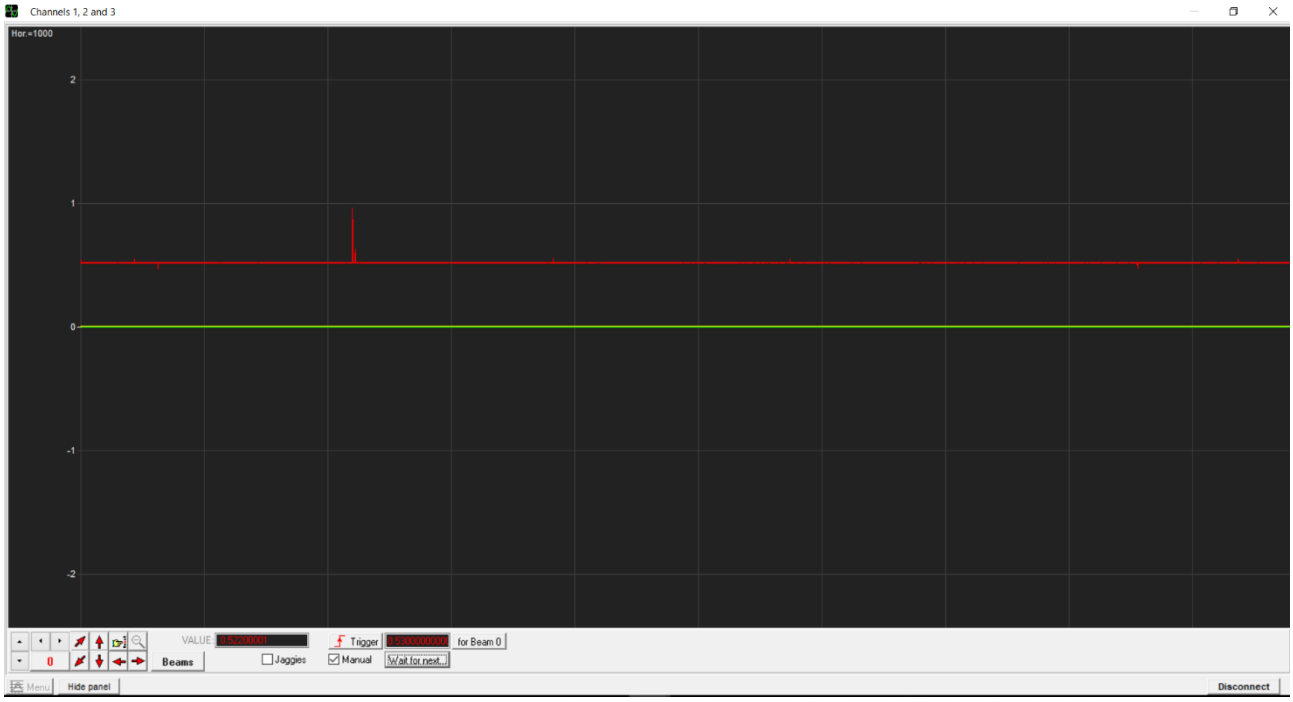

Figure 8 An example of the voltage spike, that individual events causes in instrument. It can be seen, that 1V limit is crossed.

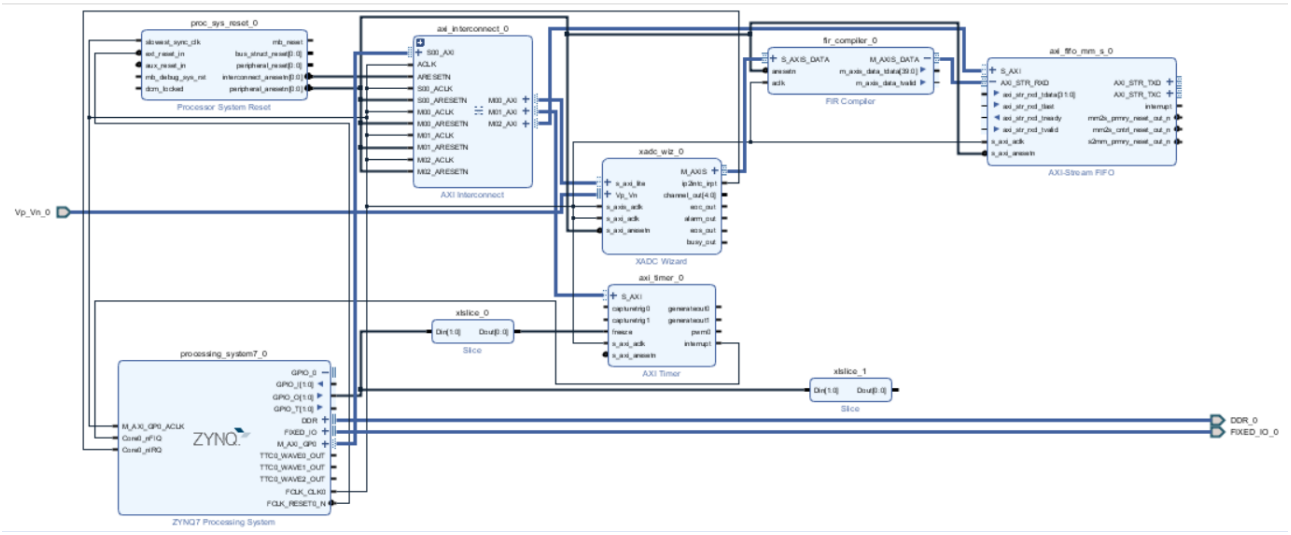

Figure 9 Third block design with fir-filter and AXI4-Stream (concept, not functioning!)