EE 618 (ZELE)

CMOS Aanlog VLSI Design : Tutorial-I

Note: Consider V_{DD}= 3V, V_{Tn} = 0.7 V and V_{Tp} = -0.8 V. Neglect body effect. Assume low frequency small signal model whenever required.

1. Sketch I_X and transconductance ($\frac{\delta I_X}{\delta V_{GS}}$) with respect to V_X for the circuit given in Figure 1, as V_X is swept from 0 to 1.5 V.

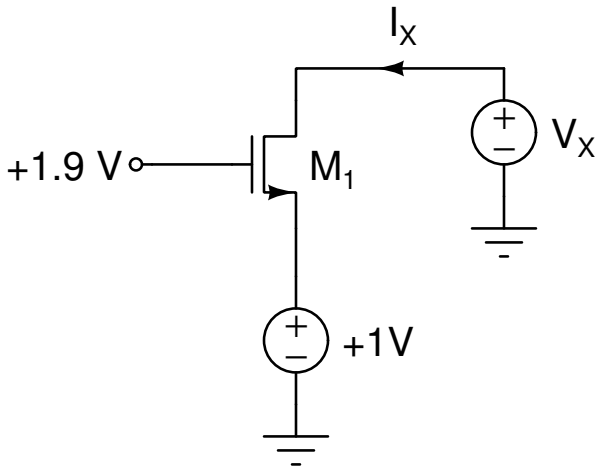

Figure 1

2. Prove that the structure in Figure 2 can be viewed as a single transistor having aspect ratio ($\frac{W}{2L}$). Assume that $\lambda = \gamma = 0$.

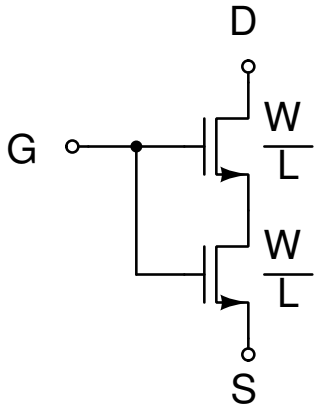

Figure 2

3. Sketch I_X versus V_X for the circuit shown in Figure 3, as V_X varies from 0 to V_{DD}.

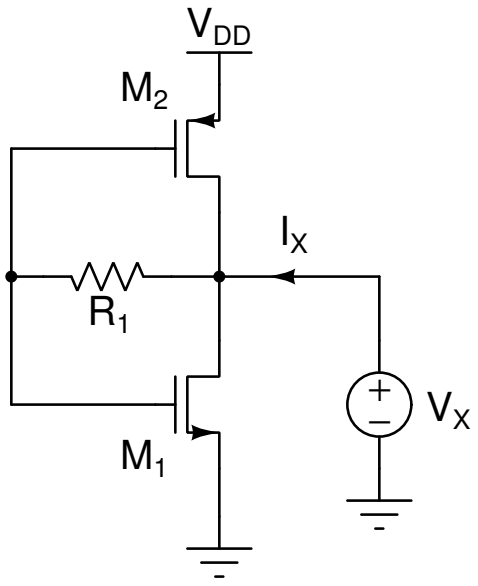

Figure 3

4. Assuming all the transistors are in a saturation, find a small signal voltage gain for the following circuit:

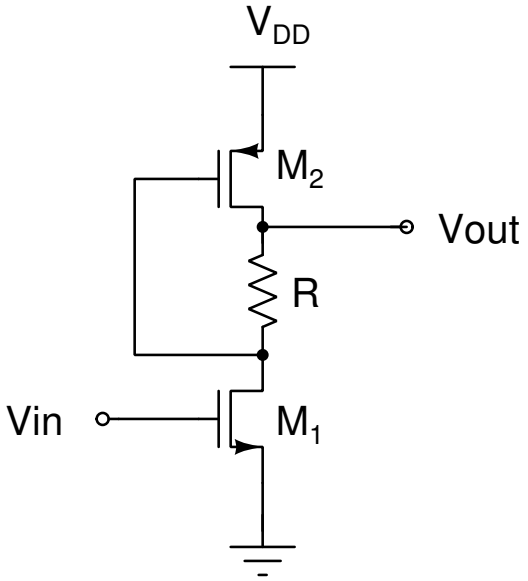

Figure 4

5. Assuming all transistors are in a saturation, find a small signal voltage gain for the following circuits:

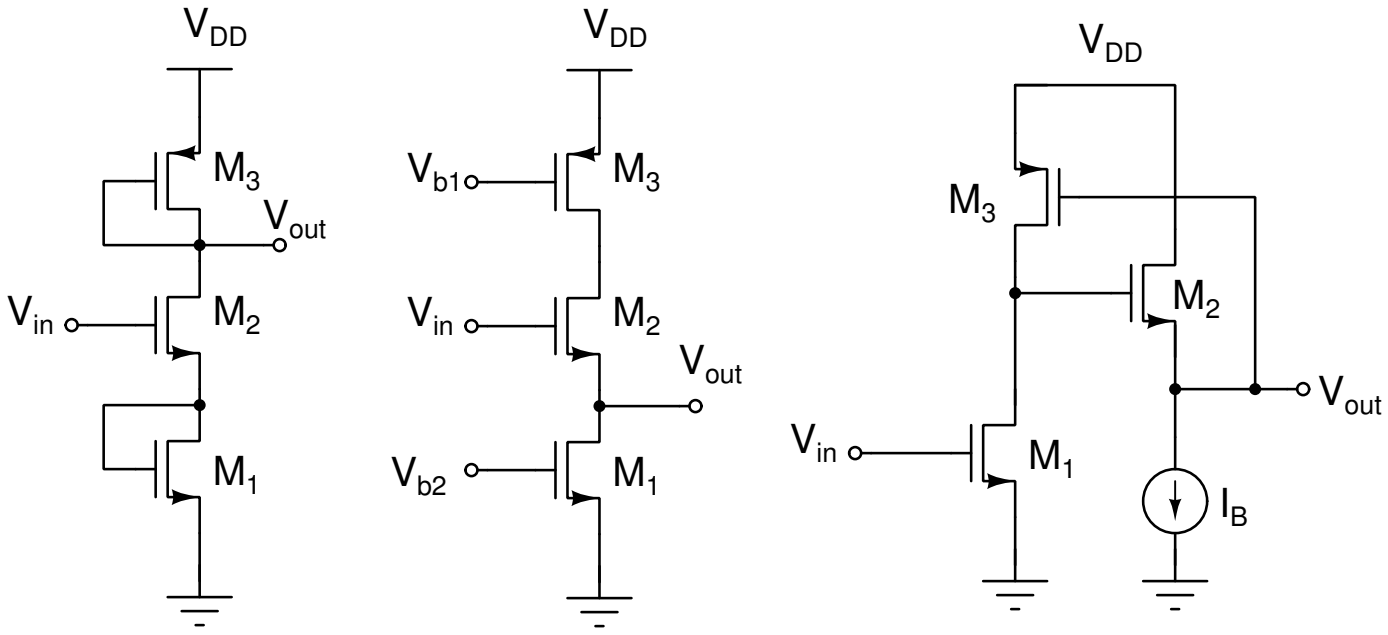

Figure 5 a) b) c)

6. Find the input impedance and transfer function of the circuit in Figure 6. Sketch the gain and phase bode plot.

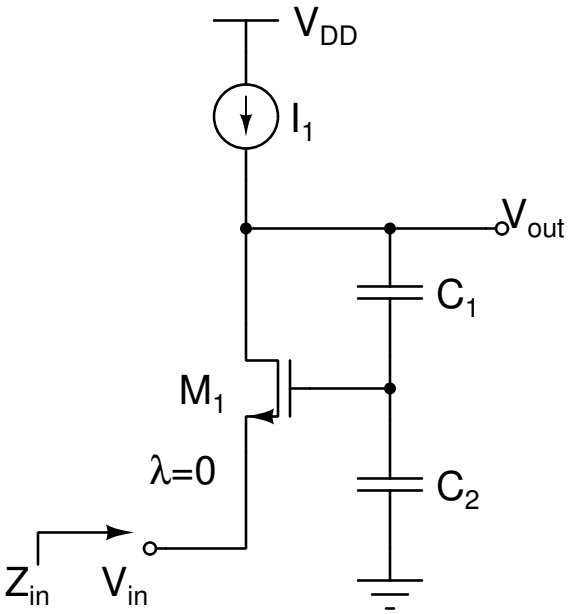

Figure 6