
August 4, 2018
Saturday

EE735: Microelectronics Simulations Lab
Assignment:#1

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Q1.

Procedure

- Enclose the given parallel plate capacitor in a potential box, in this problem the dimensions of the potential box are taken as 3000x500
- One of the plates is kept at 1 V while other one is kept at 0V. Walls of the potential box is kept at 0V;
- Divide the entire box into mesh with grid size = 1nm
- Solve poissons equation in the charge free regions and find potential across all grid points
- To find the electric field take the gradient of the potential across the all grid points
- To find the charge per unit width on the plate, find the total flux emerging out of the plates
- capacitance is given a charge per unit width divided by the capacitance across the plate

Net capacitance per unit Width = 1.072 nF. The simulated capacitance is close to the ideal value $C = (l * \epsilon)/d = 0.885nF$.

Q2.

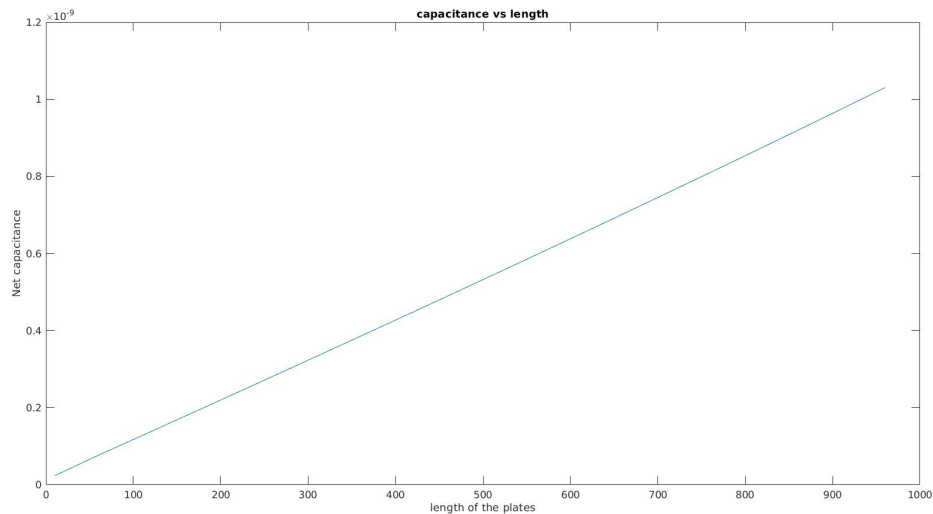


Figure 1: Net capacitance vs length

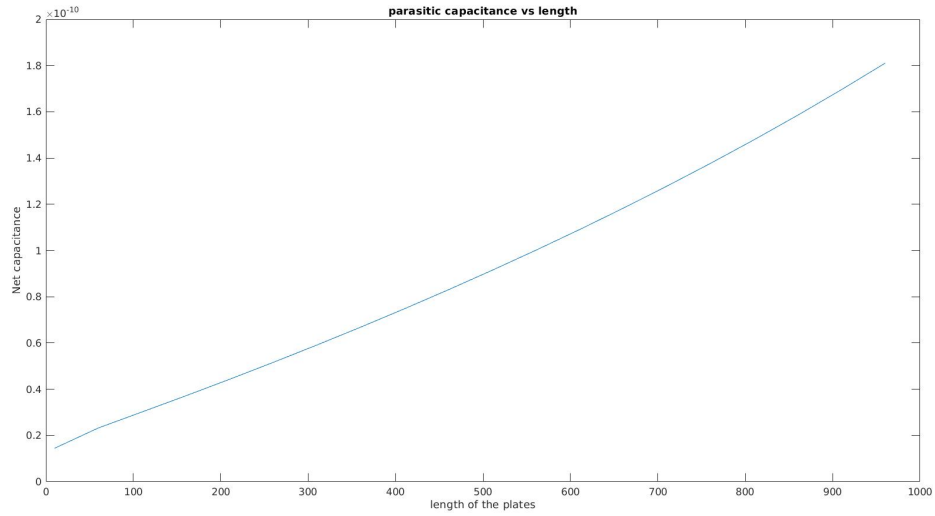


Figure 2: Parasitic capacitance vs length

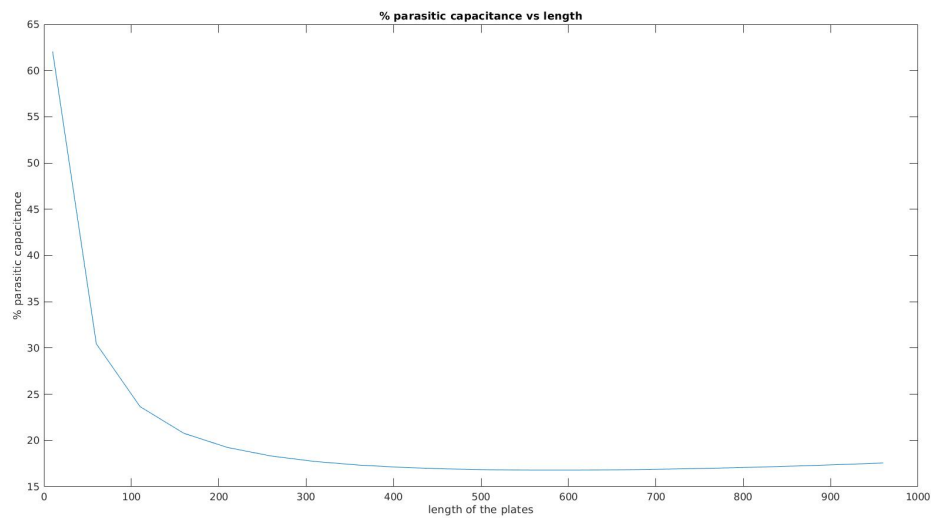


Figure 3: Percentage Parasitic capacitance vs length

As shown in Fig 3 Percentage parasitic capacitance per width decreases with increasing length. As the length of the plates decreases, the fringing of the electric field becomes more dominant adding to the net capacitance.

Q3.

Net capacitance = 29 pF

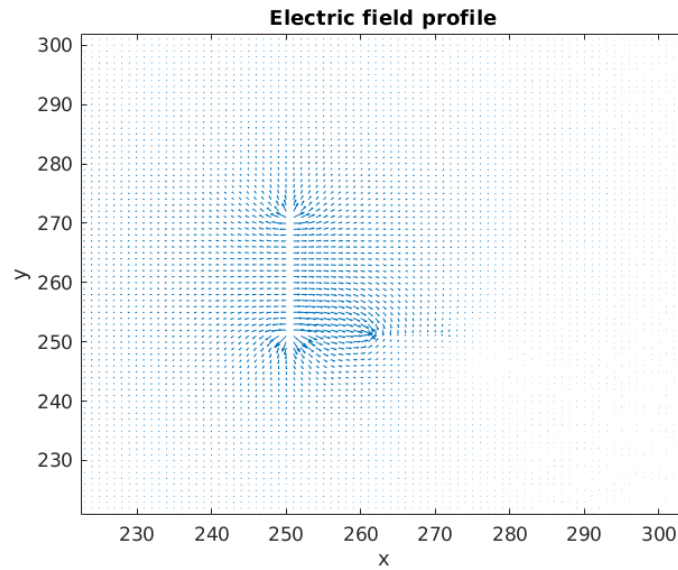


Figure 4: Electric Field Profile $E(x,y)$

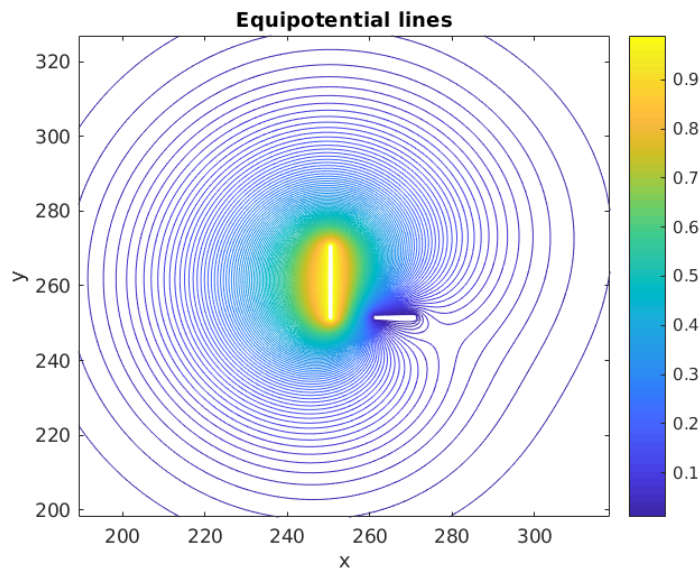


Figure 5: Equipotential lines

Maximum Electric Field : 0.23 V/m. The magnitude of the electric field is maximum at the lower end of the vertical plate which is closer to the horizontal plate. The maximum electric field is directed at angle of 47 deg anti-clockwise from the horizontal axis

File name	Description
cap_solver.m	function to find the net capacitance of a parallel plate capacitor for a given l,d
q1.m	Code for question 1
q2.m	Code for question 2
q3.m	Code for question 3
173079020_vineesh_hw1.pdf	this document

Table 1: Contents of zip file