CONTROL DECODER LOGIC																											
INSTRUCTION	OPCODE	CONDITION	ID.Rd_sel	ID.jal	RR.rs1_sel	RR.src1_sel	RR.src2_sel	RR.Rs_en(BA)	RR.jlr	RR.Br	RR.SW	EXE.Src1	EXE.Src2_1	EXE.Src2_2	EXE.Src2_3	EXE.Oper	EXE.Data	EXE.LW	EXE.Memaddr	MEM.addr_sel	MEM.data_in_sel	MEM.Wr_en	MEM.Rd_en	MEM.data	WB.C_check	WB.Z_check	WB.C_Wr	WB.Z_Wr
ADD	00_00	00	10	0	1	1	00	11	0	0	0	0	0	X	0	0	1	0	X	X	X	0	0	1	0	0	1	1
ADC	00_00	10	10	0	1	1	00	11	0	0	0	0	0	X	0	0	1	0	X	X	X	0	0	1	1	0	1	1
ADZ	00_00	01	10	0	1	1	00	11	0	0	0	0	0	X	0	0	1	0	X	X	X	0	0	1	0	1	1	1
ADI	00_01	XX	01	0	X	1	X	01	0	0	0	0	1	X	0	0	1	0	X	X	X	0	0	1	0	0	1	1
NDU	00_10	00	10	0	1	1	00	11	0	0	0	0	0	X	0	1	1	0	X	X	X	0	0	1	0	0	0	1
NDC	00_10	10	10	0	1	1	00	11	0	0	0	0	0	X	0	1	1	0	X	X	X	0	0	1	1	0	0	1
NDZ	00_10	01	10	0	1	1	00	11	0	0	0	0	0	X	0	1	1	0	X	X	X	0	0	1	0	1	0	1
LHI	00_11	XX	00	0	X	X	10	00	0	0	0	X	X	X	X	X	0	0	X	X	X	0	0	1	0	0	0	0
LW	01_00	XX	00	0	1	1	XX	10	0	0	0	0	1	X	0	1	1	1	X	1	X	0	1	0	0	0	0	1
SW	01_01	XX	XX	0	1	0	01	11	0	0	1	0	1	X	0	1	1	0	1	1	1	1	0	X	0	0	0	0
LM	01_10	XX	11	0	X	1	XX	01	0	0	0	0	X	1	1	1	1	0	X	1	X	0	1	0	0	0	0	0
SM	01_11	XX	XX	0	0	1	00	11	0	0	0	0	X	1	1	1	1	0	1	1	1	1	0	X	0	0	0	0
BEQ	11_00	XX	XX	0	1	1	01	11	0	1	0	X	X	X	X	X	X	0	X	X	X	0	0	X	0	0	0	0
JAL	10_00	XX	00	1	X	X	XX	00	0	0	0	1	X	0	1	1	1	0	X	X	X	0	0	1	0	0	0	0
JLR	10_01	XX	00	0	1	X	00	10	1	0	0	1	X	0	1	1	1	0	X	X	X	0	0	1	0	0	0	0

WB.RegWr
1
1
1
1
1
1
1
1
1
0
1
0
0
1
1