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Friday

EE705 VLSI DESIGN LAB
COURSE PROJECT - 1

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INDIVIDUAL CONTRIBUTION

The project required a little understanding of basic memory architectures. So along with Ranjith, we had undergone some literature review on basic SRAM and DRAM configurations. We also had a look at the basics of 6T and 4T cell configurations and their tradeoff with respect to speed and complexity. This gave us the importance of refresh signals that need to be given to the SDRAM so as to preserve the data even after every read or write cycle. Further looking into the data sheet of the SDRAM memory we have understood that we have an additional advantage of AUTOREFRESH which reduces the programming complexity. Also the ,chapter 8 ,ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS by David A Hodges , clearly explains the sequence in which the row and columnns need to be accessed to read or write data. In reference to this the overall architecture of the code was developed and I was handed with implementation of the READ SEQUENCE .

1.1 READ SEQUENCE

After the initialisation sequence ,the SRAM is in the idle state ad is waiting for the read or write signals from the host . A read sequence is initiated with the read activate command. The host sends in a 24bit address , where the last 9 bits correspond to a column address the next 13 bits to a row address and the first two MSB bits correspond to the bank select bits.
Once the address is received by the conroller the controller decodes the bank activate bits and selects the bank from which the data is to be read . The corresponding row to be accessed is selected by initially enabling the RAS pin and then passing the 13 it row address. This sequence is then followed by a nop command and then the required column is accesed by enabling the CAS command. Once the data is latched on to the data bus the control signals are set so to pull the output buffers to low impedance state .The auto precharge command is enabled by the status of the A10 address pin . The foolowing figure shows the timing sequence required for the READ SEQUENCE.

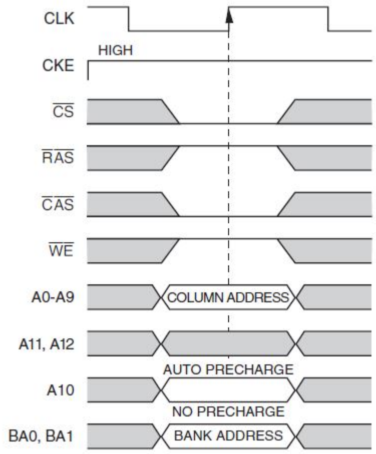

Figure 1: READ SEQUENCE