May 4, 2018	**EE705:VLSI Design Lab**	***C P Rahul***
Friday	**COURSE PROJECT**	***Roll No:173079030***

SDRAM CONTROLLER

INDIVIDUAL CONTRIBUTION

I have written the code for the auto refresh which has to be done to keep the data intact in the memory. Auto refresh has to be done in every 64ms. That is, once a row is refreshed, it has to be again refreshed after 64ms. 13 Row bits represents, 8k Rows. So $64\text{m}/8\text{k} \approx 7.8\mu s = 390$ clock cycles (for 50MHz) is the interval between the refresh of each Rows. But in case, for the second refresh of a row after 64ms if the there is a process going on(ie, the controller is busy) then the refresh has to be delayed till that process is completed which might lead to loss of data in that row. So in order to accommodate this, we take the interval 380 cycles instead of 390 so that the next refresh of a raw will be happening in around 62.2ms which will give us enough time to delay the refresh without loosing the data.

The auto refresh cycle is given below

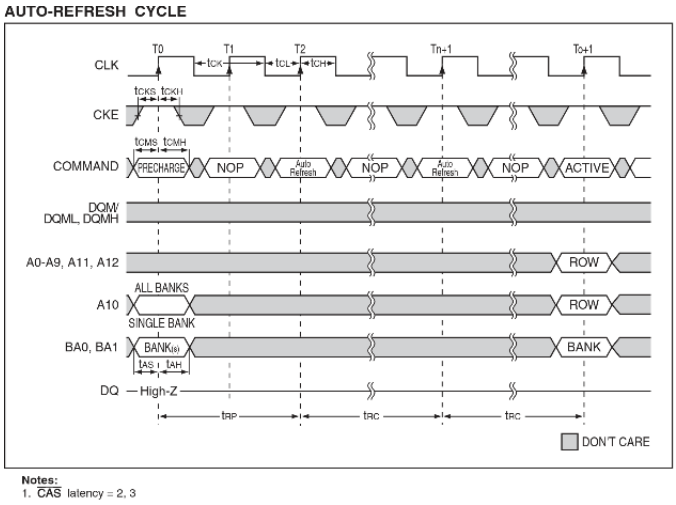

Figure 1: Auto refresh Cycle

I also added the entire SDRAM controller module as a component in the Qsys and interface it with NIOS II.Few changes in the components like adding waitrequest signal was also added in the component to make the design compatible with the Avalon interface.The complete setup was test in NIOS II Software Build Tool for Eclipse after writing the C code.