INDIVIDUAL CONTRIBUTION

The project was divided into various submodules. While Adarsh and Ranjith were going through the literature survey and sequence of control signals required for the writing and reading the data into and from memory, me and Rahul stringently went through the SRAM data sheet. I was given the task of setting up the memory before the write and read process could start.I also had to setup the counters required for the delays after each read and write cycle and build the testcases to ensure proper functioning of the SRAM controller under worst cases

1.1 INITIALIZATION

This was the challenging block I had to build so as to ensure proper read and write . Once powered up the SRAM has to be initialized before any read or write sequence . The following figure shows the timing requirement for the initialization sequence.

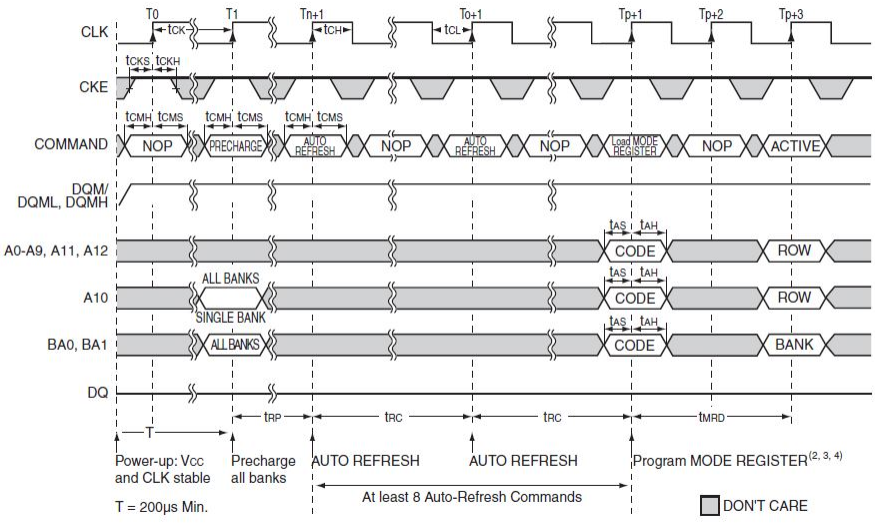

Figure 1: INITIALIZATION TIMING SEQUENCE

To ensure that after proper cold start, 200μ should be allocated for proper settling of the clock and supply. During this the SRAM controller should provide NOP(no operation signals only) . The cold start is followed by precharge cycles and then by 8 auto refresh cycles. A counter has been implemented in the count to keep track of the refresh cycles. The refresh commands are followed by the load mode register set command which sethe latency, burst mode opration and other modes of opeartion.
The codes for the same were developed and simulated using a testing bench and the timing parameters were verified.