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Sunday

EE705 VLSI DESIGN LAB
COURSE PROJECT - 1

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INTRODUCTION

The project mainly aims to implement a controller for the on-board 32MB SDRAM. Th memory is organized into 4 banks , each bank thus having a memory allocation of 8MB, which further translates to 8192 rows and 512 columns per bank .
Once powered up The SRAM has to undergo an initialization cycle, during which neither read or write cycles are responded to . The controller has to provide the necessary no operation commands followed by a sequence of precharge commands and then the mode register set command.It is the mode register that defines the operation of the SDRAM.After the initialization cycle the memory is ready to read and write data . Hence the controller gives the read and write signals. The implemented controller uses the AUTO REFRESH command of the SDRAM . The following are some of the features of the SRAM controller:

- CAS(latency)=3 when operating at frequency =100MHz.
- After the initialisation sequence controller waits for read or write requests from the host side.
- Once a read or write request s encountered the next request will be processed after nly 5 clock cycles
- Read and write cycle are single read and write processes. The memory has as additional feature of burst read and write modes which are not being used
- The refresh cycle used is AUTO REFRESH ,where 8192 rows are refreshed every 64ms.

The FSM for the read ,write,refresh and initialisation cycles are as shown below:

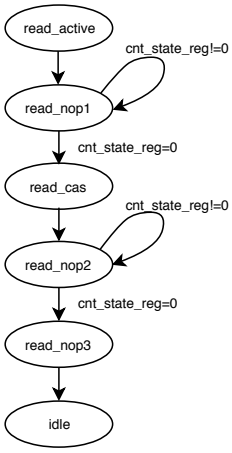

Figure 1: READ FSM

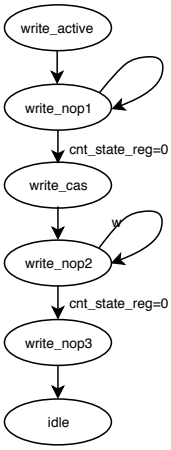

Figure 2: WRITE FSM

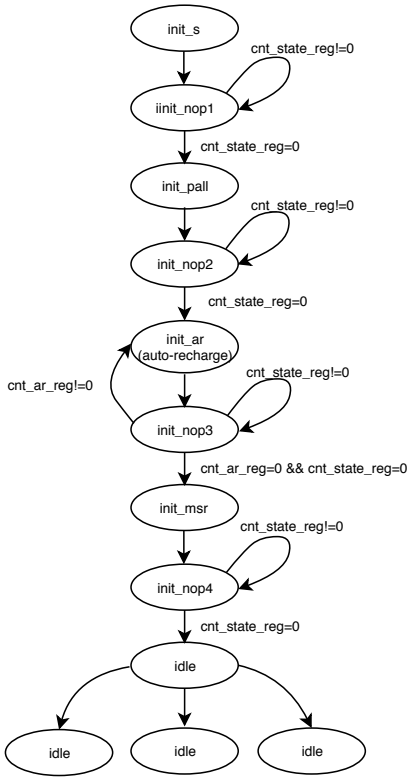

Figure 3: INITIALISATION FSM

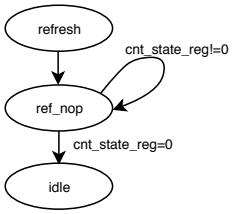

Figure 4: REFRESH SEQUENCE FSM

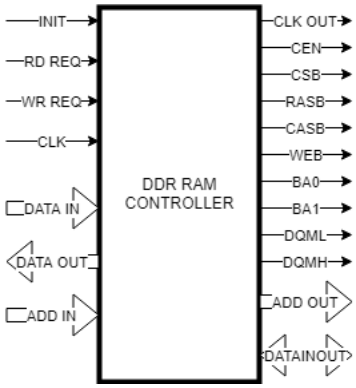

Figure 5: BLOCK DIAGRAM OF THE CONTROLLER

1.1 INITIALIZATION

Once powered up the SRAM has to be initialized before any read or write sequence . The following figure shows the timing requirement for the initialization sequence.

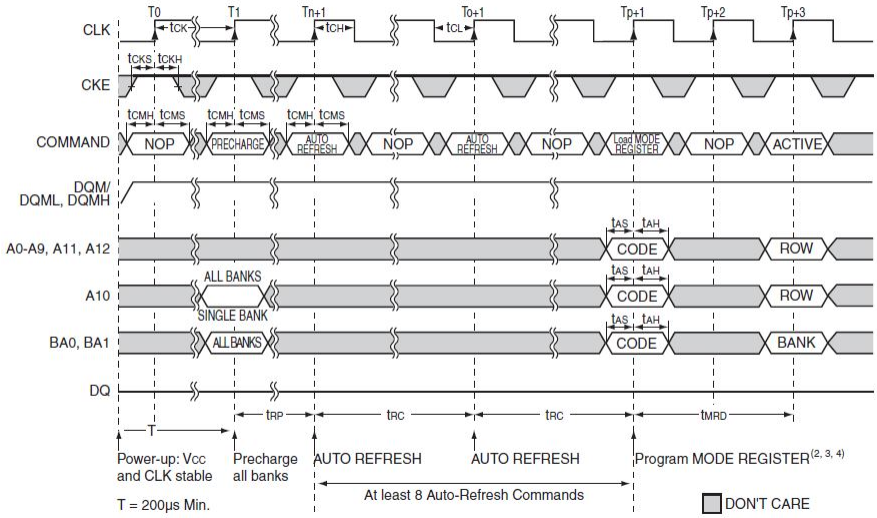

Figure 6: INITIALIZATION TIMING SEQUENCE

To ensure that after proper cold start, 200μ should be allocated for proper settling of the clock and supply. During this the SRAM controller should provide NOP(no operation signals only) . The cold start is followed by precharge cycles and then by 8 auto refresh cycles. A counter has been implemented in the count to keep track of the refresh cycles. The refresh commands are followed by the load mode register set command which sethe latency, burst mode opration and other modes of opeartion.
The codes for the same were developed and simulated using a testing bench and the timing parameters were verified.

1.2 READ SEQUENCE

After the initialisation sequence ,the SRAM is in the idle state ad is waiting for the read or write signals from the host . A read sequence is initiated with the read activate command. The host sends in a 24bit address , where the last 9 bits correspond to a column address the next 13 bits to a row address and the

first two MSB bits correspond to the bank select bits.
Once the address is received by the controller the controller decodes the bank activate bits and selects the bank from which the data is to be read . The corresponding row to be accessed is selected by initially enabling the RAS pin and then passing the 13 it row address. This sequence is then followed by a nop command and then the required column is accessed by enabling the CAS command. Once the data is latched on to the data bus the control signals are set so to pull the output buffers to low impedance state .The auto precharge command is enabled by the status of the A10 address pin . The following figure shows the timing sequence required for the READ SEQUENCE.

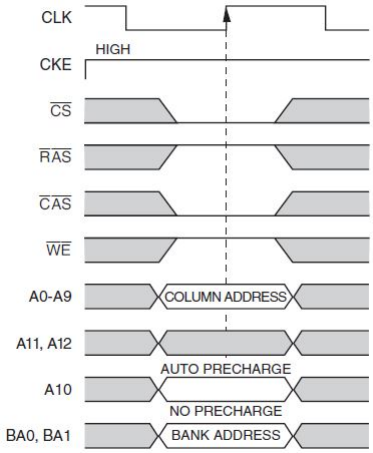

Figure 7: READ SEQUENCE

1.3 WRITE SEQUENCE

In the Idle state, Writing can be done by giving a write request. If the $wr\_req = 1$, the Bus will be activated and the next state will be $write\_act$ where the 13 bit ROW address(bits 21 to 9) a well as the two bit bank address(MSBs) is passed. Followed by the proper number of NOPs($write\_nop1$), in the next state ($write\_CAS$) the column address(9 LSBs) is passed(CAS =1).This state is also followed by some NOPs (corresponding to the CAS Latency).

1.4 AUTO REFRESH

Auto refresh has to be done in every 64ms. That is, once a row is refreshed, it has to be again refreshed after 64ms. 13 Row bits represents, 8k Rows. So 64m/8k $\approx 7.8\mu s = 390$ clock cycles (for 50MHz) is the interval between the refresh of each Rows. But in case, for the second refresh of a row after 64ms if the there is a process going on(ie, the controller is busy) then the refresh has to be delayed till that process is completed which might lead to loss of data in that row. So in order to accommodate this, we take the interval 380 cycles instead of 390 so that the next refresh of a raw will be happening in around 62.2ms which will give us enough time to delay the refresh without loosing the data.The SDRAM controller was interfaced with the neos processor to send read and write requests to the memory. The testbenches for the same has also been attached

Results RTL

2.1 Start Init sequence after 200 μs delay

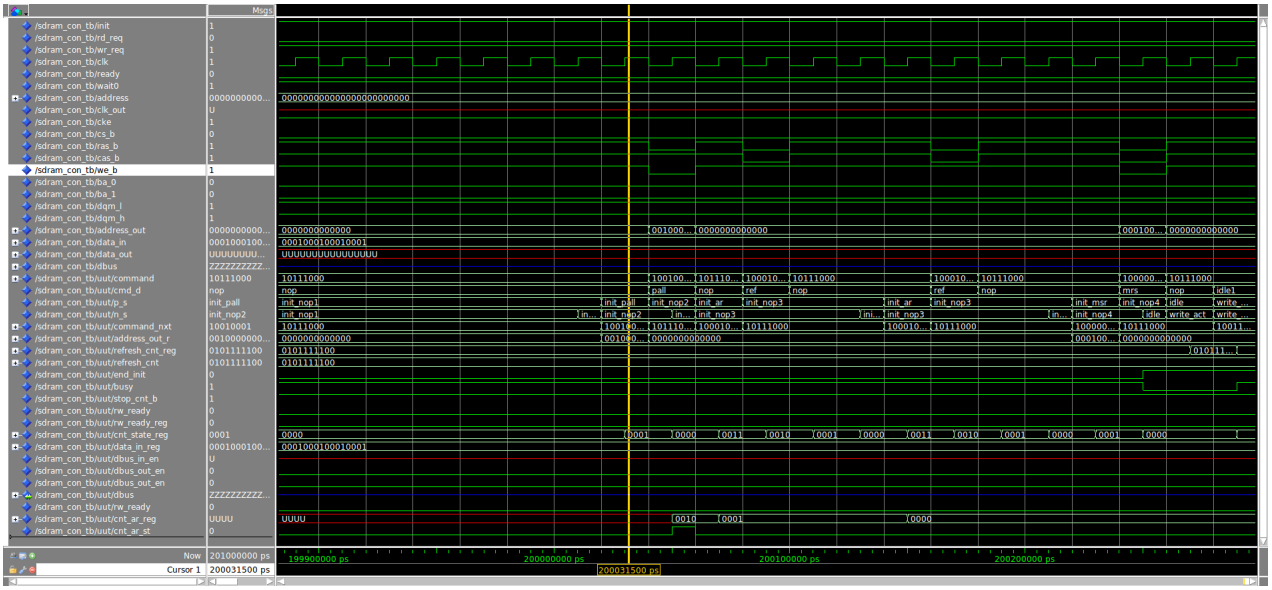

Figure 8: Initialisation sequence triggered

2.2 Read sequence

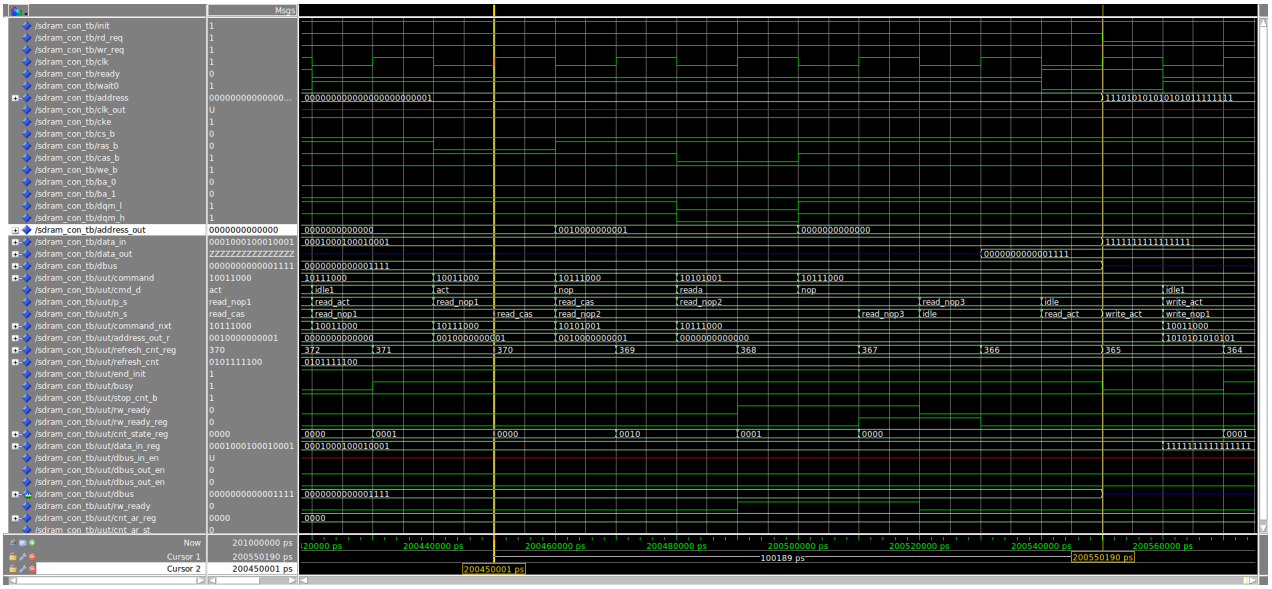

Figure 9: Read Sequence

2.3 Write Sequence

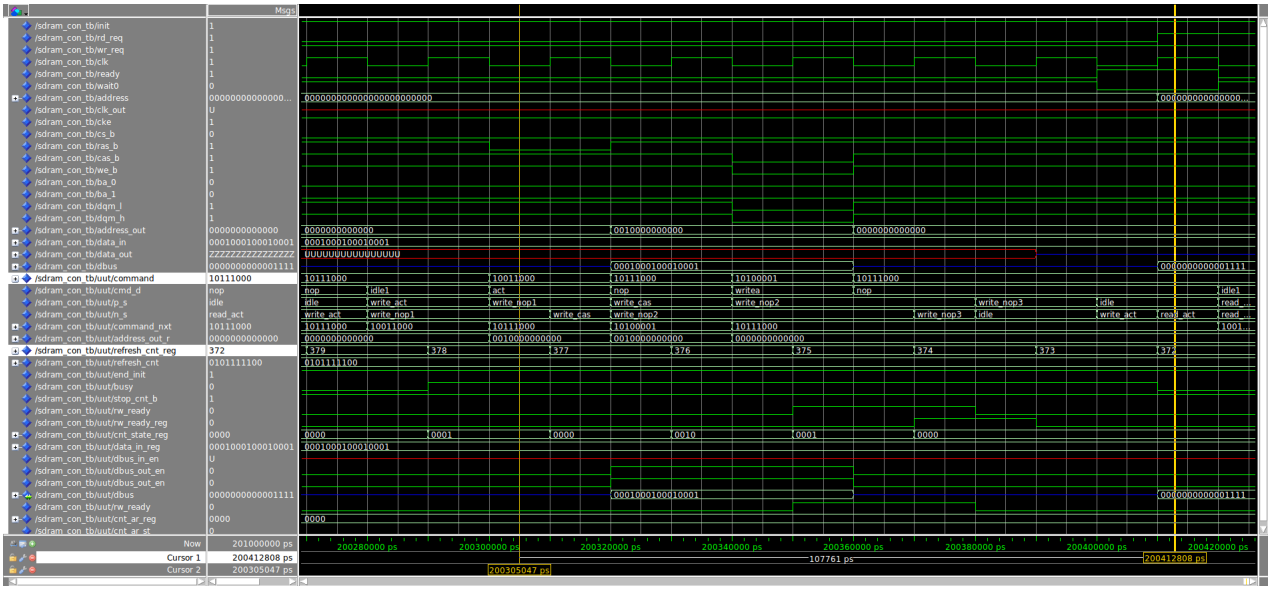

Figure 10: write Sequence

References

[1] David A Hodges, *ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS,CHAPTER 8.*

[2] *IS42S83200B DATASHEET*