Introduction

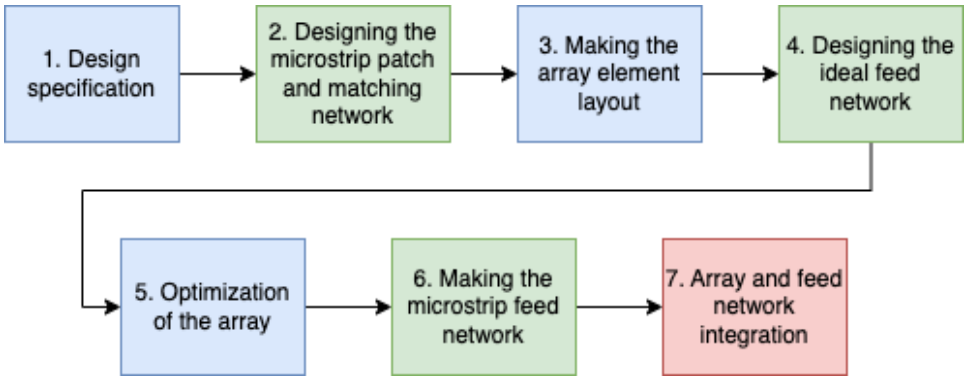
This project consists of designing and the characterization of a microstrip patch antenna element and implementing a 4-element linear array. The antenna will be designed to have a center frequency of 5.2 GHz. The electric field will be simulated and then measured, after the fabrication of the device, and the results will be compared. The figure of merits for the device are as follows:

- 10 dB input return loss bandwidth for element and array.
- 3 dB beam width for element and array (E_{Theta} and E_{Phi} directions).
- Radiation pattern of element and array (E_{Theta} and E_{Phi} directions).

The substrate that will be used in the design will be the RT/Duroid 5880. The specification of the material that will be used for the design are as follows:

- Dielectric thickness: 1.574 mm
- Dielectric constant: 2.2
- Loss tangent: 0.0009
- Copper thickness: 0.035 mm
- Conductivity: 5.817E7 S/m

The design methodology will follow the method illustrated in the flow chart:



Design

Part 1

1.2

For the assigned frequency of 5.2 GHz, we have found the free space wavelength to be about

$$\lambda_o = \frac{c}{fc} = \frac{3 \times 10^8}{5.2 \times 10^9} = \frac{3}{52} = 0.05769230769$$

$\lambda_o = 57.69230769\text{mm}$

1.3

We used TXLINE to calculate the guided wavelength for the transmission line with a characteristic impedance of 50 ohms. We found that the guided wavelength was

$$\beta = 150.593$$

$$\frac{2\pi}{\lambda_g} = 150.593$$

$\lambda_g = \frac{2\pi}{150.593} = 0.04172295729\text{m}$

A figure of the TXLINE is shown in the following figure.

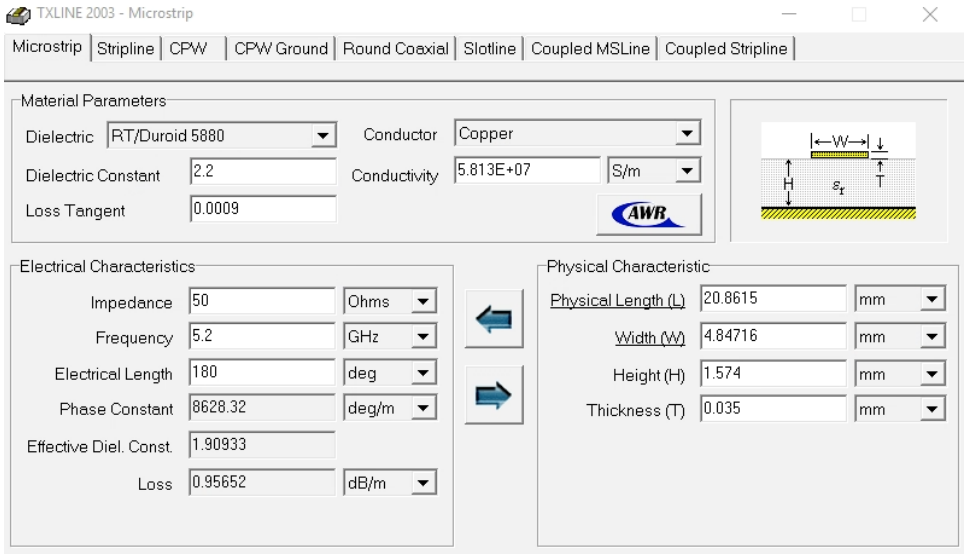


Figure 1: TXLINE for Half Wavelength

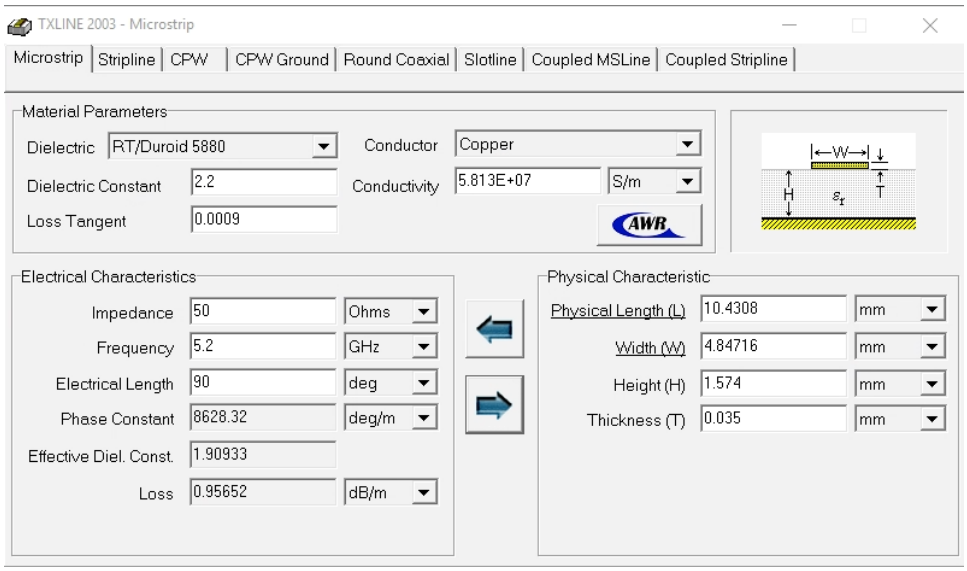
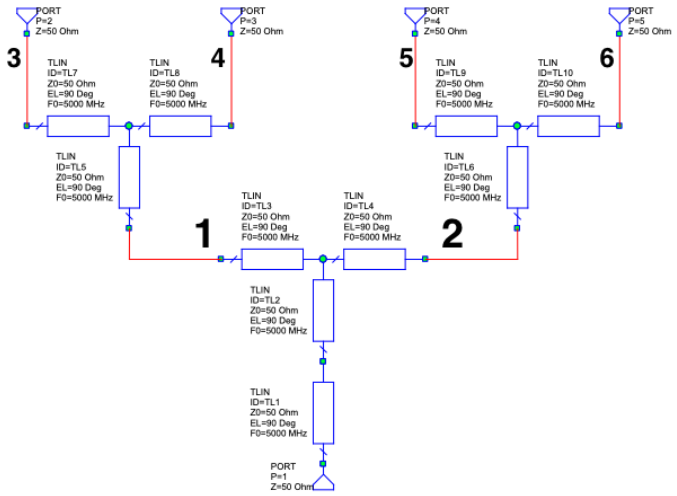


Figure 2: TXLINE for Quarter Wavelength

1.4

By looking at the feed network schematic, we can see that branches 1 and 2 will be symmetric. Also, the secondary branches 3 to 6 will be designed the same way, as well as their microstrip patch.



1.5

A block diagram illustrating the various known and unknown quantities to be determined in the design keeping in mind that the final input impedance needs to be 50 ohms is shown in the following diagram.

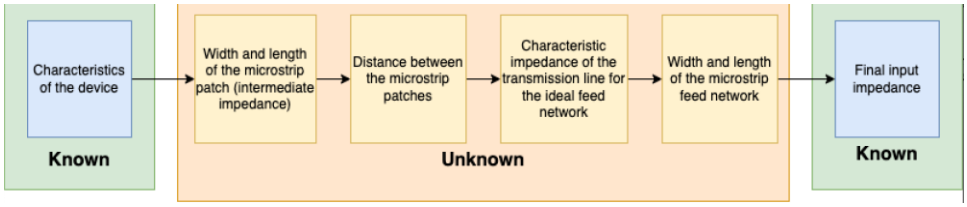


Figure 3: Block Diagram Illustrating the Known and Unknown Quantities

Part 2

2.4

The diagram showing the patch with the widths and lengths of that of a microstrip line with the characteristic impedance of 50 ohms and half wavelength long is shown in the following figure.

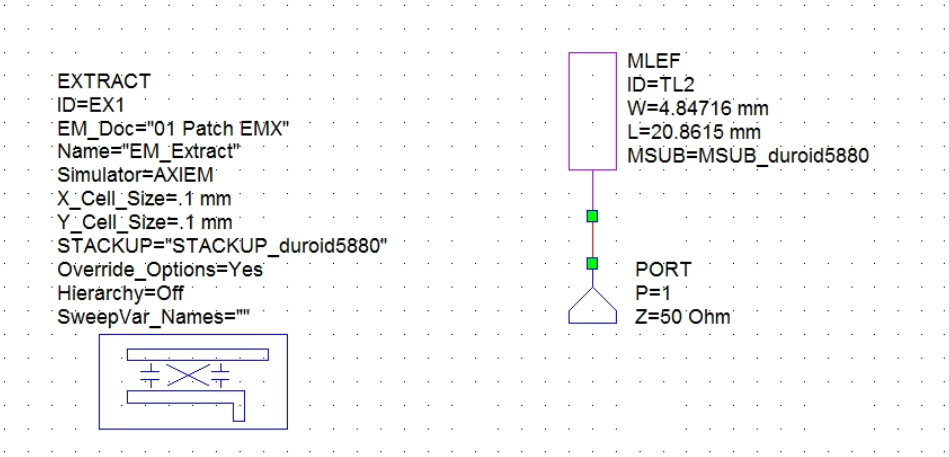


Figure 4: The Width and the Length of the Half Wavelength Patch

2.5

The following diagram shows the layout of the half wavelength long microstrip line.

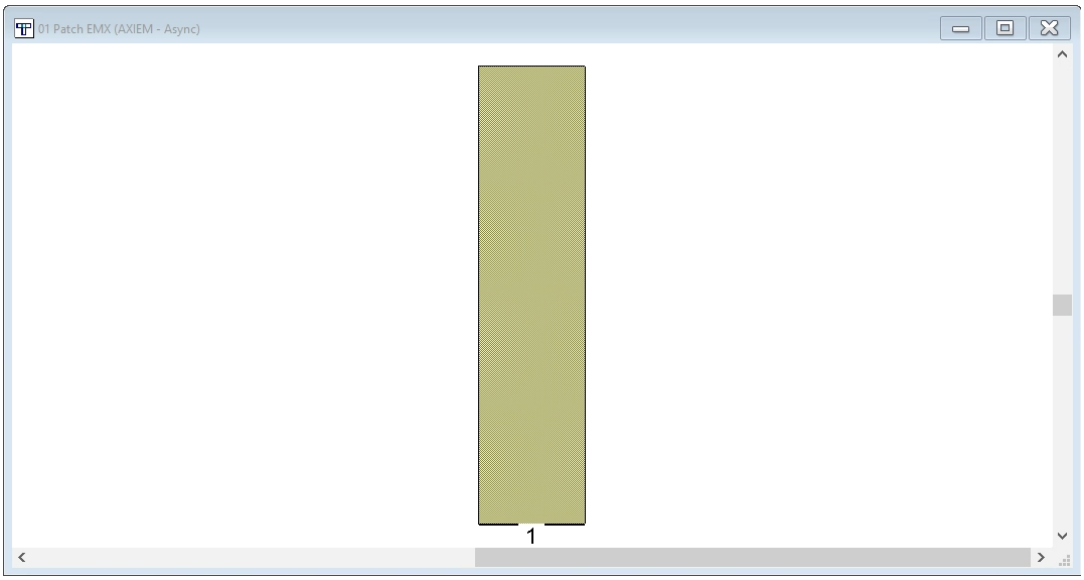


Figure 5: Extracted Patch Geometry

2.6

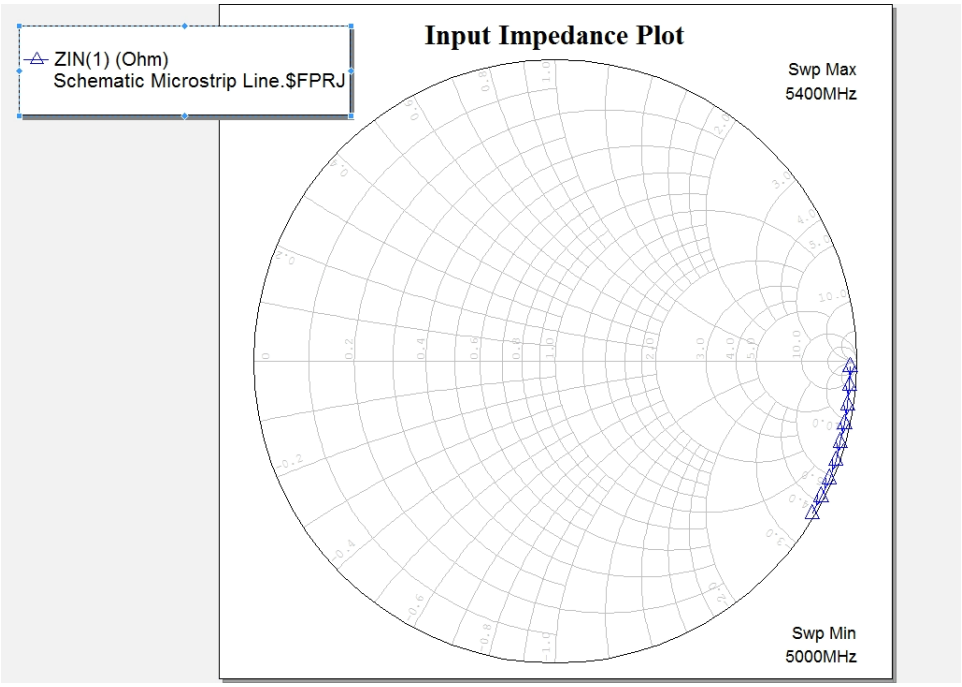


Figure 6: Plot of the Zin on the Smith Chart

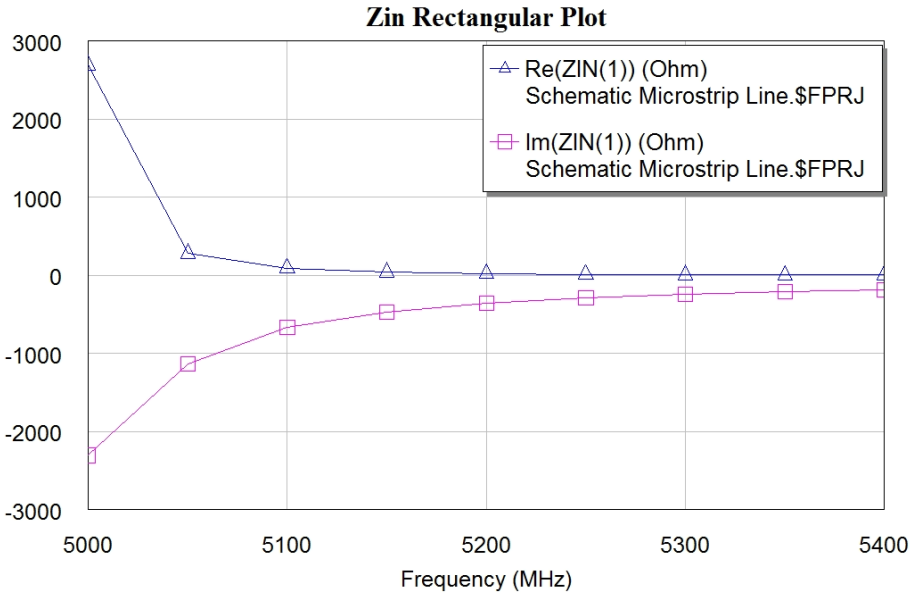


Figure 7: Plot of the Real and Imaginary Parts of Zin

2.7

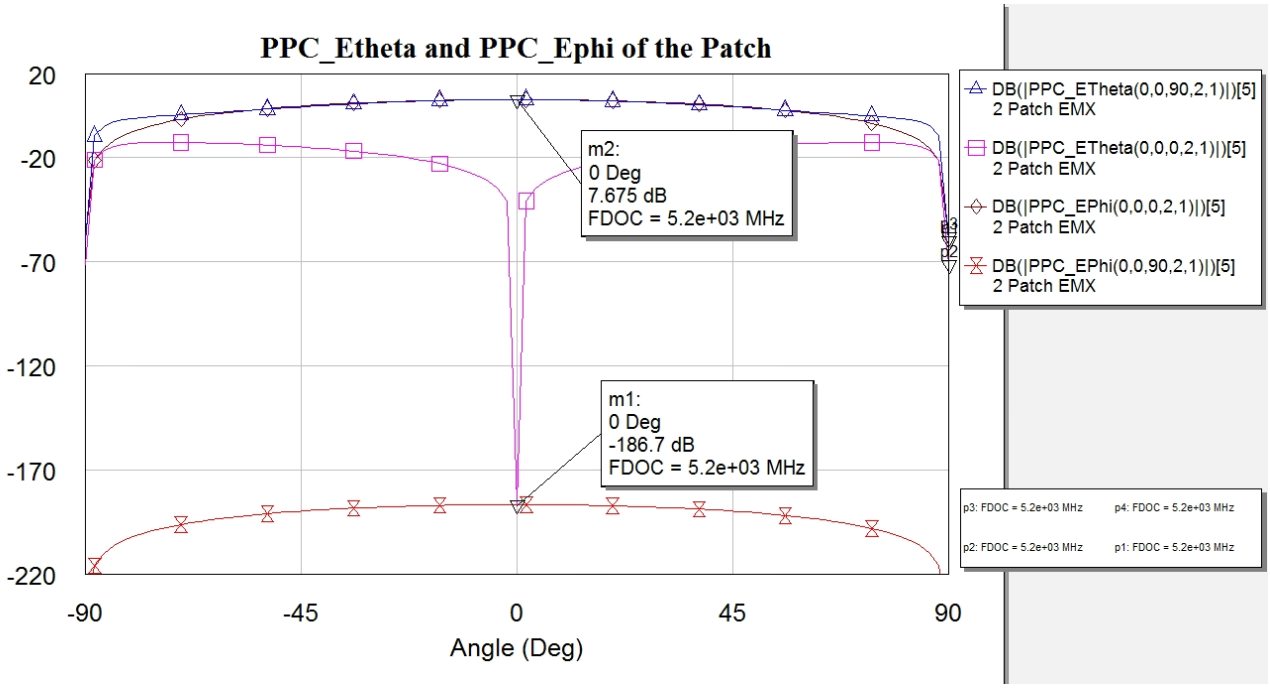


Figure 8: Plot of the PPC Etheta and PPC Ephi

2.8

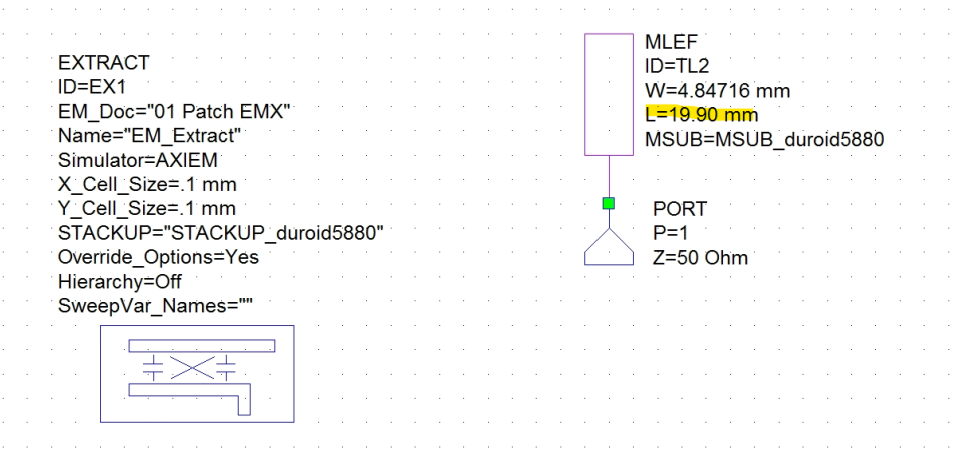


Figure 9: Adjusted Length Resonant at the Design Center Frequency (5.2GHz)

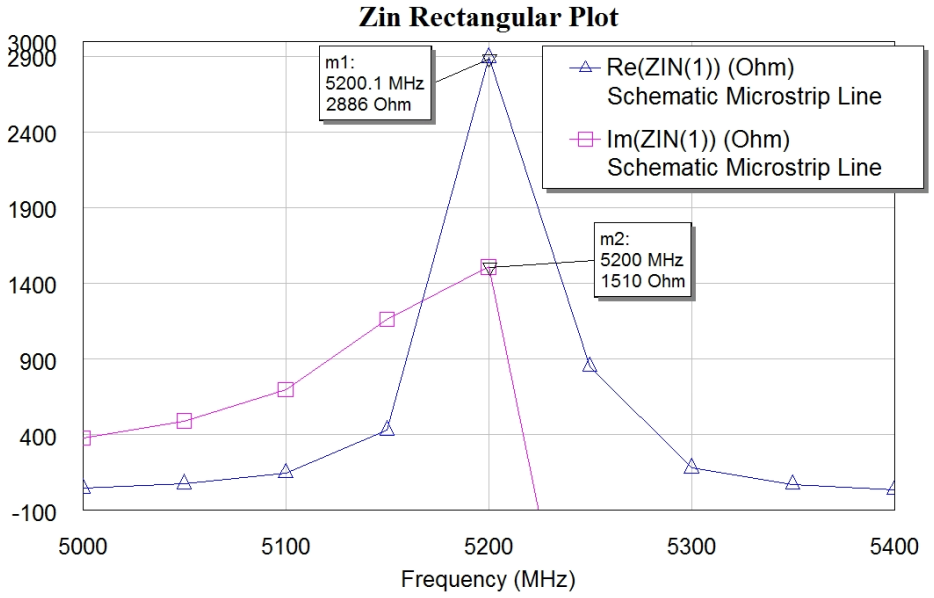


Figure 10: Plot of the Input Impedance at Resonance

The input impedance of this particular line when it is at resonance has it such that the input resistance is very high. In this particular case the input reactance is also very high although it should be approaching a small value when adjusted further.

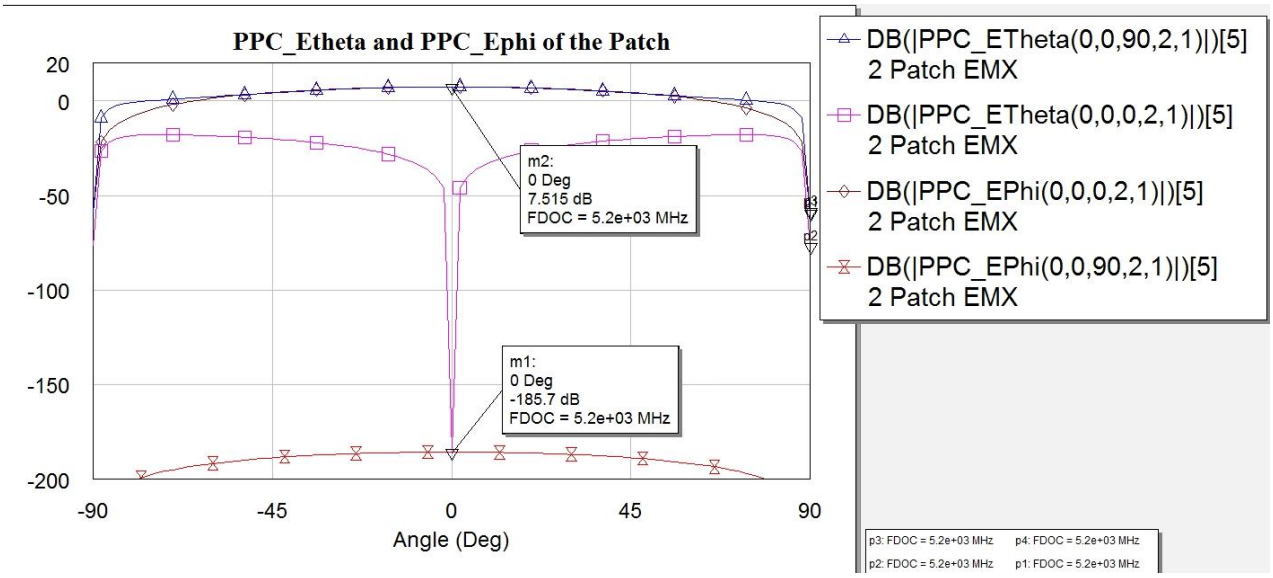


Figure 11: Plot of the PPC Etheta and PPC Ephi

As can be seen at resonance the PPC_Etheta at 90 degrees which in this case would be the H plane should be maximized while the PPC_Etheta for the electric field would be minimized. The opposite would be true for Ephi as indicated in the diagram.

2.9

Increasing the width decreased the impedance and decreasing the width increased the impedance which slightly changed the reactance as well. Increasing the length decreased the reactance and decreasing the length increased the reactance which also slightly changed the impedance. For the radiation pattern, when the reactance gets closer to 0 there is a steeper drop in the radiation pattern at resonance.

2.11

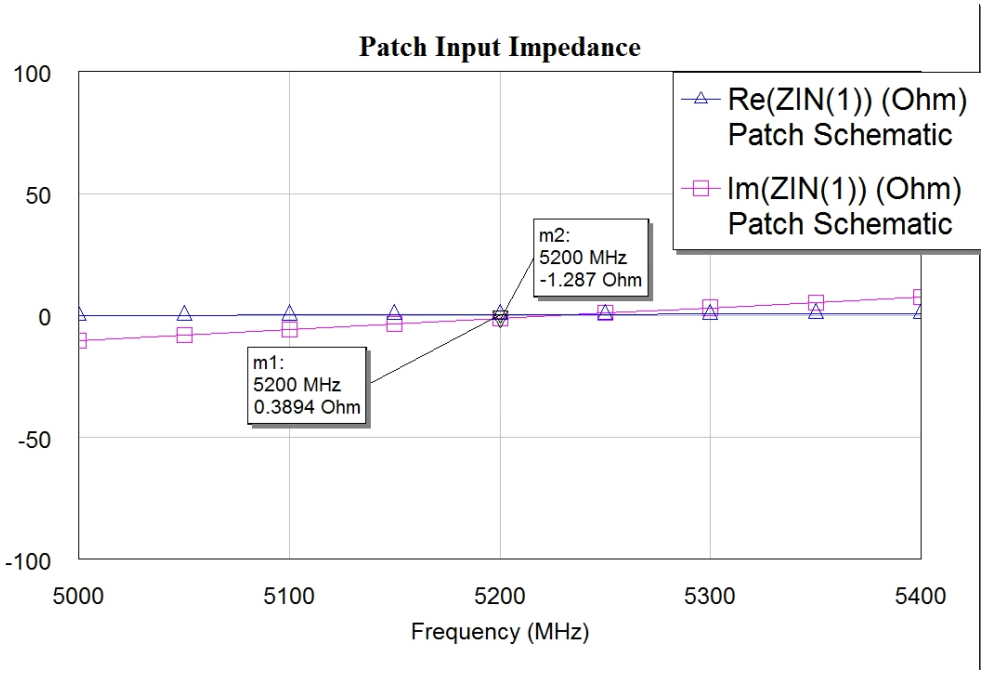


Figure 12: Input Impedance Plot with Feed Line

Adding a feed line significantly reduced the impedance and the reactance. This is not a good impedance to design hence further adjustments are required.

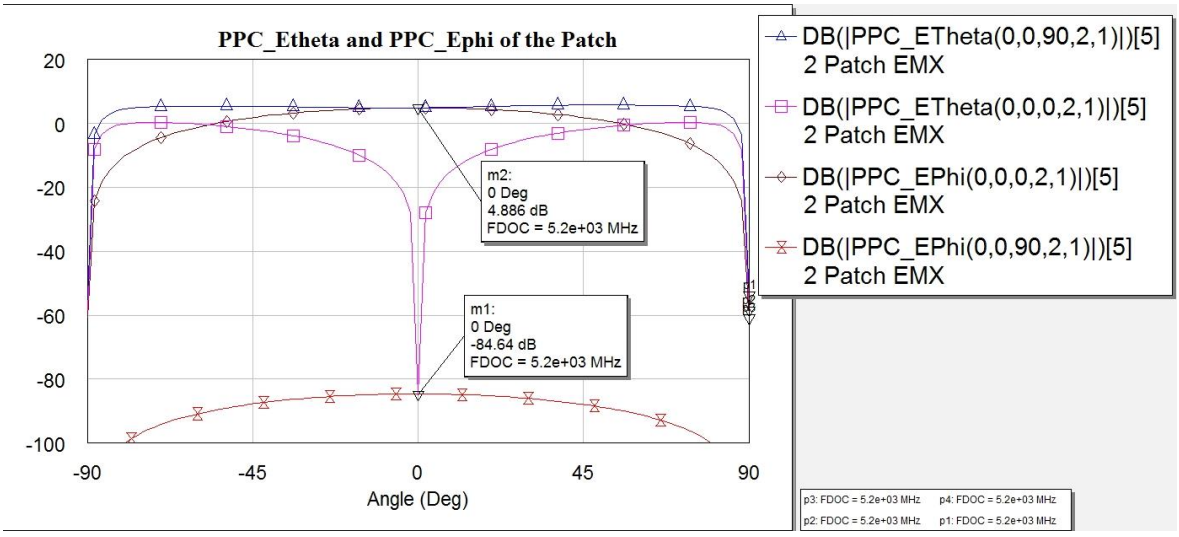


Figure 13: Plot of PPC Etheta and PPC Ephi with Feed Line

2.13

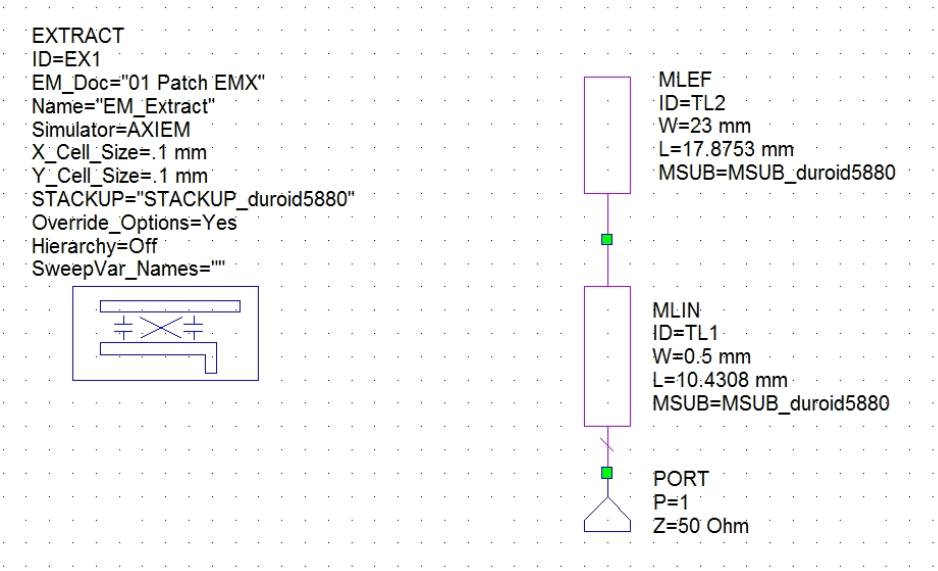


Figure 14: Adjusted Width and Length for an Intermediate Input Impedance

2.16

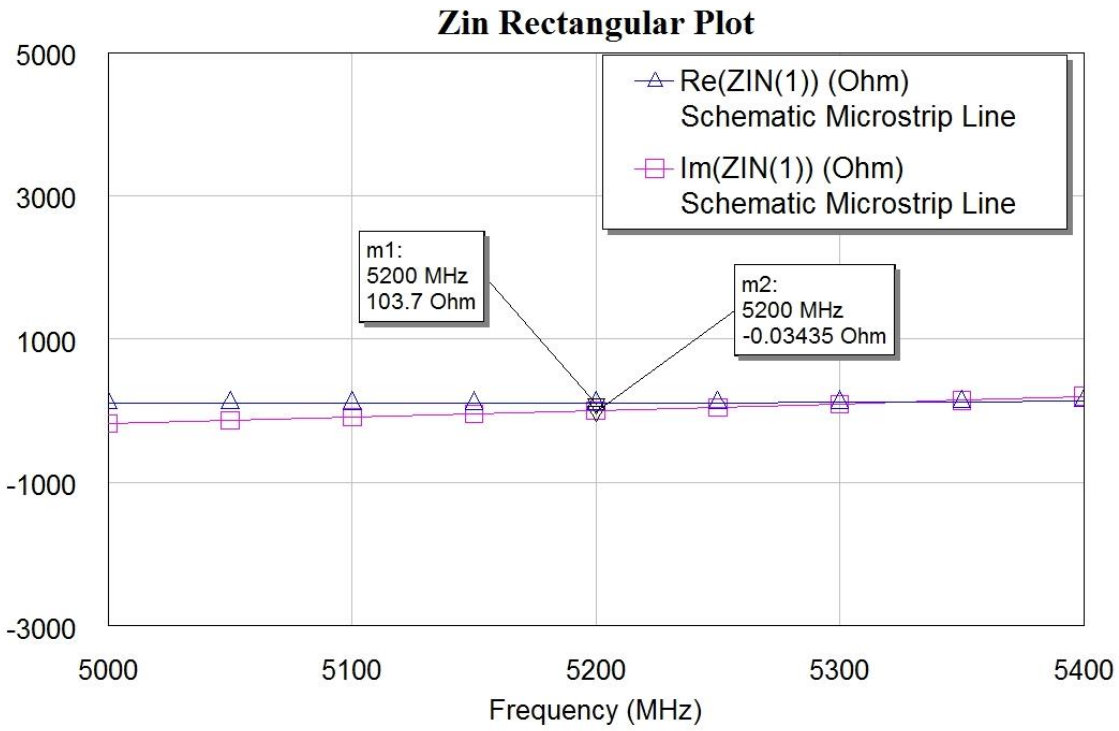


Figure 15: Overall Intermediate Input Impedance Plot

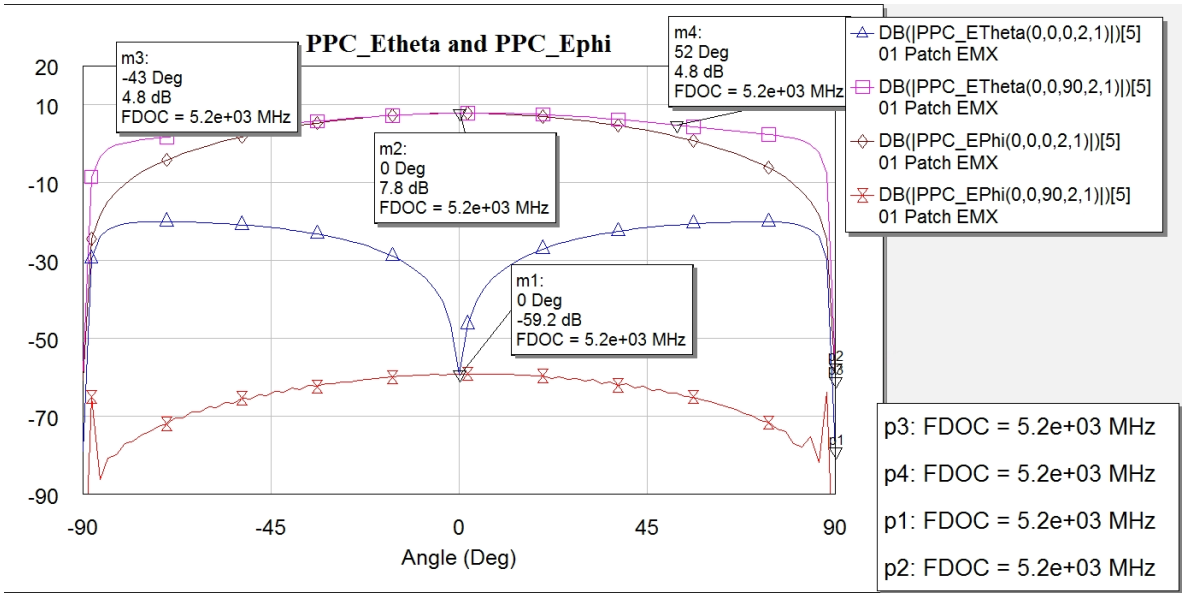


Figure 16: Plot of the PPC Etheta and PPC Ephi

Figure 17: Plot of the Return Loss

Part 3

3.3

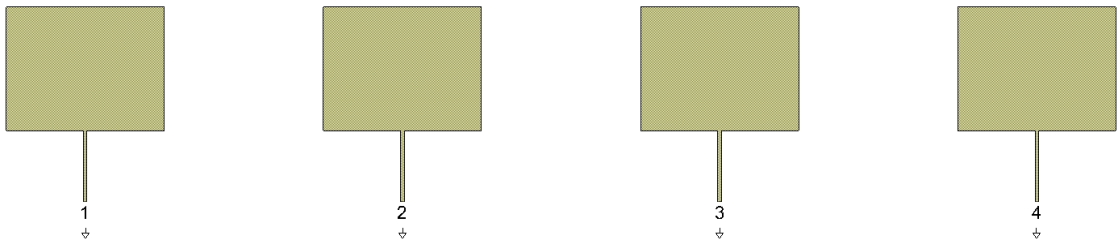


Figure 18: Array Extraction with 0.8λ Spacing

Part 4

4.1

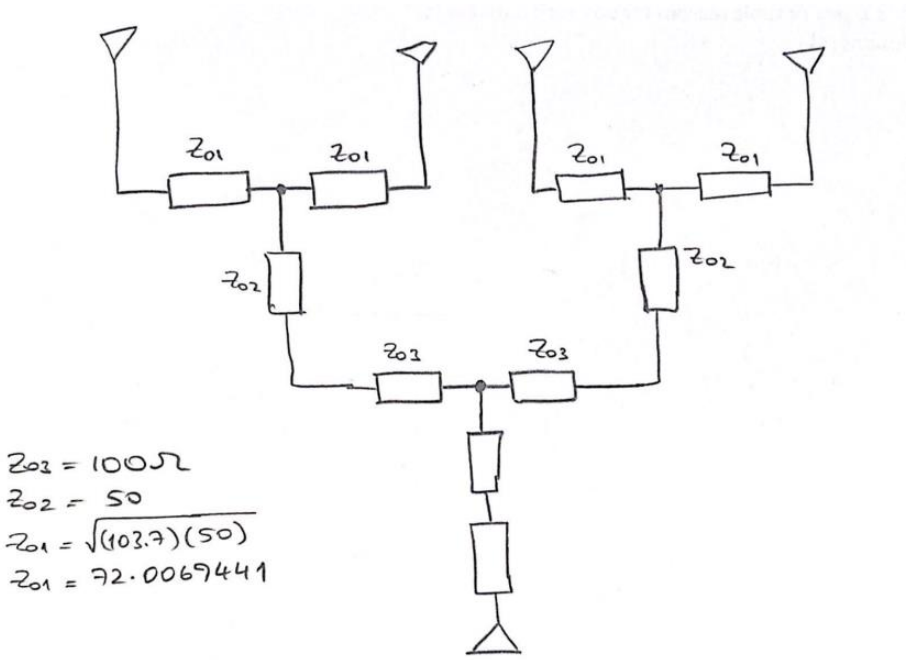


Figure 19: Design of the Ideal Feed Network

4.2

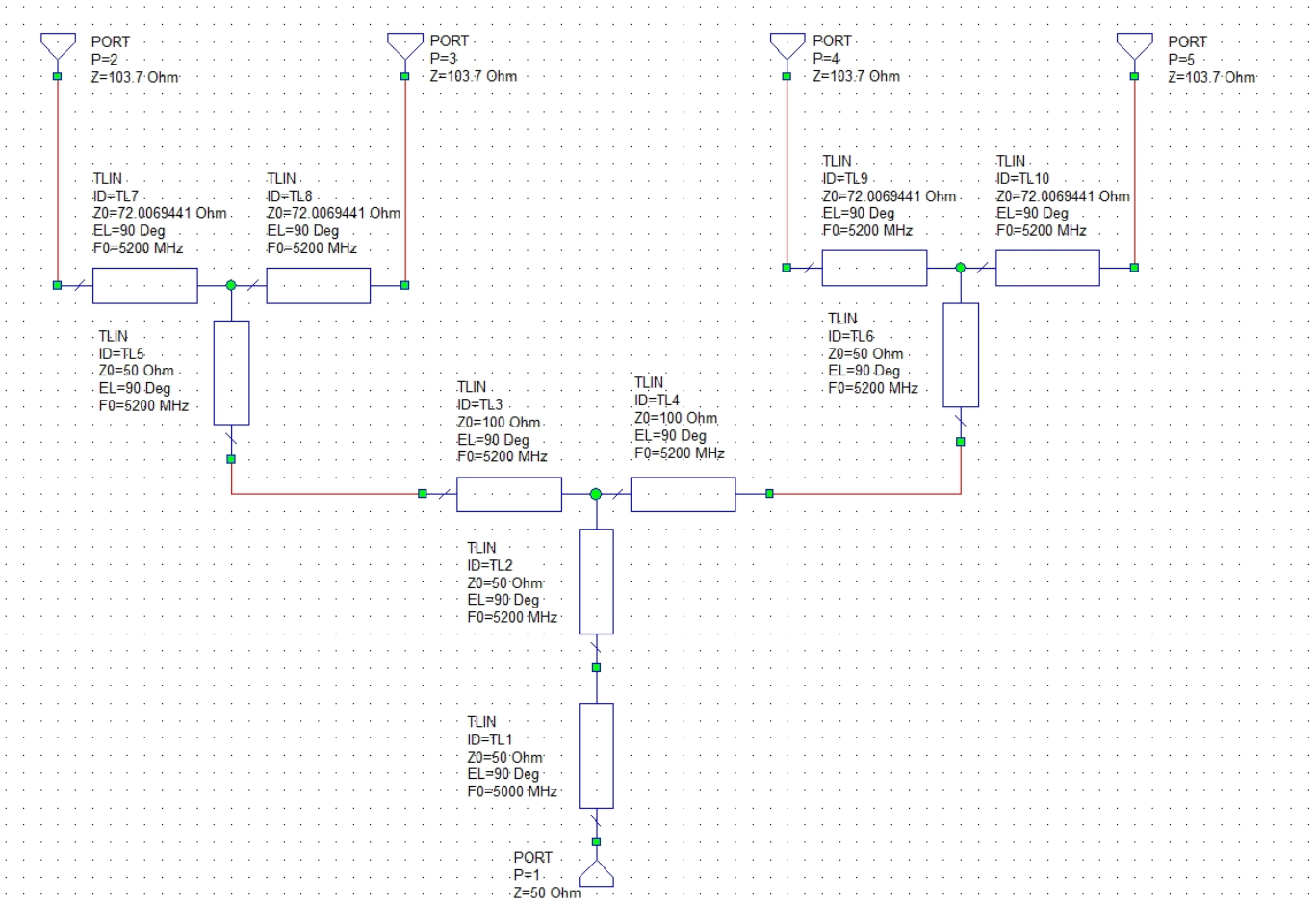


Figure 20: Ideal Feed Network Schematic

4.5

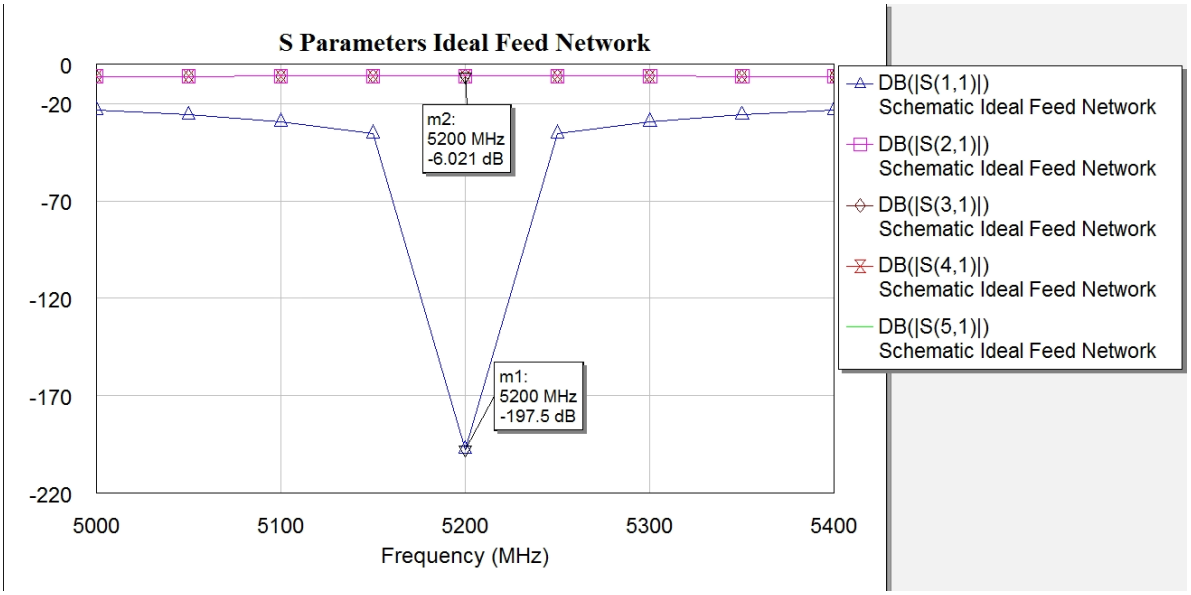


Figure 21: S Parameters for the Ideal Feed Network

Part 5

5.3

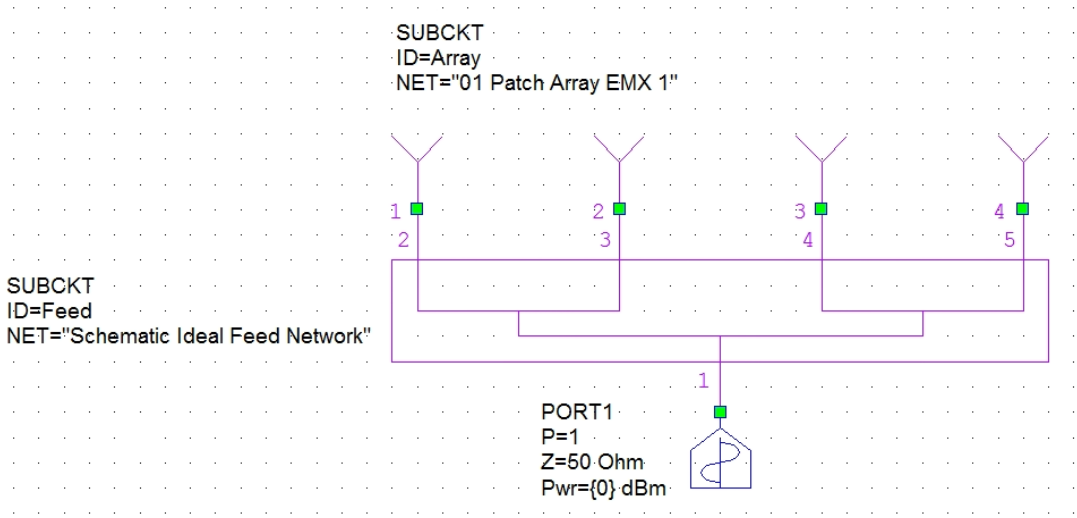


Figure 22: Ideal Feed Network and Patch Array Schematic

5.5

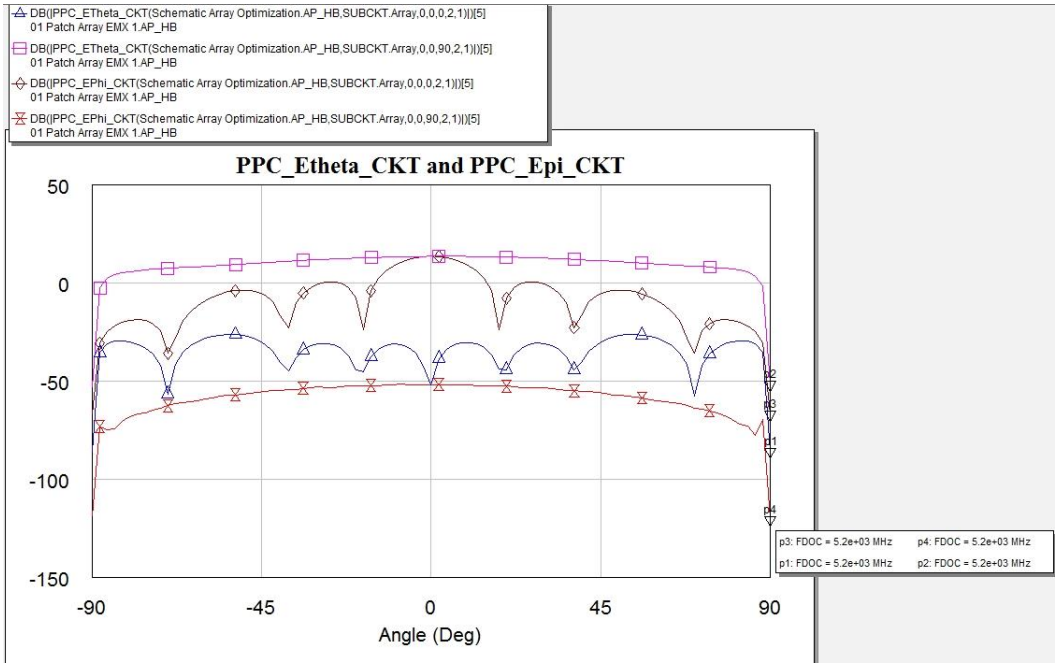


Figure 23: Plot of PPC Etheta CKT and PPC Ephi CKT

Adjusting the spacing between the elements will change the directivity of the fields. We can clearly see in the image below that when we have around 0.8 lambda value as spacing between the elements, we have a maximum of directivity, if we increase or decrease it, the directivity will be lower.

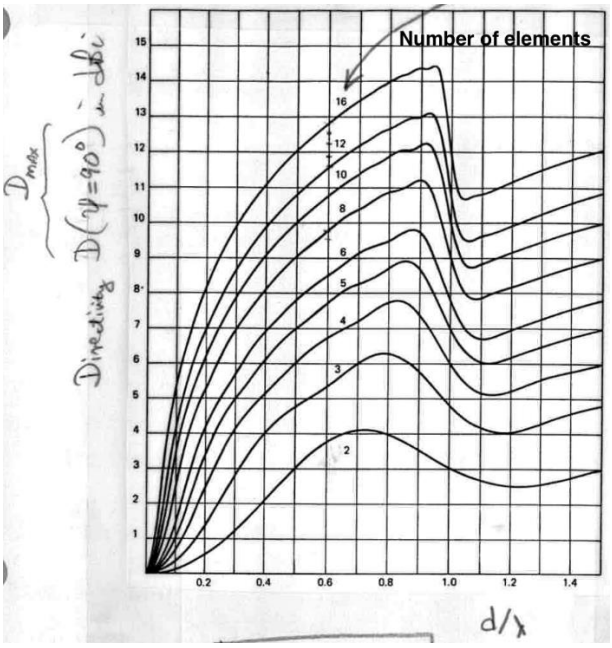


Figure 24: Directivity in terms of the spacing between the elements (spacing is in distance/lambda)

Part 6

6.1

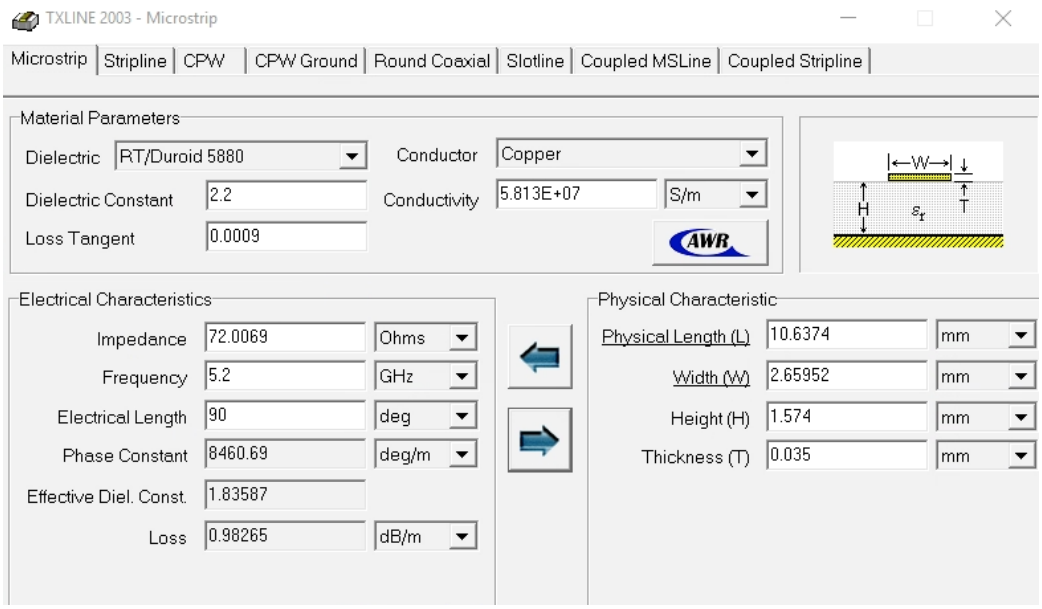


Figure 25: TXLINE Result for Zo=72.0069

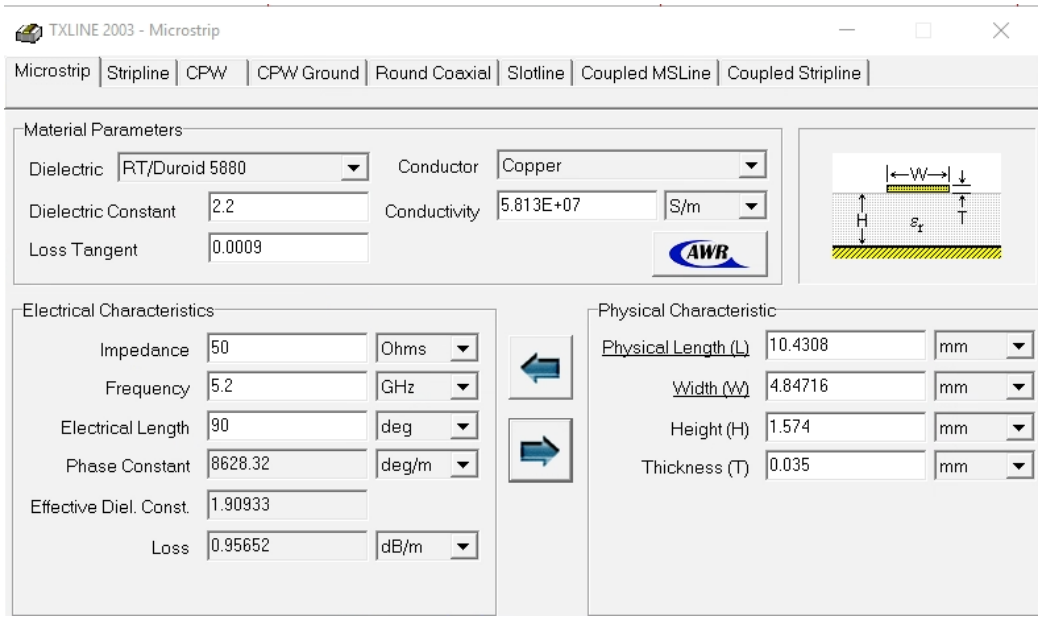


Figure 26: TXLINE Result for Zo=50

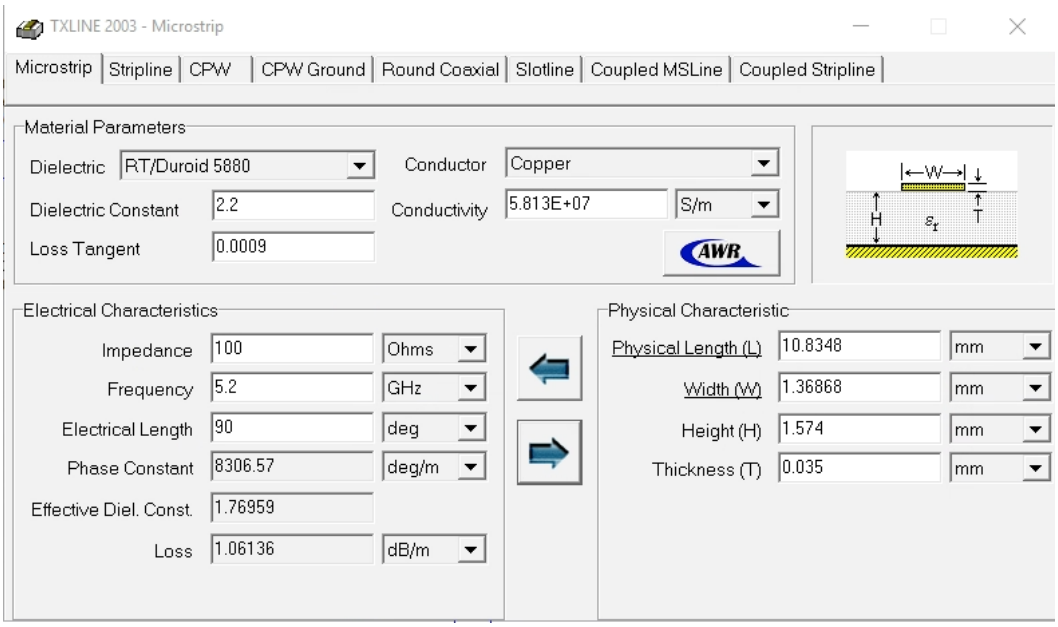


Figure 27: TXLINE Result for Zo=100

6.2

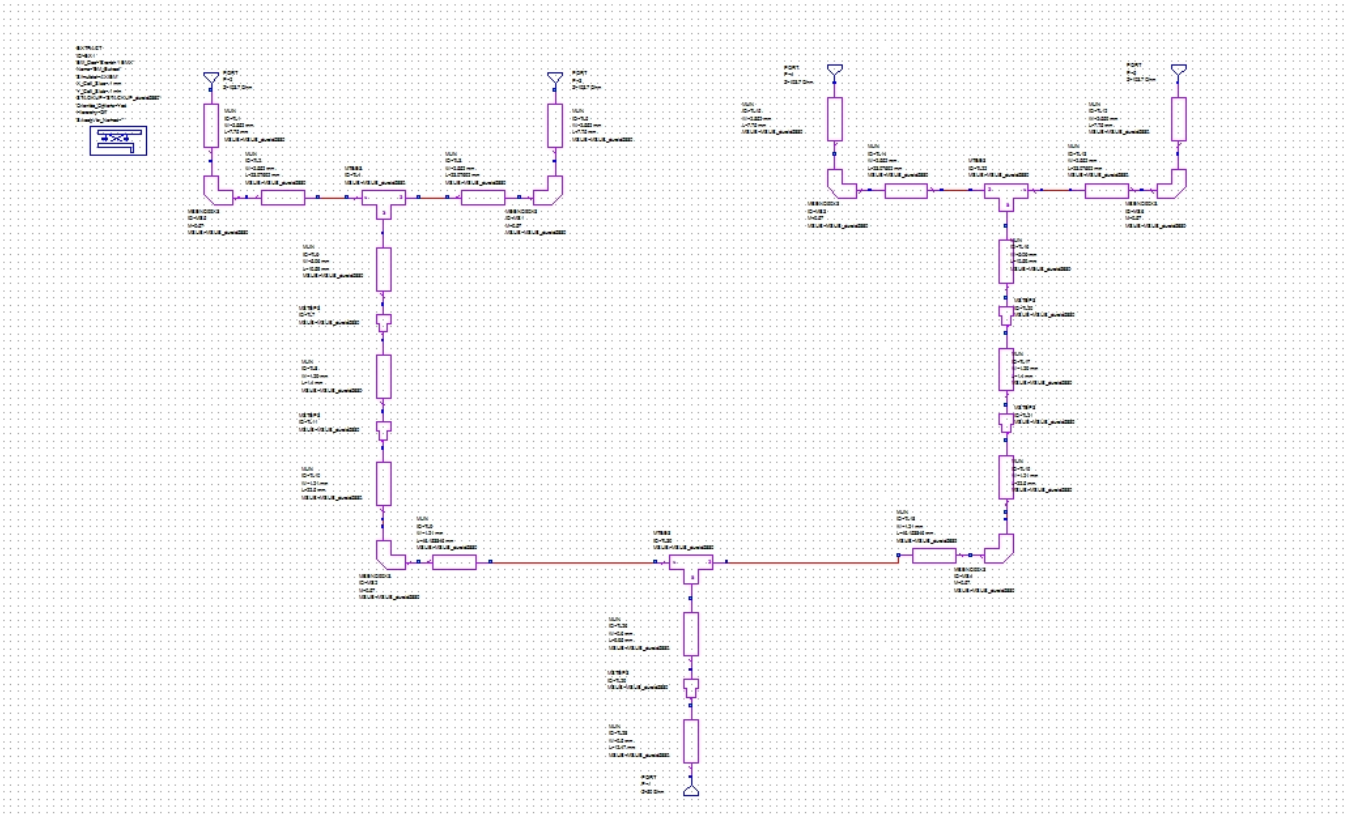


Figure 28: Microstrip Feed Network Schematic

6.3

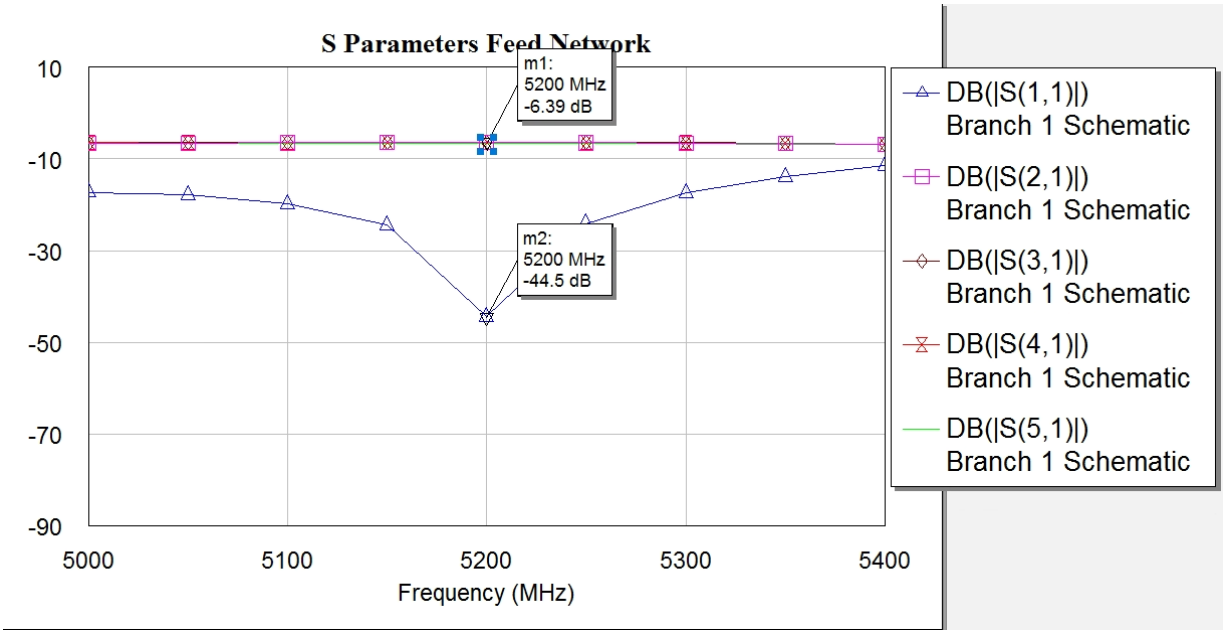


Figure 29: S Parameters for the Microstrip Feed Network

Part 7

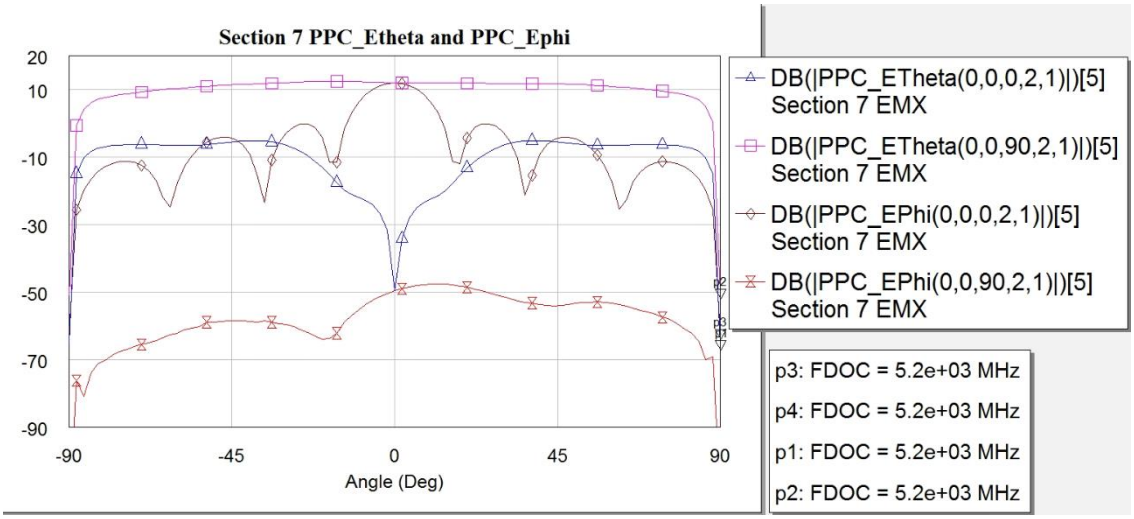


Figure 30: Plot of PPC Etheta and PPC Ephi

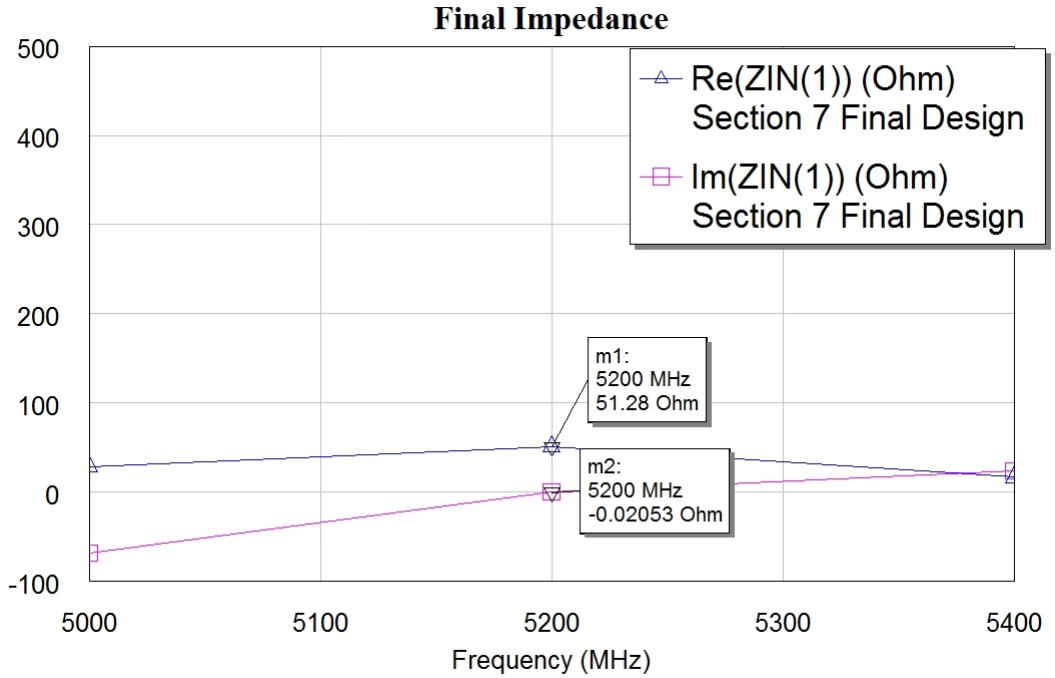


Figure 31: Final Input Impedance Plot

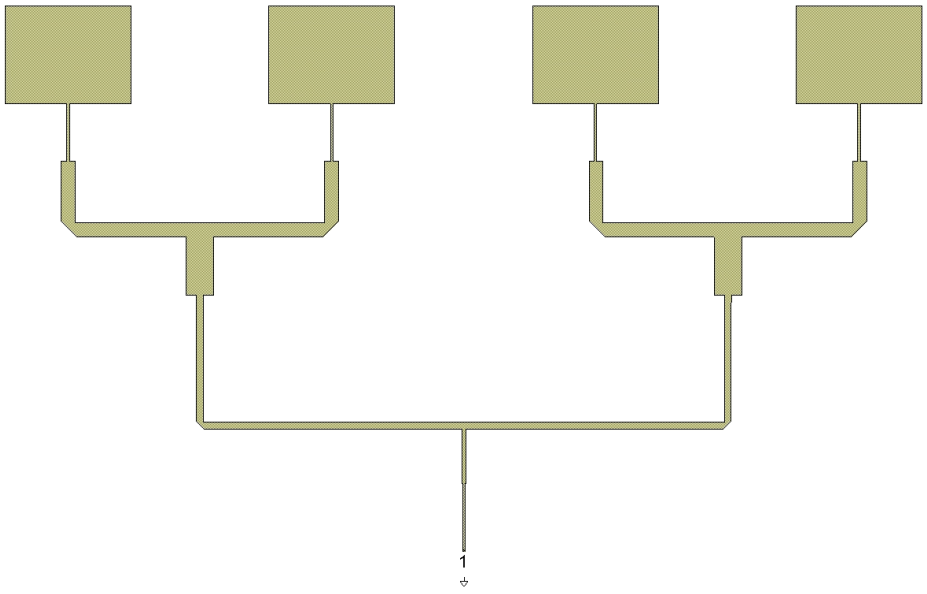


Figure 32: Extracted Layout of the Array Realization

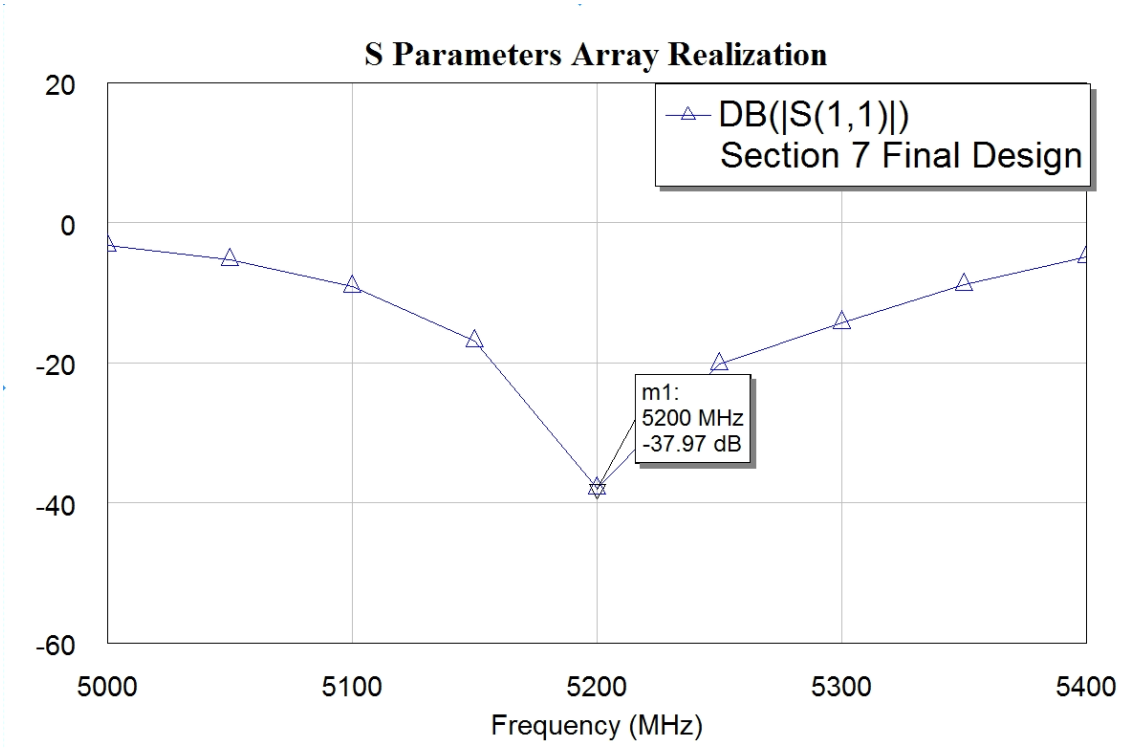


Figure 33: Return Loss of the Array Realization