Table of Contents

1 Abstract

The intention of this project is to highlight the design steps and fabrication of a microwave circuit. The design can be highlighted in two steps. These steps include the theoretical design and the tweaking processes involving the use of microwave circuit simulation software. The simulation software used for the tweaking design in this case was AWR Microwave Office. The circuit utilized an AT41486 BJT manufactured by Hewlett-Packard. S parameter specifications were found in the spec sheet (see appendix). Biasing the circuit, in order to achieve maximum gain and reduce reflections was achieved using balanced stubs and planar microstrip transmission lines that approximate that of a TEM (Transverse Electromagnetic) lossless line.

2 Introduction

For the assigned frequency of 3.1 GHz, we had the goal of optimizing 4 main parameters. These four main parameters include minimizing the S11 and S22 scattering parameters, maximizing the bandwidth of the device, maximizing the gain (both the S12 and the S21 scattering parameters), and maintaining stability across the key bandwidths.

This design was going to be done using microstrip transmission lines. The transmission lines utilized balanced open-circuited stubs as a means of matching the input of the BJT. Input and output capacitors will be utilized to couple the input signal to the BJT for amplification purposes. A DC biasing circuit also needed to be appended to the circuit in order to ensure that the device was biased to the correct operating current (I_{ce}) and operating voltage (V_{ce}). A diagram of this design is shown in the following figure.

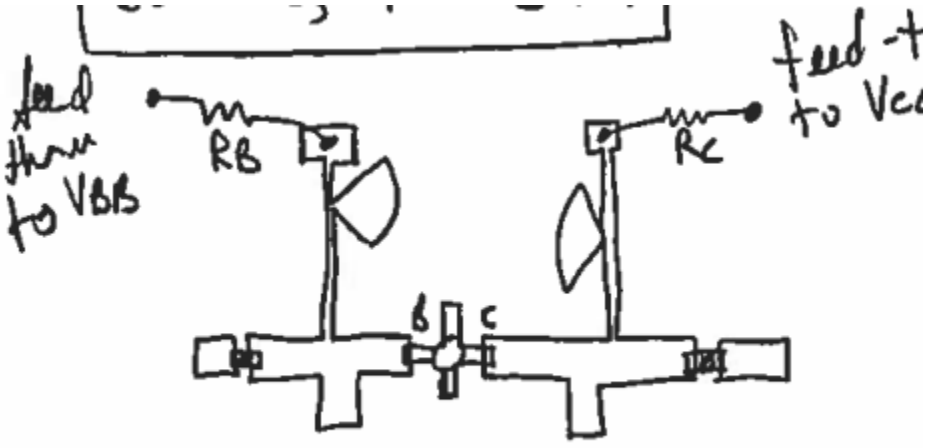

Figure 1: General Outline of Circuit

3 Theoretical Design

3.1 Wavelength and Permittivity Calculations

The theoretical design of the circuit was done using Smith Charts in conjunction with TXline provided by the AWR MWO software package.

The substrate material parameters were provided before design and include the following:

Type: Rogers RT/Duroid 5880

Thickness: 787.41 µm

Dielectric Constant: $\varepsilon_r = 2.20 \pm 0.04$

Dielectric Losses: $\tan\delta = 0.0009$

Copper Thickness: 34 µm

The preliminary calculations are shown as follows:

Frequency = 3.1 GHz

$$\lambda o \; = \; \frac{3 \cdot 10^8}{3.1 \cdot 10^9} = 0.09677419355m$$

$\frac{w}{h} = \frac{2382.05\mu m}{787.41\mu m} = 3.025$ (The width was determined using AWR Txline)

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \left(\frac{1}{\sqrt{1 + 12 \cdot \frac{h}{w}}} \right) = \frac{2.2 + 1}{2} + \left(\frac{2.2 - 1}{2} \right) \cdot \left(\frac{1}{\sqrt{1 + 12 \cdot \left(\frac{1}{3.025} \right)}} \right)$$

$$\epsilon_{eff} = 1.86922, \; Zo \; = 50$$

$$\lambda g = \frac{0.09677419355}{\sqrt{1.86922}} = 0.070783m \; = \; 70.7831m$$

3.2 Stability Calculations

The stability of the circuit was calculated using the S parameters for 25mA and 8V. The reason for this is because these set of S parameters (as provided by the spec sheet) give a higher gain for the design frequency of 3.1 GHz. The values of the S parameters at 3.1 GHz were interpolated as follows:

$$S_{11} = 0.66\angle 126.6$$

$$S_{21} = 2.45\angle 32$$

$$S_{12} = 0.0862\angle 56.8$$

$$S_{22} = 0.376\angle -51$$

The conditions for unconditional stability is that: $|S_{11}| < 1,\ |S_{22}| < 1, |\Delta| < 1, |K| > 1$.

These values are calculated as follows:

$$|\Delta| = S_{11} \cdot S_{22} - S_{12} \cdot S_{21} = 0.06431\angle 27.022$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12} \cdot S_{21}|} = 1.011317$$

As seen in the above conditions for unconditional stability the following S parameters would produce a stable circuit.

This is the theoretical largest gain that can be achieved under these S parameters.

$$G_{Tmax} = \frac{|S_{21}| \cdot \left(K - \sqrt{K^2 - 1}\right)}{|S_{12}|} = 24.456$$

$$G_{Tmax} = 13.884\ dB$$

The gain that could be achieved using the other biasing (Ic=10mA) is 16.791 (12.25 dB). This is smaller which means that the other biasing was chosen.

3.3 Input/Output Matching Network Design

The reflection coefficients are calculated as follows.

$$\Gamma_s = \frac{B_1 \pm \sqrt{B_1^2 - 4 \cdot |C_1|^2}}{2 \cdot C_1}$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4 \cdot |C_2|^2}}{2 \cdot C_2}$$

The B and C variables are calculated as follows.

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

$$B_1 = 1 + 0.66^2 - 0.376^2 - 0.0643^2$$

$$B_1 = 1.29008951$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2$$

$$B_2 = 1 + (0.376)^2 - (0.66)^2 - (0.0643)^2$$

$$B_2 = 0.70164151$$

$$C_1 = S_{11} - \Delta S_{22}^*$$

$$C_1 = 0.66\angle 126.6 - (0.06431\angle 27.02) \cdot (0.376\angle 51)$$

$$C_1 = 0.64426\angle 128.213$$

$$C_2 = S_{22} - \Delta S_{11}^*$$

$$C_2 = 0.376\angle - 51 - (0.06431\angle 27.02) \cdot (0.66\angle - 126.6)$$

$$C_2 = 0.349373\angle - 45.77$$

These values are then plugged into the formula for the reflections to get the following values.

$$\Gamma_s = \frac{1.29008951 - \sqrt{1.29008951^2 - 4 \cdot (0.64426)^2}}{2 \cdot (0.64426\angle 128.213)}$$

$$\Gamma_s = 0.95170966\angle - 128.21$$

$$\Gamma_L = \frac{0.70164151 - \sqrt{0.70164151^2 - 4 \cdot (0.349373)^2}}{2 \cdot (0.349373\angle - 45.77)}$$

$$\Gamma_L = 0.91301\angle 45.77$$

After that the load impedance and source impedance are calculated as follows.

$$Z_L = Z_o \cdot \left(\frac{1 + \Gamma_L}{1 - \Gamma_L}\right) = 50 \cdot \left(\frac{1 + \Gamma_L}{1 - \Gamma_L}\right) = 14.861417 + i \cdot 116.852141$$

$$Z_s = Z_o \cdot \left(\frac{1 + \Gamma_s}{1 - \Gamma_s}\right) = 1.5284719 - i \cdot 24.254944$$

The design utilizing the Smith Chart is shown as follows:

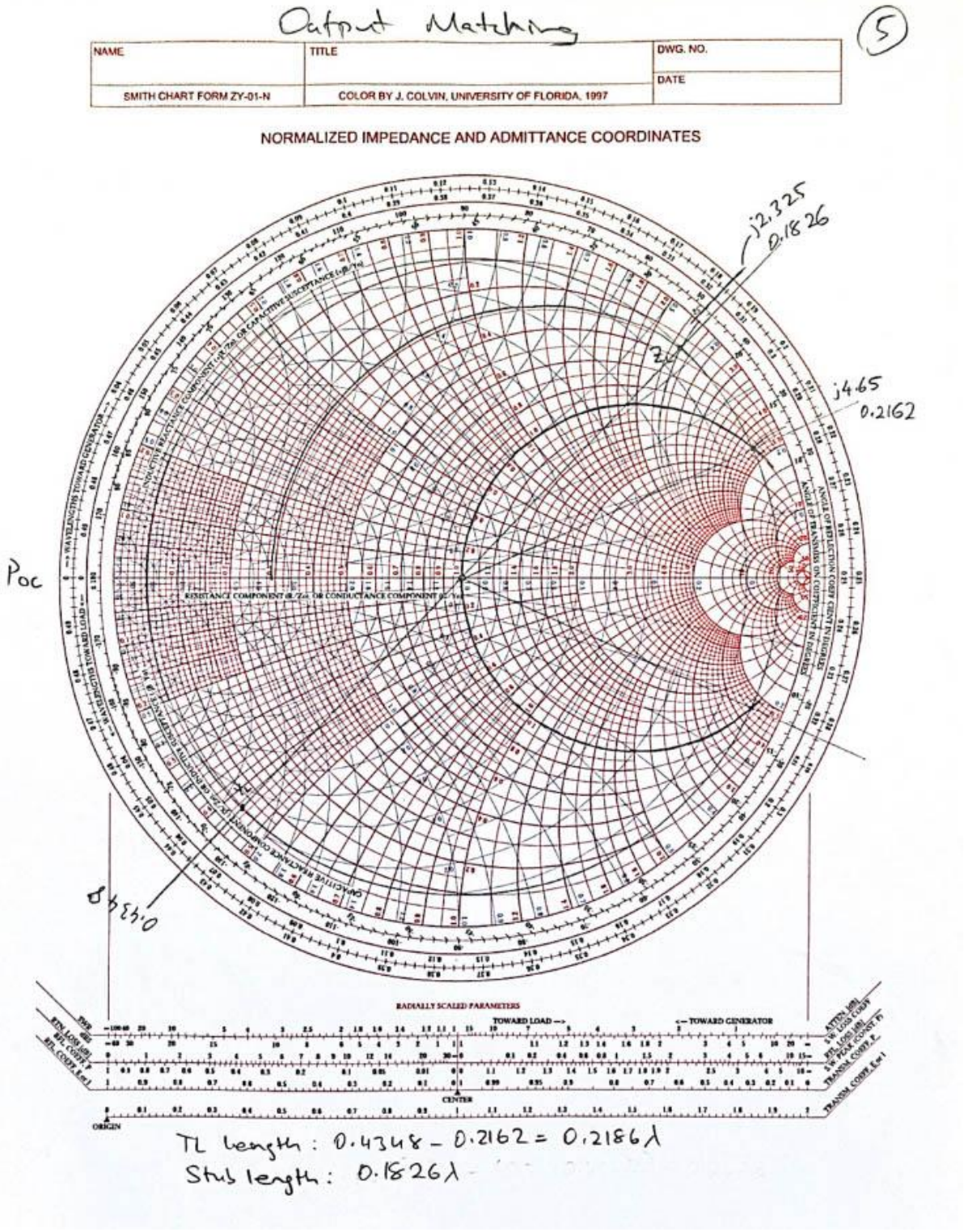

Figure 2: Output Matching Network

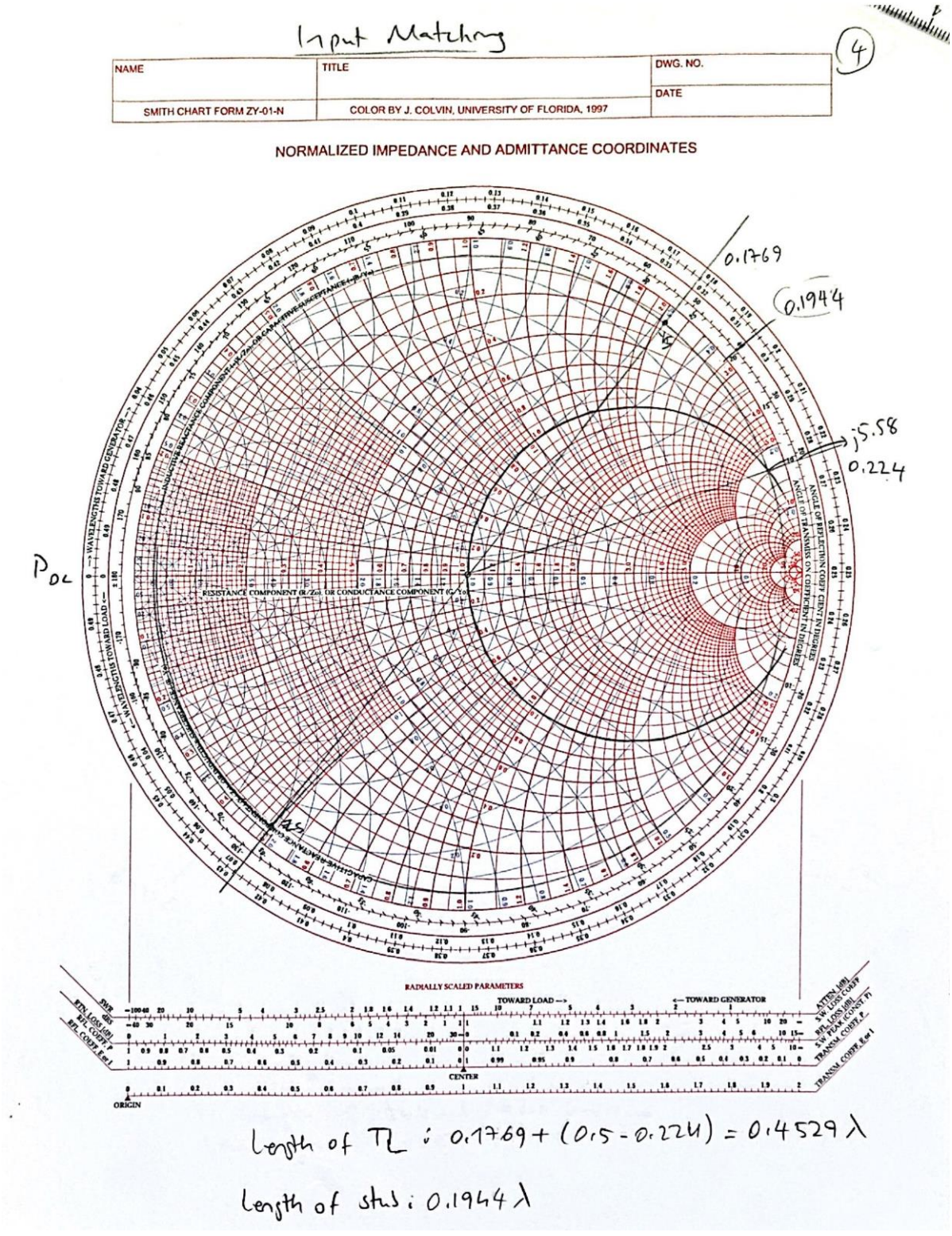

Figure 3: Input Matching Network

The following values were found for the input and output matching networks.

Output Matching Network

Length of the transmission line:

$$l_1 = 0.4348\lambda - 0.2162\lambda = 0.2186\lambda$$

Length of the balanced stub:

$$l_2 = 0.1944\lambda$$

Input Matching Network

Length of the transmission line:

$$l_1 = 0.1769\lambda + (0.5 - 0.224)\lambda = 0.4529\lambda$$

Length of the balanced stub:

$$l_2 = 0.1944\lambda$$

After multiplying by the appropriate wavelength (λ_g) one gets the following values.

Output Matching Network

$$l_1 = 0.2186 \cdot 70.7831 = 15.473186$$

$$l_2 = 0.1826 \cdot 70.7831 = 12.92499406$$

Input Matching Network

$$l_1 = 0.4529 \cdot 70.7831 = 32.05767$$

$$l_2 = 0.1944 \cdot 70.7831 = 13.76023$$

All the above values are in millimeters.

The diagrams for the input and output matching networks are shown in the following figures.

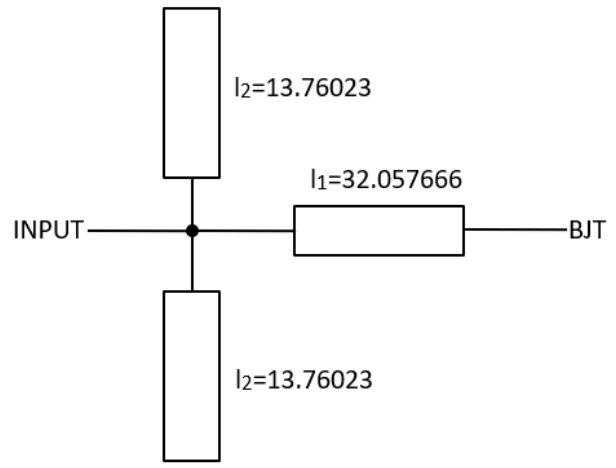

Figure 4: Diagram of Input Matching Network

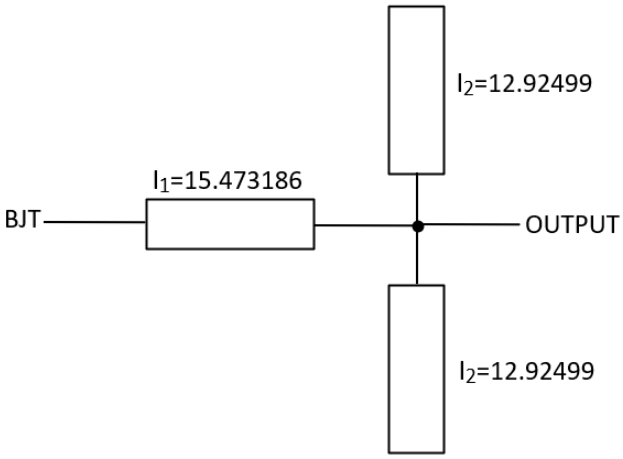

Figure 5: Diagram of Output Matching Network

3.4 DC Biasing

The transistor's collector-emitter current must be biased to 25mA and its collector-emitter voltage must be 8V. In order to determine the values of the DC bias resistors the following calculations were performed.

$$I_c = 25mA$$

$$V_{ce} = 8V$$

$$V_{BB} = 12V$$

$$V_{cc} = 12V$$

$$R_C = \frac{12 - 8}{25 \cdot 10^{-3}} = 67500\Omega$$

$$R_B = \frac{12 - 0.7}{\frac{I_C}{\beta}} = 160\Omega$$

3.5 RF Choke

The RF choke is used to prevent the small signal component from mixing with that of the DC biasing signal voltages. As indicated in the class, the length of the microstrip line should be as thin as possible (0.5mm according to the fabrication technology available) and a length of $\frac{\lambda_g}{4}$. This would give a length of 17.695775mm. On top of this, a 60 degree radical stub was used with a length as indicated in the AWR file.

4 Software Design

4.1 TXLINE Parameters

The AWR Microwave office computer aided design software was used to simulate the circuit and ensure the accuracy of our theoretical design. The parameters indicated above in the theoretical design were plugged into TXLINE to get the width of the transmission lines. The results are shown in the following figure.

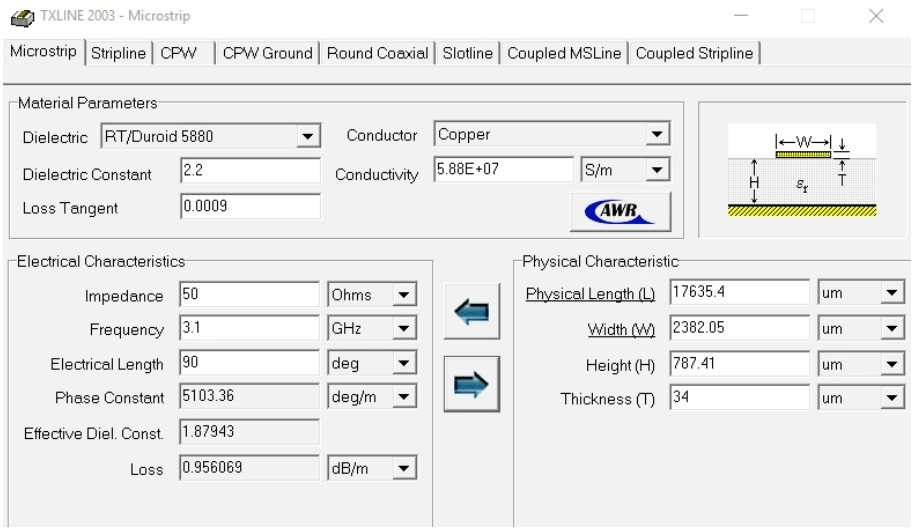

Figure 6: TXLINE Parameter Generation

4.2 DC Biasing

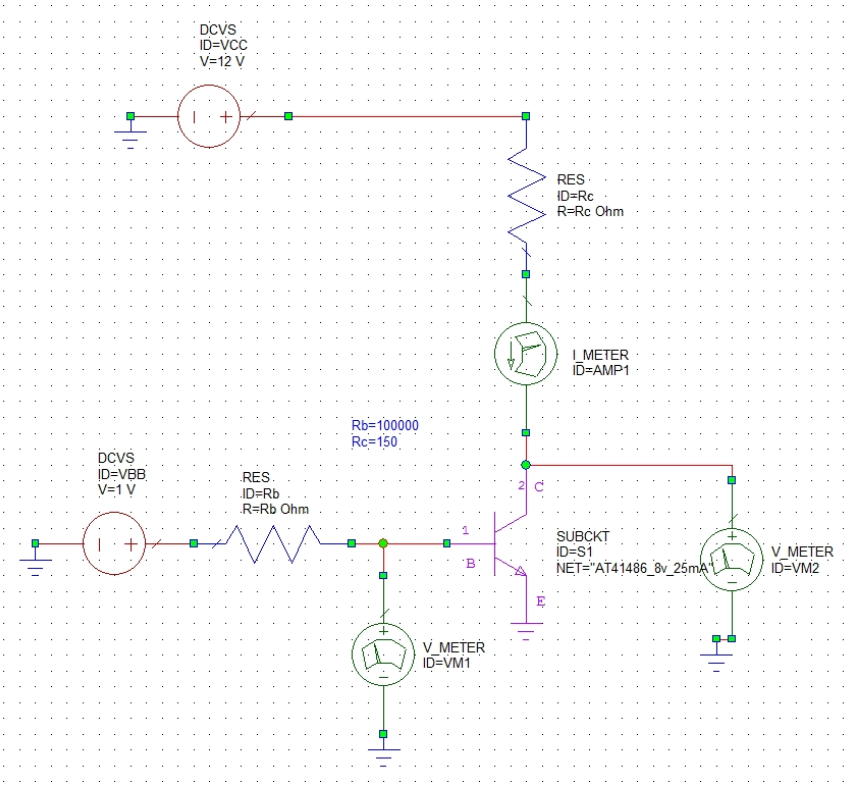

Figure 7: AWR Diagram of DC Biasing Circuit

In the DC biasing circuit, we were able to get the biasing parameters of collector current being 25mA and the voltage of the collector-emitter being 8 V using a V_{BB} of 1V, a V_{CC} of 12 volts as well as an R_c of 150 ohms and a R_b of 100000 ohms. When the circuit was actually constructed, we realized that the circuit simulation may be off for small Vbe and thus the other (one provided in the theoretical section) were chosen as the required voltage and resistance values.

4.3 Microwave Circuit

4.3.1 Input Matching Network

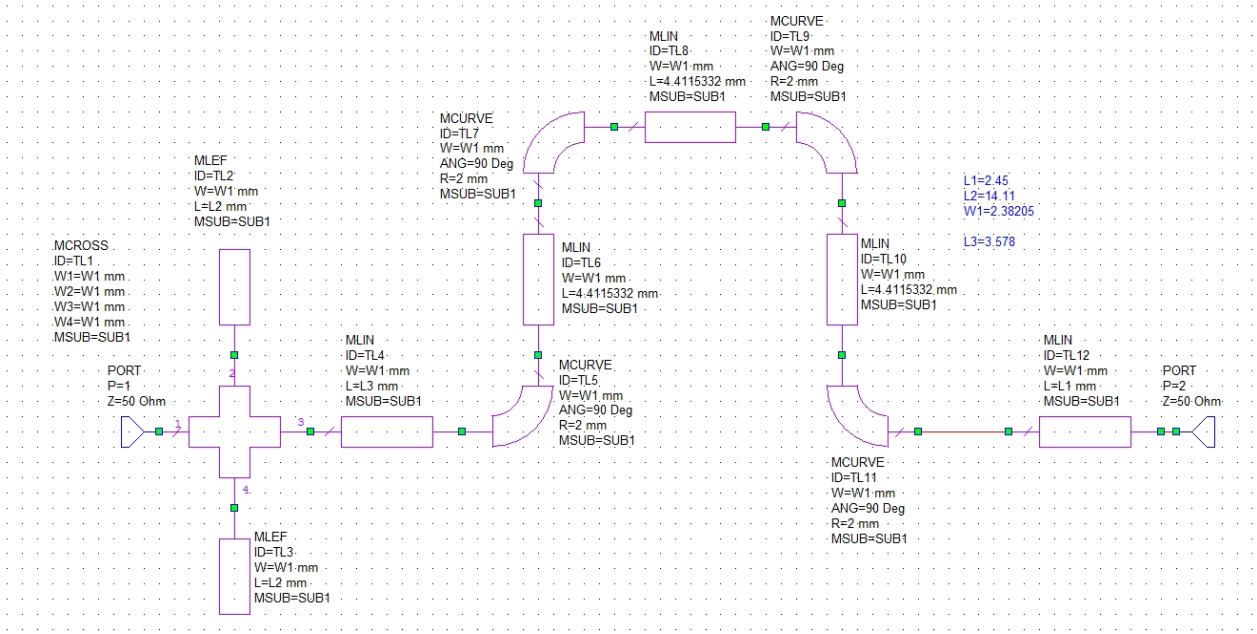

Figure 8: AWR Circuit for Input Matching Network

The circuit had to be curved in order to be able to fit it on the board. The circuit was tweaked from the given theoretical values such that the input port 2 can be matched. This matching was verified on a smith chart by making sure that the reflection coefficient seen looking into port 2 is that of gamma L. This is shown in the following figure.

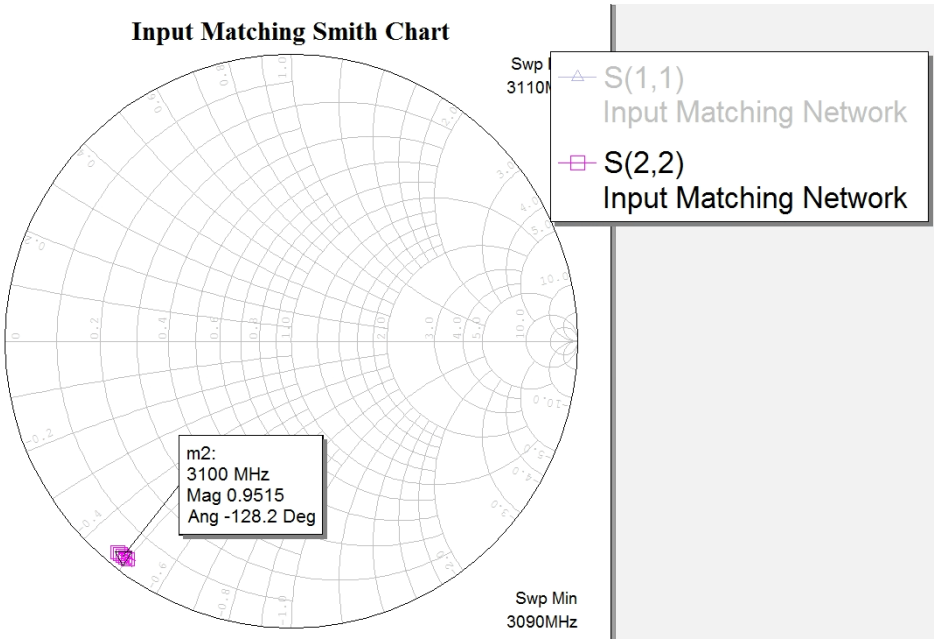

Figure 9: Smith Chart Verifying that the Input Circuit is Matched

4.3.2 Output Matching Network

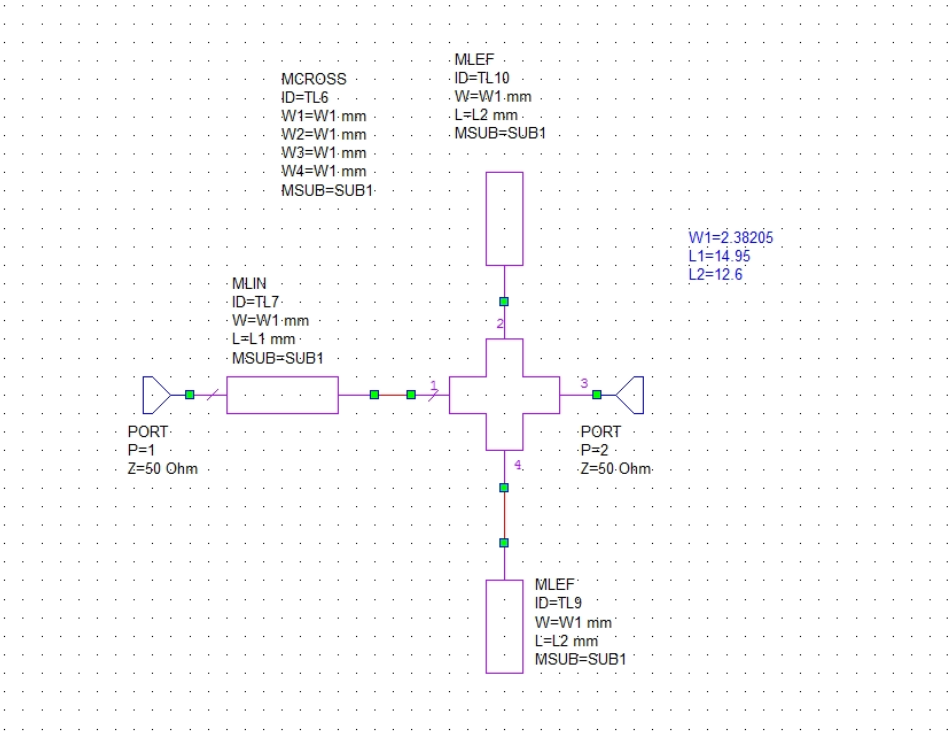

Figure 10: AWR Circuit for Output Matching Network

The circuit was tweaked in comparison to that of theoretical values in order to ensure that the reflection coefficient looking into port 1 is gamma S. This is verified using the proper smith chart shown below.

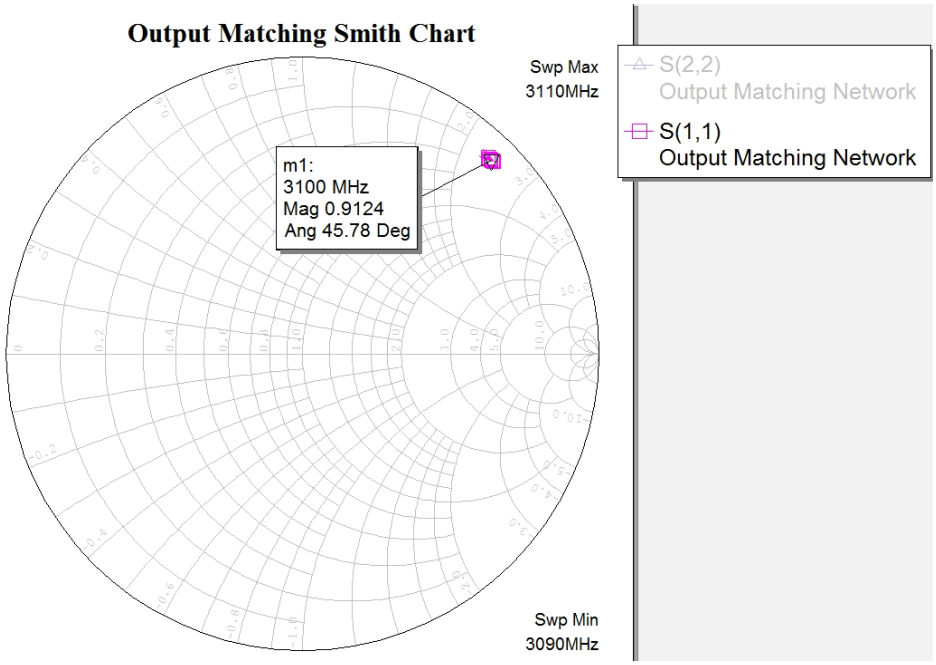

Figure 11: Smith Chart Verifying that the Output Circuit is Matched

4.3.3 RF Choke

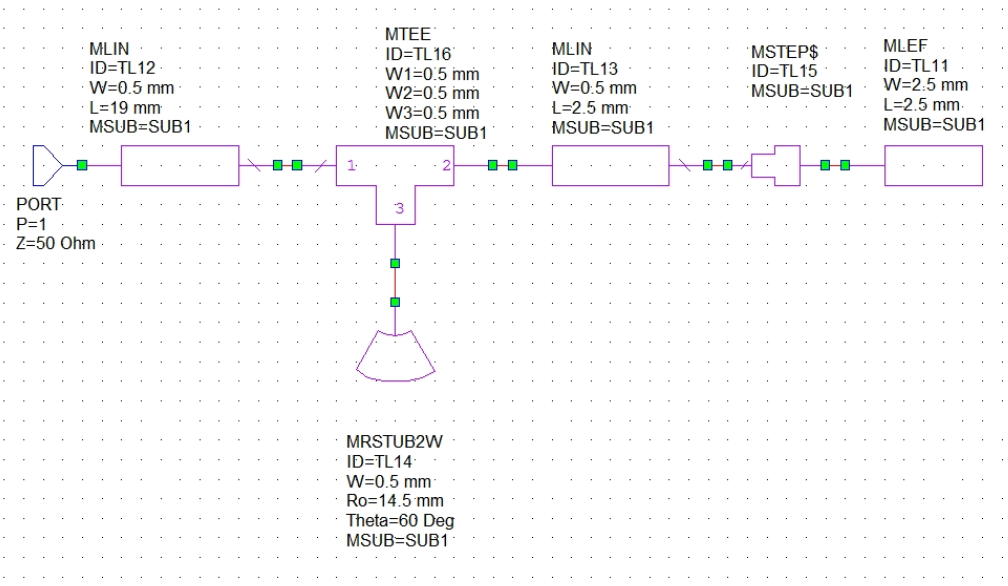

Figure 12: AWR Circuit for RF Choke

The design for the RF choke is shown in the above figure. In the original theoretical design, the RF choke had a length of $\frac{\lambda_g}{4}$. This was not used in the final design due to the fact that another value gave larger gain after the circuit was tweaked.

4.4 Complete Circuit

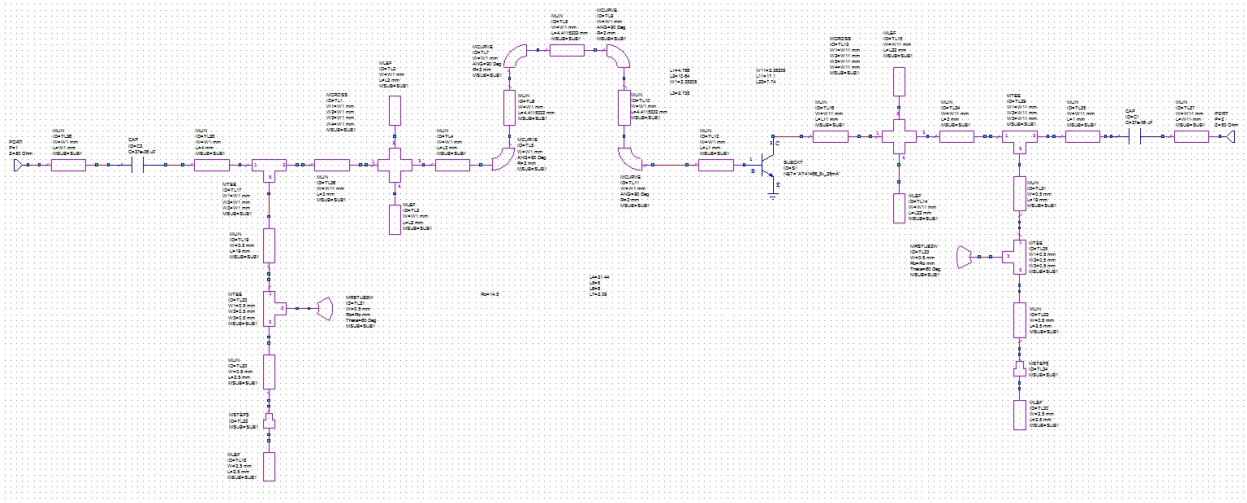

Figure 13: AWR Complete Circuit

The above diagram shows the final circuit schematic. Access lines had to be added such that the design can fit to the edge of the board (where it would then be connected to a coaxial line). To block the DC signal from coming in from the input signal, a capacitor of value 27 pF is used.

4.5 Optimization

Optimization had to be done for a variety of different reasons. One of the main reasons is that transmission lines are not perfectly transverse electromagnetic. They are also not entirely lossless. In addition to this, our theoretical design was not created using a bend in the line (which could have some effect on the resulting electromagnetic waves). Therefore, some tweaking had to be done to ensure that the entire system had a zero reflection coefficient at the input and that the gain was maximized.

The final results of the input and output matching networks are shown below.

Input Matching Network

-Shunt stub length: 10.64 mm

-Line length: 30.29 mm

Output Matching Network

-Shunt stub length: 7.74 mm

-Line length: 17.1 mm

4.6 Simulation

After the design had been tweaked, the final simulation results are shown in the following figure.

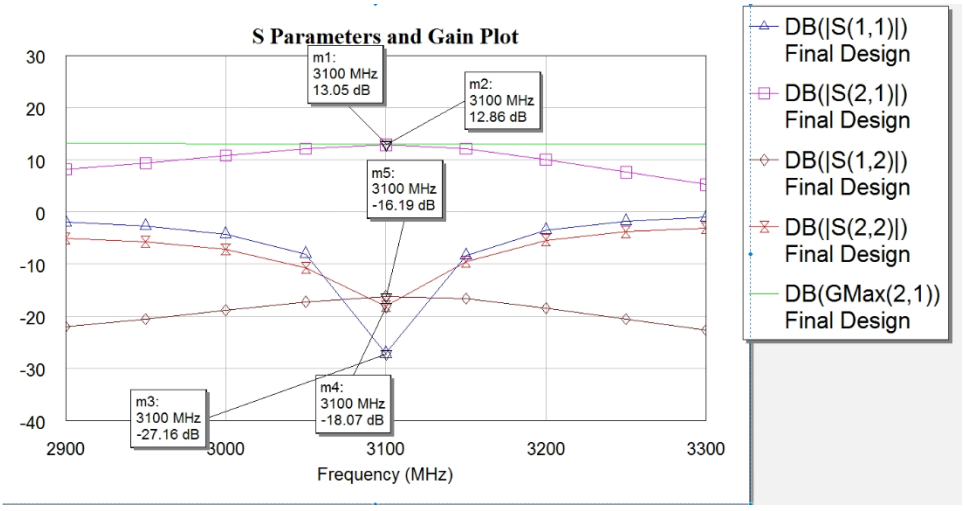

Figure 14: Scattering Parameters and Max Gain Results

The gain value matched fairly well to our theoretically calculated gain (which was about 13dB).

4.7 Layout

The layout for the design is shown in the following figure.

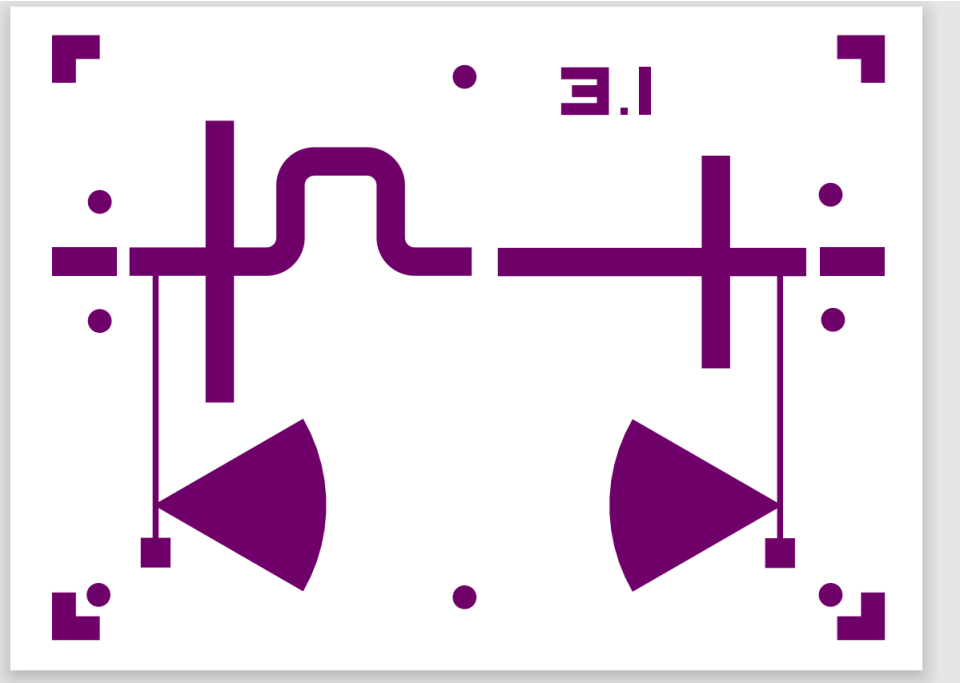

Figure 15: Layout of Circuit Generated by AWR MWO

5 Fabrication and Integration

The board was fabricated by the University of Ottawa's lab staff, Jean-Noel Nugu. It was constructed using a subtractive manufacturing process. In this process, one of two layers of copper is removed using an etching tool while the other is left intact. The two layers are separated by the material duroid 5880 dielectric. The other components were soldered onto the board. These components include the surface mount capacitors, the AT41486 transistor and two of the resistors used for biasing. In addition to this, the coaxial lines had to be soldered to the board. In regard to the BJT transistor, the emitter legs were soldered to the ground plane while the base was soldered to the left side and the emitter to the right. The board was screwed down to the jig. This created a solid ground connection for the board. The other leg of the resistor was connected to the end of the jig to create a solid connection.

The entire soldering job proved to be quite difficult. Many times, the legs of the transistors had popped off due to too much heat applied to them causing the transistor to be replaced couple times before testing. The soldering of the transistor also had to be soldered last while wearing a ground strap to prevent static shock from damaging it.

The diagram of the final soldered board and jig is shown in the following diagram.

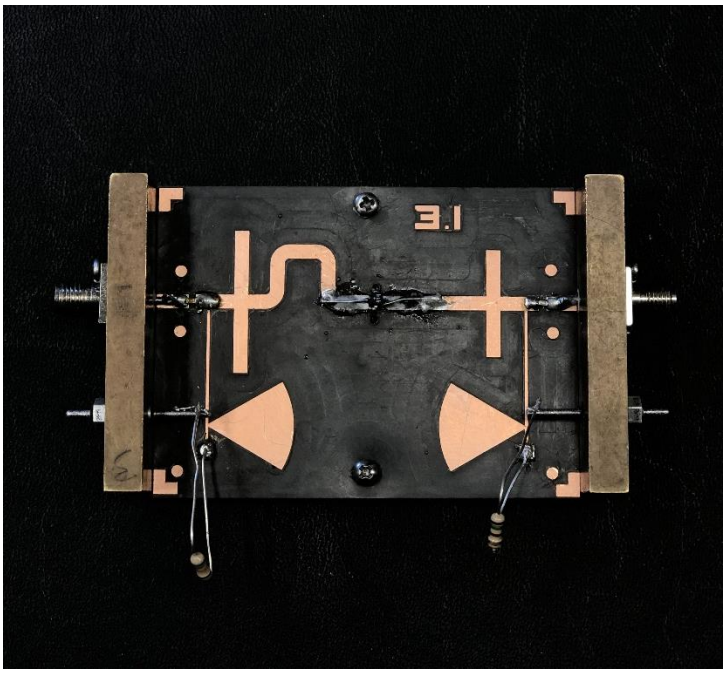

Figure 16: Final Board and Jig

6 Results

During the first iteration of the test on the Vector Network Analyzer there seemed to be no gain in the device. This was most likely due to the transistor being damaged, due to overheating or static shock. The board had to be built for a second time. During the second time, the board was able to be biased correctly under the required I_{ce} of 25mA and V_{ce} of 8V. When the board and the jig were tested there ended up being no gain as before. During that time, it was determined that the board was not properly secured to the jig. In doing this, the other transistor got damaged and had to be replaced. Finally, after reassembling the board and jig for the third time one was able to get the required results. That is, the transistor was able to be biased to 25mA and 8V with a gain as well as input return loss visible and resonant on the required frequency of 3.1 GHz.

The biasing result for the transistor is shown in the following figure.

Figure 17: Results of the Biasing of the Transistor

The results of the vector network analyzer are shown in the following diagram.

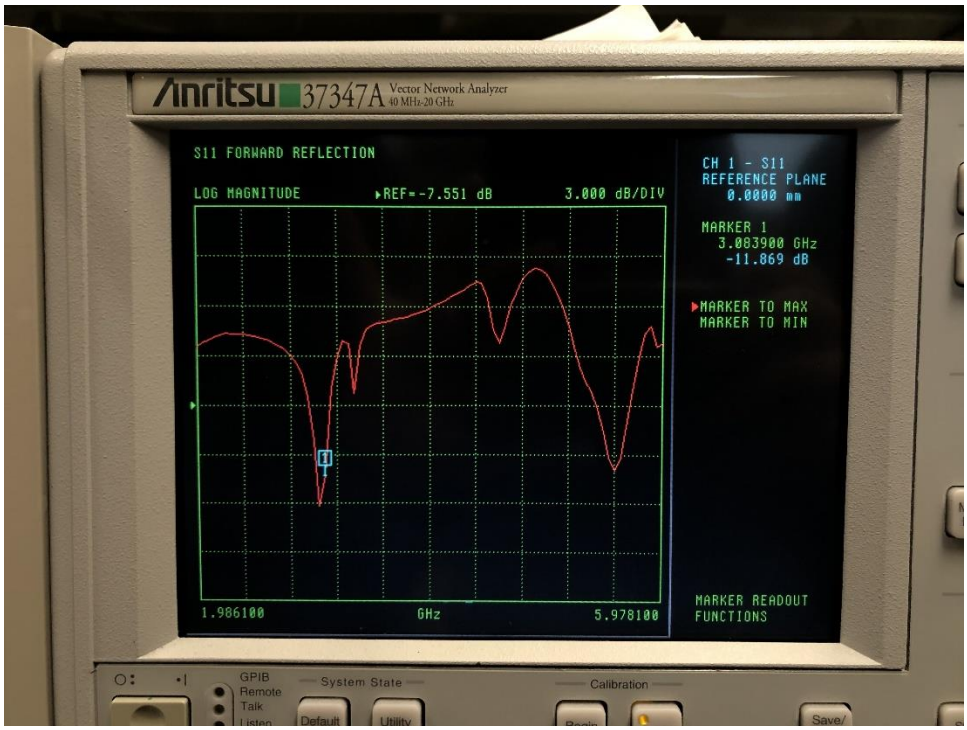

Figure 18: Results of the Vector Network Analyzer (S11 Parameter)

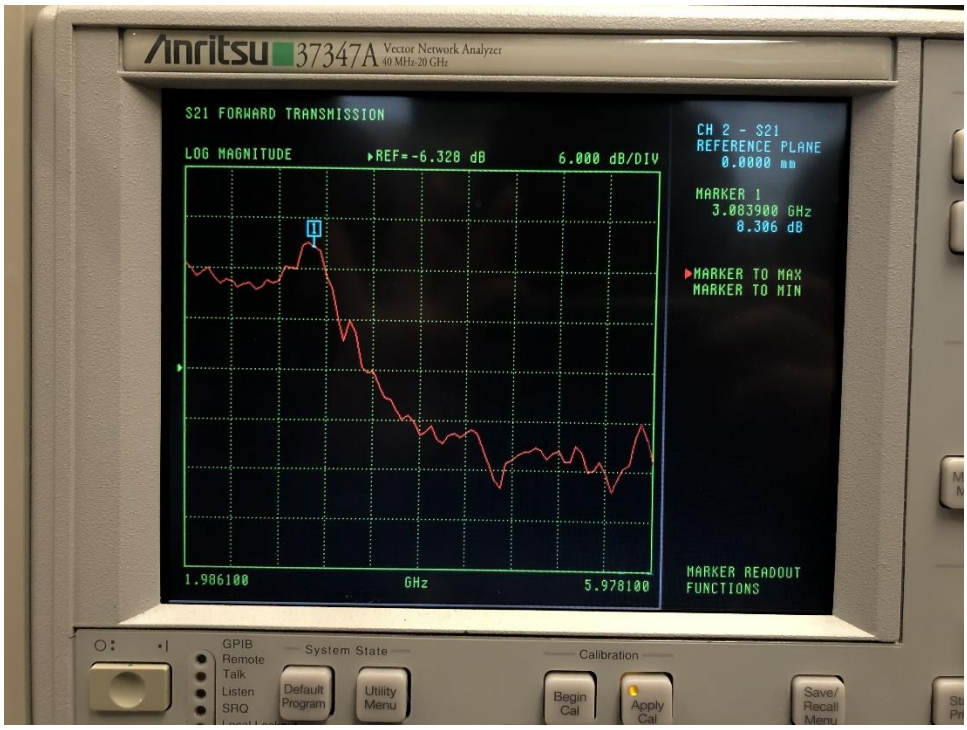

Figure 19: Results of the Vector Network Analyzer (Gain)

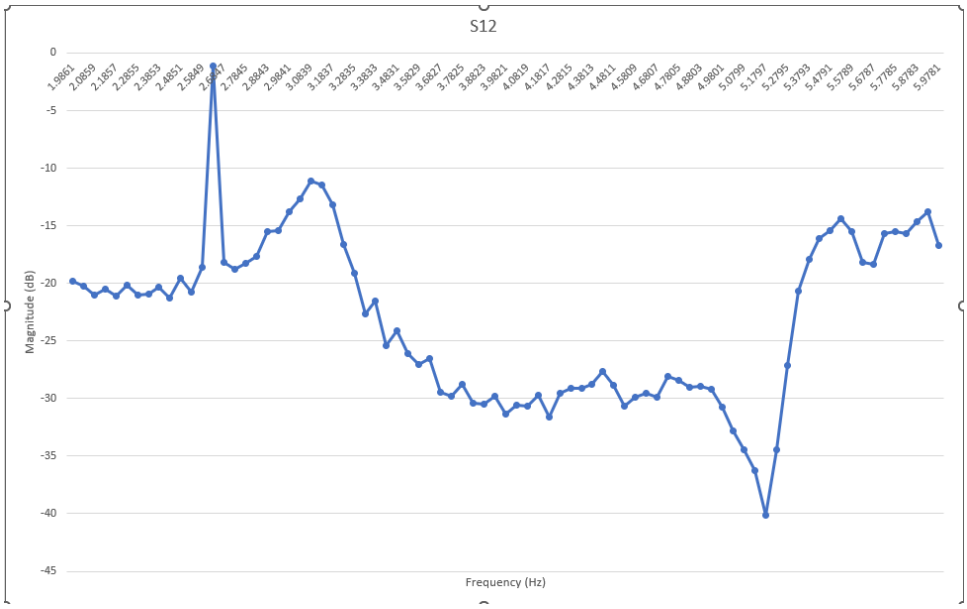

Figure 20: Results of the Vector Network Analyzer (S12)

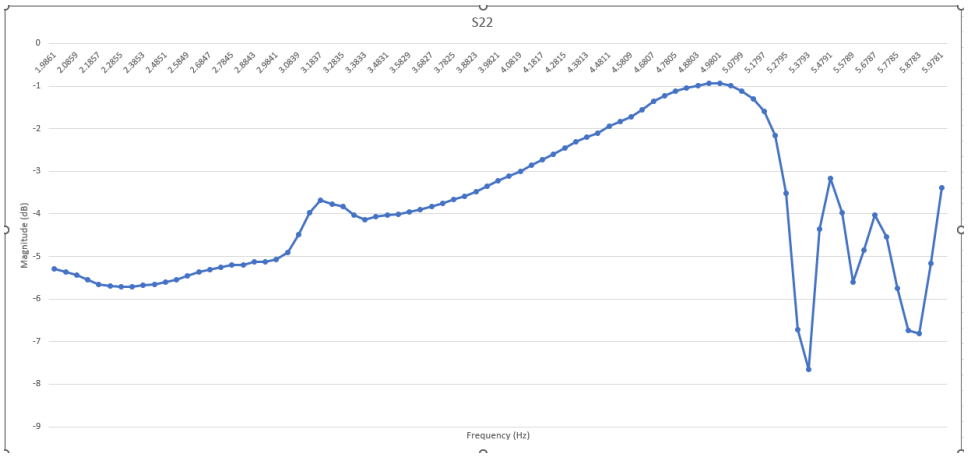

Figure 21: Results of the Vector Network Analyzer (S22)

As seen in figure 18, the S11 (input return loss) is resonant at the design frequency of 3.1 GHz. The results from the simulation determined that the required input return loss should be –27.16 dB while the measured results were only around –12dB. The discrepancy is most likely due to the input coaxial not being torqued properly. This is hypothesized since while the VNA was being torques to the coaxial inputs the results were jumping between the simulated value and the one shown above.

As seen in figure 19, the measured gain was determined to be 8.306 dB. This was off from the simulated one of about 13 dB. The reason for this can also be attributed to the hypothesis above.

7 Discussion and Improvements

The lab was an overall success despite the many hiccups that were faced in the construction of the board and soldering of the components. The setup of the board and jig was able to get reasonably passable results. Despite the success, there are still some things that could have been done differently.

One of the major successes was that the gain and input return loss (S11) were resonant at the required frequency of 3.1 GHz. Despite this, the values of these parameters were slightly off from the simulated results.

The main reason for this was hypothesized in the results section. The reason provided was that while screwing the leads of the VNA to the coaxial inputs of the board the results on the VNA were jumping between the simulated results and those given in the simulation portion of the report. As such, the leads of the VNA might not have made as good of a connection as they could have due to not torquing properly resulting in a gain that is not as high as it could have been.

In addition to this, the capacitors on either side of the board used for coupling the signal might not have made as good of a contact as it should. Before testing, a multimeter was used to determine if the capacitors were soldered properly to the board. In doing so the one side was able

to measure the required 27pF while the other was only able to be measured at a maximum of 10pF. This may not have been a problem; as in they could have been connected properly to being with and that it was just a measurement error since it was hard to place a large probe on a tiny strip.

8 Conclusion

In the end, one was able to achieve reasonable results that met the design criteria. One was able to go from design, to simulation, to tweaking, to fabrication and finally verification of results. This was all done using AWR and combined effort of the lab tech, TA, and the group itself.

9 References

Pozar, David M. Microwave Engineering. Hoboken, NJ: Wiley, 2012