AN2728
Application note

ST1S12
small synchronous buck converter

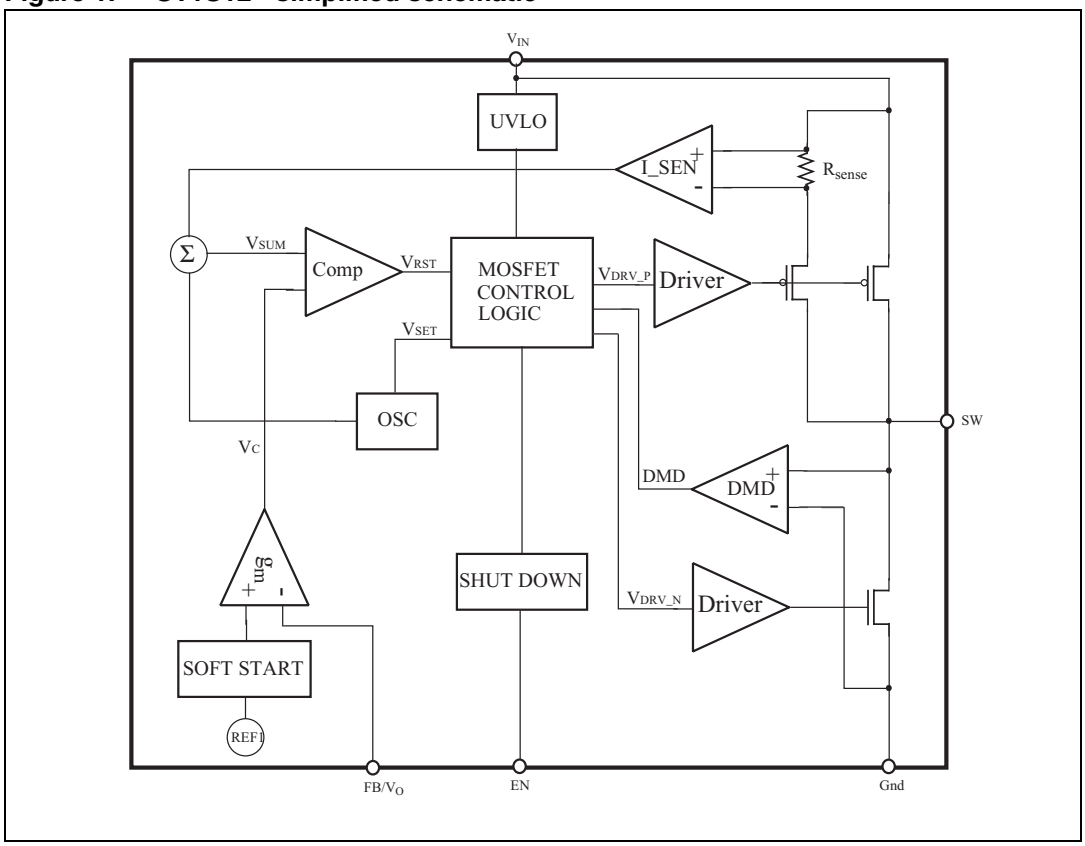
Introduction

The ST1S12 family of synchronous step-down DC-DC converters optimized for powering low-voltage digital cores in HDD applications is generally used to replace the high-current linear solution when the power dissipation may cause high heating of the application environment. It provides up to 0.7 A over an input voltage range of 2.5 V to 5.5 V.

A high switching frequency (1.7 MHz) allows the use of tiny surface-mount components. A resistor divider to set the output voltage value, an inductor, and two capacitors are required for the adjustable version. Only an inductor and 2 capacitors are needed for the 1.2 V and 1.8 V fixed version. A low output ripple is guaranteed by the current mode PWM topology and by the use of low ESR surface-mount ceramic capacitors.

The device is thermal protected and current limited to prevent damages due to accidental short-circuit. This family of products is available in the TSOT23-5L package.

Figure 1. ST1S12 - simplified schematic



Contents

1 **ST1S12 description 4**

1.1 Enable function 5

1.2 Current limit and short-circuit protection 6

2 **Selecting components for your applications 7**

2.1 Output voltage selection 7

2.2 Input capacitor 8

2.3 Output capacitor 9

2.4 Inductor 9

2.5 Layout considerations 10

3 **Thermal considerations 11**

4 **Demonstration board usage recommendation 13**

4.1 External component selection 14

4.2 Capacitors selection 14

4.3 Inductor selection 15

5 **Bill of materials 17**

6 **Recommended footprint 18**

7 **Revision history 19**

List of figures

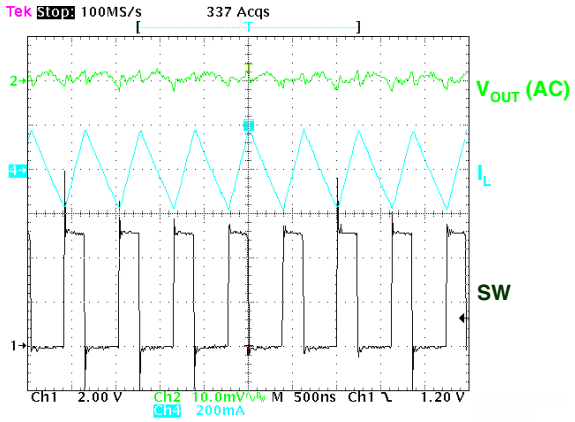
Figure 1. ST1S12 - simplified schematic . . . 1
Figure 2. Inductor current at no load . . . 4
Figure 3. Inductor current at medium load . . . 4
Figure 4. Inrush current . . . 4
Figure 5. Enable voltage vs. temperature . . . 5
Figure 6. Short-circuit protection simplified schematic . . . 6
Figure 7. Typical application schematic . . . 7
Figure 8. Drop vs. temperature . . . 7
Figure 9. Feedback voltage vs. temperature . . . 8
Figure 10. Layout considerations . . . 10
Figure 11. ST1S12 demonstration board layout . . . 13
Figure 12. Demonstration board layers . . . 13
Figure 13. Demonstration board schematic . . . 14
Figure 14. Efficiency vs. output current . . . 15
Figure 15. Efficiency vs. output voltage . . . 15
Figure 16. Efficiency vs. inductor at V_O = 1.8 V . . . 16
Figure 17. Efficiency vs. inductor at V_O = 3.3 V . . . 16
Figure 18. Efficiency vs. input voltage . . . 16
Figure 19. TSOT23-5L footprint dimensions . . . 18

1 ST1S12 description

The ST1S12 is an adjustable current mode PWM synchronous step-down DC-DC converter with an internal 0.7 A power switch. It is a complete 0.7 A switching regulator with internal compensation which eliminates the need for additional components.

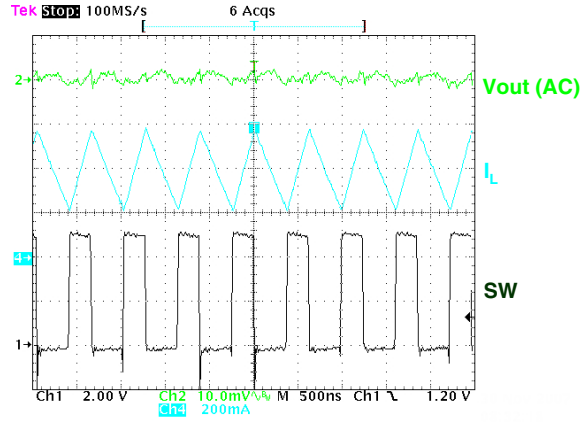
The device operates with typically 1.7 MHz fixed frequency, and in order to guarantee the lowest switching ripple, operates in pulse width modulation (PWM) mode even at low-load condition. (*Figure 2* and *Figure 3*)

Figure 2. Inductor current at no load



$V_{EN}=V_{IN}$=5 V, V_{OUT}=1.8 V, no load, CH1=SW, CH2=V_{OUT}, CH4=I_L

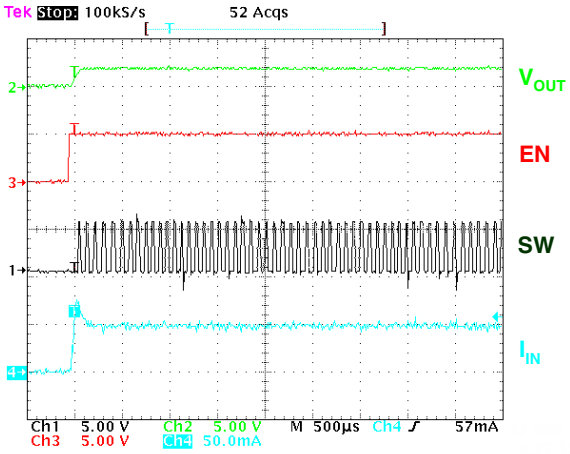
Figure 3. Inductor current at medium load



$V_{EN}=V_{IN}$=5 V, V_{OUT}=1.8 V, R_{LOAD}=4.7 Ω, CH1=SW, CH2=V_{OUT}, CH4=I_L

To clamp the error amplifier reference voltage, a soft-start control block generating a voltage ramp is implemented. When switching on the power supply, it allows controlling the inrush current value (*Figure 4*).

Figure 4. Inrush current



$V_{EN}=V_{IN}$=5 V, V_{OUT}=1.8 V, R_{LOAD} =15 Ω, Ch1=SW, CH2=V_{OUT}, CH3=EN, CH4=I_{IN}

Other protection circuits in the device are the thermal shutdown block which turns off the regulator when the junction temperature exceeds 150 °C (typ.) and the cycle-by-cycle current limiting that provides protection against shorted outputs.

The few components required for operation of the device are an inductor, two capacitors, and a resistor divider. The inductor chosen must be capable of withstanding peak current level without saturating. The value of the inductor should be selected keeping in mind that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be chosen when it is important to reduce the package size and the total application cost. The ST1S12 has been designed to work properly with X5R or X7R SMD ceramic capacitors both at the input and at the output. These types of capacitors, thanks to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used according to the need of the application without compromising the right functioning of the device.

Finally, if the input voltage falls close to the output voltage, the ST1S12 can run at 100 % duty cycle, in this mode the PMOS switch is continuously maintained ON. In this case the output voltage value is the input voltage minus the voltage drop across the PMOS switch and the resistance of the inductor.

The minimum input voltage to guarantee the right output voltage is:

$$V_{IN_MIN} = I_{OUT_MAX} \times (R_{DS(on)_P} + DCR_L) + V_{OUT}$$

where DCR_L is DC resistance of the inductor and $R_{DS(on)_P}$ is the resistance of the PMOS.

Due to the high switching frequency and peak current, it is important to optimize the application environment such as reducing the length of the PCB traces and placing all external components near the device.

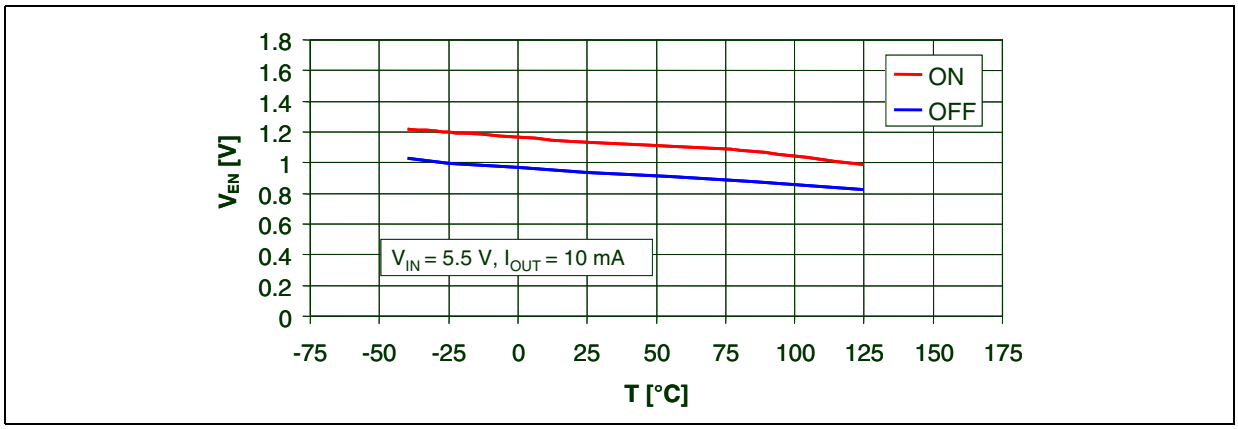
1.1 Enable function

The ST1S12 features an enable function (pin 1). When the EN voltage is higher than 1.5 V the device is ON and if it is lower than 0.5 V the device is OFF, *Figure 5* shows the enable voltage vs temperature. In shutdown mode consumption is lower than 1 µA.

The EN pin does not have an internal pull-up, which means that the enable pin cannot be left floating.

If the enable function is not used, the EN pin must be connected to V_{IN}.

Figure 5. Enable voltage vs. temperature

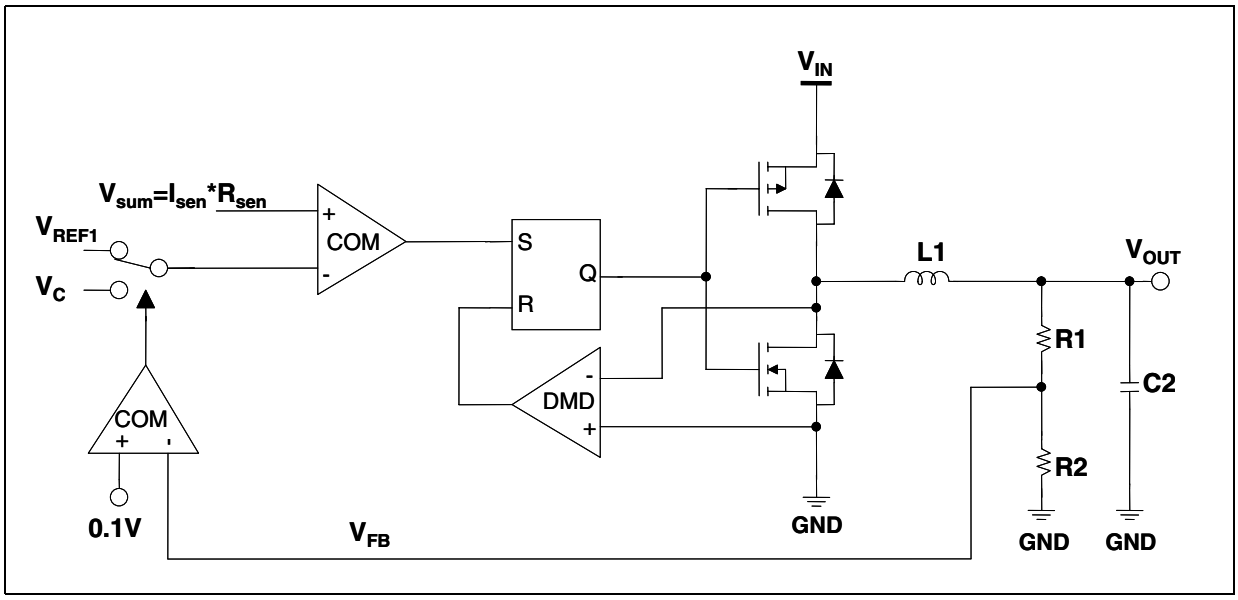


1.2 Current limit and short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit, the device reduces t_{ON} down to its minimum value. In these conditions, the duty cycle is strongly reduced and, in most applications, this is enough to limit the current to I_{lim}.

In case of heavy short-circuit when the feedback voltage is lower than 0.1 V (typ.), the loop switches to short mode automatically. In this condition the voltage $V_{sum}=I_{sen} * R_{sen}$ is compared with 0.4 V (typ.) to clamp the upper limit of the inductor current. In this condition the maximum output limitation current is reduced to 300 mA instead of 1 A. At the same time the DMD circuit clamps the lower boundary of the inductor current. One RS flip-flop is being used to control the PMOS and NMOS switches. When the feedback voltage is higher than 0.1 V (typ.) voltage, the device returns to normal closed-loop switching operation (*Figure 6*).

Figure 6. Short-circuit protection simplified schematic

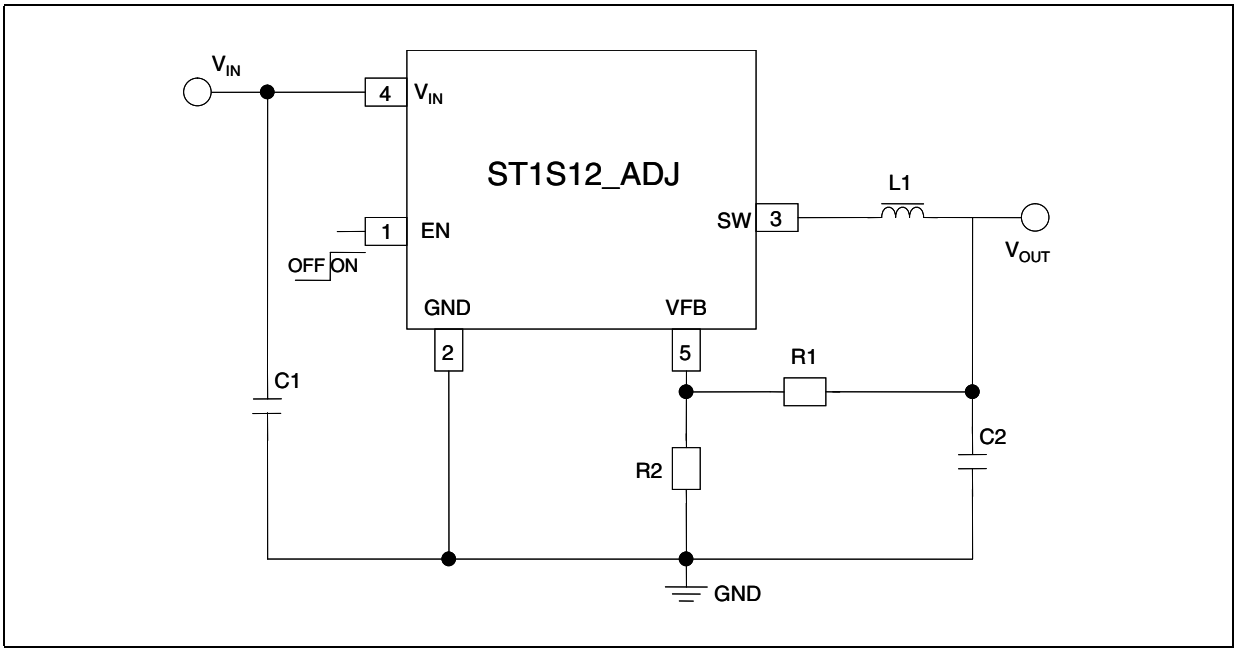


2 Selecting components for your applications

This section provides information to assist in the selection of the most appropriate components for your applications.

Figure 7 shows the typical application schematic.

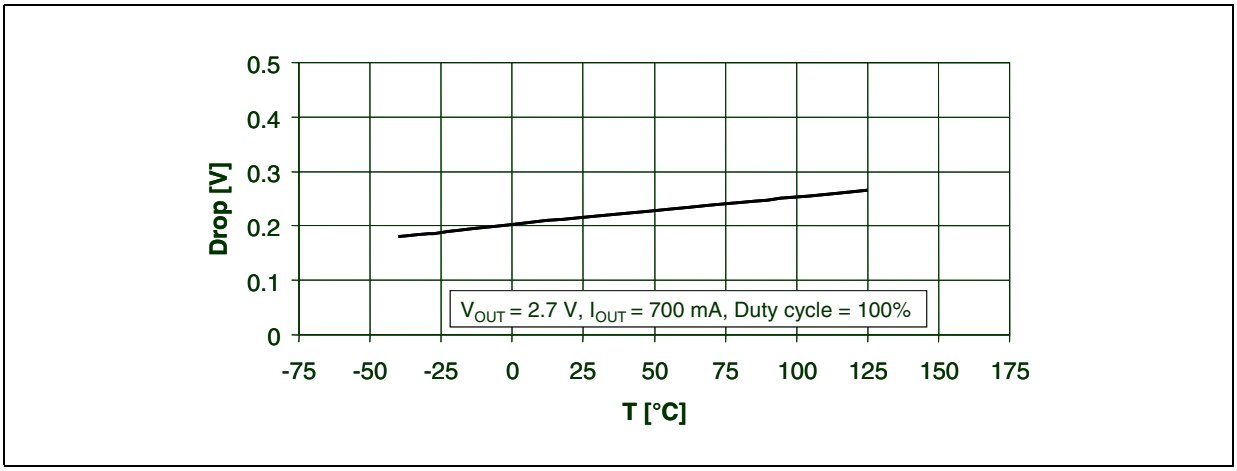
Figure 7. Typical application schematic



2.1 Output voltage selection

The output voltage can be adjusted from 0.6 V up to input voltage (D_{MAX} = 100 %) minus the voltage drop across the PMOS switch and the DC resistance of the inductor by connecting a resistor divider between the V_{FB} pin and the output, thus allowing remote voltage sensing.

Figure 8. Drop vs. temperature



You must choose the resistor divider according to the following equation:

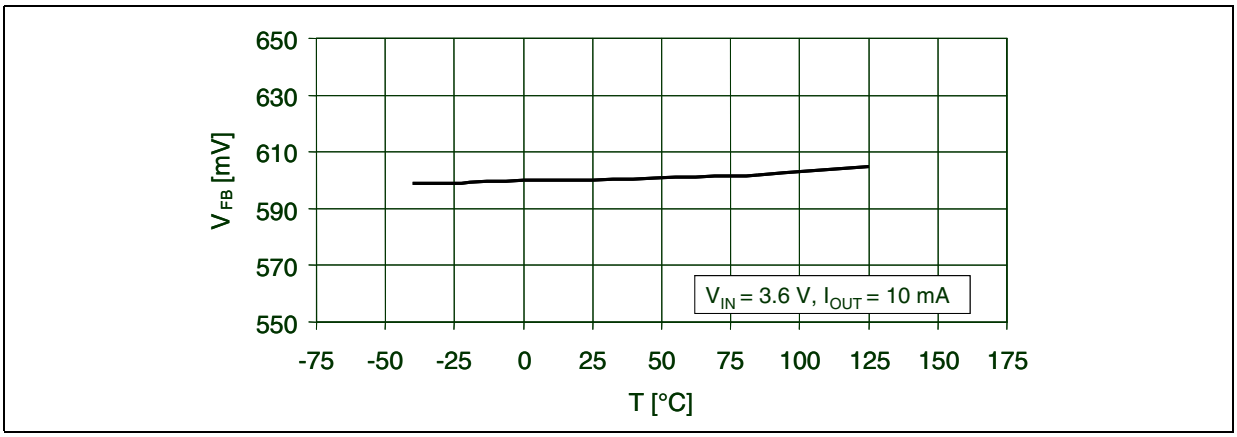
Equation 1

$$V_{OUT} = V_{FB}\left[1+\frac{R_1}{R_2}\right]$$

with V_{FB} = 0.6 V.

Figure 9 shows the feedback voltage versus temperature.

Figure 9. Feedback voltage vs. temperature



We suggest using a resistor with values in the range of 10 kΩ to 100 kΩ Lower values are suitable as well but increase current consumption.

For output voltages close to the feedback voltage, we suggest adding a very small capacitor in parallel with R_1 in the range of 10 pF. As an alternative, we suggest increasing the current in the resistor divider by decreasing the R_1 and R_2 value.

2.2 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb switching current that can be as high as the load current divided by two (worst case, with duty cycle of 50 %). For this reason, the quality of these capacitors has to be very high to minimize its power dissipation generated by the internal ESR, thus improving the system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

Equation 2

$$I_{RMS} = I_{OUT} \times \sqrt{D - \frac{2 \times D^2}{\eta} + \frac{D^2}{\eta}}$$

where η is the expected system efficiency, D is the duty cycle and I_{OUT} the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_{OUT} divided by 2 (considering η= 1).

The maximum and minimum duty cycles are:

Equation 3

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 4

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

where V_F it is the voltage drop across the internal NMOS and V_{SW} the voltage drop across the internal PMOS. Considering the range D_{MIN} to D_{MAX} it is possible to determine the maximum I_{RMS} flowing through the input capacitor.

The use of ceramic capacitors with voltage ratings in the range of 1.5 times the maximum output voltage is recommended.

2.3 Output capacitor

The output capacitor is very important to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the coil, but increases the current ripple. So, in order to reduce the output voltage ripple a low ESR capacitor is required. The output voltage ripple (V_{OUT_RIPPLE}) is:

Equation 5

$$V_{OUT_RIPPLE} = \Delta I \times \left[ESR + \frac{1}{8 \times C_{OUT} \times F_{SW}} \right]$$

where Δ I is the ripple current and F_{SW} is the switching frequency.

The use of ceramic capacitors with voltage ratings in the range of 1.5 times the maximum output voltage is recommended.

2.4 Inductor

The inductor value is very important because it fixes the ripple current flowing through output capacitor. The ripple current is usually fixed at 20-40 % of I_{OUT_MAX}, that is 0.14-0.28 A with I_{OUT_MAX} = 0.7 A. The inductor value is approximately obtained by the following formula:

Equation 6

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D x T.

The peak current through the inductor is given by:

Equation 7

$$I_{PK} = I_{OUT} + \frac{\Delta I}{2}$$

It can be observed that if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. So, for fixed peak current protection, higher value of the inductor permits a higher value of the output current.

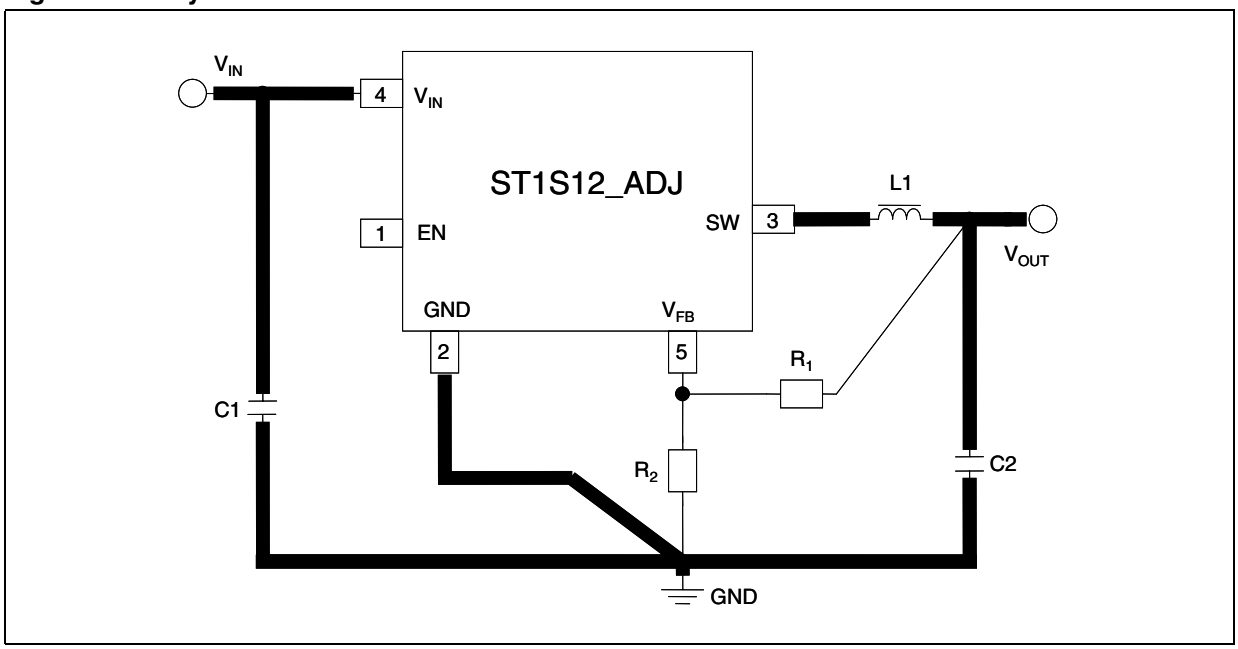
2.5 Layout considerations

Due to the high switching frequency and peak current, the layout is an important design step for all switching power supplies. If the layout is not carefully done, important parameters such as efficiency and output voltage ripple could be compromised.

Short, wide traces must be implemented for main current and for power ground paths as shown in bold in *Figure 10*. The input capacitor must be placed as close as possible to the device pins as well as the inductor and output capacitor.

A common ground node minimizes ground noise, as shown in *Figure 10*.

Figure 10. Layout considerations



3 Thermal considerations

The dissipated power of the device is determined by three different factors:

- Switch losses due to the non-negligible $R_{DS(on)}$. These are equal to:

Equation 8

$$P_{ON_P} = R_{DS(on)_P} \times I_{OUT}^2 \times D$$

and

Equation 9

$$P_{ON_N} = R_{DS(on)_N} \times I_{OUT}^2 \times (1 - D)$$

where D is the duty cycle of the application.

Note: The duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but in practice it is significantly higher than this value in order to compensate for the losses of the overall application. Due to this reason, the switching losses related to the $R_{DS(on)}$ increase compared to an ideal case.

- On and off switching losses. These are given by the following relation:

Equation 10

$$P_{SW} = V_{IN} \times I_{OUT} \times \frac{(T_{ON} + T_{OFF})}{2} \times F_{SW} = V_{IN} \times I_{OUT} \times T_{SW} \times F_{SW}$$

where T_{ON} and T_{OFF} are the overlap times of the voltage across the power switch and the current flowing into it during the turn-on and turnoff phases. T_{SW} is the equivalent switching time.

- Quiescent current losses:

Equation 11

$$P_Q = V_{IN} \times I_Q$$

where I_Q is the quiescent current.

The overall losses are:

Equation 12

$$P_{TOT} = R_{DS(on)_P} \times I_{OUT}^2 \times D + R_{DS(on)_N} \times I_{OUT}^2 \times (1 - D) + V_{IN} \times I_{OUT} \times T_{SW} \times F_{SW} + V_{IN} \times I_Q$$

When the device operates at V_{OUT} close to V_{IN} (high duty cycle) the power dissipated can be approximated by:

Equation 13

$$P_{TOT} = R_{DS(ON)_P} \times I_{OUT}^2 + V_{IN} \times I_Q$$

The junction temperature of device is:

Equation 14

$$T_J = T_A + R_{thJA} \times P_{TOT}$$

where T_A is the ambient temperature and R_{thJA} is the junction-to-ambient thermal resistance.

4 Demonstration board usage recommendation

The demonstration board shown in *Figure 11* is provided with Kelvin connection, which means that two lines are available for each pin. One used for supplying or sinking current (V_{OUT_F} and V_{IN_F}) and the other (V_{OUT_S} and V_{IN_S}) used to perform the needed measurement.

Figure 11. ST1S12 demonstration board layout

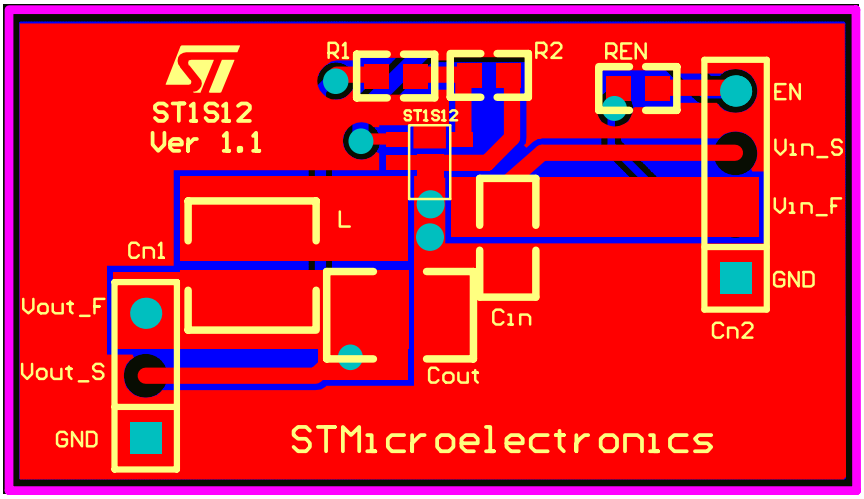
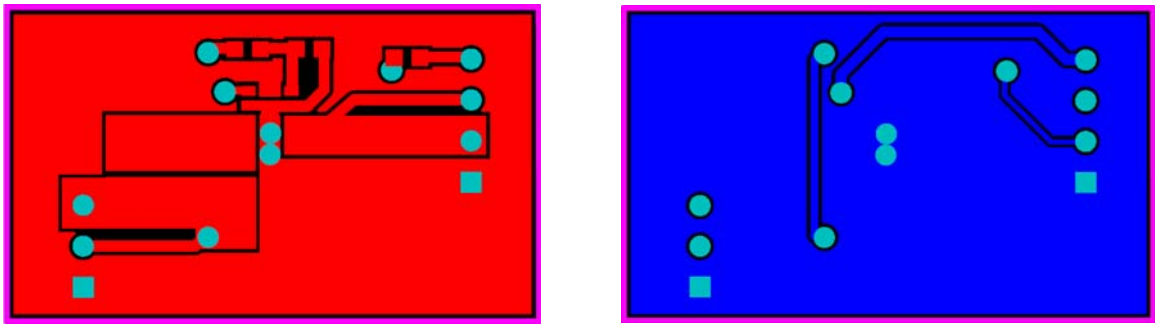


Figure 12. Demonstration board layers



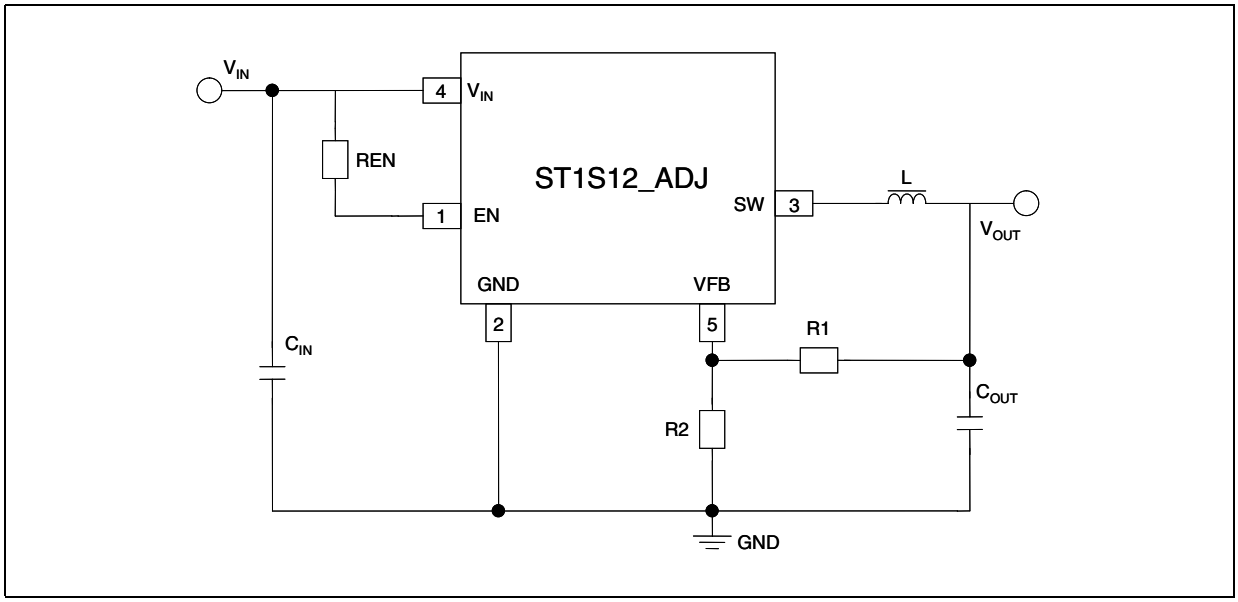
Top layer **Bottom layer**

The board has one enable pin available which is located on the right side of the board. This pin can be used to supply the enable pin with a external voltage higher than 1.5 V to turn on or lower than 0.5 V to turn off the device.

4.1 External component selection

Figure 13 shows the demonstration board schematic.

Figure 13. Demonstration board schematic



The R_{EN} is used to pull up the EN pin to V_{IN}. We suggest using a resistor with a value in the range of 500 kΩ to 1 MΩ in order to reduce current consumption.

In order to obtain the needed output voltage, the resistor divider must be selected in accordance with the following formula:

Equation 15

$$V_{OUT} = V_{FB}\left[1+\frac{R_1}{R_2}\right]$$

with V_{FB} = 0.6 V.

Table 1. Recommended resistor divider

V_{OUT}	R_1	R_2
1.2 V	68 kΩ	68 kΩ
3.3 V	68 kΩ	15 kΩ

The resistors given in *Table 1* are good choices in terms of current consumption.

4.2 Capacitors selection

It is possible to use any X5R or X7R ceramic capacitor:

- C_{IN} = 4.7 µF (ceramic) or higher
- C_{OUT} = 10 µF (ceramic) or higher

It is possible to put several capacitors in parallel in order to reduce the equivalent series resistance and improve the ripple present in the output voltage.

4.3 Inductor selection

Due to the high switching frequency (1.5 MHz) it is possible to use very small inductor values. In this board the device was tested with inductors in the range of 1 µH to 10 µH, with very good efficiency performances (see *Figure 14* and *15*).

As the device is able to provide an operative output current of 0.7 A, the use of inductors capable of managing at least 1.5 A is strongly recommended.

Figure 14. Efficiency vs. output current

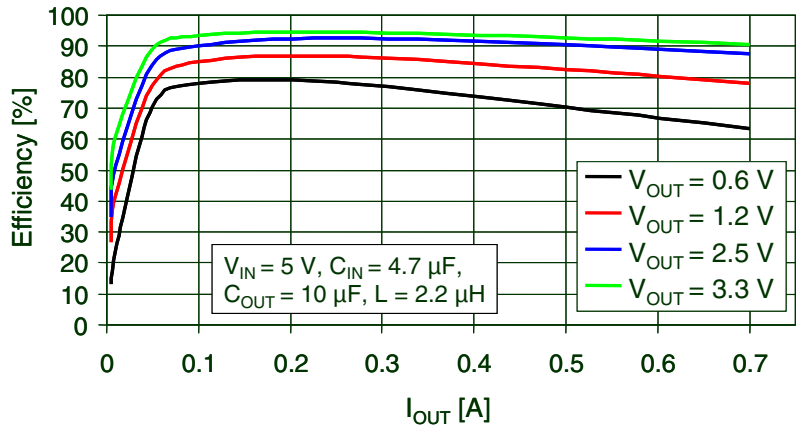


Figure 15. Efficiency vs. output voltage

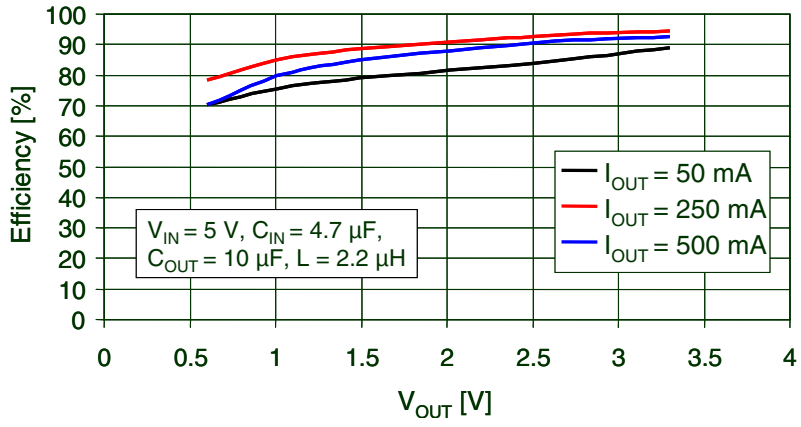


Figure 16. Efficiency vs. inductor at V_O = 1.8 V

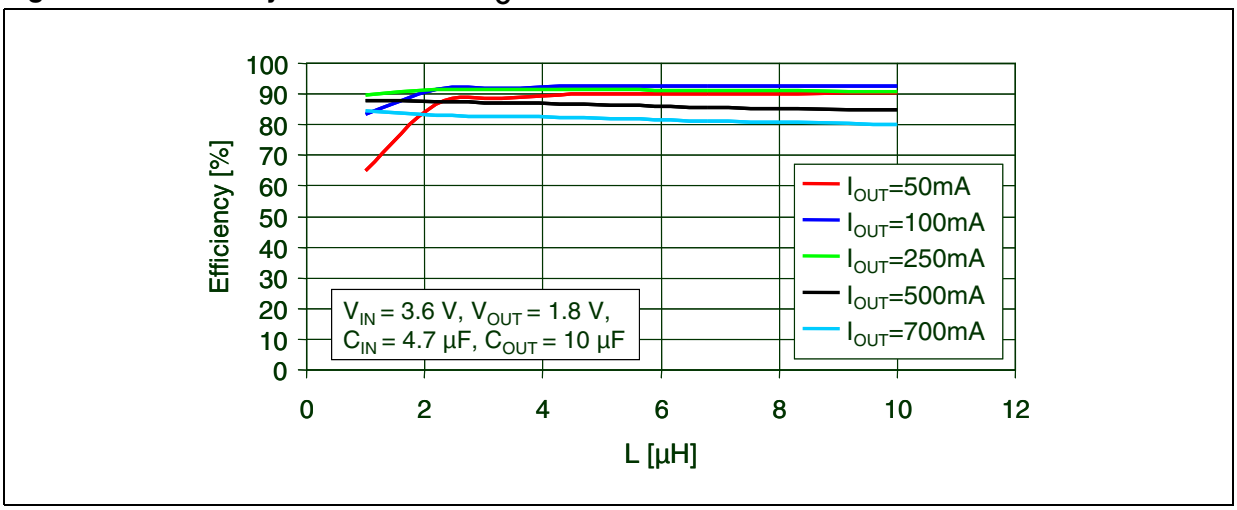


Figure 17. Efficiency vs. inductor at V_O = 3.3 V

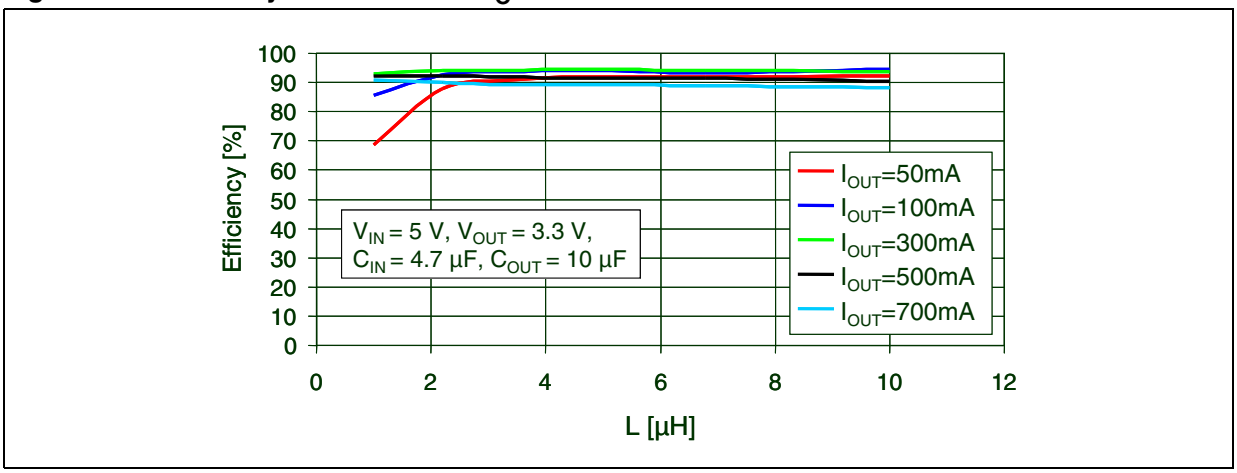
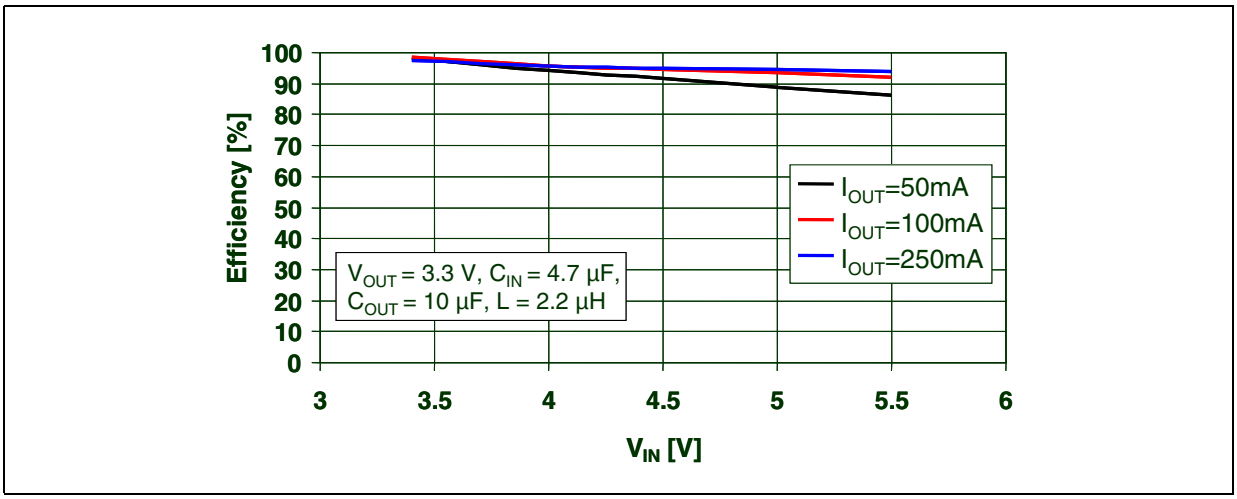


Figure 18. Efficiency vs. input voltage



5 Bill of materials

Table 2. Bill of materials with most common components

Name	Value	Material	Manufacturer	P/N
C_{IN}	4.7µF	Ceramic	Murata	GRM21BR61E475KA12B
C_{OUT}	10µF	Ceramic	Murata	GRM21BR61A106KE19L
			Murata	GRM31CR61E106KA12B
L	2.2µH		Coilcraft	LPS4018-222MLB
			Coiltronics	DR73-2R2
REN	1MΩ			

6 Recommended footprint

Figure 19. TSOT23-5L footprint dimensions

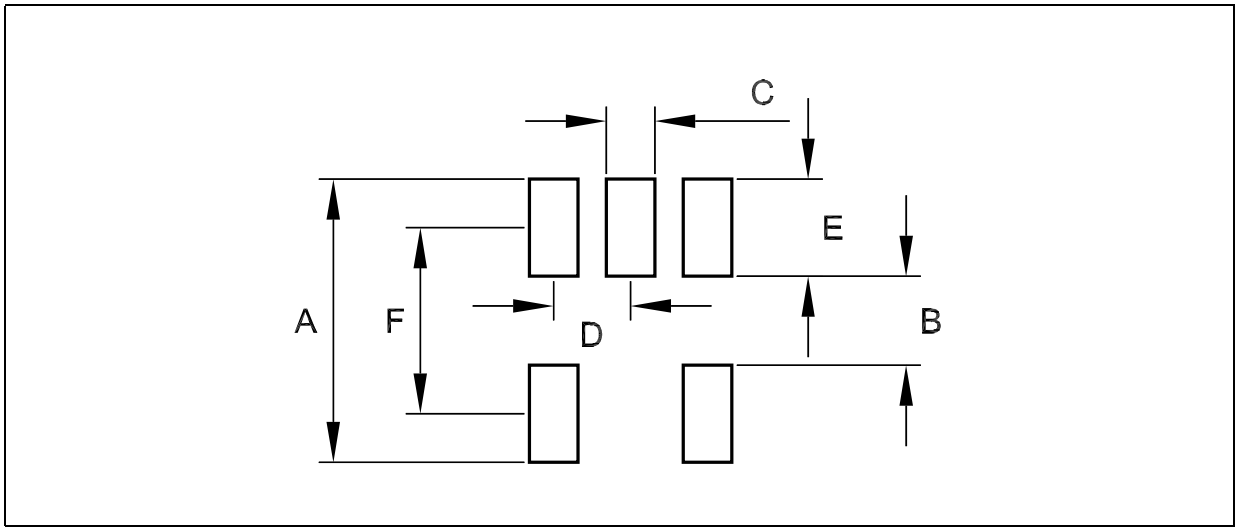


Table 3. Footprint data

Values		
Dim.	**mm.**	**in.**
A	3.50	0.138
B	1.10	0.043
C	0.60	0.024
D	0.95	0.037
E	1.20	0.047
F	2.30	0.090

7 Revision history

Table 4. Document revision history

Date	Revision	Changes
22-Apr-2008	1	Initial release.

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