Justin Shaytar

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Professional Summary

I am a Computer Engineering BS student pursuing challenging and interesting full-time employment in **FPGA Engineering** post-graduation. I have over **2 years of experience** in **VHDL, Python, SystemVerilog, TCL, and C**.

Education

Rochester Institute of Technology (3.82 GPA) — Rochester, NY
Bachelor of Science in Computer Engineering — *Aug 2019 - May 2024*

Work Experience

FPGA Engineer Coop — Jan. 2022 - June 2022, Jan. 2023 - Current
Mastodon Design, LLC, a CACI Company — *Rochester, NY*

- Engineered **IP** module for real-time display of values for **SPI, GPIO, AXIS, and I2C** data transmission protocols. Integrated with **PuTTY** terminal, facilitating advanced hardware debugging across diverse product lines using **VHDL**.
- Led **FPGA** efforts in enhancing an existing product with new functionality, collaborating with **Software** Engineers.
- Developed **15** intricate self-checking **SystemVerilog** simulations for diverse **IP** components located within a **GitLab** submodule for consistent utilization across projects.
- Created a **Python** script to generate **SystemVerilog** testbenches for **VHDL** files, enhancing development efficiency.
- Wrote a **Python** script to automate locating and running simulations in a designated folder. The script produces concise **HTML** reports indicating run success/failure, with hyperlinks to respective simulation log files.
- Contributed to the maintenance of the **FPGA** scripts **GitLab** submodule, while also incorporating **10** new features.
- Built a **Python** script to scrape **XCI** files for **IP** configuration, generating Vivado/simulation-ready **TCL** scripts.
- Designed a **Python** script to create formatted **HTML** documentation of **IP** usage within a specified directory.

Projects

Partial MIPS Processor — Rochester Institute of Technology

- Engineered a partial pipelined integer MIPS processor, adeptly accommodating R-type and I-type instructions using **VHDL**. Designed **VHDL** components encompassed Instruction Memory, Register File, ALU, Control Unit, and Data Memory. Functionality verification was conducted at both the component and holistic design levels using **VHDL**.

Autonomous Car — Rochester Institute of Technology

- Developed **C** code for an autonomous car utilizing **PID** control to smoothly navigate an unknown course. The code processed line scan camera data for position determination, controlled steering via servos, and managed rear wheel power for speed regulation and rear-wheel steering.

Roundnet Season Tracker and Pool Calculator — Personal Project

- Created a **Python** tool for analyzing season-long player and team rankings and calculating tournament pools using a snake pattern on sorted teams by extracting pertinent information from **HTML** elements for each tournament.

Technical Skills

Languages : VHDL, Python, TCL, C, SystemVerilog, Verilog, Java, HTML, CSS, Javascript, Matlab
Dev Tools : Visual Studio Code, Git, GitLab, GitHub, Xilinx Vivado, Aldec Riviera, Cygwin

Achievements

Texas Instruments Cup 2nd Place — Rochester Institute of Technology

- Participated in an autonomous car competition where teams of two collaborated to efficiently navigate an unfamiliar course while making informed design choices that struck a balance between speed and consistency.

Engineering Dean's List — Rochester Institute of Technology

- Maintained a GPA of 3.5 or better