Flip-Flops

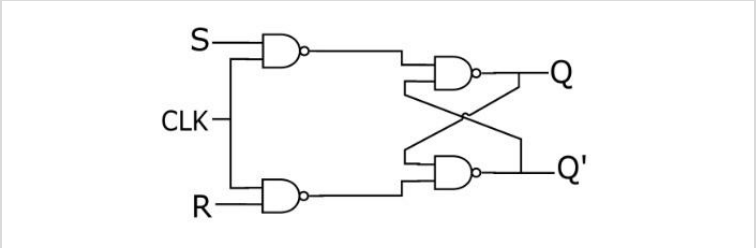
A flip-flop is a sequential digital electronic circuit having two stable states that can be used to store one bit of binary data. Flip-flops are the fundamental building blocks of all memory devices.

Types of Flip–Flops

1. S-R flip-flop
2. J-K flip-flop
3. D flip-flop
4. T flip-flop

S-R Flip-flop

This is the simplest flip-flop circuit. It has a set input (S) and a reset input (R). When in this circuit when S is set as active, the output Q would be high and the Q' will be low. If R is set to active then the output Q is low and the Q' is high. Once the outputs are established, the results of the circuit are maintained until S or R get changed, or the power is turned off.



Truth table of S-R flip-flop

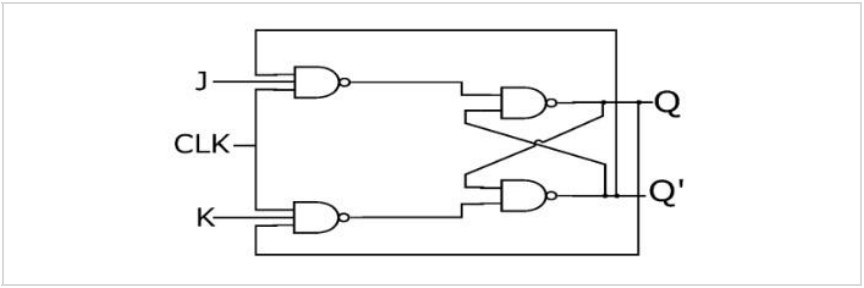
S	R	Q	State
0	0	0	No Change
0	1	0	Reset
1	0	1	Set
1	1	X	

Characteristics equation of S-R flip-flop

$$Q(t+1)=S+R'Q(t)Q(t+1)=S+R'Q(t)$$

J-K Flip-flop

Because of the invalid state corresponding to S=R=1 in the SR flip-flop, there is a need of another flip-flop. The JK flip-flop operates with only positive or negative clock transitions. The operation of the JK flip-flop is similar to the SR flip-flop. When the input J and K are different then the output Q takes the value of J at the next clock edge. When J and K both are low then NO change occurs at the output. If both J and K are high, then at the clock edge, the output will toggle from one state to the other.



Truth table of JK flip-flop

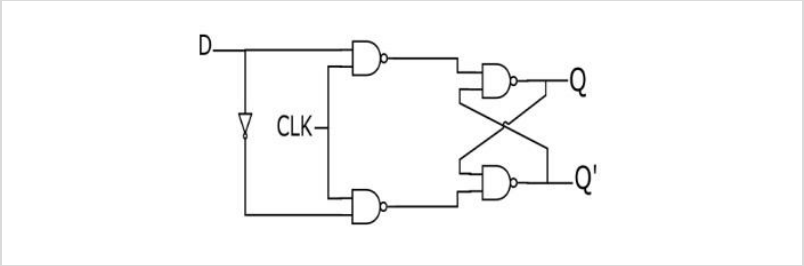
J	K	Q	State
0	0	0	No Change
0	1	0	Reset
1	0	1	Set
1	1	Toggles	Toggle

Characteristics equation of JK flip-flop

$$Q(t+1)=jkQ(t)‘+K‘Q(t)Q(t+1)=jkQ(t)‘+K‘Q(t)$$

D Flip-flop

In a D flip-flop, the output can only be changed at positive or negative clock transitions, and when the inputs changed at other times, the output will remain unaffected. The D flip-flops are generally used for shift-registers and counters. The change in output state of D flip-flop depends upon the active transition of clock. The output (Q) is same as input and changes only at active transition of clock.



Truth table of D flip-flop

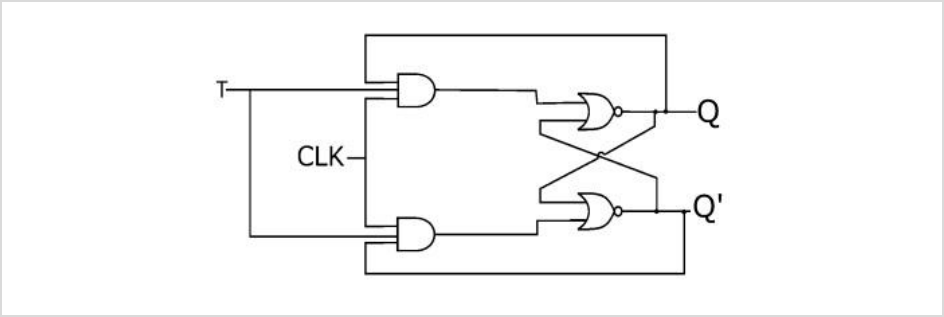
D	Q
0	0
1	1

Characteristics equation of D flip-flop

$$Q(t+1)=DQ(t+1)=D$$

T Flip-flop

A T flip-flop (Toggle Flip-flop) is a simplified version of JK flip-flop. The T flop is obtained by connecting the J and K inputs together. The flip-flop has one input terminal and clock input. These flip-flops are said to be T flip-flops because of their ability to toggle the input state. Toggle flip-flops are mostly used in counters.



Truth Table of T flip-flop

T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristics equation of T flip-flop

$$Q(t+1)=T'Q(t)+TQ(t)'=T\oplus Q(t)Q(t+1)=T'Q(t)+TQ(t)'=T\oplus Q(t)$$

Applications of Flip-flops

Counters

Shift Registers

Storage Registers, etc.

Flip Flop Conversion

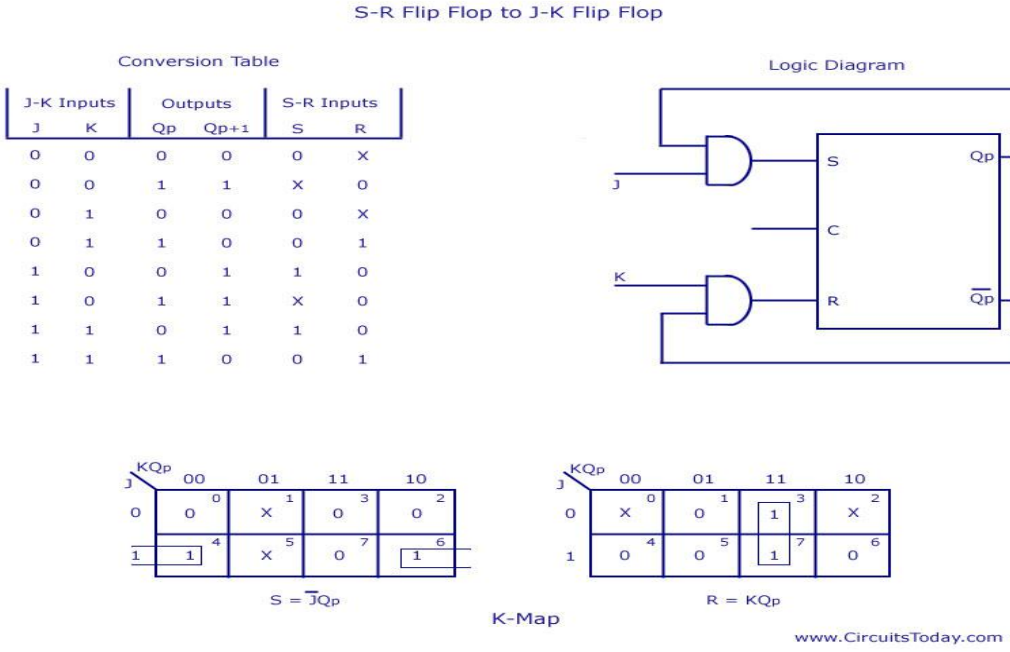
For the conversion of one flip flop to another, a combinational circuit has to be designed first. If a JK Flip Flop is required, the inputs are given to the combinational circuit and the output of the combinational circuit is connected to the inputs of the actual flip flop. Thus, the output of the actual flip flop is the output of the required flip flop. In this post, the following flip flop conversions will be explained.

1. SR Flip Flop to JK Flip Flop
2. JK Flip Flop to SR Flip Flop
3. SR Flip Flop to D Flip Flop
4. D Flip Flop to SR Flip Flop
5. JK Flip Flop to T Flip Flop
6. JK Flip Flop to D Flip Flop
7. D Flip Flop to JK Flip Flop

SR Flip Flop to JK Flip Flop

J and K will be given as external inputs to S and R. As shown in the logic diagram below, S and R will be the outputs of the combinational circuit.The truth tables for the flip flop conversion are given below. The present state is represented by Qp and Qp+1 is the next state to be obtained when the J and K inputs are applied.

For two inputs J and K, there will be eight possible combinations. For each combination of J, K and Qp, the corresponding Qp+1 states are found. Qp+1 simply suggests the future values to be obtained by the JK flip flop after the value of Qp. The table is then completed by writing the values of S and R required to get each Qp+1 from the corresponding Qp. That is, the values of S and R that are required to change the state of the flip flop from Qp to Qp+1 are written.

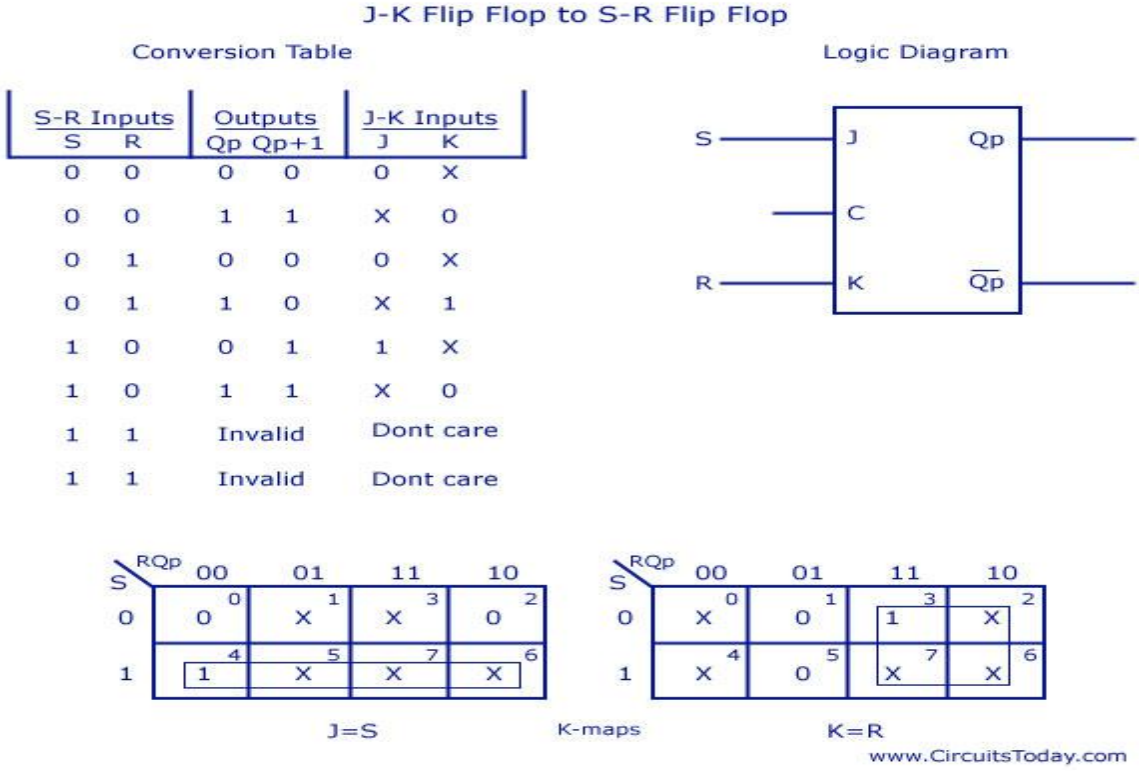


J-K Inputs		Outputs		S-R Inputs	
J	K	Qp	Qp+1	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

JK Flip Flop to SR Flip Flop

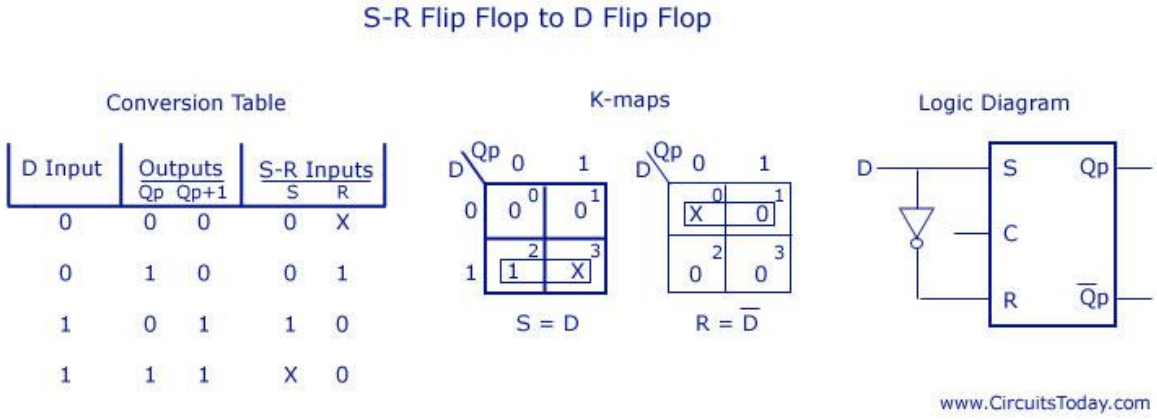
This will be the reverse process of the above explained conversion. S and R will be the external inputs to J and K. As shown in the logic diagram below, J and K will be the outputs of the combinational circuit. Thus, the values of J and K have to be obtained in terms of S, R and Qp. The logic diagram is shown below.

A conversion table is to be written using S, R, Qp, Qp+1, J and K. For two inputs, S and R, eight combinations are made. For each combination, the corresponding Qp+1 outputs are found ut. The outputs for the combinations of S=1 and R=1 are not permitted for an SR flip flop. Thus the outputs are considered invalid and the J and K values are taken as "don't cares".



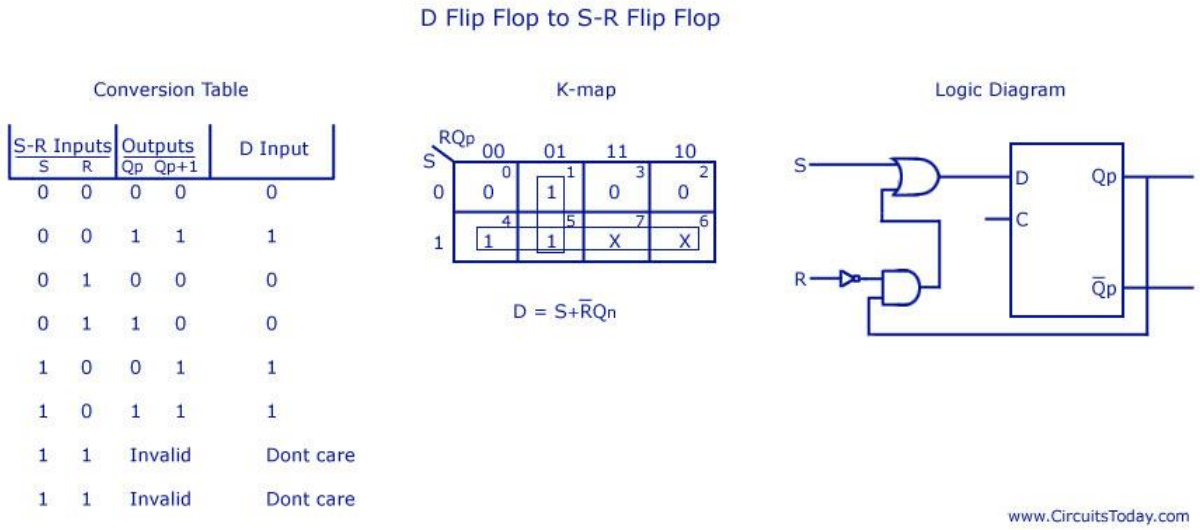
SR Flip Flop to D Flip Flop

As shown in the figure, S and R are the actual inputs of the flip flop and D is the external input of the flip flop. The four combinations, the logic diagram, conversion table, and the K-map for S and R in terms of D and Qp are shown below.



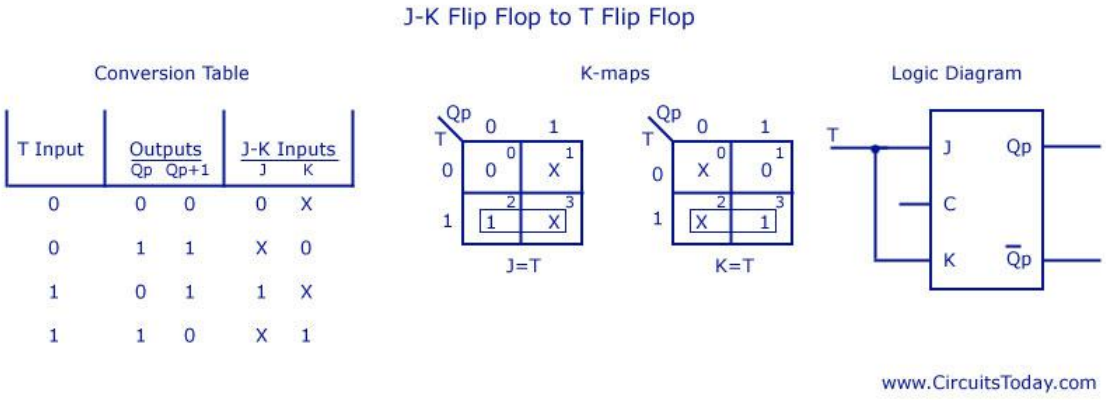
D Flip Flop to SR Flip Flop

D is the actual input of the flip flop and S and R are the external inputs. Eight possible combinations are achieved from the external inputs S, R and Qp. But, since the combination of S=1 and R=1 are invalid, the values of Qp+1 and D are considered as "don't cares". The logic diagram showing the conversion from D to SR, and the K-map for D in terms of S, R and Qp are shown below.



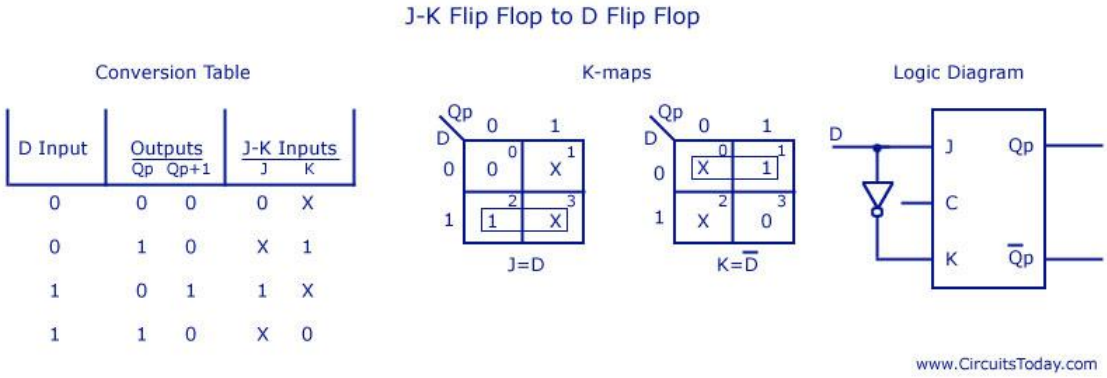
JK Flip Flop to T Flip Flop

J and K are the actual inputs of the flip flop and T is taken as the external input for conversion. Four combinations are produced with T and Qp. J and K are expressed in terms of T and Qp. The conversion table, K-maps, and the logic diagram are given below.



JK Flip Flop to D Flip Flop

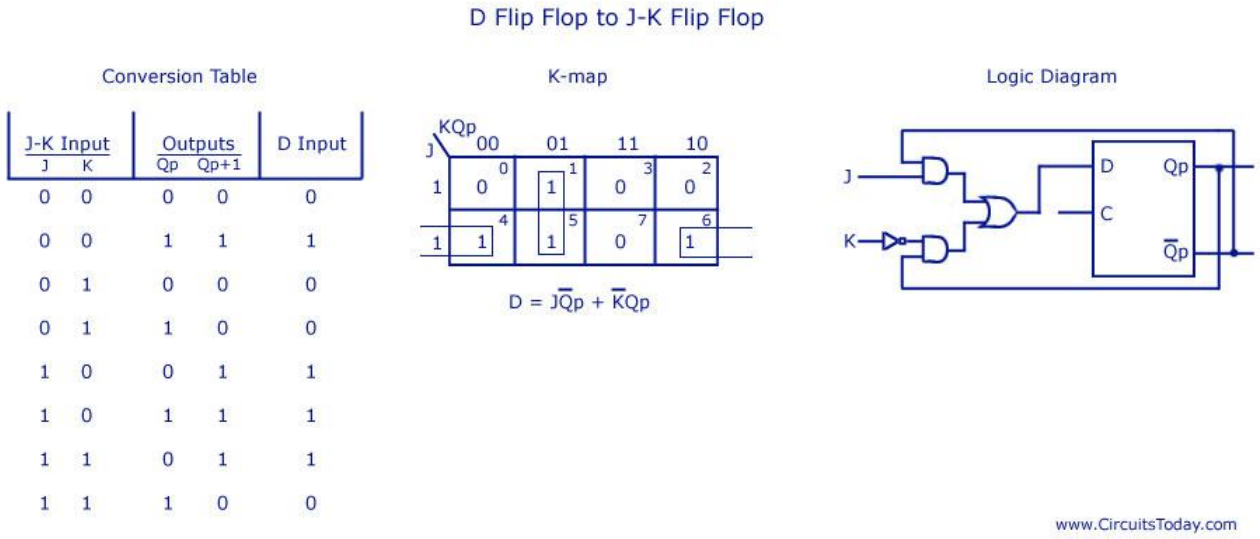
D is the external input and J and K are the actual inputs of the flip flop. D and Qp make four combinations. J and K are expressed in terms of D and Qp. The four combination conversion table, the K-maps for J and K in terms of D and Qp, and the logic diagram showing the conversion from JK to D are given below.



D Flip Flop to JK Flip Flop

In this conversion, D is the actual input to the flip flop and J and K are the external inputs. J, K and Qp make eight possible combinations, as shown in the conversion table below. D is expressed in terms of J, K and Qp.

The conversion table, the K-map for D in terms of J, K and Qp and the logic diagram showing the conversion from D to JK are given in the figure below.



MCQ

1. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
a) Low input voltages
b) Synchronous operation
c) Gate impedance
d) Cross coupling

Answer: d
Explanation: Latch is a type of bistable multivibrator having two stable states. Both inputs of a latch are directly connected to the other's output. Such types of structure is called cross coupling and due to which latches remain in the latched condition.

2. One example of the use of an S-R flip-flop is as _____
a) Transition pulse generator
b) Racer
c) Switch debouncer
d) Astable oscillator

Answer: c
Explanation: The SR flip-flop is very effective in removing the effects of switch bounce, which is the unwanted noise caused during the switching of electronic devices.

3. The truth table for an S-R flip-flop has how many VALID entries?
a) 1
b) 2
c) 3
d) 4

Answer: c
Explanation: The SR flip-flop actually has three inputs, Set, Reset and its current state. The Invalid or Undefined State occurs at both S and R being at 1.

4. When both inputs of a J-K flip-flop cycle, the output will _____
a) Be invalid
b) Change
c) Not change
d) Toggle

Answer: c
Explanation: After one cycle the value of each input comes to the same value. Eg: Assume J=0 and K=1. After 1 cycle, it becomes as J=0->1->0(1 cycle complete) and K=1->0->1(1 cycle complete). The J & K flip-flop has 4 stable states: Latch, Reset, Set and Toggle.

5. Which of the following is correct for a gated D-type flip-flop?
a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
b) The output complement follows the input when enabled
c) Only one of the inputs can be HIGH at a time
d) The output toggles if one of the inputs is held HIGH

Answer: a
Explanation: In D flip flop, when the clock is high then the output depends on the input otherwise reminds previous output. In a state of clock high, when D is high the output Q also high, if D is '0' then output is also zero. Like SR flip-flop, the D-flip-flop also have an invalid state at both inputs being 1.

6. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates
b) XOR or XNOR gates
c) NOR or NAND gates
d) AND or NOR gates

Answer: c
Explanation: The basic S-R flip-flop can be constructed by cross coupling of NOR or NAND gates. Cross coupling means the output of second gate is fed to the input of first gate and vice-versa.

7. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

Answer: b
Explanation: In sequential circuits, the output signals are fed back to the input side. So, The circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called sequential circuits. Unlike sequential circuits, if output depends only on the present state, then it's known as combinational circuits.

8. Whose operations are more faster among the following?
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

Answer: a
Explanation: Combinational circuits are often faster than sequential circuits. Since the combinational circuits do not require memory elements whereas the sequential circuits need

memory devices to perform their operations in sequence. Latches and Flip-flops come under sequential circuits.

9. How many types of sequential circuits are?
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: There are two type of sequential circuits viz., (i) synchronous or clocked and (ii) asynchronous or unclocked. Synchronous Sequential Circuits are triggered in the presence of a clock signal, whereas, Asynchronous Sequential Circuits function in the absence of a clock signal.

10. The sequential circuit is also called _____
a) Flip-flop
b) Latch
c) Strobe
d) Adder

Answer: b
Explanation: The sequential circuit is also called a latch because both are a memory cell, which are capable of storing one bit of information.

11. The basic latch consists of _____
a) Two inverters
b) Two comparators
c) Two amplifiers
d) Two adders

Answer: a
Explanation: The basic latch consists of two inverters. It is in the sense that if the output Q = 0 then the second output Q' = 1 and vice versa.

12. In S-R flip-flop, if Q = 0 the output is said to be _____
a) Set
b) Reset
c) Previous state
d) Current state

Answer: b
Explanation: In S-R flip-flop, if Q = 0 the output is said to be reset and set for Q = 1.

13. The output of latches will remain in set/reset untill _____
a) The trigger pulse is given to change the state

b) Any pulse given to go into previous state
c) They don’t get any pulse more
d) The pulse is edge-triggered

Answer: a
Explanation: The output of latches will remain in set/reset untill the trigger pulse is given to change the state.

14. What is a trigger pulse?
a) A pulse that starts a cycle of operation
b) A pulse that reverses the cycle of operation
c) A pulse that prevents a cycle of operation
d) A pulse that enhances a cycle of operation

Answer: a
Explanation: Trigger pulse is defined as a pulse that starts a cycle of operation.

15. The circuits of NOR based S-R latch classified as asynchronous sequential circuits, why?
a) Because of inverted outputs
b) Because of triggering functionality
c) Because of cross-coupled connection
d) Because of inverted outputs & triggering functionality

Answer: c
Explanation: The cross-coupled connections from the output of one gate to the input of the other gate constitute a feedback path. For this reason, the circuits of NOR based S-R latch classified as asynchronous sequential circuits. Moreover, they are referred to as asynchronous because they function in the absence of a clock pulse.