

# **ADS1198ECG-FE**

## **ECG Front-End Performance Demonstration Kit**

### **User's Guide**



Literature Number: SBAU180  
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# ADS1198ECG-FE

This user's guide describes the characteristics, operation, and use of the ADS1198ECG-FE. This EVM is an evaluation module for the [ADS1198](#), an eight-channel, 16-bit, low-power, integrated analog front-end (AFE) designed for patient monitoring and portable and high-end electrocardiogram (ECG) and electroencephalogram (EEG) applications. The ADS1198ECG-FE is intended for prototyping and evaluation. This user's guide includes a complete circuit description, schematic diagram, and bill of materials.

The following related documents are available through the Texas Instruments web site at [www.ti.com](http://www.ti.com).

Device	Literature Number
<a href="#">ADS1198</a>	<a href="#">SBAS471</a>

## 1 ADS1198ECG-FE Overview

### 1.1 *Important Disclaimer Information*

#### CAUTION

**NOTICE:** The ADS1198ECG-FE is intended for feasibility and evaluation testing only in laboratory and development environments. This product is not for diagnostic use. This product is not for use with a defibrillator.

The ADS1198ECG-FE is to be used only under these conditions:

- The ADS1198ECG-FE is intended only for **electrical** evaluation of the features of the ADS1198 device in a laboratory, simulation, or development environment.
- The ADS1198ECG-FE is **not** intended for direct interface with a patient, patient diagnostics, or with a defibrillator.
- The ADS1198ECG-FE is intended for development purposes **ONLY**. It is not intended to be used as all or part of an end equipment application.
- The ADS1198ECG-FE should be used only by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems, and subsystems.
- You are responsible for the safety of yourself, your fellow employees and contractors, and your co-workers when using or handling the ADS1198ECG-FE. Furthermore, you are fully responsible for the contact interface between the human body and electronics; consequently, you are responsible for preventing electrical hazards such as shock, electrostatic discharge, and electrical overstress of electric circuit components.

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Microsoft, Windows are registered trademarks of Microsoft Corporation.  
SPI is a trademark of Motorola Inc.  
MATLAB is a registered trademark of The Math Works, Inc.  
All other trademarks are the property of their respective owners.

## 1.2 Information About Cautions and Warnings

This document contains caution statements. The information in a caution statement is provided for your protection. Be sure to read each caution carefully.

### CAUTION

This is an example of a caution statement. A caution statement describes a situation that could potentially damage your software or equipment.

## 2 Overview

### 2.1 Introduction

The ADS1198ECG-FE is intended for evaluating the [ADS1198](#) low-power, 16-bit, simultaneously sampling, eight-channel front-end for ECG and EEG applications. The digital SPI™ control interface is provided by the MMB0 Modular EVM motherboard (Rev. C or higher) that connects to the ADS1x98 ECG FE evaluation board (Rev. C). The ADS1198ECG-FE (see [Figure 1](#)) is **NOT** a reference design for ECG and EEG applications; rather, its purpose is to expedite evaluation and system development. The output of the ADS1198 yields a raw, unfiltered ECG signal.

The MMB0 motherboard allows the ADS1198ECG-FE to be connected to the computer via an available USB port. This manual shows how to use the MMB0 as part of the ADS1198ECG-FE, but does not provide technical details about the MMB0 itself.

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1198ECG-FE.

### 2.2 Supported Features

#### Hardware Features:

- Configurable for bipolar or unipolar supply operation
- Configurable for internal and external clock and reference via jumper settings
- Configurable for ac- or dc-coupled inputs
- Configurable for up to 12 standard ECG leads
- External Right Leg Drive (RLD) Reference ( $V_{CC} - V_{EE}/2$ )
- External shield drive amplifier
- External Wilson central voltage
- Easy connectivity to popular ECG simulators

#### Software Features:

- Analysis tools including a virtual oscilloscope, histogram, FFT, and ECG display
- File printing for post-processing of raw ECG data
- Sets the ADS1198 register settings via easy-to-use graphic user interface (GUI) software

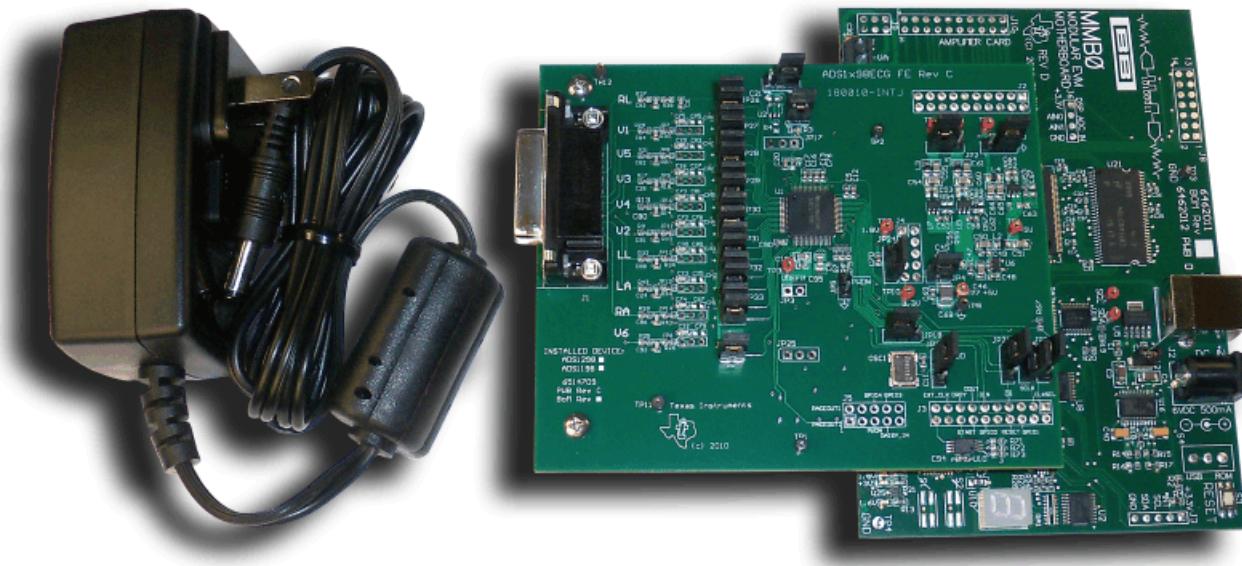
## 2.3 Features Not Supported in Current Version

**NOTE:** The following features are NOT SUPPORTED by the current version of the firmware.

- Real-time data processing
- AC lead-off detection filters
- QRS detection algorithms
- Software PACE detection algorithms
- High-pass filtering
- 50Hz/60Hz notch filtering at rates other than 500SPS

## 2.4 ADS1198ECG-FE Hardware

Figure 1 shows the hardware included in the ADS1198ECG-FE kit. Contact the factory if any component is missing. Also, it is highly recommended that you check the TI website at <http://www.ti.com> to verify that you have the latest software.



**Figure 1. ADS1198ECG-FE Kit**

The complete kit includes the following items:

- ADS1x98 ECG FE printed circuit board (PCB), Rev C
- MMB0 (Modular EVM motherboard, Rev C or higher)
- Universal ac to dc wall adapter, 120V to 240V ac to +6V dc

## 3 Software Installation

### 3.1 Minimum Requirements

Before installing the software, verify that your PC meets the minimum requirements outlined in this section.

#### 3.1.1 Required Setup for ADS1198ECG-FE Software

Install the software on a PC-compatible computer that meets these specifications:

- Pentium III®/ Celeron® processor, 866MHz or equivalent
- Minimum 256MB of RAM (512MB or greater recommended)
- USB 1.1-compatible input
- Hard disk drive with at least 200MB free space
- Microsoft® Windows® XP operating system with SP2 (Windows Vista and Windows 7 are **NOT** supported)
- Mouse or other pointing device
- 1280 x 960 minimum display resolution

### 3.2 Installing the Software

#### CAUTION

Do not connect the ADS1198ECG-FE before installing the software on a suitable PC. Failure to observe this caution may cause Microsoft Windows to not recognize the ADS1198ECG-FE.

The latest software is available from the TI web site at

<http://focus.ti.com/docs/toolsw/folders/print/ADS1198ecgfe-pdk.html>; check the TI web site regularly for updated versions.

To install the ADS1198 software, download the executable. Then follow the prompts illustrated in [Figure 2](#) through [Figure 5](#).



Figure 2. Initialization of ADS1198ECG-FE

You must accept the license agreement (shown in [Figure 3](#)) before you can proceed with the installation.

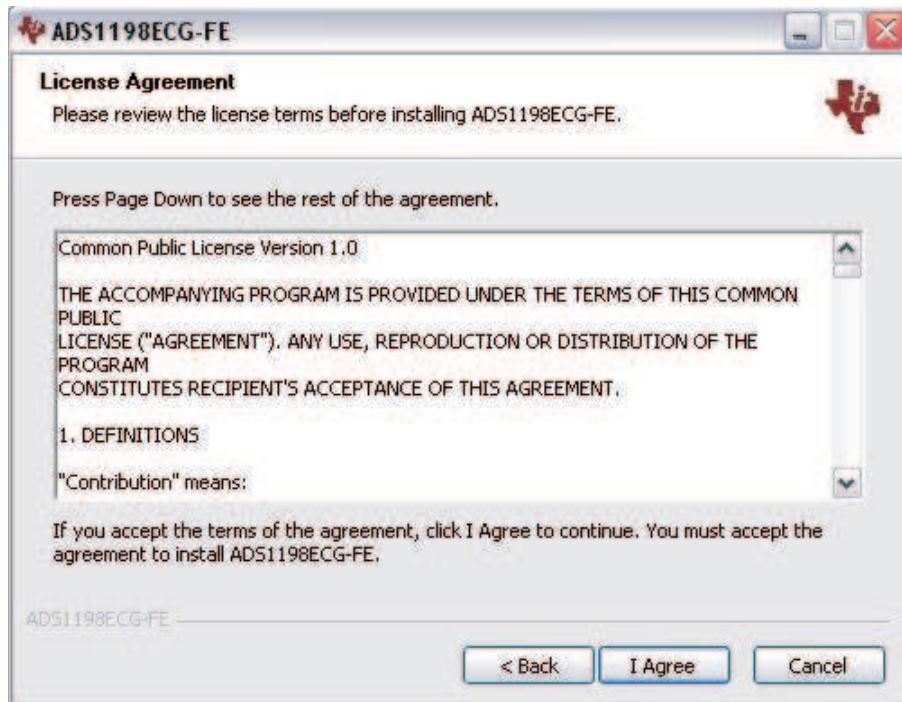
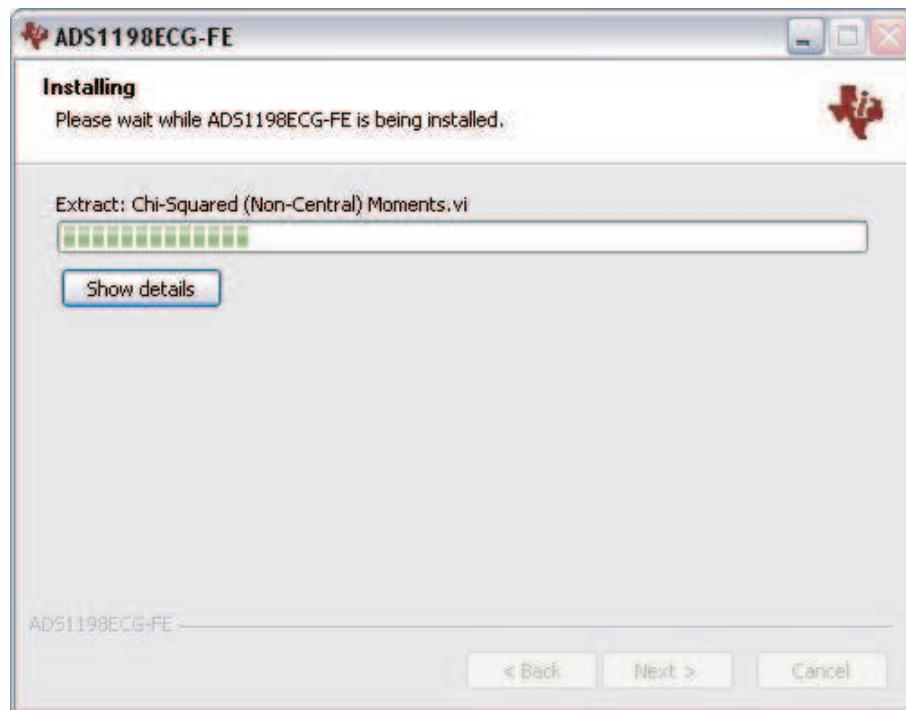


Figure 3. License Agreement



**Figure 4. Installation Process**



**Figure 5. Completion of ADS1198 Software Installation**

## 4 ADS1198ECG-FE Daughter Card Hardware Introduction

### CAUTION

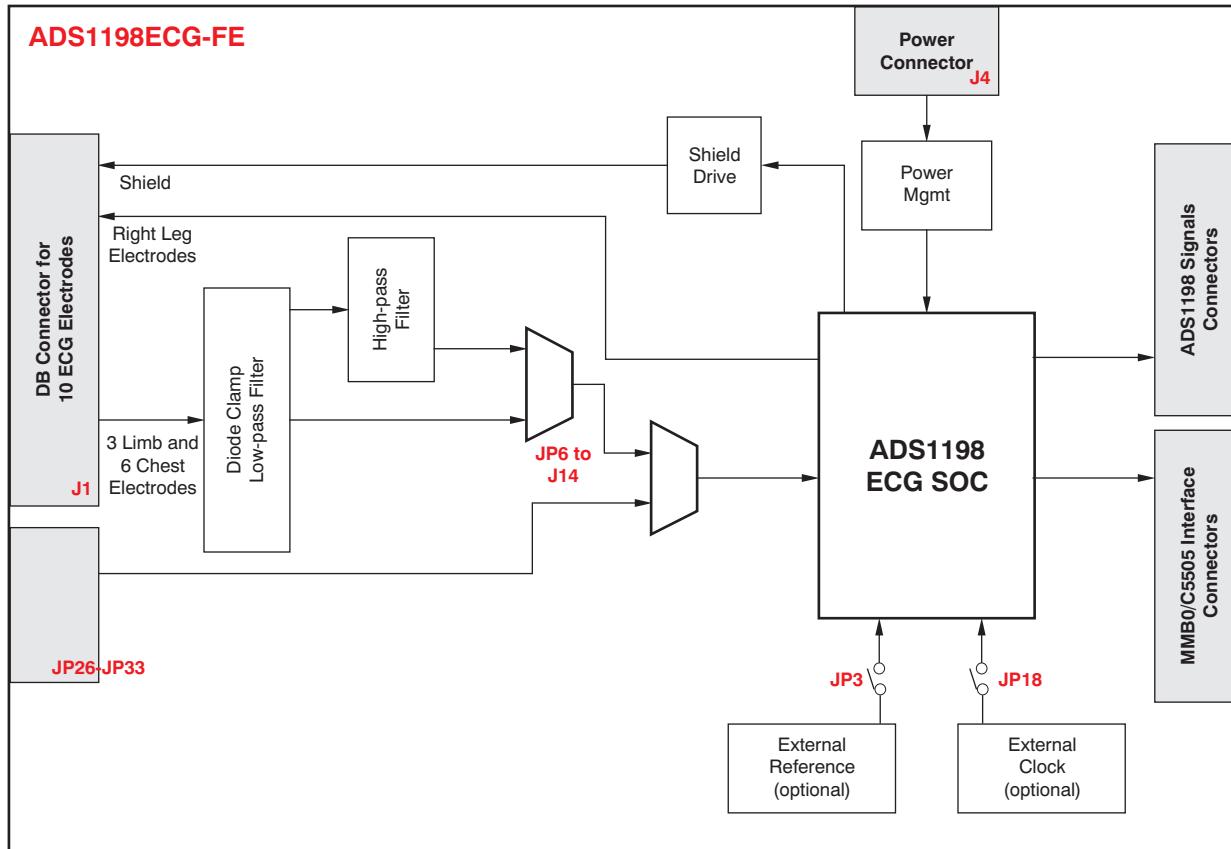
Many of the components on the ADS1198ECG-FE are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap, bootstraps, or mats at an approved ESD workstation. An electrostatic smock and safety glasses should also be worn.

The ADS1198 ECG front-end evaluation board is configured to be used with the TI MMB0 data converter evaluation platform. The key features of the ADS1198 system on a chip (SOC) are:

- Eight integrated INAs and eight 16-bit high-resolution ADCs
- Suitable for three-lead, five-lead and 12-lead ECG applications
- Low power consumption (1mW/channel)
- Data rates of 250SPS to 32kSPS
- 3V to 5V unipolar or bipolar analog supply, 1.8V to 3V digital supply.
- Lead off and PACE detection circuitry
- On-chip oscillator
- On-chip RLD amplifier
- On-chip WCT driver
- SPI data interface

The ADS1198ECG-FE can be used as a demonstration board for standard, 12-lead ECG applications with an input configuration of 10 electrodes. Users can also bypass the 12-lead configuration and provide any type of signal directly to the ADS1198 through a variety of hardware jumper settings (JP26-JP33; see [Section 8.2](#)). External support circuits are provided for testing purposes such as external references, clocks, lead-off resistors, and shield drive amplifiers.

**Figure 6** shows the functional block diagram with important jumper names for the EVM.



**Figure 6. ADS1198ECG-FE Front-End Block Diagram**

The ADS1198ECG-FE board is a four-layer circuit board. The board layout is provided in [Section 8](#); the schematics are appended to this document. The following sections explain some of the hardware settings possible with the EVM for evaluating the ADS1198 under various test conditions.

#### 4.1 Power Supply

The ECG front-end EVM mounts on the MMB0 motherboard with connectors J2, J3 and J4. The main power supplies (+5V, +3V and +1.8V) for the front-end board are supplied by the host boards (MDK or MMB0) through connector J4. All other power supplies needed for the front-end board are generated on board by power management devices. The EVM is shipped in +3V unipolar supply configuration.

The ADS1198 can operate from +3.0V to +5.0V analog supply (AVDD/AVSS) and +1.8V to +3.0V digital supply (DVDD). A bipolar analog supply ( $\pm 1.5V$  to  $\pm 2.5V$ ) can be used as well. The power consumption of the front-end board can be measured by using the JP4 jumper and JP24 jumper. The ADS1198 can be powered down by shorting jumper JP5.

Test points TP5, TP6, TP7, TP8, TP9, TP10, and TP14 are provided to verify that the host power supplies are correct. The corresponding voltages are shown in [Table 1](#).

**Table 1. Power-Supply Test Points**

Test Point	Voltage
TP7	+5.0V
TP9	+1.8V
TP10	+3.3V
TP5	+3.0V
TP13	+2.5V
TP6	-2.5V
TP8	GND

The front-end board must be properly configured in order to achieve the various power-supply schemes. The default power-supply setting for the ADS1198ECG-FE is a unipolar analog supply of 3V or a bipolar analog supply of  $\pm 2.5V$  and DVDD of either +3V or +1.8V. [Table 2](#) shows the board and component configurations for each analog power-supply scheme; [Table 3](#) shows the board configurations for the digital supply.

**Table 2. Analog Supply Configurations (AVDD/AVSS)**

AVDD/AVSS	Unipolar Analog Supply		Bipolar Analog Supply	
	3V	5V	$\pm 1.5V$	$\pm 2.5V$
JP24	1-2	1-2	2-3	2-3
JP2	2-3	2-3	1-2	1-2
U10	<a href="#">TPS73230-EP</a>	<a href="#">TPS73250</a>	Don't Care	Don't Care
U12	Don't Care	Don't Care	<a href="#">TPS73201</a>	<a href="#">TPS73201</a>
U11	Don't Care	Don't Care	<a href="#">TPS72301</a>	<a href="#">TPS72301</a>
R52	Don't Care	Don't Care	21k $\Omega$	47.5k $\Omega$
R53	Don't Care	Don't Care	78.7k $\Omega$	43k $\Omega$
R56	Don't Care	Don't Care	23.3k $\Omega$	49.9k $\Omega$
R57	Don't Care	Don't Care	95.3k $\Omega$	46.4k $\Omega$
C87, C66, C62	Not Installed	Not Installed	Not Installed	Not Installed

**Table 3. Digital Supply Configurations (DVDD/DGND)**

DVDD	+3.0V	+1.8V
JP24	1-2	2-3

## 4.2 Jumpers

**Table 4** summarizes the default jumpers for the ADS1198ECG-FE.

**Table 4. Default Jumper Configuration**

Shunt Jumpers	Default Position	Description
JP1	Installed	RLD feedback
JP2	Bipolar power configuration – Installed pins 1-2	Used with JP20 to set ADS1198 power-supply configuration. For unipolar operation, install jumpers on pins 2-3.
JP4	Installed	Provides +5V power from J4 to U6 – U9.
JP5	Open	Power down: close JP5 to put the ADS1198 in Power-Down mode
JP6 to JP14	Header not installed	Foil shorted pins 1-2 for dc-coupled inputs. For ac-coupled inputs, cut the foil short and jumper pins 2-3.
JP15	Installed 2-3	Shield device. Default is open (via U2); to ground the shield, move the shunt on JP15 to pins 1-2.
JP16	Installed	Wilson Central Terminal connection; default is WCT connected to INM for CH1 and CH4-8.
JP17	Header not installed	Controls input to ECG shield drive; install U2 before using JP17.
JP19	Installed 1-2	OSC1 enable; move to pins 2-3 to disable.
JP20	Bipolar power configuration – Installed pins 2-3	Used with JP2 to set ADS1198 power-supply configuration. For unipolar operation, install jumpers on pins 1-2.
JP21	Installed 1-2	ADS1198 CS input comes from J3.1.
JP22	Installed 2-3	ADS1198 Start Signal comes from J3.20.
JP23	Installed 1-2	ADS1198 CLKSEL input is grounded, device uses Ext Master Clock (OSC1).
JP24	Installed 2-3	DVDD supply option, default is 3.3V. For DV <sub>DD</sub> = 1.8V, move jumper to cover pins 1-2.
JP25	Header not installed	External reference selections; install U3 and/or U4. Must install JP3 before using external reference source.
JP26	Installed 1-2 (top) Installed 3-4 (bottom)	Input connections for CH8, WCT + ELG_V1
JP27	Installed 1-2 (top) Installed 3-4 (bottom)	Input connections for CH7, WCT + ECG_V5
JP28	Installed 1-2 (top) Installed 3-4 (bottom)	Input connections for CH6, WCT + ECG_V4
JP29	Installed 1-2 (top) Installed 3-4 (bottom)	Input connections for CH5, WCT + ECG_V3
JP30	Installed 1-2 (top) Installed 3-4 (bottom)	Input connections for CH4, WCT + ECG_V2
JP31	Installed 1-2 (top) Installed 3-4 (bottom)	Input connections for CH3, WCT + ECG_LL+ ECG_RA
JP32	Installed 1-2 (top) Installed 3-4 (bottom)	Input connections for CH2, ECG_RA + ECG_LA
JP33	Installed 1-2 (top) Installed 3-4 (bottom)	Input connections for CH1, WCT + ECG_V6

### 4.3 Clock

The ADS1198 has an on-chip oscillator circuit that generates a 2.048MHz clock (nominal). This clock can vary by  $\pm 5\%$  over temperature. For applications that require higher accuracy, the ADS1198 can also accept an external clock signal. The ADS1198ECG-FE provides an option to test both internal and external clock configurations. Jumper JP18 is provided as a means to select the external master clock source from either OSC1 (default condition) when a shunt is installed on pins 2-3, or an external clock source via J3 pin 17.

The onboard oscillator is powered by the DVDD supply of the ADS1198. Care must be taken to ensure that the external oscillator can operate either with +1.8V or +3.0V, depending on the DVDD supply configuration. [Table 5](#) shows the jumper settings for the three options for the ADS1198 clocks.

**Table 5. ADS1198 Master Clock Options**

	JP18	JP19	JP23
ADS1198 internal oscillator	OPEN	Don't care	OPEN, or shorted pins 2-3 and controlled through GPIO on J3.2
Onboard OSC1 oscillator	Closed pins 2-3	Closed pins 1-2	Closed pins 1-2 (default)
External source via J3.17	Closed pins 1-2	Don't care	Closed pins 1-2 (default)

OSC1 is suitable for operation with a DVDD supply of +3.3VD. When operating the ADS1198EVM with a DVDD supply of +1.8V, it is recommended to replace OSC1 with oscillator part number SiT8002AC-34-18E-2.048.

### 4.4 Reference

The ADS1198 has an on-chip internal reference circuit that provides reference voltages to the device. Alternatively, the internal reference can be powered down and VREFP can be applied externally. This configuration is achieved with the external reference generators (U3 and U4) and driver buffer. The external reference voltage can be set to either 4.096V or 2.5V, depending on the analog supply voltage. Measure TP3 to make sure the external reference is correct. The setting for the external reference is described in [Table 6](#).

**Table 6. External Reference Jumper Options**

ADS1198 Reference	Internal Reference	External Reference	
	VREF = 2.5V	VREFP = 4.096V	VREFP = 2.5V
JP18	Don't Care	2-3	1-2
JP3	Not Installed	Installed	Installed

The software uses the  $V_{REF}$  value entered in the Global Registers control tab (refer to [Section 5.2](#)) to calculate the input-referred voltage value for all the tests. The default value is 2.4V. If any other value is used, the user must update this field in the Global Registers control tab.

#### 4.5 Accessing ADS1198 Analog Signals

Some ADS1198 output signals are provided as test points for probing purposes through J6. [Table 7](#) lists the various test signals with the corresponding test points. The PACEOUT pins can also be used as an auxiliary differential input channel. These pins can also be used to perform PACE detection with external PACE detection circuitry, with appropriate user register settings (see [Section 5.7.2](#)).

**Table 7. Test Signals**

Signal	J5 Pin Number		Signal
PACEOUT2	1	2	PACEOUT1
RESERVED	3	4	RESERVED
PWDN	5	6	GPIO4
DAISY_IN	7	8	GPIO3
AGND	9	10	RESERVED

#### 4.6 Accessing ADS1198 Digital Signals

The ADS1198 digital signals (including SPI interface signals, some GPIO signals, and some of the control signals) are available at connector J3. These signals are used to interface to the MMB0 board DSP. The pinout for this connector is given in [Table 8](#).

**Table 8. Serial Interface Pinout**

Signal	J3 Pin Number		Signal
START/CS	1	2	CLKSEL
CLK	3	4	GND
NC	5	6	GPIO1
CS	7	8	RESETB
NC	9	10	GND
DIN	11	12	GPIO2
DOUT	13	14	NC/START
DRDYB	15	16	NC
EXTCLK	17	18	GND
NC	19	20	NC

## 4.7 Analog Inputs

The ADS1198ECG-FE provides users the option to feed in standard ECG signals from a patient simulator to the DB15 connector, or to feed inputs from any arbitrary signal source directly to the ADS1198.

### 4.7.1 Patient Simulator Input

The output from any typical patient simulator can be directly fed in to the DB15 connector. For all measurements in this user guide, a Fluke medSim 300B simulator was used, as Figure 7 shows. The simulator is capable of generating ECG signals down to 50 $\mu$ V of amplitude. Particular attention must be given to the common-mode value of the input signal for proper data capture. Refer to the [ADS1198 product data sheet](#) for the common-mode range for various programmable gain amplifier (PGA) gain settings. Section 7.1 explains the process used to capture 12-lead ECG data.



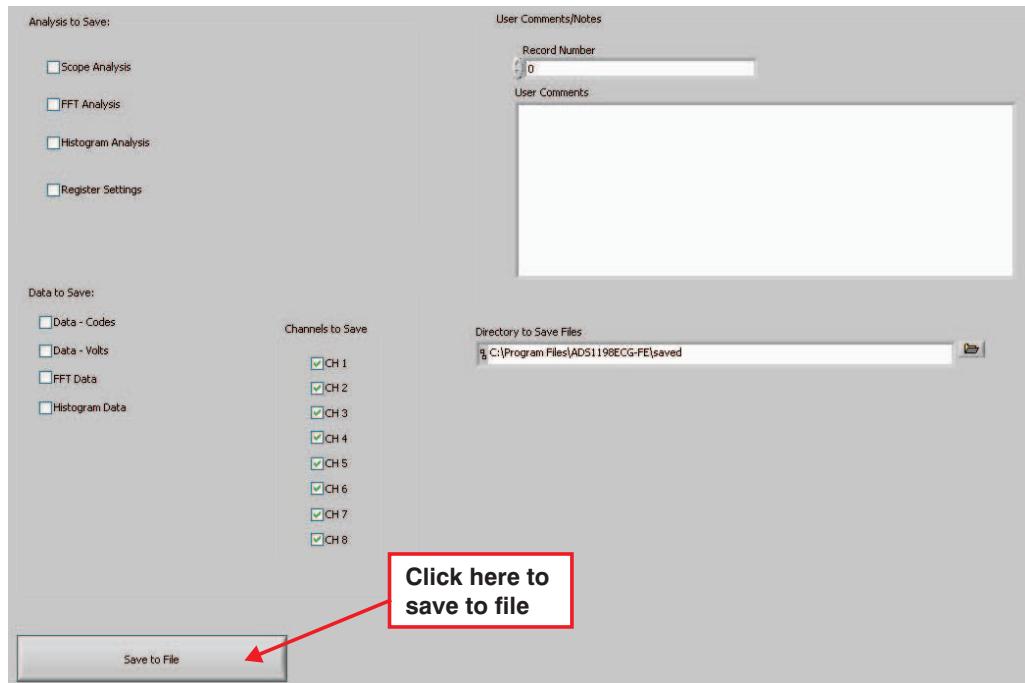
**Figure 7. Fluke Simulator Configuration**

### 4.7.2 Arbitrary Input Signals

Arbitrary input signals can be fed to the ADS1198 by bypassing the DB15 connector and feeding the signal directly at jumpers JP26-JP33. Remove the set of 16 jumpers at JP26-JP33. The signal must be fed in differentially because all channel inputs are differential. If single-ended signals are used, bias the negative input of the channels to a mid-supply voltage. Again, care must be taken to ensure that the single-ended signal has an offset equal to the voltage supplied at the negative input of the channel.

## 5 Using the Software: ADS1198 Control Registers and GUI

Before starting to use the EVM software, there is one important feature that users should be aware of. The software GUI contains a Save tab that allows all data from any combination of channels to be saved in a given directory location with notes to describe the saved data. [Figure 8](#) shows the Save tab options.



**Figure 8. File Save Option Under Save Tab**

### 5.1 Overview and Features

This section provides a quick overview of the various features and functions of the ADS1198ECG-FE software package.

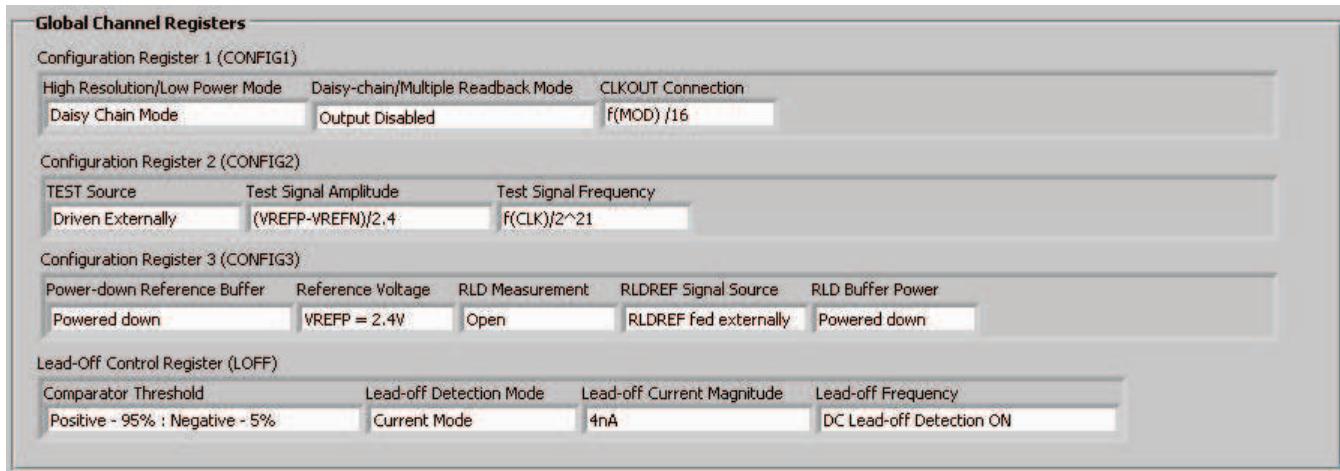
There are four primary tabs across the left side of the GUI:

- **About** tab: Provides information about the EVM and software version revisions.
- **ADC Register** tab: Includes all of the control registers for the ADS1198, in a series of related sub-tabs:
  - Channel Registers tab
  - LOFF and RLD tab
  - GPIO and Other Registers tab
  - Register Map tab
- **Analysis** tab: Provides different ways to analyze captured data in the time or frequency domain, with a series of related sub-tabs:
  - Scope tab
  - FFT tab
  - Histogram tab
  - ECG Display tab
- **Save** tab: Provides options for saving data

### 5.2 Global Channel Registers

The first section under the *Channel Registers*→*Global Channel Registers* tab allows the user to manipulate all of the ADS1198 configuration and lead-off registers. The Global Channel Registers box includes Configuration Register 1 (controls resolution, daisy-chain/MRB mode, clock, and data rate); Configuration Register 2 (controls internal test source amplitude and frequency); Configuration Register 3

(controls the reference buffer power-up/-down processes, the reference voltage, the right leg drive (RLD) enable/disable, and the RLD reference); and the Lead Off Control Register, which controls the comparator threshold, lead-off detection mode (either resistive pull-up or current source), and the magnitude and frequency of the lead-off signal. [Figure 9](#) shows the GUI panel to manipulate these registers and the respective settings for each.



**Figure 9. Channel Registers GUI for Global Channel Registers**

[Table 9](#) highlights the respective section of the Register Map table taken from the [ADS1198 product data sheet](#).

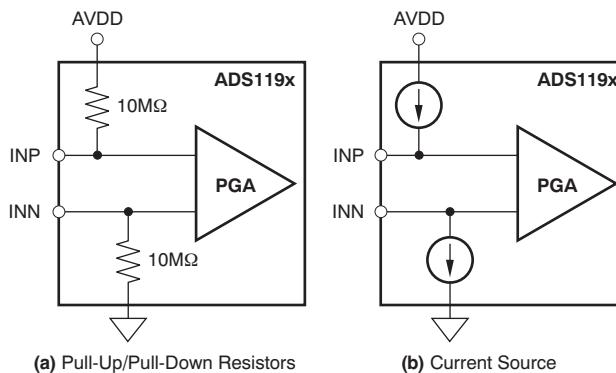
**Table 9. Register Assignments: Global Channel Registers**

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>Global Settings Across Channels</b>										
01h	CONFIG1	06	HR	DAISY_EN	CLK_EN	0	0	DR2	DR1	DR0
02h	CONFIG2	40	0	1	0 <sup>(1)</sup>	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0
03h	CONFIG3	40	PD_REFBUF	1	VREF_4V	RLD_MEAS	RLDREF_INT	PD_RLD	RLD_LOFF_SENS	RLD_STAT
04h	LOFF	00	COMP_TH2	COMP_TH1	COMP_TH0	VLEAD_OFF_EN	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0

<sup>(1)</sup> This register bit must be written to '1' at power-up if hardware PACE detect is used on a lead using the WCT signal.

### 5.2.1 Lead-Off Control Register

The Lead-Off Control Register allows the user to configure the threshold for the lead-off comparator, resistive pull-up or current-source excitation, the lead-off current magnitude, and dc or ac detection. Figure 10 illustrates a simplified diagram of the resistive pull-up and excitation options for the lead-off detect feature.

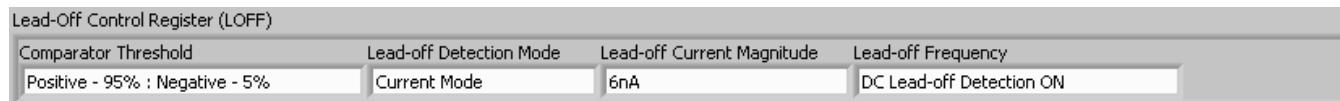


**Figure 10. Lead-Off Excitation Options**

Table 10 shows the corresponding register and Figure 11 shows the respective GUI controls.

**Table 10. LOFF: Lead-Off Control Register (Address: 04h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMP_TH2	COMP_TH1	COMP_TH0	VLEAD_OFF_EN	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0



**Figure 11. Lead-Off Control Register GUI Controls**

### 5.2.2 Configuration Register 1

Configuration Register 1 enables the user to control the resolution mode (that is, high-resolution or low-power mode), enable the daisy-chain configuration options, and program the data rate. Table 11 shows the register settings. Figure 12 illustrates the respective GUI controls.

**Table 11. CONFIG1: Configuration Register 1 (Address = 01h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HR	DAISY_EN	CLK_EN	0	0	DR2	DR1	DR0



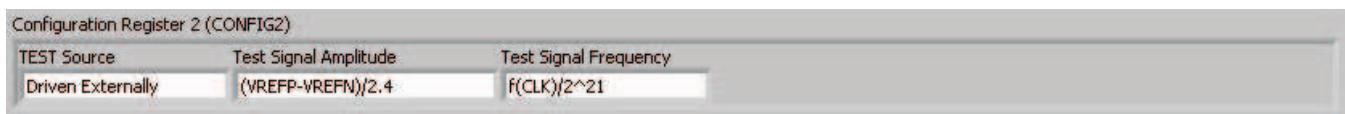
**Figure 12. Configuration Register 1 GUI Panel**

### 5.2.3 Configuration Register 2

Configuration Register 2 enables the user to select and program an internal square wave test source amplitude to  $\pm 1\text{mV}$  or  $\pm 2\text{mV}$  and its frequency to dc, 2Hz, or 4Hz. [Table 12](#) shows the register map for Configuration Register 2; the GUI controls are shown in [Figure 13](#).

**Table 12. CONFIG2: Configuration Register 2 (Address = 02h)**

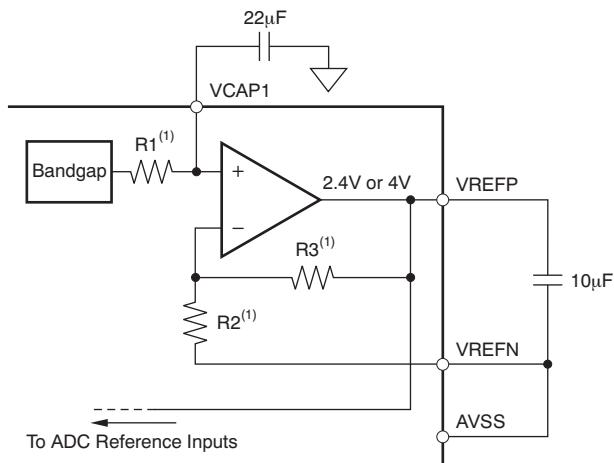
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0



**Figure 13. Configuration Register 2 GUI Controls**

### 5.2.4 Configuration Register 3

Configuration Register 3 controls the bandgap reference (illustrated in [Figure 14](#)) and right leg drive (RLD) options. This register enables the user to select between an external or internal reference voltage, enable/disable the internal reference buffer, toggle between a 2.4V or a 4.0V output voltage, and to enable/disable the RLD as well as choose whether the RLD voltage is provided internally or externally. The register map is provided in [Table 13](#); [Figure 15](#) shows the GUI display for Configuration Register 3.



**Figure 14. Internal Reference and Buffer Connections**

**Table 13. CONFIG3: Configuration Register 3 (Address = 03h)**

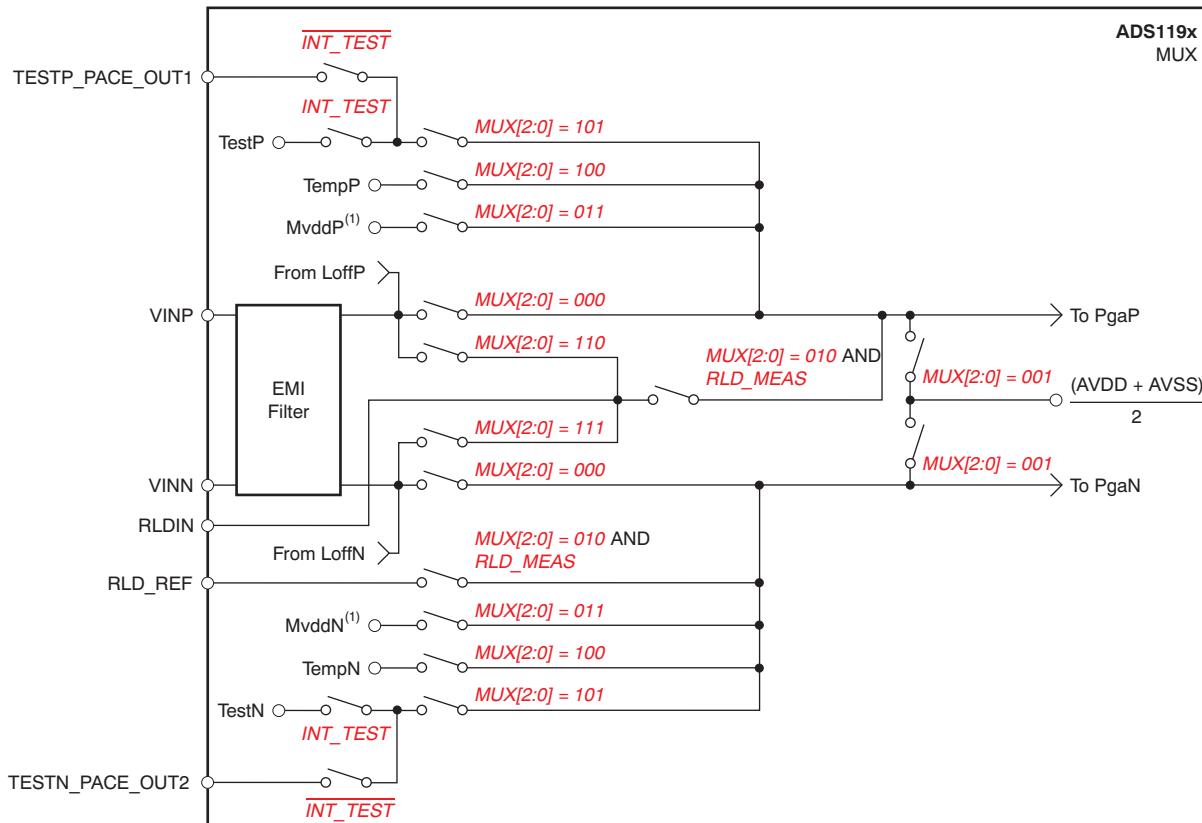
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PD_REFBUF	1	VREF_4V	RLD_MEAS	RLDREF_INT	PD_RLD	RLD_LOFF_SENS	RLD_STAT



**Figure 15. Configuration Register 3 GUI Controls**

### 5.3 Channel Control Registers

The second section under the Channel Registers tab is the *Channel Control Registers* box. This panel allows the user to uniquely configure the front-end MUX for each channel. Additionally, at the top of the Channel Control Registers box is the option to globally set all channels to the same setting. The channel-specific MUX is illustrated in Figure 16.



**Figure 16. Input Multiplexer for a Single Channel**

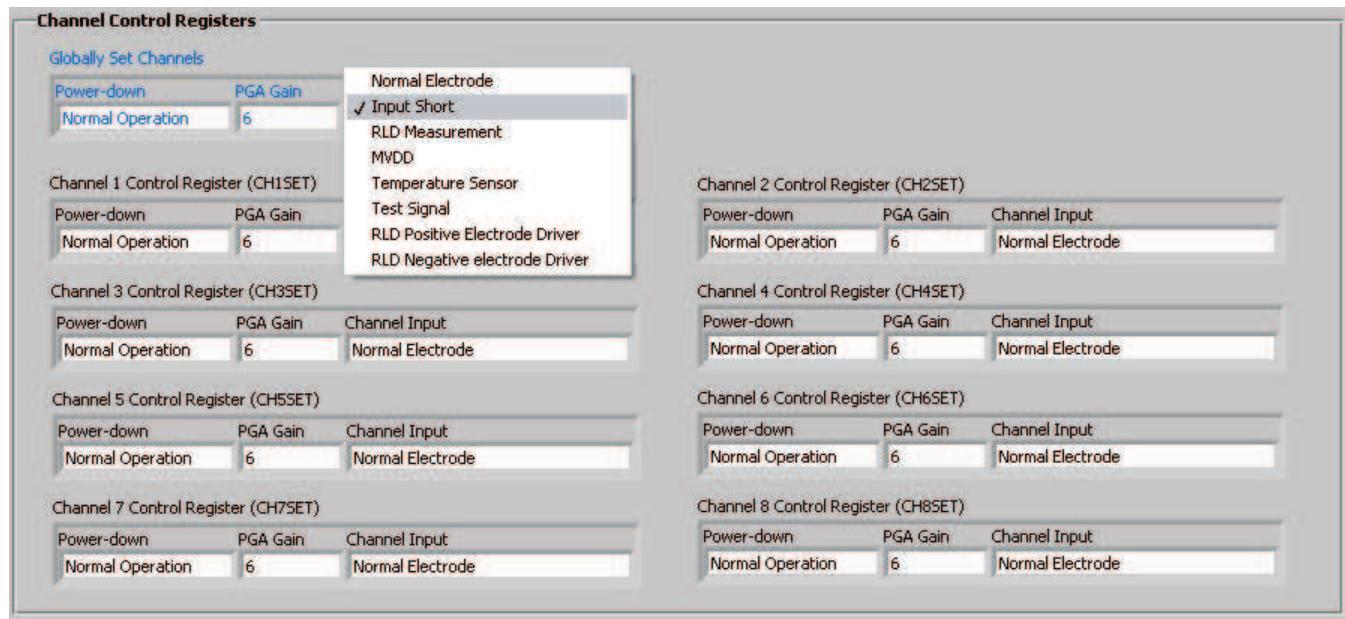
Table 9 lists the register map, while the GUI panel for this MUX and register map is given in Figure 17.

**Table 14. Register Assignments: Channel-Specific Settings**

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>Channel-Specific Settings</b>										
05h	CH1SET	00	PD1	GAIN12	GAIN11	GAIN10	0	MUXn2	MUXn1	MUXn0
06h	CH2SET	00	PD2	GAIN22	GAIN21	GAIN20	0	MUX22	MUX21	MUX20
07h	CH3SET	00	PD3	GAIN32	GAIN31	GAIN30	0	MUX32	MUX31	MUX30
08h	CH4SET	00	PD4	GAIN42	GAIN41	GAIN40	0	MUX42	MUX41	MUX40
09h	CH5SET <sup>(1)</sup>	00	PD5	GAIN52	GAIN51	GAIN50	0	MUX52	MUX51	MUX50
0Ah	CH6SET <sup>(1)</sup>	00	PD6	GAIN62	GAIN61	GAIN60	0	MUX62	MUX61	MUX60
0Bh	CH7SET <sup>(1)</sup>	00	PD7	GAIN72	GAIN71	GAIN70	0	MUX72	MUX71	MUX70
0Ch	CH8SET <sup>(1)</sup>	00	PD8	GAIN82	GAIN81	GAIN80	0	MUX82	MUX81	MUX80
0Dh	RLD_SENSP <sup>(2)</sup>	00	RLD8P <sup>(1)</sup>	RLD7P <sup>(1)</sup>	RLD6P <sup>(1)</sup>	RLD5P <sup>(1)</sup>	RLD4P	RLD3P	RLD2P	RLD1P
0Eh	RLD_SENSN <sup>(2)</sup>	00	RLD8N <sup>(1)</sup>	RLD7N <sup>(1)</sup>	RLD6N <sup>(1)</sup>	RLD5N <sup>(1)</sup>	RLD4N	RLD3N	RLD2N	RLD1N
0Fh	LOFF_SENSP <sup>(2)</sup>	00	LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P
10h	LOFF_SENSN <sup>(2)</sup>	00	LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N
11h	LOFF_FLIP	00	LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1

<sup>(1)</sup> CH5SET and CH6SET are not available for the ADS1294. CH7SET and CH8SET registers are not available for the ADS1294 and ADS1296.

<sup>(2)</sup> The RLD\_SENSP, PACE\_SENSP, LOFF\_SENSP, LOFF\_SENSN, and LOFF\_FLIP registers bits[5:4] are not available for the ADS1294. Bits[7:6] are not available for the ADS1294/6.



**Figure 17. Channel Control Registers GUI Panel**

## 5.4 Internal Test Signals Input and the ECG Display Tab

Configuration Register 2 controls the signal amplitude and frequency of an internally-generated square wave test signal. The primary purpose of this test signal is to verify the functionality of the front-end MUX, the PGA, and the ADC. The test signals may be viewed on the *Analysis*→*ECG Display* tab, as Figure 18 shows. Detailed instructions for using the *Analysis*→*ECG Display* tab is provided in [Section 6.1.4](#).

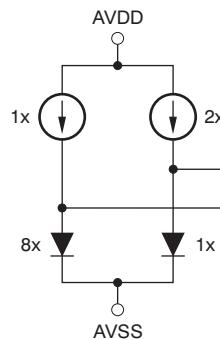


**Figure 18. Example of Internal Test Signals Viewed on the ECG Display Tab**

## 5.5 Temperature Sensor and the Scope Tab

The internal temperature sensor on the ADS1198 is shown in [Figure 19](#). When the internal MUX is routed to the temperature sensor input, the output voltage of the ADC may be converted to a temperature value, using [Equation 1](#).

$$\text{Temperature } (\text{°C}) = \left( \frac{\text{Temperature Reading } (\mu\text{V}) - 145,300\mu\text{V}}{490\mu\text{V}/\text{°C}} \right) + 25\text{°C} \quad (1)$$



**Figure 19. Internal Temperature Sensor**

The output voltage corresponding to a give temperature can be read selecting the *Temperature Sensor* option on the Channel Control Registers GUI (see [Figure 17](#)) and verified using the *Analysis*→*Scope tab* as shown in [Figure 20](#). The number **0.1447V** (on the y-axis) can be calculated as a temperature using [Equation 1](#):

$$\text{Temperature} = (0.1447 - 0.145300) / 0.00049 + 25 = 23.78\text{°C}$$

A more detailed description of the Scope tab is provided in [Section 6.1.1](#).



**Figure 20. Eight-Channel Read of Internal Temperature**

## 5.6 Normal Electrode Input and the ECG Display Tab

The *Normal electrode* input on the MUX routes the inputs (VINP and VINV) differentially to the internal PGA, as Figure 16 illustrates. In this mode, an ECG, sine wave, or pulse generator may be connected to test the ADS1198.

Figure 21 shows a typical six-lead output when connected to a 5mV<sub>PEAK</sub>, 80BPM ECG signal.



**Figure 21. Normal Electrode ECG Connection in ECG Display Tab**

### 5.6.1 MV<sub>DD</sub> Input and the Scope Tab

The MV<sub>DD</sub> input option allows the measurement of the supply voltage  $V_S = (AV_{DD} + AV_{SS})/2$  for channels 1, 2, 5, 6, 7, and 8; however, the supply voltage for channel 3 will be DV<sub>DD</sub>/2. As an example, in bipolar supply mode, AV<sub>DD</sub> = 3.0V and AV<sub>SS</sub> = -2.5V. Therefore, with the PGA gain = 1, the output voltage measured by the ADC will be approximately 0.25V.

### 5.6.2 RLD Measurement, RLD Positive Electrode Driver, and RLD Negative Electrode Driver

This measurement takes the voltage at the RLDIN pin and measures it on the PGA with respect to (AV<sub>DD</sub> + AV<sub>SS</sub>)/2. This feature is beneficial if the user would like to optimize the gain of the RLD loop. The voltage used to derive the right leg drive for both the positive and negative electrodes may also be measured with respect to (AV<sub>DD</sub> + AV<sub>SS</sub>)/2.

## 5.7 GPIO and Other Registers

The *GPIO and Other Registers* tab, located under the *Analysis* tab, includes controls for GPIO1 through GPIO4, respiration phase and frequency, routing of the Wilson amplifiers, and derivation of the Goldberger terminals.

### 5.7.1 General-Purpose I/O Register (GPIO)

The GPIO registers control four general-purpose I/O pins; [Table 15](#) shows the respective register to control these pins. Note that if respiration mode is enabled, these GPIO pins become dedicated to respiration functions and are not available for other use. [Figure 22](#) illustrates the GPIO Control Register GUI panel.

**Table 15. GPIO: General-Purpose I/O Register (Address = 14h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1



**Figure 22. GPIO Control Register GUI Panel**

### 5.7.2 PACE Detect Register

The PACE Detect Register **does not** enable a special PACE measurement mode; rather, it configures Pace Amplifier 1 to connect to input channels 1-4 or Pace Amplifier 2 to connect to input channels 5-8. [Table 16](#) and [Figure 23](#) show register settings (from the data sheet) and the GUI controls, respectively, for setting the PACE Register amplifiers.

**Table 16. PACE: PACE Detect Register (Address = 15h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	PACEE1	PACEO0	PACEO1	PACEO0	PD_PACE



**Figure 23. PACE Detect Register GUI Controls**

### 5.7.3 Respiration Control Register

The Respiration Control Register allows the user to configure the respiration frequency, single-shot or continuous-conversion mode, routing of the Wilson Central terminals to the RLD reference, and enabling/disabling the lead-off comparators. The register table is given in [Table 17](#), and the Respiration Register GUI controls are illustrated in [Figure 24](#).

**Table 17. RESP: Respiration Control Register (Address = 16h)**

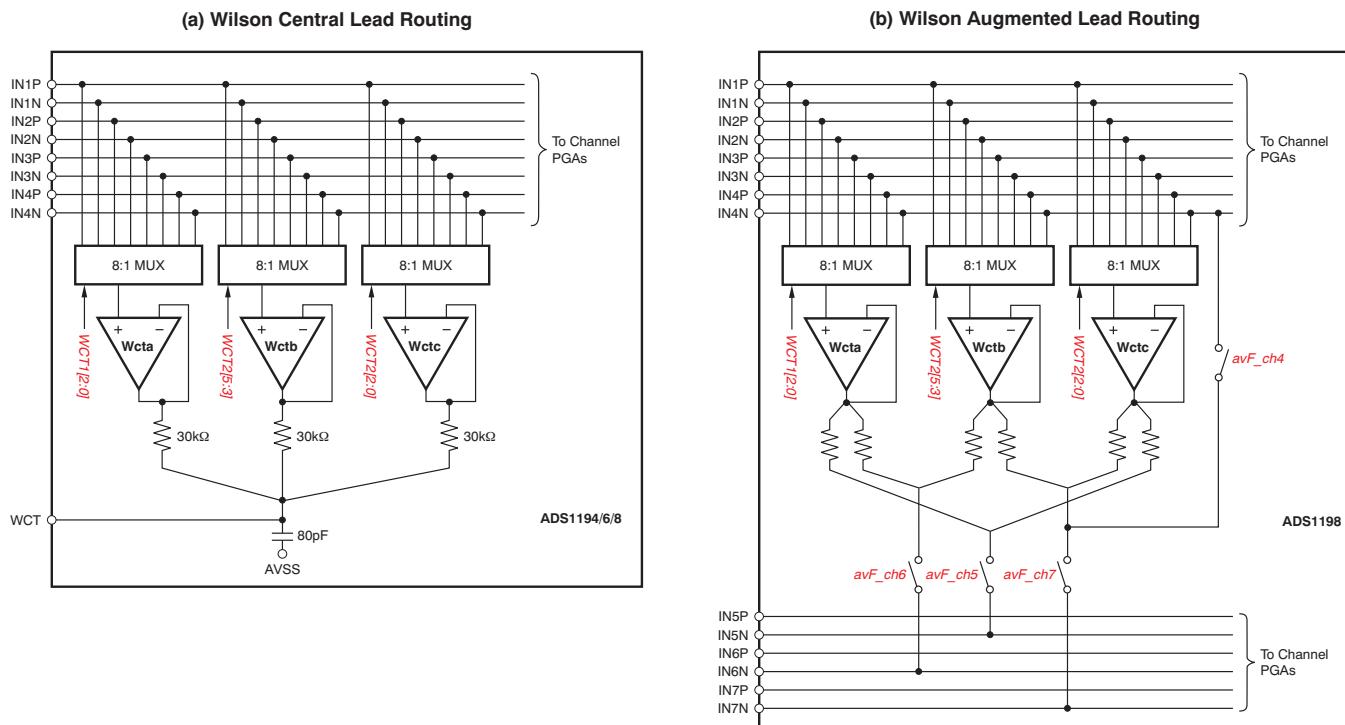
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RESP_DEMOD_EN1	RESP_MOD_EN1	RESP_MOD_VREFP	RESP_PH2	RESP_PH1	RESP_PH0	RESP_CTRL1	RESP_CTRL0



**Figure 24. Respiration Control Register GUI Panel**

### 5.7.4 Wilson Central and Augmented Lead Registers

The Wilson Central Voltage (an average voltage between the right arm [RA], left arm [LA], and left leg [LL] connections) can be derived from any combination of positive and negative terminals from channels 1-4 and routed to the WCT pin. Likewise, the Augmented Leads (AVF, AVL, AVR) may be derived from channels 1-4 and routed to the negative terminal of channels 5, 6, and 7. [Figure 25](#) shows these configurations; [Figure 25a](#) illustrates the central lead routing, and [Figure 25b](#) shows the augmented lead routing.



**Figure 25. Wilson Central and Augmented Lead Routing Diagrams**

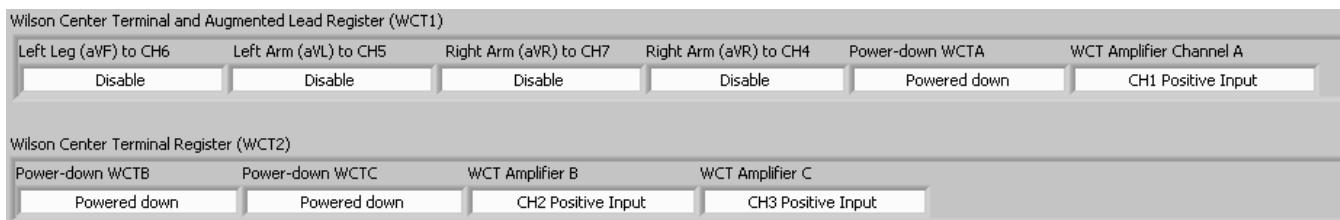
Table 18 and Table 19 show the respective register settings. Figure 26 illustrates the GUI control panel for these registers.

**Table 18. WCT1: Wilson Center Terminal and Augmented Lead Control Register (Address = 18h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
aVF_CH6	aVL_CH5	aVR_CH7	aVR_CH4	PD_WCTA	WCTA2	WCTA1	WCTA0

**Table 19. WCT2: Wilson Center Terminal Control Register (Address = 19h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PD_WCTC	PD_WCTBC	WCTB2	WCTB1	WCTB0	WCTC2	WCTC1	WCTC0



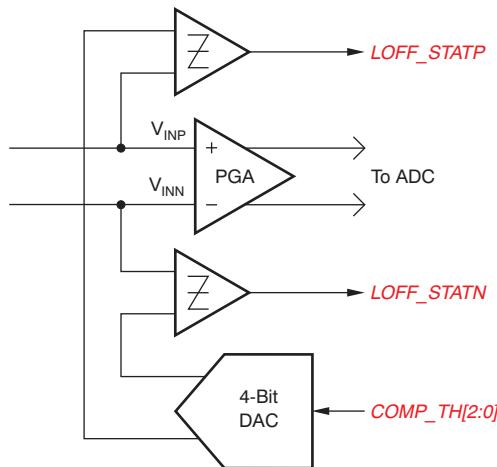
**Figure 26. Wilson Central and Augmented Lead Register GUI Controls**

## 5.8 Lead-Off and RLD Registers

The Lead-Off Detection and Current Control Registers and the Right Leg Derivation Control Registers are located under the *ADC Register→LOFF and RLD tab*.

### 5.8.1 Lead-Off Sense (LOFF\_SENSP and LOFF\_SENSN) Registers

These registers enable lead-off detection for both the positive and negative channels. Figure 10 describes the mode for Lead-Off Detection (that is, resistive or current source) and the 4-bit DAC settings to configure the lead-off threshold. Note that the LOFF\_FLIPx bits change the direction of the lead-off current if this option is selected. Figure 27 illustrates the connections from the positive and negative inputs to the lead-off comparators. Table 20 through Table 22 list the register tables for the lead-off comparators, and Figure 28 shows the respective GUI panel on the EVM software.



**Figure 27. LOFF\_STATP and LOFF\_STATN Comparators**

**Table 20. LOFF\_SENSP (Address = 0Fh)**

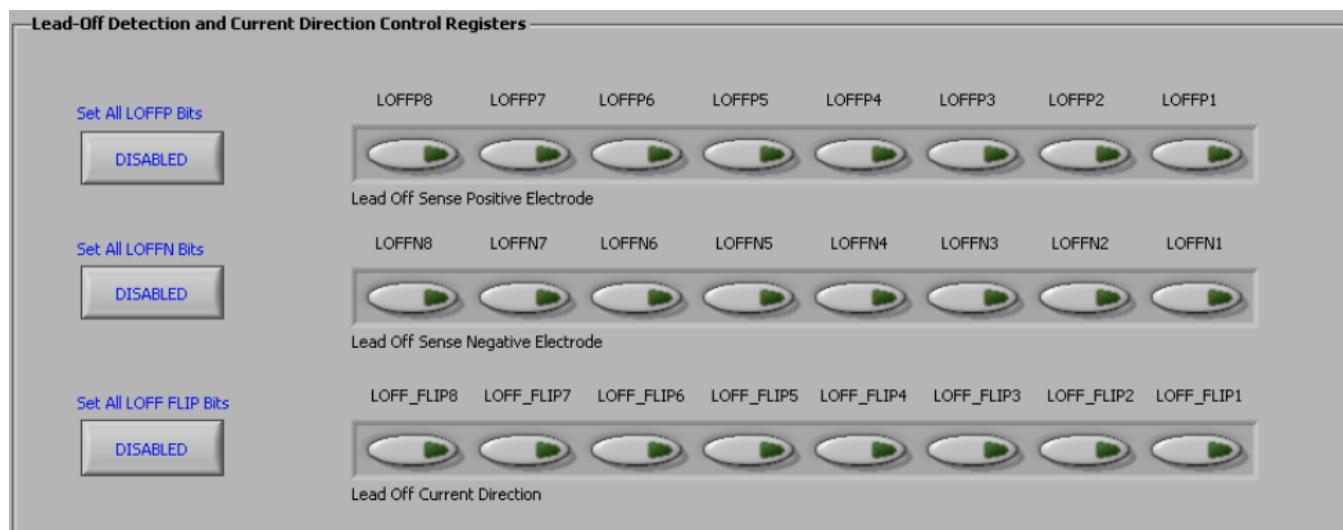
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P

**Table 21. LOFF\_SENSN (Address = 10h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N

**Table 22. LOFF\_FLIP (Address = 11h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1

**Figure 28. LOFF\_SENSP and LOFF\_SENSN Registers GUI Controls**

### 5.8.2 Lead-Off Status Registers (LOFF\_STATP and LOFF\_STATN)

These registers (shown in [Table 23](#) and [Table 24](#)) store the output of the lead-off comparator that corresponds with each input. When a lead is disconnected, the corresponding register bit activates low. The GUI for this feature is enabled by clicking in the upper right-hand corner of the EVM software on the **Show/Poll Lead-Off Status** button. Pressing this button causes a pop-up box that shows the status of the lead-off registers. The GUI shows when a lead is disconnected by turning its bit from green to red. [Figure 29](#) illustrates the Lead-Off Status Registers GUI controls.

**Table 23. LOFF\_STATP (Read-Only; Address = 12h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF

**Table 24. LOFF\_STATN (Read-Only; Address = 13h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF

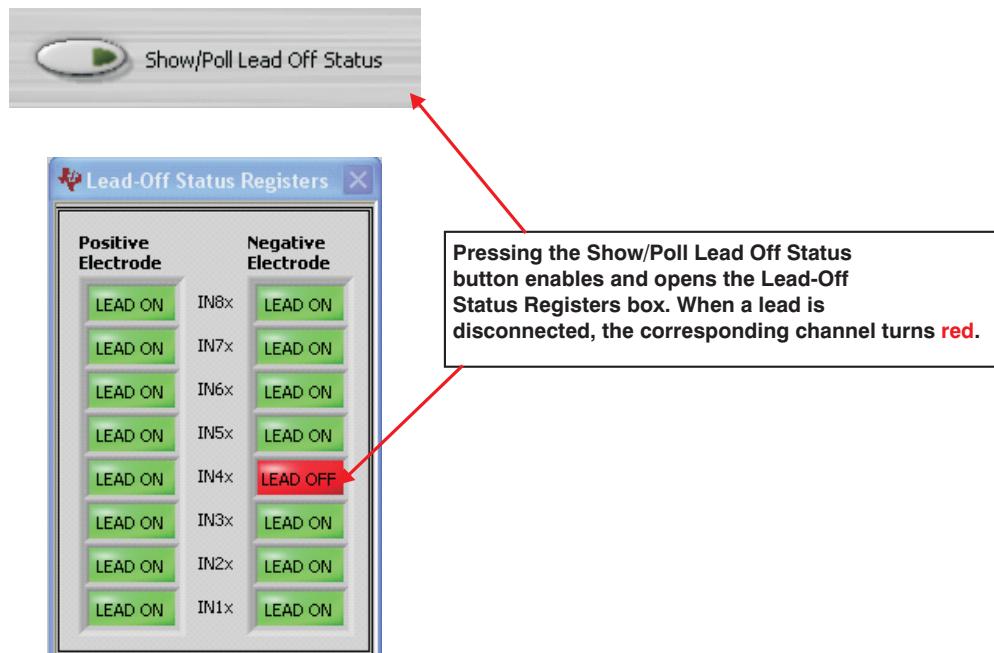


Figure 29. Lead-Off Status Registers GUI Controls

### 5.8.3 Right Leg Drive Derivation Control Registers

The Right Leg Drive Derivation Control Registers enable the user to set any combination of positive and/or negative electrodes to derive the RLD voltage that is fed to the internal right leg drive amplifier. [Table 25](#) and [Table 26](#) list the RLD\_SENSP and RLD\_SESN registers, respectively, that control these bits. [Figure 30](#) shows the corresponding GUI controls.

Table 25. RLD\_SENSP (Address = 0Dh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RLD8P	RLD7P	RLD6P	RLD5P	RLD4P	RLD3P	RLD2P	RLD1P

Table 26. RLD\_SESN (Address = 0Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RLD8N	RLD7N	RLD6N	RLD5N	RLD4N	RLD3N	RLD2N	RLD1N

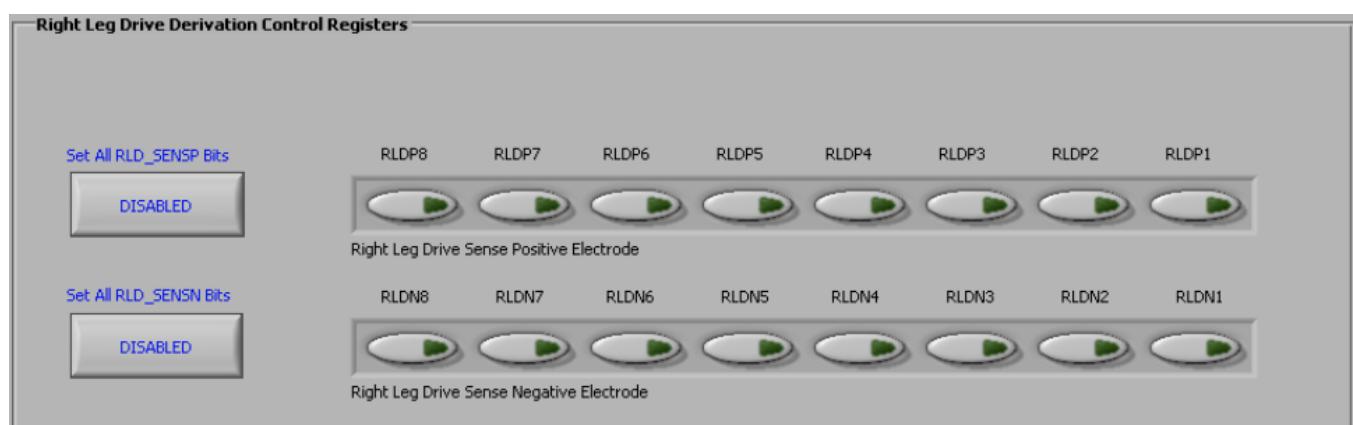


Figure 30. RLD\_SENSP and RLD\_SESN GUI Controls

## 5.9 Register Map

The *Register Map→ Device Registers* tab is a helpful debug feature that allows the user to view the state of all the internal registers. This tab is illustrated in [Figure 31](#).

Device Registers										
Register	Address	Value	D7	D6	D5	D4	D3	D2	D1	D0
ID	0x00	0xB6	1	0	1	1	0	1	1	0
CONFIG1	0x01	0x06	0	0	0	0	0	1	1	0
CONFIG2	0x02	0x10	0	0	0	1	0	0	0	0
CONFIG3	0x03	0xDC	1	1	0	1	1	1	0	0
LOFF	0x04	0x13	0	0	0	1	0	0	1	1
CH1SET	0x05	0x05	0	0	0	0	0	1	0	1
CH2SET	0x06	0x05	0	0	0	0	0	1	0	1
CH3SET	0x07	0x05	0	0	0	0	0	1	0	1
CH4SET	0x08	0x05	0	0	0	0	0	1	0	1
CH5SET	0x09	0x05	0	0	0	0	0	1	0	1
CH6SET	0x0A	0x05	0	0	0	0	0	1	0	1
CH7SET	0x0B	0x05	0	0	0	0	0	1	0	1
CH8SET	0x0C	0x05	0	0	0	0	0	1	0	1
RLD_SENSP	0x0D	0x00	0	0	0	0	0	0	0	0
RLD_SENSN	0x0E	0x00	0	0	0	0	0	0	0	0
LOFF_SENSP	0x0F	0xFF	1	1	1	1	1	1	1	1
LOFF_SENSN	0x10	0xFF	1	1	1	1	1	1	1	1
LOFF_FLIP	0x11	0x00	0	0	0	0	0	0	0	0
LOFF_STATP	0x12	0x00	0	0	0	0	0	0	0	0
LOFF_STATN	0x13	0x00	0	0	0	0	0	0	0	0
GPIO	0x14	0x00	0	0	0	0	0	0	0	0
PACE	0x15	0x00	0	0	0	0	0	0	0	0
CONFIG4	0x17	0x02	0	0	0	0	0	0	1	0
WCT1	0x18	0x0A	0	0	0	0	1	0	1	0
WCT2	0x19	0xE3	1	1	1	0	0	0	1	1

Refresh Registers
(automatically updates if coming from another page)

**Figure 31. Device Registers Settings**

## 6 ADS1198ECG-FE Analysis Tools

Under the *Analysis* tab in the ADS1198ECG-FE GUI software, there are four different analysis tools shown that enable a detailed examination of the signals selected by the front-end MUX:

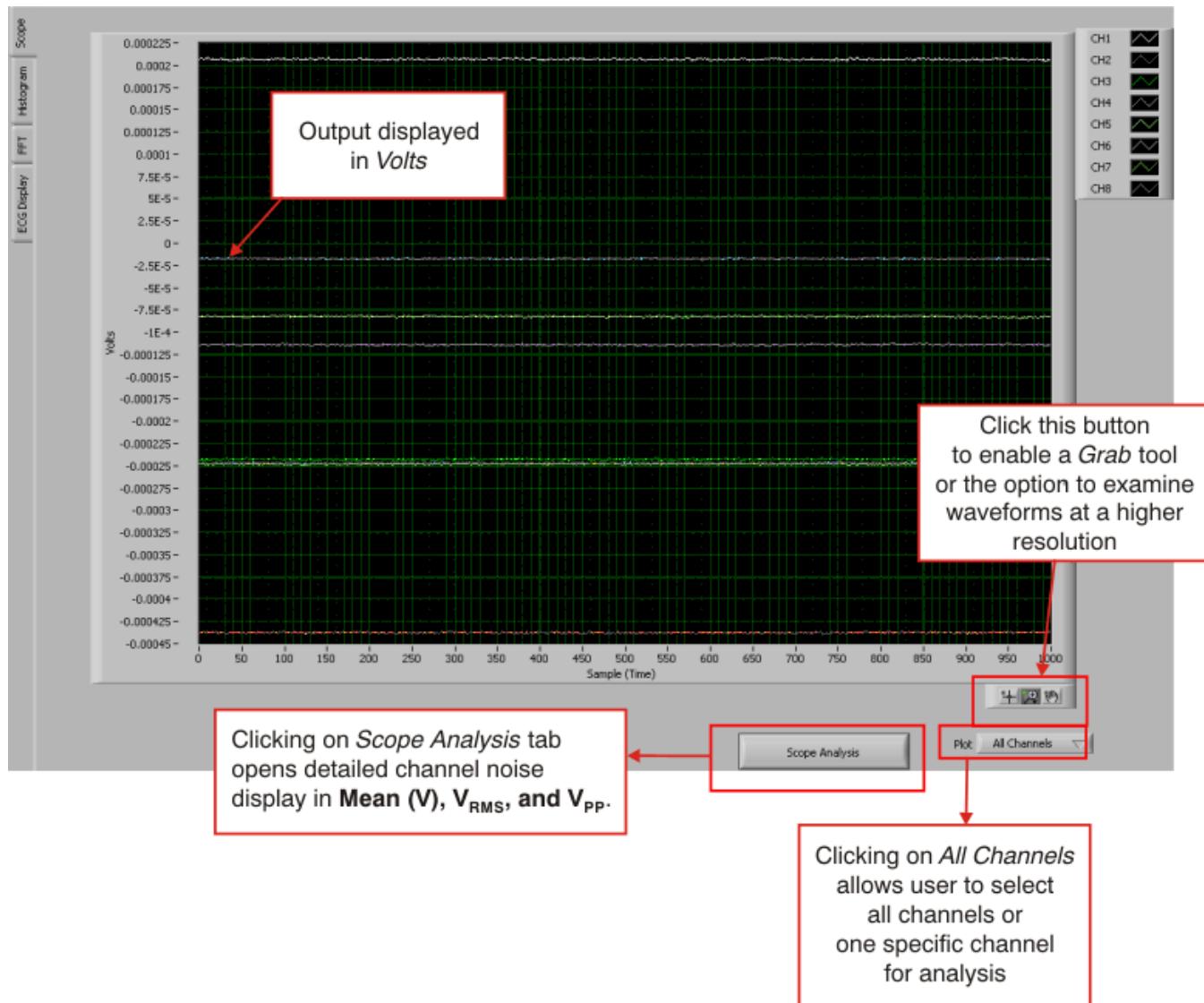
- Scope
- Analysis
- Histogram
- FFT

These tools are detailed in the following subsections.

### 6.1 Scope Tab

#### 6.1.1 Using the Analysis→Scope Tool

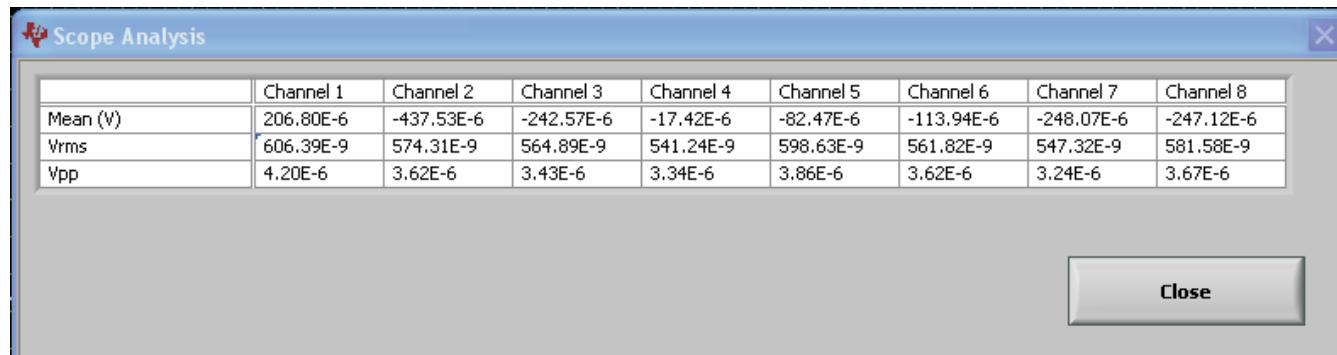
The Scope tool (available under the *Analysis* tab) is a very useful means of examining the exact amplitude of the measured input signals from each channel. Additionally, users can determine the noise contribution from each channel at a given resolution, and review the sampling rate, the PGA gain, and the input signal amplitude. [Figure 32](#) illustrates the Scope tool features.



**Figure 32. Scope Tool Features**

### 6.1.2 Scope Analysis Button

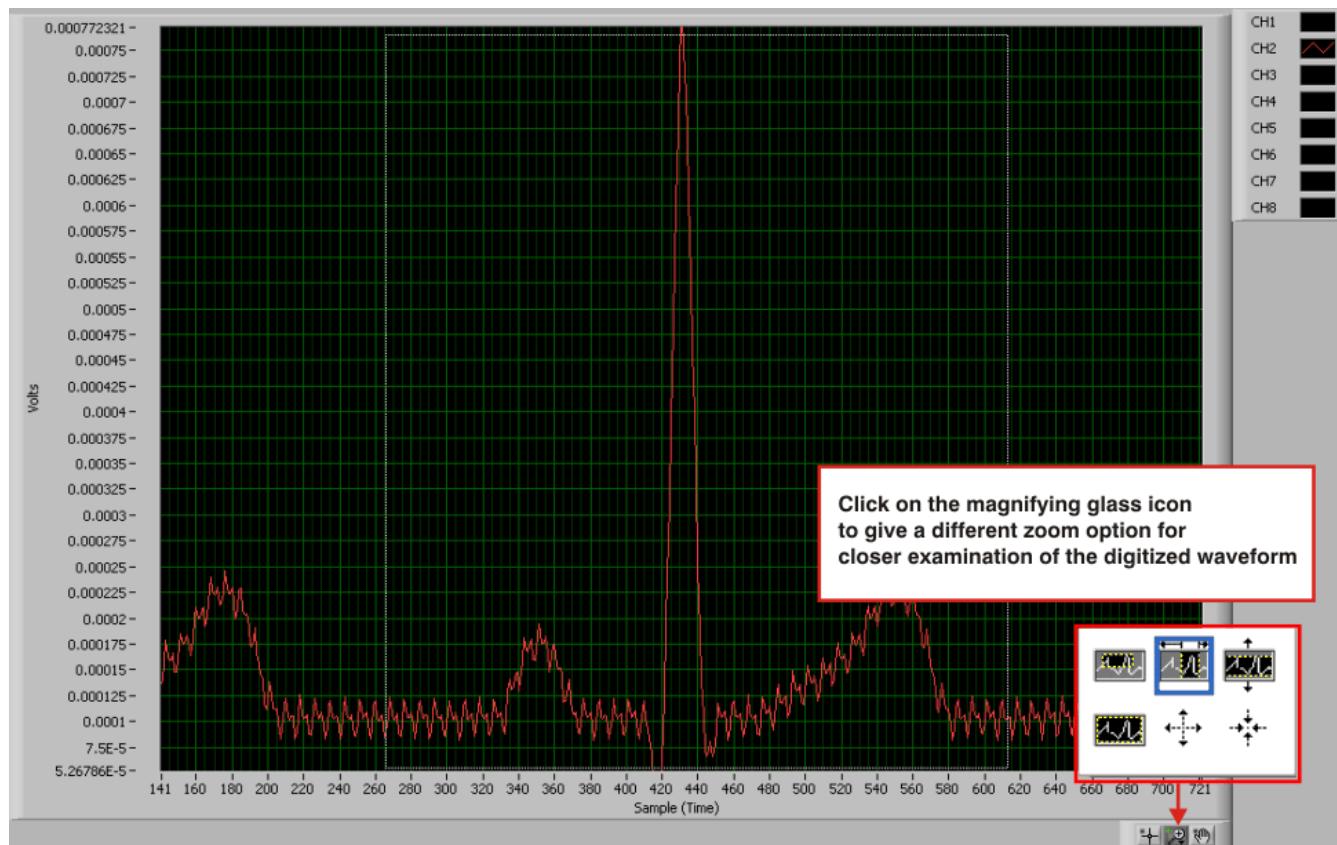
In the *Scope Analysis* tab, as [Figure 33](#) illustrates, the different noise levels are displayed when the MUX is selected as *Input Short*, PGA gain is set to 6 (default), and the sample rate is set to 500 samples per second (SPS).



**Figure 33. Scope Analysis Tab (Noise Levels for Each Channel Shown)**

### 6.1.3 Waveform Examination Tool

The waveform examination tool allows the user to zoom in either on all channels simultaneously or on a single channel. [Figure 34](#) shows an example of the waveform examination tool with the magnifying glass zoomed in on Channel 2. In this case, the tool makes it much easier to determine that the noise seen on the ECG waveform is a result of 50Hz/60Hz line cycle noise.



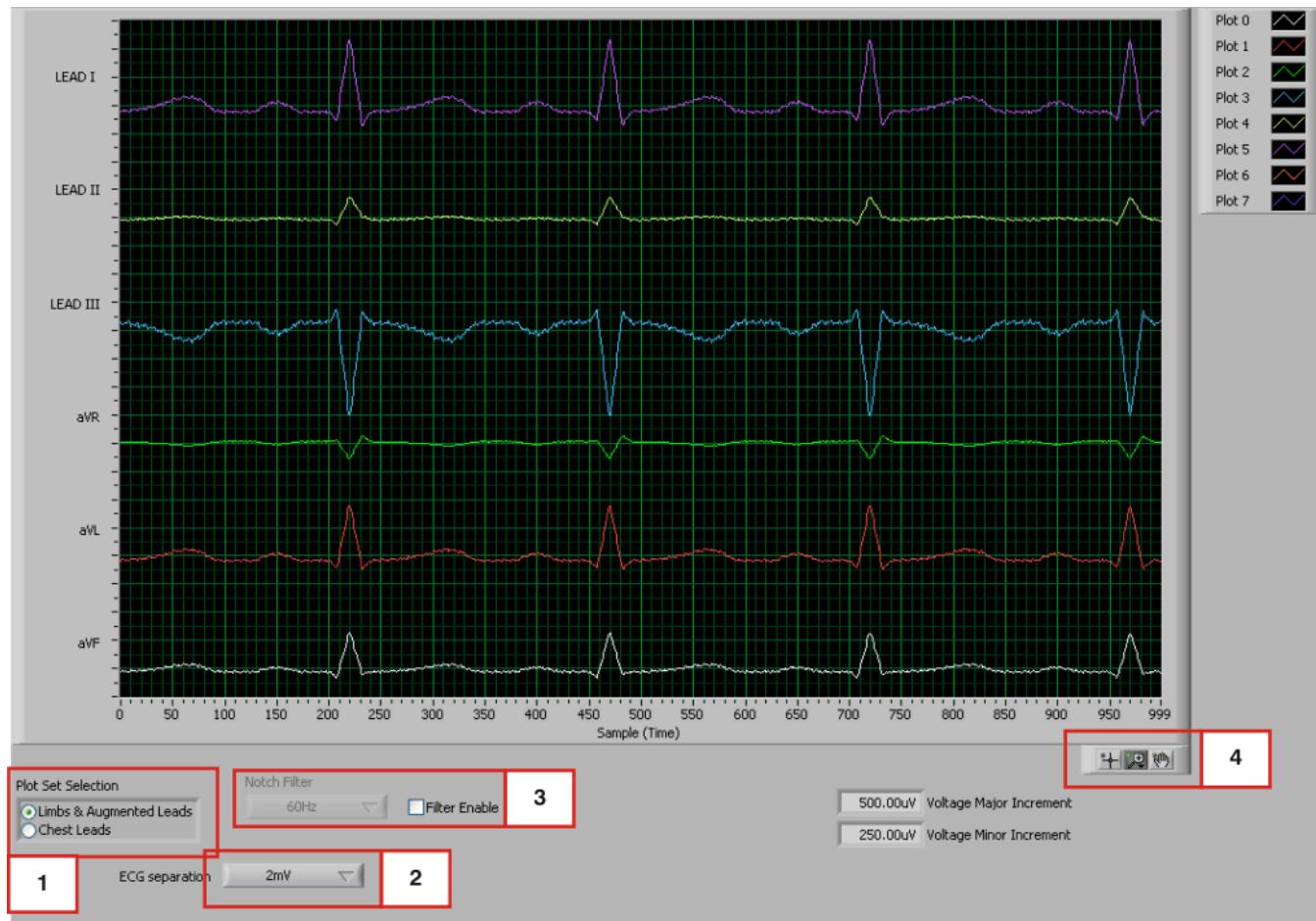
**Figure 34. Zoom Option on the Waveform Examination Tool**

## 6.1.4 ECG Display Tool

The ECG display tool is located under the *Analysis*→*ECG Display* tab.

### 6.1.4.1 Using the Analysis→Scope Tool

This tool allows the user to examine the input signal according to the different lead configurations. For a detailed description of the lead configurations, see [Table 27 in Section 7.2](#). [Figure 35](#) shows Leads I-III and the Augmented Lead outputs with the input MUX configured in *Normal Electrode* mode. [Figure 35](#) also shows numerical annotations 1 to 4, which highlight the different features of this tool. These features are described in detail in the following subsections.



**Figure 35. ECG Display Tab Showing LEAD I-III and Augmented Leads**

#### Plot Set Feature: 1

The Plot Set feature, indicated by Box 1 in [Figure 35](#), allows the user to change the visual selection between the Leads I-III and the augmented leads, and the chest leads.

#### ECG Separation Feature: 2

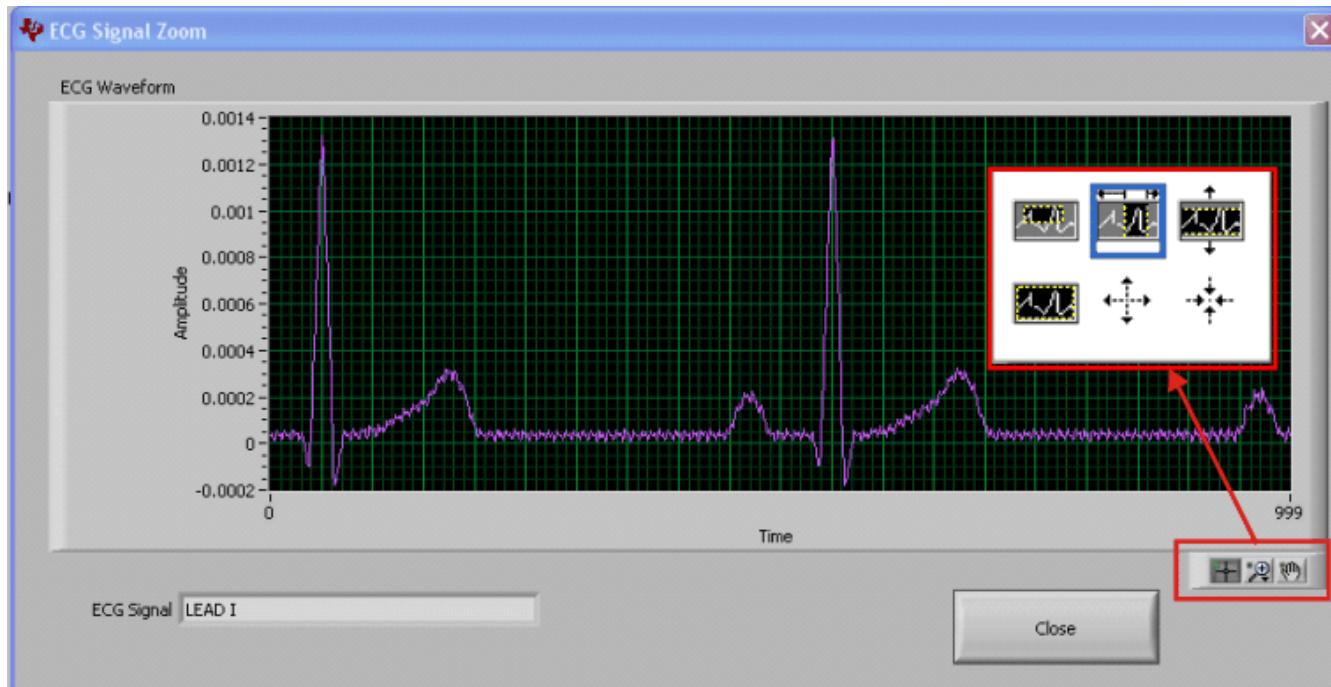
The ECG Separation feature (marked as Box 2) toggles the vertical distance between the input plots. This capability is useful when ECG signals are large and require more separation to avoid overlap, or to collapse the range between signals when the ECG signals are small.

#### Notch Filter Feature: 3

The Notch Filter is a finite-impulse response (FIR) filter that may be enabled only at sample rates greater than 500SPS. To activate this feature, check the box *Filter Enable* and select the notch frequency of either 50Hz or 60Hz.

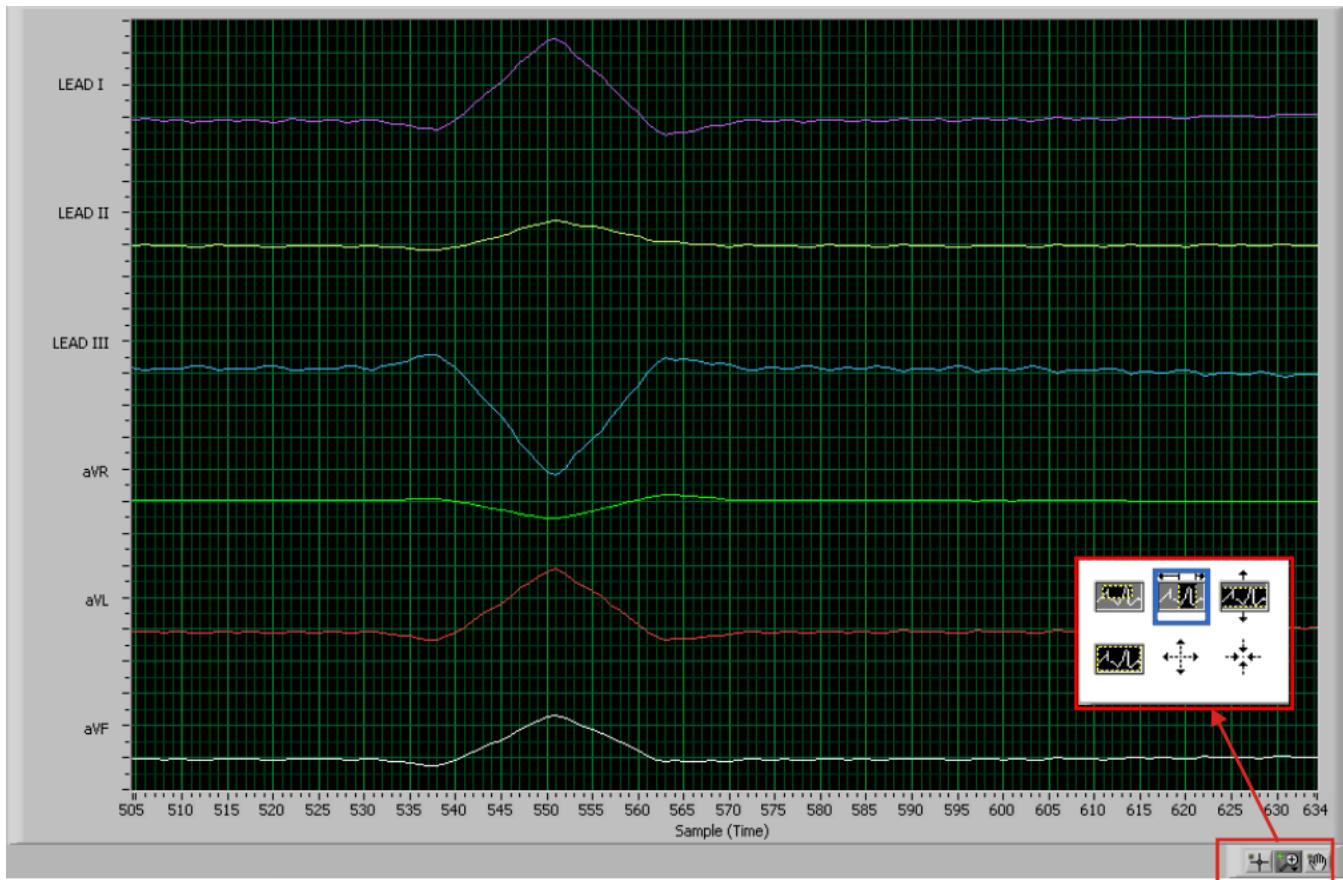
#### ECG Signal Zoom Feature: 4

The ECG Signal Zoom feature, similar to the waveform examination tool, may be enabled by moving the mouse (which appears as a magnifying glass) over the lead of interest and clicking on it. As **Figure 36** illustrates, a pop-up box will appear with the signal analysis options in the lower right-hand corner. Using these options allows a much closer zoom on the waveform.



**Figure 36. ECG Signal Zoom Feature for Lead 1**

The ECG Signal Zoom feature may also be used on all six leads, as shown in [Figure 37](#).



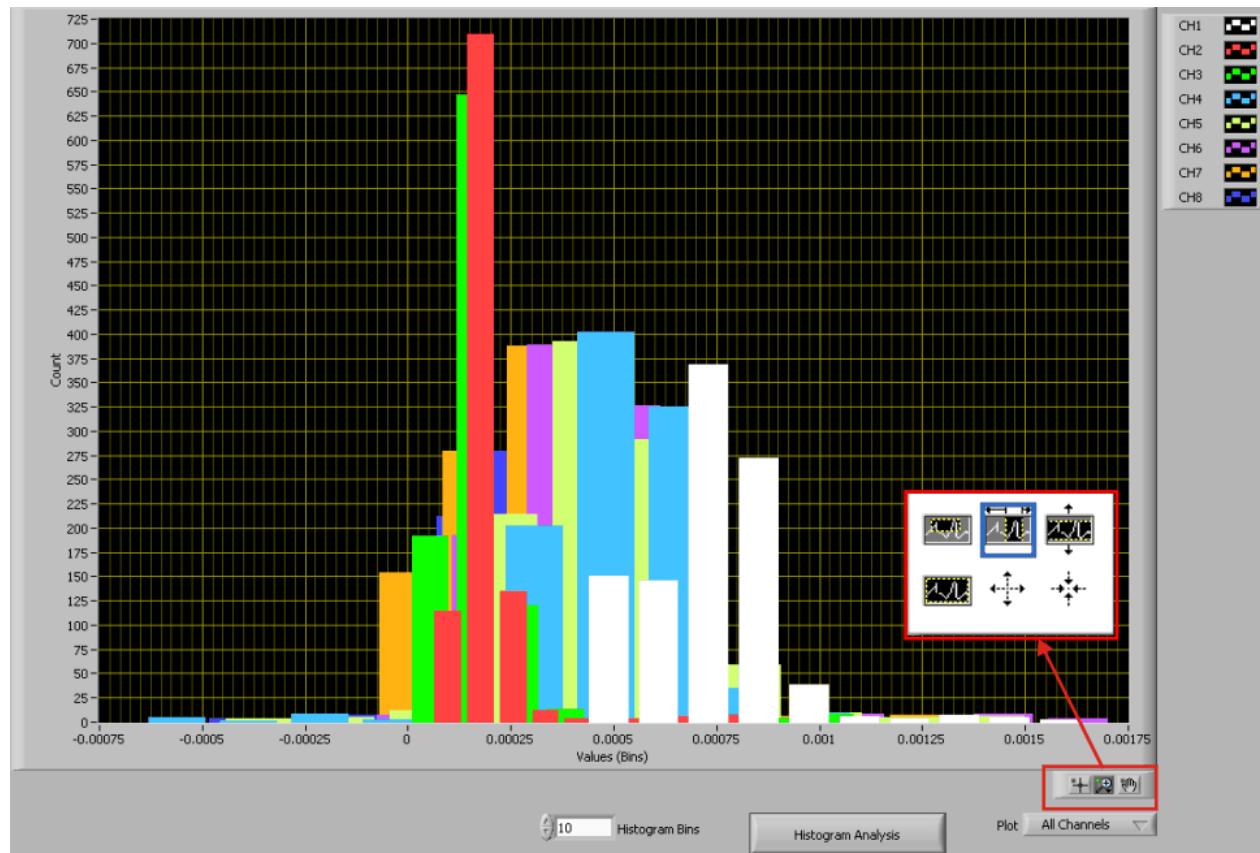
**Figure 37. ECG Signal Zoom Feature for Six Leads**

## 6.2 Histogram Tool

The Histogram tool is located under the *Analysis→Histogram* tab.

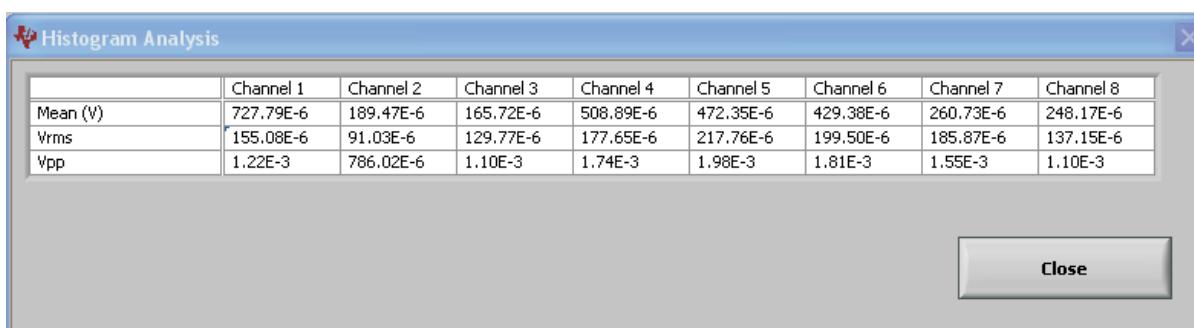
### 6.2.1 Using the Analysis→Histogram Tool

The *Analysis→Histogram* tool is used primarily to see the bin separation of the different amplitudes of the ECG waveform harmonics. **Figure 38** illustrates the histogram output for a 12-lead signal. The same ECG Signal Zoom analysis may be used on the histogram plots for a more detailed examination of the amplitude bins.



**Figure 38. Histogram Bins for 12-Lead ECG Signal**

Figure 39 describes how clicking on the **Histogram Analysis** button (at the bottom of the screen in Figure 38) yields the mean,  $V_{RMS}$ , and  $V_{PP}$  channel amplitude bins.



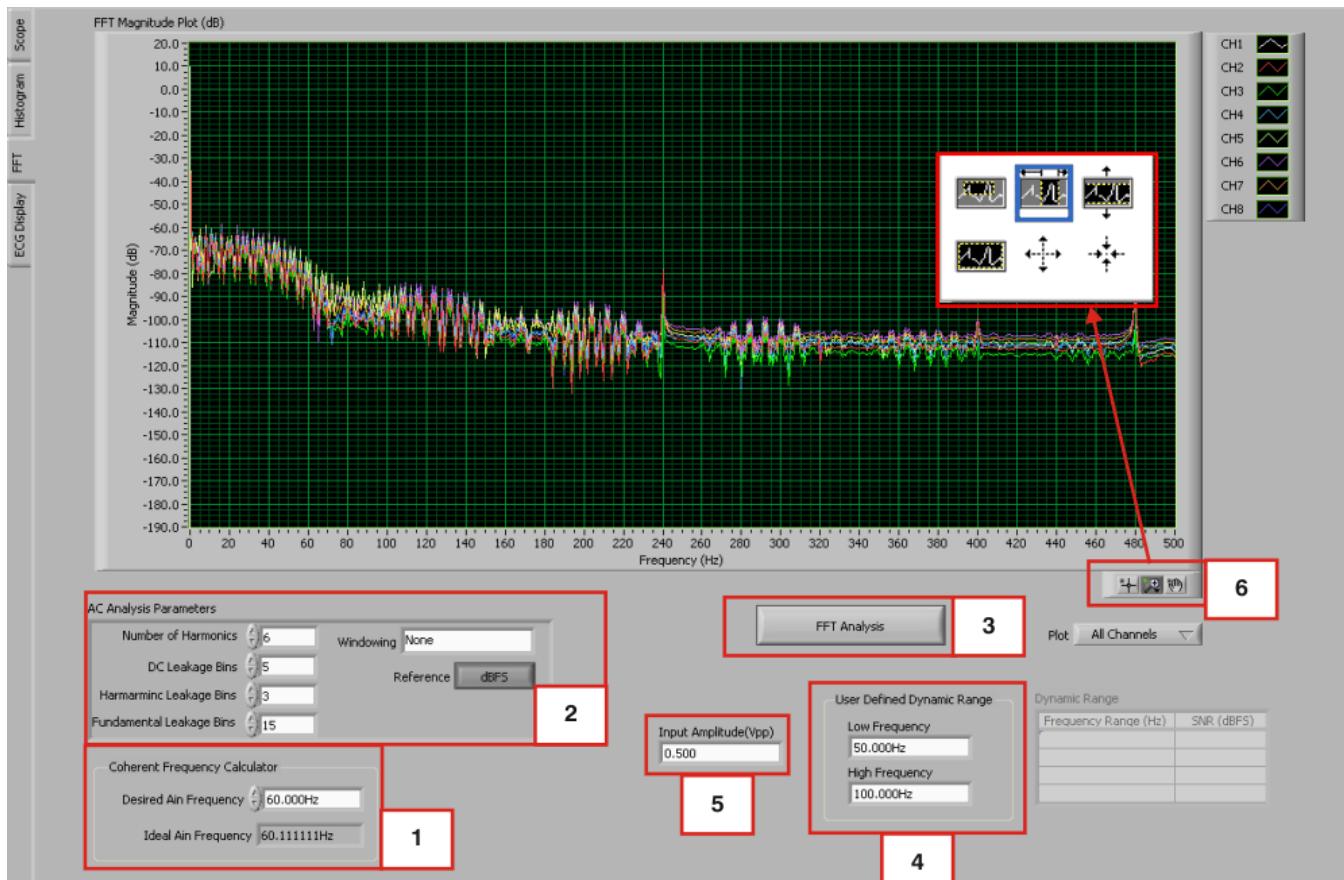
**Figure 39. Statistics for the Signal Amplitude of Eight ECG Channels**

## 6.3 FFT Tool

The FFT tool is located under the *Analysis*→*FFT* tab.

### 6.3.1 Using the Analysis→FFT Tool

The *Analysis*→*FFT* tool allows the user to examine the channel-specific spectrum as well as typical figures of merit such as SNR, THD, ENOB, and CMRR. Each feature is numbered below and described in detail in the following subsections. [Figure 40](#) illustrates an *Analysis*→*FFT* plot for a normal electrode configuration.



**Figure 40. Analysis→FFT Graph of Normal Electrode Configuration**

#### Coherent Frequency Calculator: 1

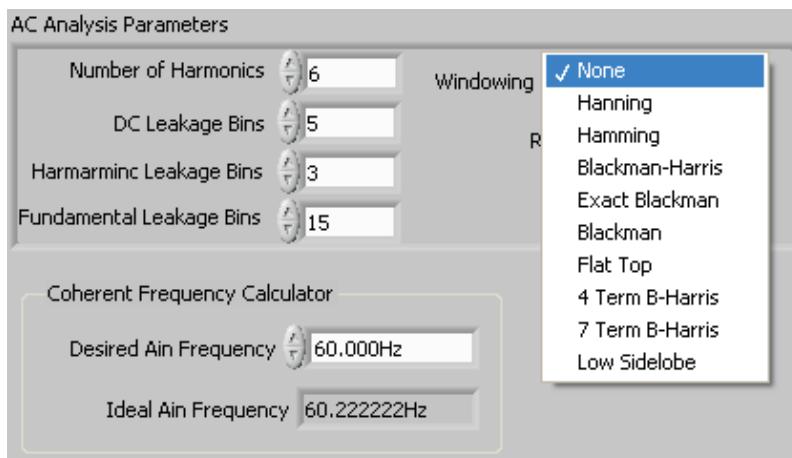
Coherent sampling in an FFT is defined as  $F_{AIN}/F_{SAMPLE} = N_{WINDOW}/N_{TOTAL}$ , where:

- $F_{AIN}$  is the input frequency
  - $F_{SAMPLE}$  is the sampling frequency of the ADS1198
  - $N_{WINDOW}$  is the number of odd integer cycles during a given sampling period
  - $N_{TOTAL}$  is the number of data points (in powers of 2) that is used to create the FFT
- If the conditions for coherent sampling can be met, the FFT results for a periodic signal will be optimized. The *Ideal A<sub>IN</sub> Frequency* is a value that is calculated based on the sampling rate, such that the coherent sampling criteria can be met.

### AC Analysis Parameters: 2

This section of the tool allows the user to dictate the number of harmonics, dc leakage bins, harmonic leakage bins, and fundamental leakage bins that are used in the creation of various histograms.

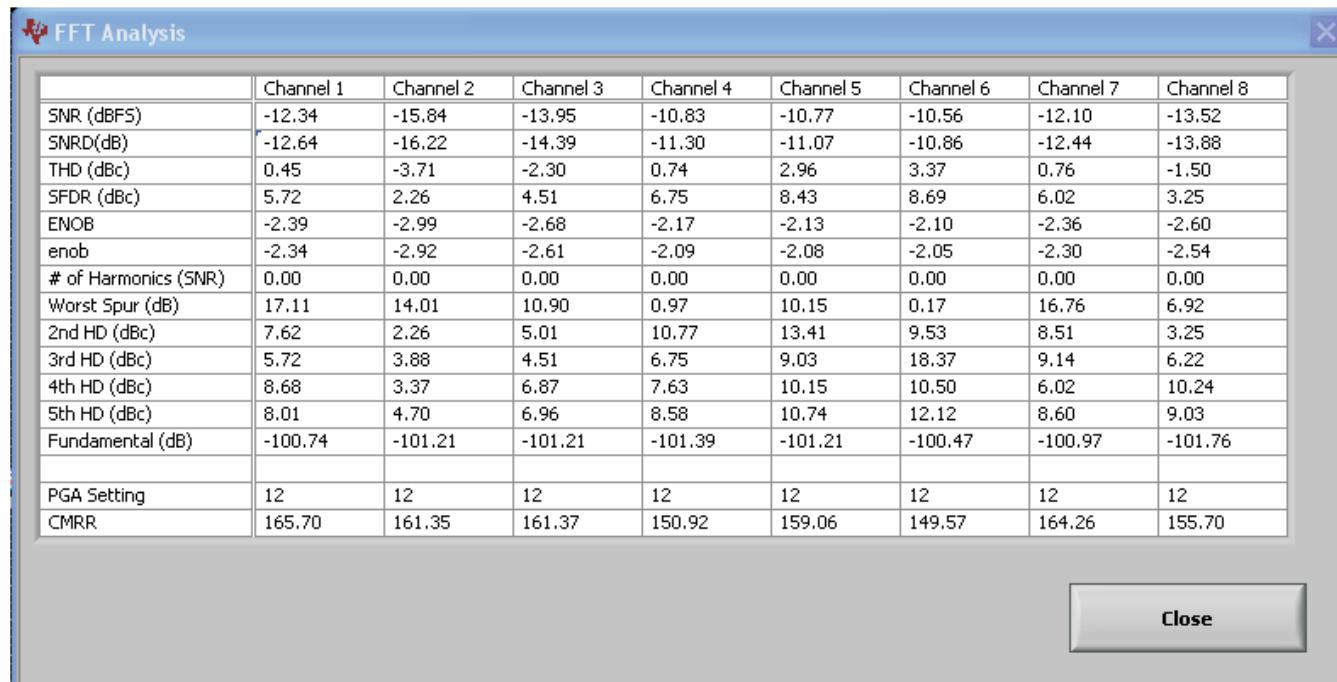
Pressing the **Windowing** button, illustrated in [Figure 41](#), allows the user to evaluate the FFT graph under a variety of different windows. Note that pressing the **Reference** button toggles between dBFS (decibels, full-scale) and dBc (decibels to carrier).



**Figure 41. Analysis→FFT→AC Analysis Parameters: Windowing Options**

### FFT Analysis: 3

Pressing the **FFT Analysis** button pulls up the window shown in [Figure 42](#). This window can be useful because the different tabulated figures of merit can show more detailed information about the channel-to-channel noise.



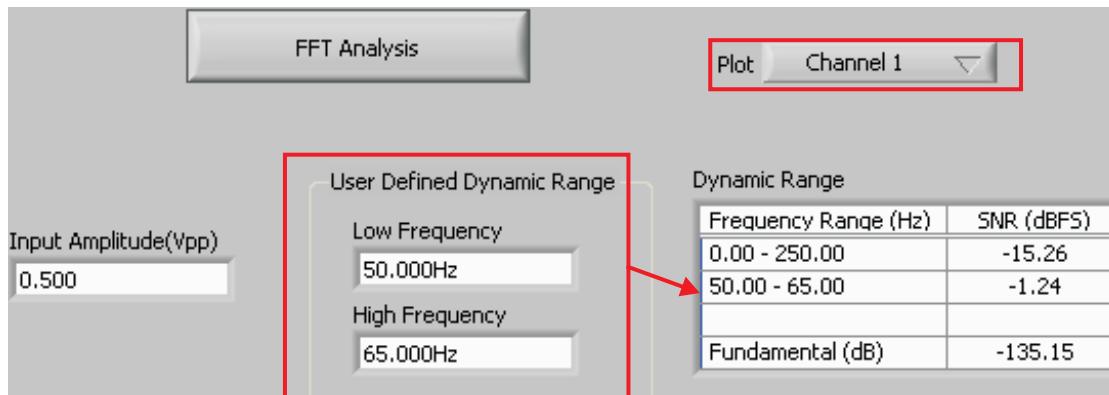
The screenshot shows the 'FFT Analysis' window with a table of data for eight channels. The columns are labeled 'Channel 1' through 'Channel 8'. The rows include various performance metrics such as SNR (dBFS), SNRD (dB), THD (dBc), SFDR (dBc), ENOB, enob, # of Harmonics (SNR), Worst Spur (dB), 2nd HD (dBc), 3rd HD (dBc), 4th HD (dBc), 5th HD (dBc), Fundamental (dB), PGA Setting, and CMRR. A 'Close' button is located in the bottom right corner of the window.

	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
SNR (dBFS)	-12.34	-15.84	-13.95	-10.83	-10.77	-10.56	-12.10	-13.52
SNRD(dB)	-12.64	-16.22	-14.39	-11.30	-11.07	-10.86	-12.44	-13.88
THD (dBc)	0.45	-3.71	-2.30	0.74	2.96	3.37	0.76	-1.50
SFDR (dBc)	5.72	2.26	4.51	6.75	8.43	8.69	6.02	3.25
ENOB	-2.39	-2.99	-2.68	-2.17	-2.13	-2.10	-2.36	-2.60
enob	-2.34	-2.92	-2.61	-2.09	-2.08	-2.05	-2.30	-2.54
# of Harmonics (SNR)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Worst Spur (dB)	17.11	14.01	10.90	0.97	10.15	0.17	16.76	6.92
2nd HD (dBc)	7.62	2.26	5.01	10.77	13.41	9.53	8.51	3.25
3rd HD (dBc)	5.72	3.88	4.51	6.75	9.03	18.37	9.14	6.22
4th HD (dBc)	8.68	3.37	6.87	7.63	10.15	10.50	6.02	10.24
5th HD (dBc)	8.01	4.70	6.96	8.58	10.74	12.12	8.60	9.03
Fundamental (dB)	-100.74	-101.21	-101.21	-101.39	-101.21	-100.47	-100.97	-101.76
PGA Setting	12	12	12	12	12	12	12	12
CMRR	165.70	161.35	161.37	150.92	159.06	149.57	164.26	155.70

**Figure 42. Analysis→FFT→FFT Analysis: Input Short Condition**

#### User-Defined Dynamic Range: 4

This section enables the user to examine the SNR of a specific channel within a given frequency band defined by *Low Frequency* and *High Frequency*. The SNR displayed in this window will also show under the *Dynamic Range* heading as [Figure 43](#) illustrates.



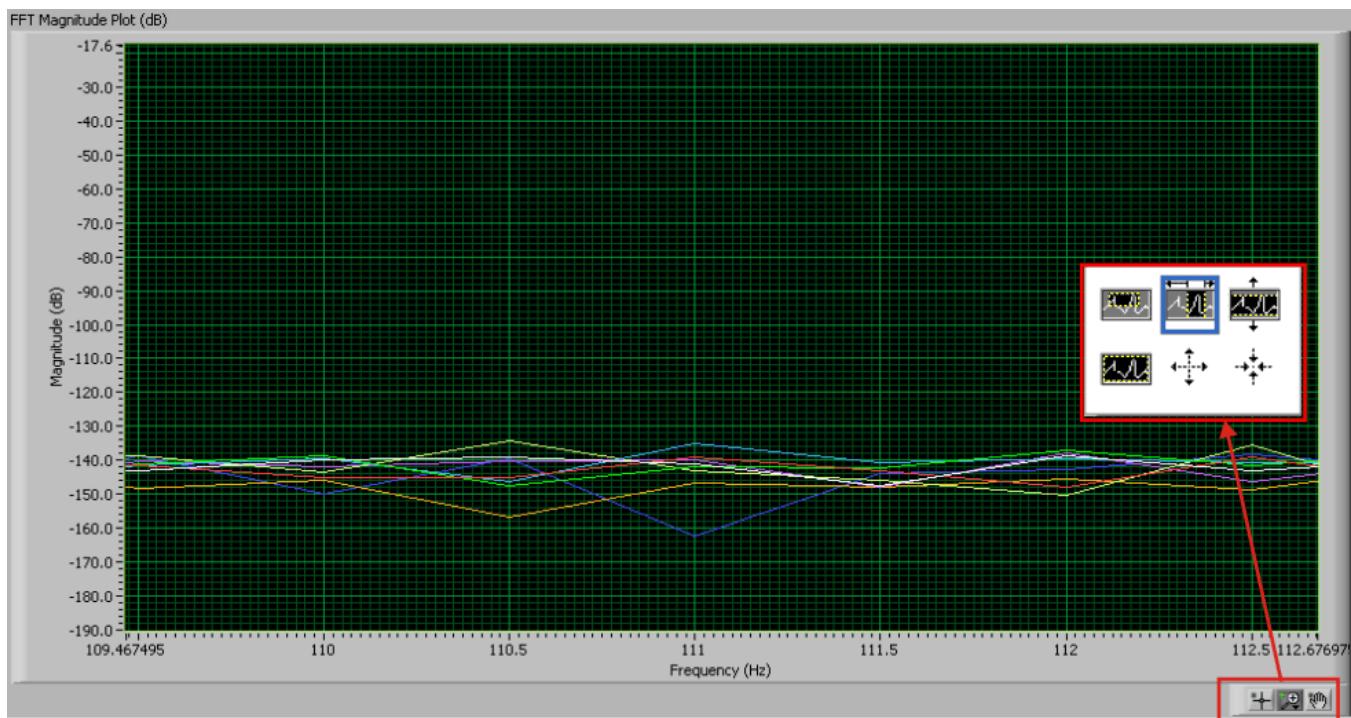
**Figure 43. Changing the User-Defined Dynamic Range for Channel 1**

#### Input Amplitude: 5

This field is a user input that is important for accurately calculating the CMRR of each channel.

#### Waveform Zoom Tool: 6

As with the Analysis, Histogram, and Scope tool, this zoom function allows a closer examination of the FFT at frequencies of interest, as shown in [Figure 44](#).

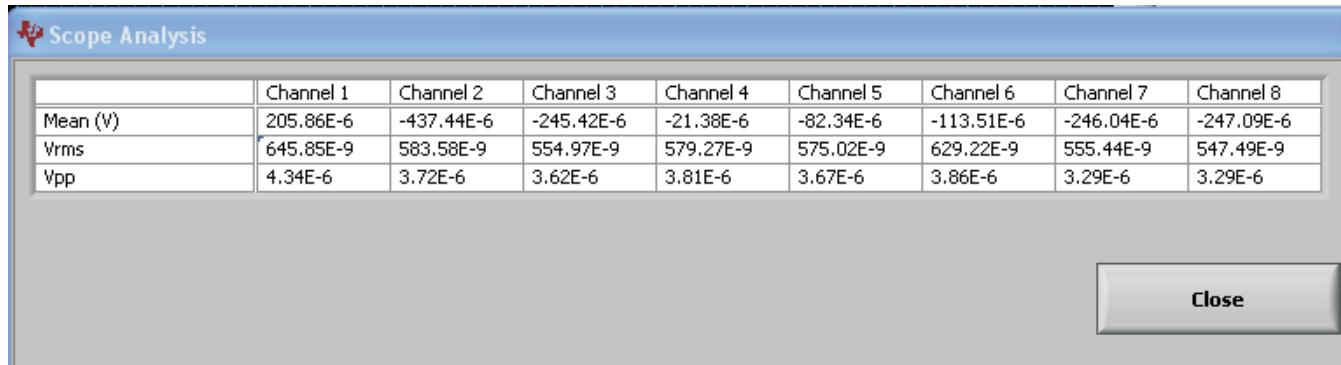


**Figure 44. FFT Plot Using Zoom Tool**

## 7 Evaluation of Specific ECG Functions

**NOTE:** Before evaluating specific ECG functions, it is recommended that the user acquire data with inputs shorted internally. This configuration ensures that the board is operating properly.

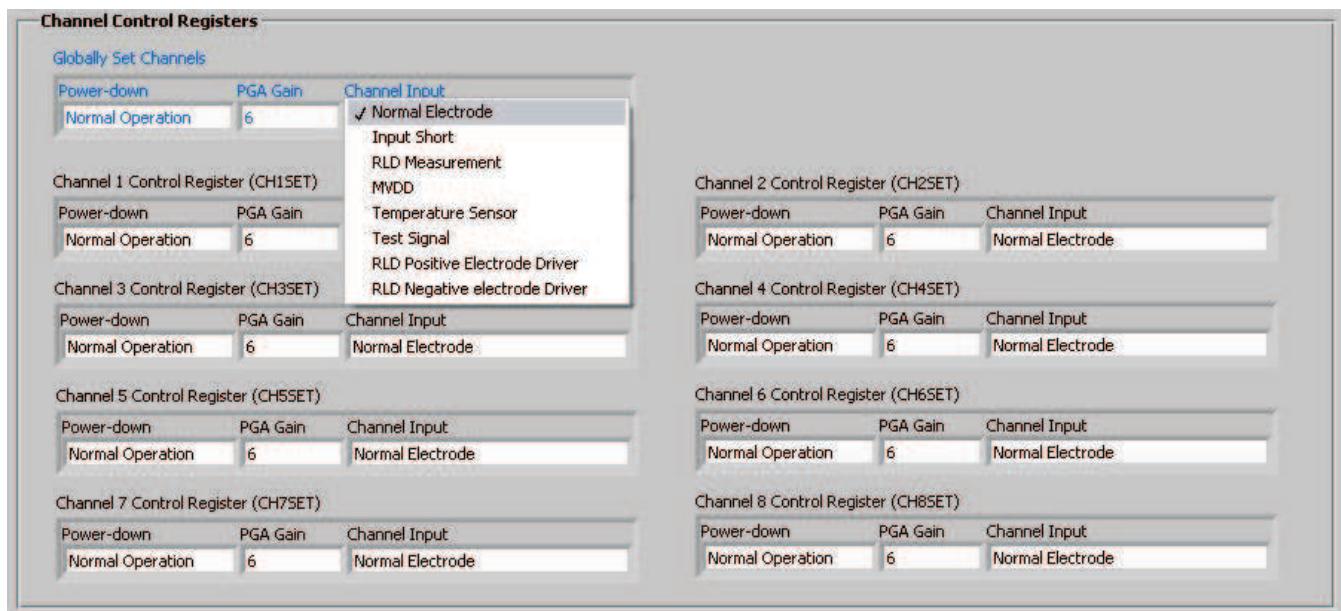
By default, when the board is powered up, it sets the individual channels to an internal short with a data rate of 500SPS and a PGA gain of 6. Once the **Acquire** button is pressed, the Scope tab under the Tests tab should reflect input-referred  $V_{PP}$  values less than  $5\mu V_{PP}$ , as [Figure 45](#) illustrates.



**Figure 45. Input Short Data for Two Seconds Sampled at 500SPS**

### 7.1 Capturing 12-Lead ECG Signals

To capture signals from external inputs, configure the inputs of each channel to *Normal Electrode* as shown in [Figure 46](#).



**Figure 46. MUX Configured with All Inputs Set to Normal Electrode**

The 10 ECG electrodes from the Fluke simulator are provided through the DB15 connector (J1). Refer to [Section 8.3](#) for the ECG cable details. The ECG electrode signals are passed through a single pole RC filter followed by the lead configuration. For ECG signal processing, the electrode signals are routed through JP26 to JP33 to the ADS1198 input. The signal path in the board can be chosen by jumper settings, depending on the application.

## 7.2 Lead Derivation

The EVM is configured to generate 12 leads of ECG signals from the 10 electrodes using the eight channels of the ADS1198. Two of the limb leads and the six chest leads are computed purely in the analog domain (Leads I, II, V1, V2, V3, V4, V5 and V6). The augmented leads and Lead III are computed digitally. The channel assignments are described in [Table 27](#).

**Table 27. Lead Generations**

ADS1198 Input Channels	Derived Lead <sup>(1)</sup>
1	V6 = V6 – WCT
2	LI = LA – RA
3	LII = LL – RA
4	V2 = V2 – WCT
5	V3 = V3 – WCT
6	V4 = V4 – WCT
7	V5 = V5 – WCT
8	V1 = V1 – WCT

<sup>(1)</sup> WCT = (LA + RA + LL)/3

## 7.3 Wilson Center Terminal (WCT)

The Wilson Center Terminal voltage is internally generated by the ADS1198 device. The device gives register bit controls so that any of the eight inputs (CH1P to CH4P, CH1M to CH4M) can be routed to the three integrated amplifiers to generate the WCT signal.

The ADS1198ECG-FE is configured for 12-lead ECG inputs, with the limb electrodes connected as shown in [Table 27](#). During EVM power-up, the firmware sets up the register bits such that the CH2P, CH2M, and CH3P (RA, RL, LL) bits are routed to the internal buffers. This arrangement creates the  $(RA + RL + LL)/3$  signal at the WCT pin. This signal is routed back to the negative inputs of channel 1 and channels 4 to 8 by shorting JP16 with a shunt jumper.

## 7.4 Measured 12 -Lead ECG Outputs

---

**NOTE:** The current firmware does not support digital dc removal (high-pass filtering). Data can be saved and post-processed with a digital high-pass filter and a 60Hz notch filter for analysis.

---

Data presented in this section are captured for two amplitudes. The 5mV ECG signal is a widely-used test condition that is reliable enough for doing basic QRS detection. Data with a 50 $\mu$ V ECG signal (the lowest that the Fluke simulator can generate) shows the full capability of the ADS1198 integrated front-end. Graphs in this section show the measured ECG signal under the following conditions:

1. DC-coupled input with RLD (5mV ECG signal)
2. DC-coupled input with RLD and bipolar supply (1mV ECG signal)
3. DC-coupled input with RLD (50 $\mu$ V ECG signal, zoomed in on one channel)

### DC-Coupled with Right Leg Drive: 5mV ECG Signal

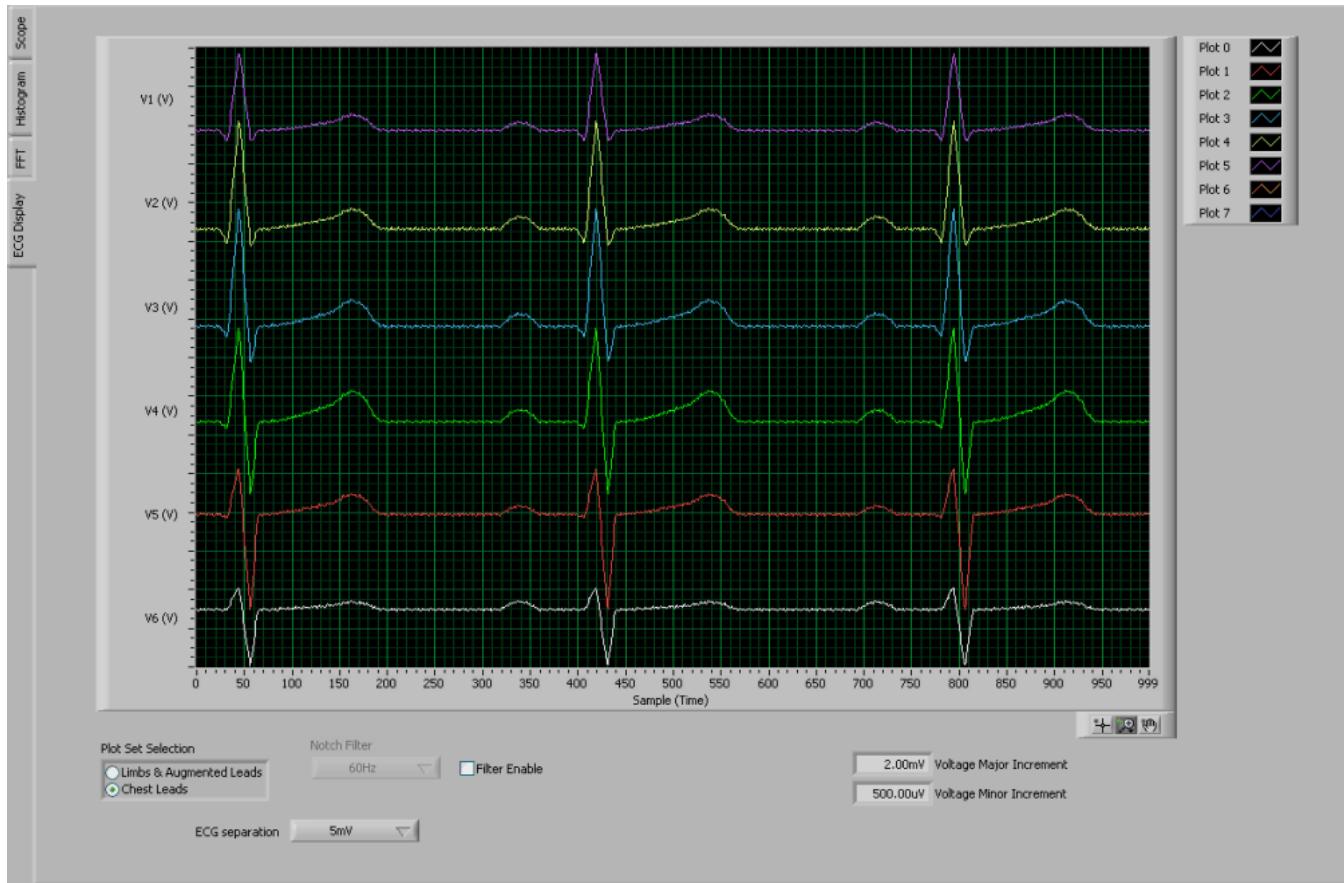
Figure 47 shows the acquisition of a 5mV ECG signal with a dc-coupled input.



**Figure 47. Acquisition of 5mV ECG Signal with DC-Coupled Inputs**

### DC-Coupled with Right Leg Drive: 1mV ECG Signal

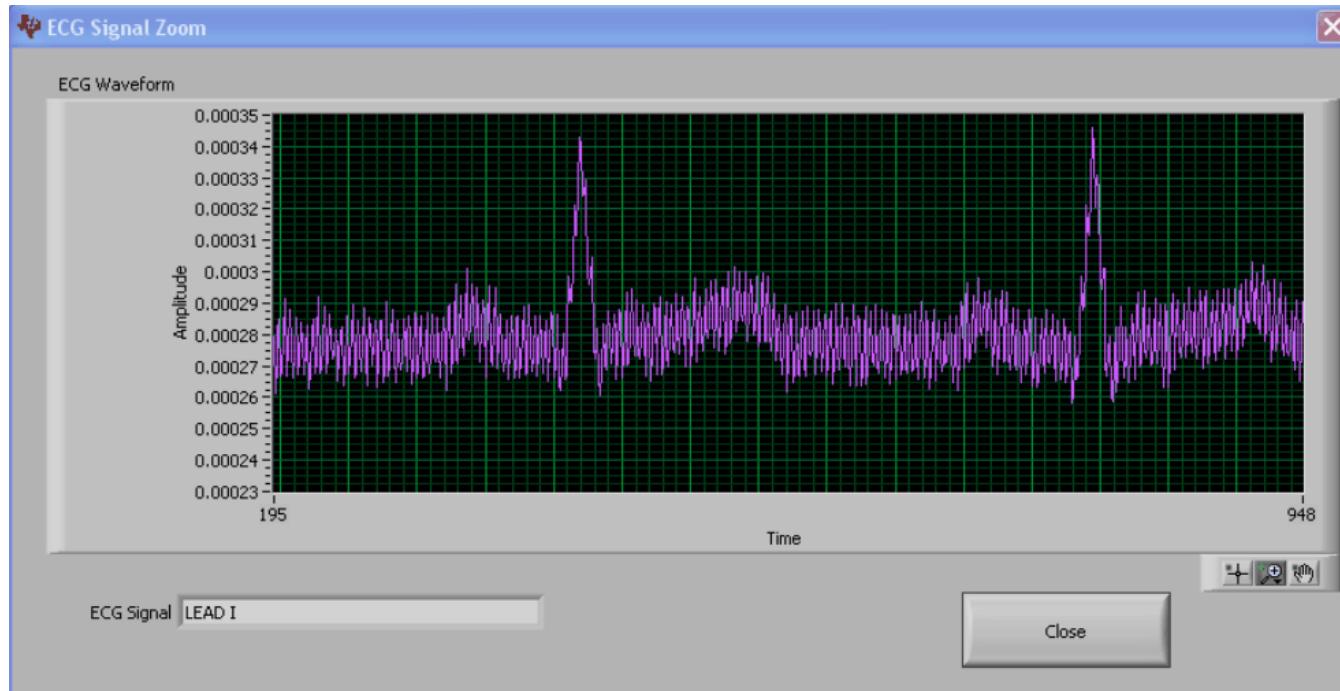
Figure 48 illustrates the acquisition of a 1mV ECG signal with dc-coupled inputs.



**Figure 48. Acquisition of 1mV ECG Signal with DC-Coupled Inputs**

### DC-Coupled with Right Leg Drive: 50 $\mu$ V ECG Signal

Acquisition of a 50 $\mu$ V ECG signal with a dc-coupled inputs is shown in [Figure 49](#).



**Figure 49. Acquisition of 50 $\mu$ V ECG Signal with DC-Coupled Inputs**

[Figure 49](#) shows the output measured a 50 $\mu$ V ECG input signal measured in a Lead I configuration. This signal is the minimum ECG signal amplitude that the Fluke Medsim simulator can generate. It can be seen that the ADS1198 integrated front end can resolve ECG signals down to 50 $\mu$ V. With the default right-leg drive (RLD) loop in the EVM, the power line (50Hz/60Hz) interference is limited to approximately 20 $\mu$ V<sub>PP</sub>. This interference can be removed by using a 50Hz/60Hz digital notch filter. Alternatively, the RLD loop can be further optimized to reduce the interference as well.

## 7.5 Right Leg Drive

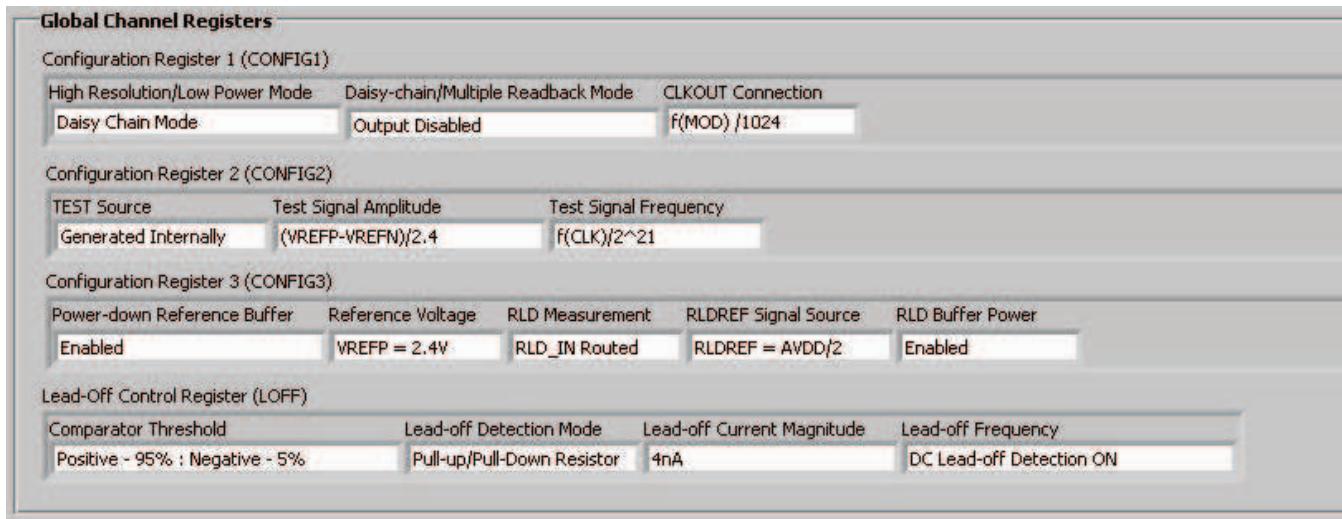
The RL electrode is driven directly by the RLD signal generated on-chip by the ADS1198. The bandwidth of the RLD loop is determined by R8 (390k $\Omega$ ) and C20 (10nF). Users can change these values to set the bandwidth based on the specific application. The stability of the loop is determined by the user's specific system. Therefore, tweaking may be needed on the feedback component values to ensure stability if additional filtering components and long cables are added before the ADS1198ECG-FE.

Typically, the RLD is implemented by choosing the average of RA, LA, and LL. The ADS1198, however, offers full flexibility by letting the user select any combination of the electrodes to generate the RLD. Refer to the [ADS1198 data sheet](#) for more details.

The reference voltage for the on-chip right leg drive can be driven externally. The on-chip voltage is set to mid-supply. If the application requires the common mode to be set to any other voltage, this configuration can be accomplished by setting the appropriate bit in the [Configuration 3 Register](#). The external RLDREF voltage is set by resistor R1 and adjustable resistor R2.

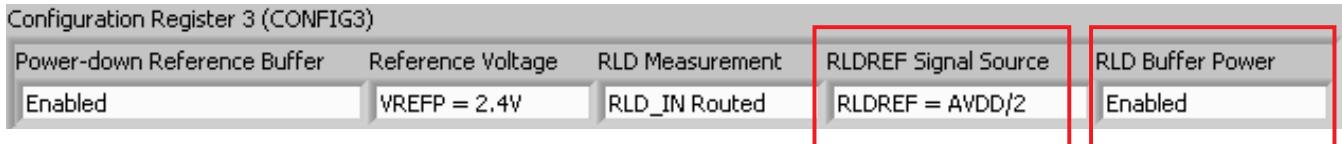
By default at power-up, the firmware sets all the registers needed for proper RLD operation. In the event of a reset signal, the register values return to the device defaults. In such a scenario, the following procedure can be applied to reactivate the RLD circuitry.

Step 1. Verify that the input multiplexer is set to the Normal Electrode mode, as [Figure 50](#) shows.



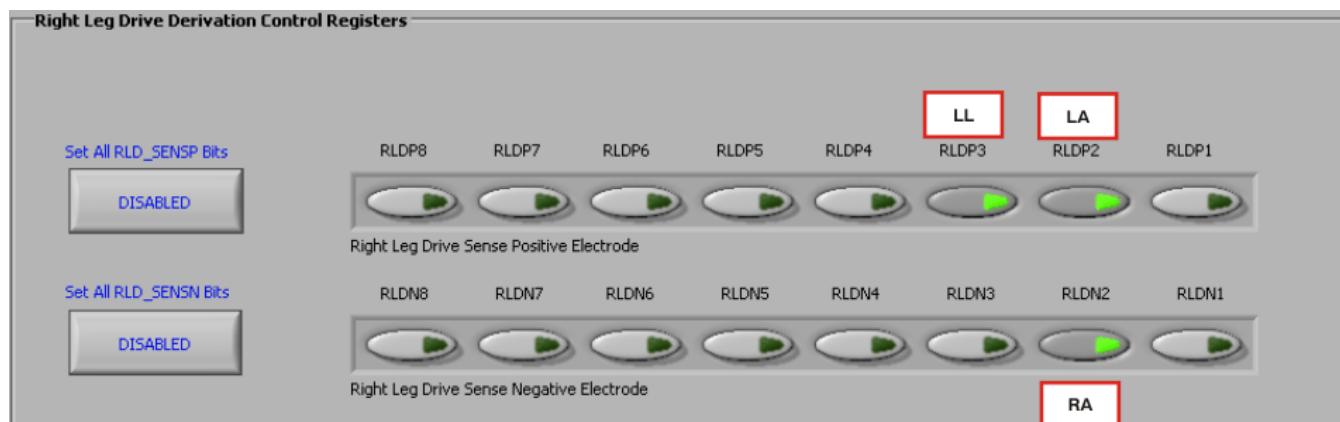
**Figure 50. Settings for Normal Electrode**

Step 2. Turn on the RLD buffer and set the internal RLD reference; refer to [Figure 51](#).



**Figure 51. Configuring RLDREF and RLD Buffer**

Step 3. Select the electrodes to be chosen for the RLD loop. In this case, the RA, LA, and LL signals are used (as Figure 52 shows).



**Figure 52. Setting Up the RLD Loop**

Once these steps are completed, measure and verify that the voltage on either side of R37 is close to mid-supply. This measurement confirms whether the RLD loop is functional.

Apart from the RLD signal, the ADS1198ECG-FE also offers three options to drive the cable shield. The ECG cable shield signal can be connected to either the in-phase or out-of-phase RLD signal, or the board AGND using jumpers JP10 and JP17. Table 28 summarizes these options.

**Table 28. RLD Jumper Options**

ECG Cable ELEC_SHD signal	JP10	JP17
AGND	1-2	Don't Care
RLD (0: In phase)	2-3	2-3
RLD (180: Out of phase)	2-3	1-2

The on-chip RLD signal can be fed back into the ADS1198 by shorting JP1. This RLD signal can then be sent to the ADC (to measure for debug purposes) or to other electrodes for driving (to change the reference drive in case the RL electrode falls off). Refer to the [ADS1198 product data sheet](#) for additional details.

## 7.6 Lead-Off Detection

The ADS1198 provides multiple schemes to implement the lead-off detection function. These techniques include current source dc, current source ac, pull-up resistor dc, and pull-up resistor ac lead-off detection options. Refer to the [ADS1198 product data sheet](#) for additional details.

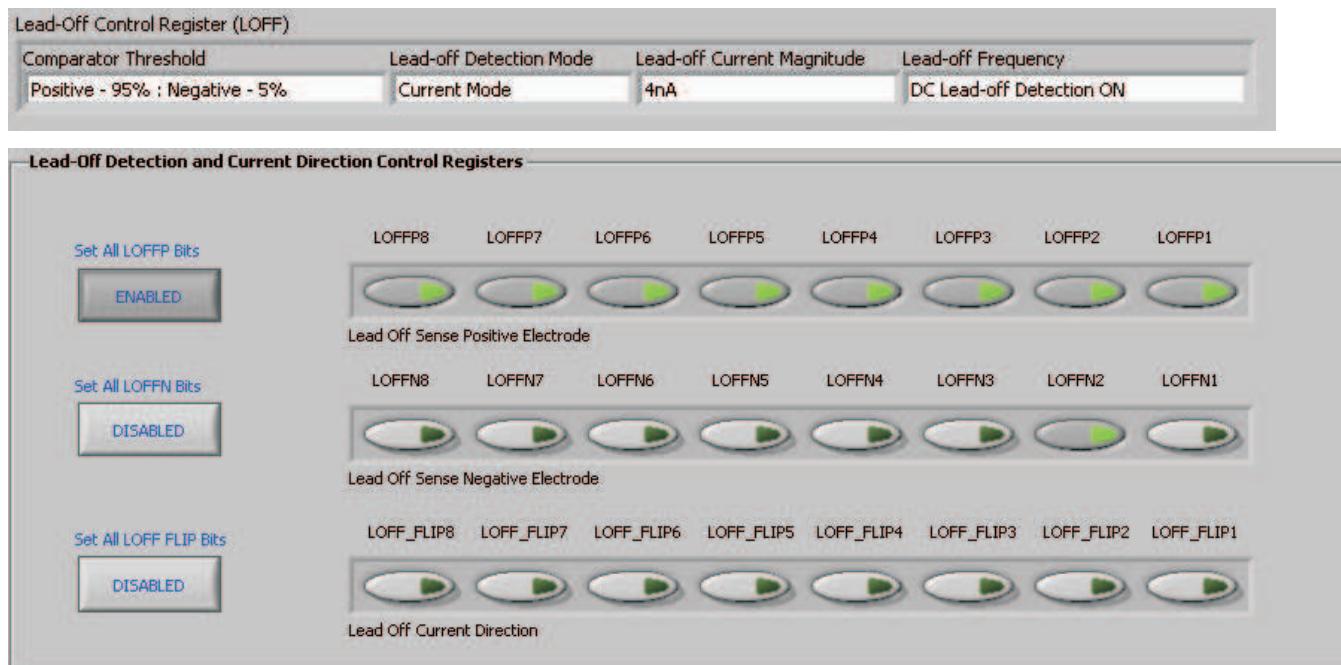
While attempting to use the lead-off detection, care must be taken to analyze the input signal. If the input signal is dc-coupled, the dc lead-off scheme can be used. If the input signal is ac-coupled, the ac lead-off scheme must be used. When using the dc lead-off scheme, be sure to turn on the RLD loop to set the input common-mode before activating lead-off detection.

The EVM gives flexibility to exercise any of the above schemes. The two schemes discussed in the following sections show a typical sequence to activate the current source dc lead-off circuitry and V/R mode ac lead-off circuitry.

### 7.6.1 DC Lead-Off

At board power-up, the firmware sets the appropriate registers so that dc lead-off is selected. In the event of a reset signal, the register values default to the device default settings. In such a scenario, follow this procedure to reactivate the lead-off circuitry.

- Step 1. Make sure the input is dc-coupled and that the RLD circuit is operational, as explained in [Section 7.5](#).
- Step 2. Choose the lead-off scheme by setting the respective bits in the LOFF register (in the [LOFF control tab](#)). Select the *DC Lead-Off Detect, 6.25nA, Current Source* scheme, and set the comparator threshold to 95%. Select the appropriate inputs for lead-off detection by clicking the bits of the LOFF\_SENSP and LOFF\_SENSM Registers. The LOFF tab should appear as shown in [Figure 53](#).



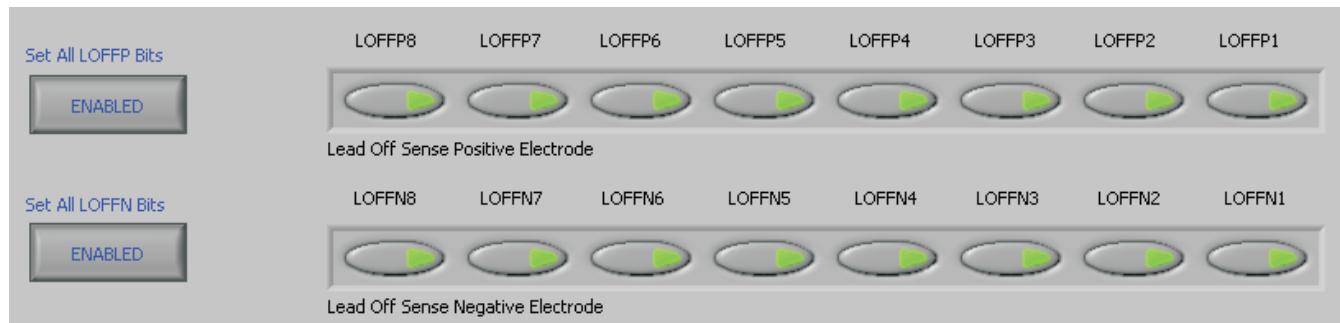
**Figure 53. Setting the LOFF Register Bits**

- Step 3. Turn on the lead-off comparator by setting the bit in the Configuration 4 Register in the Global Registers control tab, as [Figure 54](#) shows.



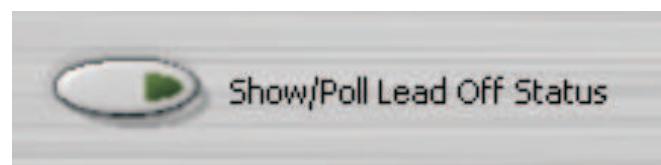
**Figure 54. Configuring the Lead-Off Comparator**

- Step 4. The software has an option where the LOFF\_STATP and LOFF\_STATM Registers are continuously polled (set the *Read Status Registers* switch as shown in [Figure 55](#)). This option allows the user to see the lead-off detection scheme work in real time.



**Figure 55. Setting the Lead-Off Bits to Work in Real Time**

When the simulator is disconnected from the DB15 connector, the LOFF\_STAT registers automatically update. They may be viewed in real time by clicking on the **Show/Poll Lead Off Status** button, as shown in [Figure 56](#). The LOFF\_STATM (bit7 to bit2) are driven by the WCT amplifiers and thus do not show a LEAD OFF status.



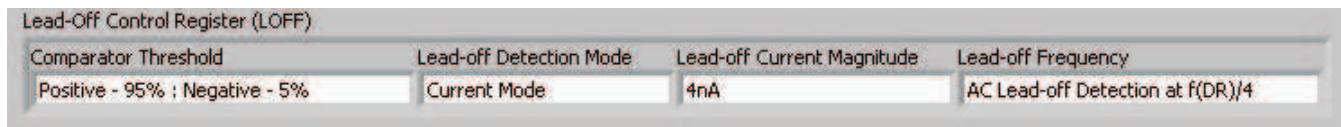
Positive Electrode	Negative Electrode
LEAD OFF	IN8x LEAD ON
LEAD OFF	IN7x LEAD ON
LEAD OFF	IN6x LEAD ON
LEAD OFF	IN5x LEAD ON
LEAD OFF	IN4x LEAD ON
LEAD OFF	IN3x LEAD OFF
LEAD OFF	IN2x LEAD OFF
LEAD OFF	IN1x LEAD ON

**Figure 56. Lead-Off Status Registers**

## 7.6.2 AC Lead-Off Detection

Follow these steps to configure ac lead-off detection.

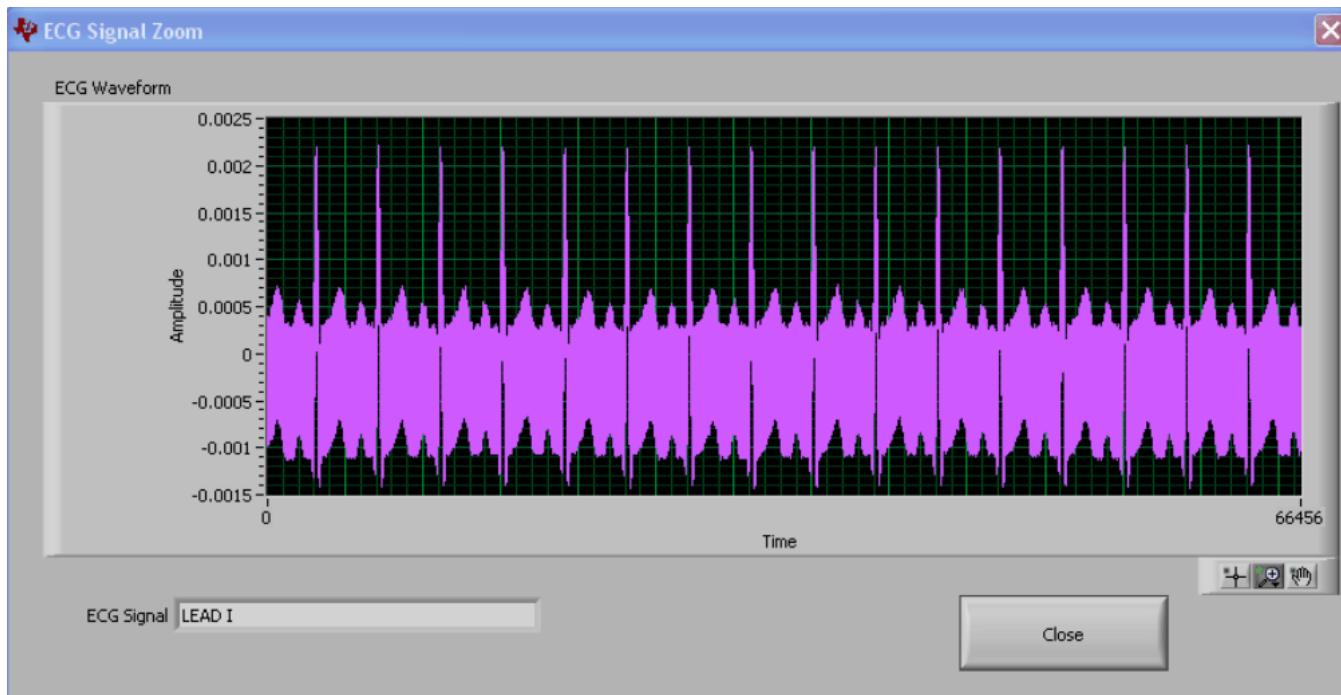
- Step 1. If dc-coupled input is used, turn on the RLD loop as explained in [Section 7.5](#).
- Step 2. Choose the lead-off scheme by setting the bits in the LOFF register (in the [LOFF control tab](#)). Select the *AC Lead-Off Detect at  $f_s/4$ , V/R mode* scheme. The state of the other bits in the register does not matter. Select all the channels for lead-off detection by clicking the respective bits of the LOFF\_SENSP and LOFF\_SENSM Registers. The LOFF tab should now appear as shown in [Figure 57](#).



**Figure 57. Setting the Lead-Off Register for AC Lead-Off Detection**

- Step 3. Once the frequency of the ac lead-off is determined, the data rate must be chosen to be four times the lead-off frequency. As an example, a data rate of 8kHz is chosen by setting the DR bit in the Configuration 1 Register in the Global Registers control tab.

Once these steps are completed, data can be captured with the patient simulator connected. A typical time domain waveform (65,536 points) is shown in [Figure 58](#).



**Figure 58. AC Lead-Off Time Domain Waveform for Lead I (DR = 8kSPS)**

- Step 4. Post-processing must be done to extract the lead-off signal and the ECG signal from the waveform. In future versions of the ADS1198ECG-FE firmware, it is planned to incorporate post-processing filters. In the meantime, the raw channel data can be saved to a file by enabling the *Save Sorted Raw Channel (V)* option in the Print Options tab and pressing the *Print to File* button. Post-processing can be done using tools such as MATLAB®.

**NOTE:** The ADS1198ECG-FE does **not** include software to extract the ECG signal from the lead-off signal.

## 7.7 Pace Detection

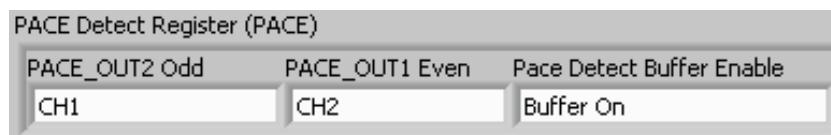
The ADS1198 supports data rates up to 32kSPS to allow for software pace detection, which typically requires a data rate of at least 8kSPS.

---

**NOTE:** The ADS1198ECG-FE does **not** include software PACE detection algorithms.

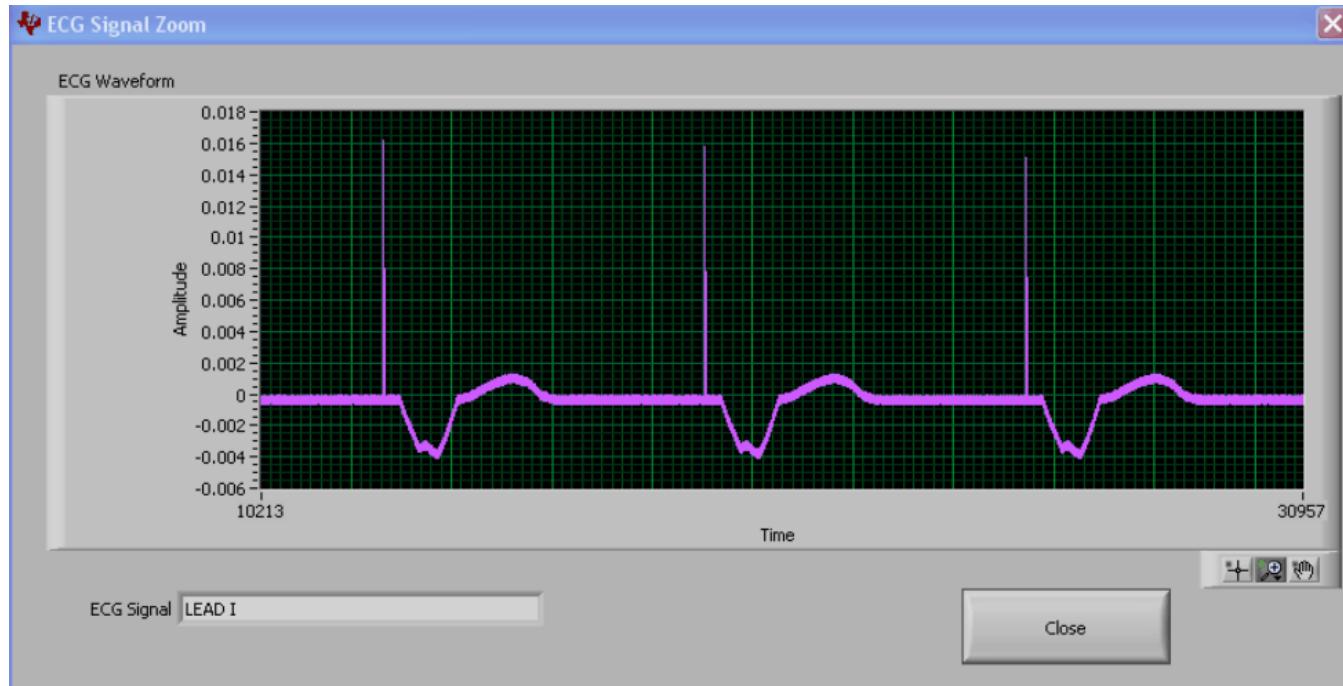
---

The ADS1198 provides the user the flexibility of doing hardware pace detection with external circuitry. Pace detection can be done simultaneously on two channels: one from the odd channels and one from the even channels. Refer to the [ADS1198 product data sheet](#) for additional details. To turn on the Pace buffer and select the channels, set the PACE Register from the PACE tab as shown in [Figure 59](#). The PGA outputs of the selected channels are available at connectors J5, pins 1 and 2.



**Figure 59. Setting the Pace Register**

[Figure 60](#) shows an example waveform created by a Fluke Medsim 300B processed by the ADS1198 at a data rate of 8kSPS. Using higher data rates increases power consumption because all channels must sample at this data rate simultaneously; thus, the PACE buffers offer the flexibility to process PACE signals separately from the ADS1198.



**Figure 60. Example Processing of PACE Detect with ECG Waveform**

## 8 BOM, Layout, and Schematics

This section contains the complete bill of materials, printed circuit board (PCB) layouts, and schematic diagrams for the ADS1198ECG-FE.

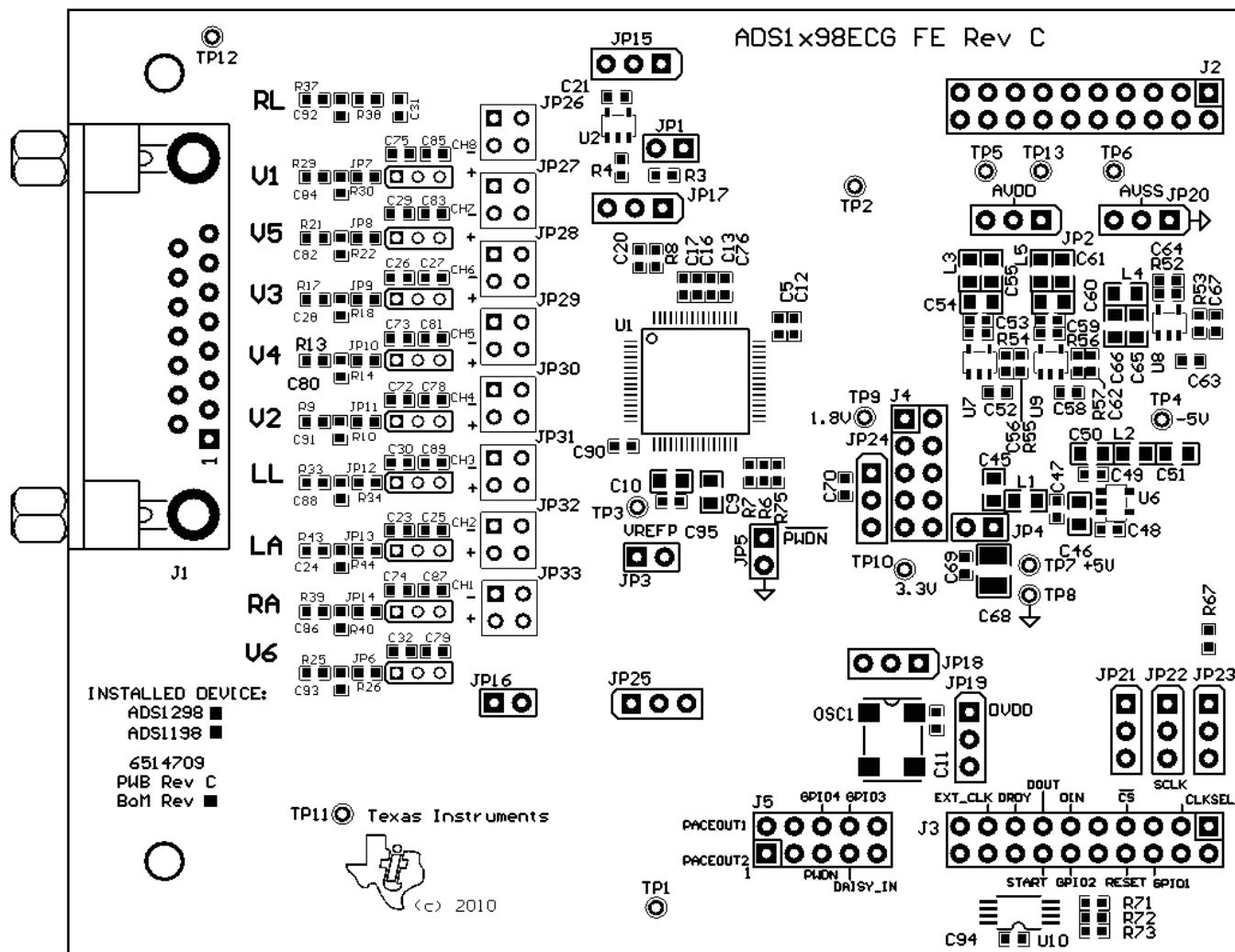
**NOTE:** Board layouts are not to scale. These are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS1198ECG-FE PCBs.

### 8.1 ADS1198ECG-FE Front-End Board Schematics

The ADS1198ECG-FE schematic is appended to this document.

### 8.2 Printed Circuit Board Layout

Figure 61 through Figure 66 show the ADS1198ECG-FE PCB layouts.



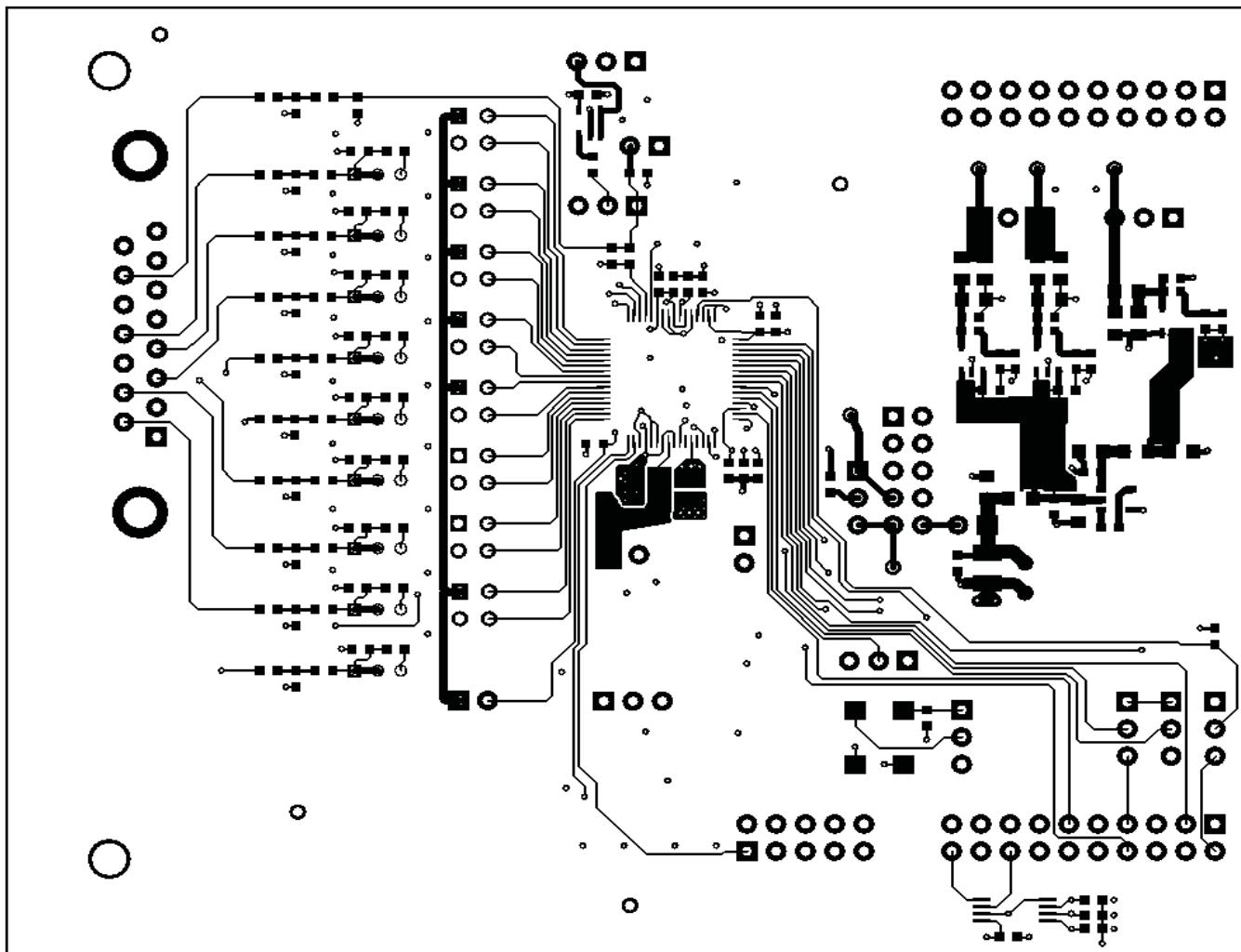


Figure 62. Top Layer

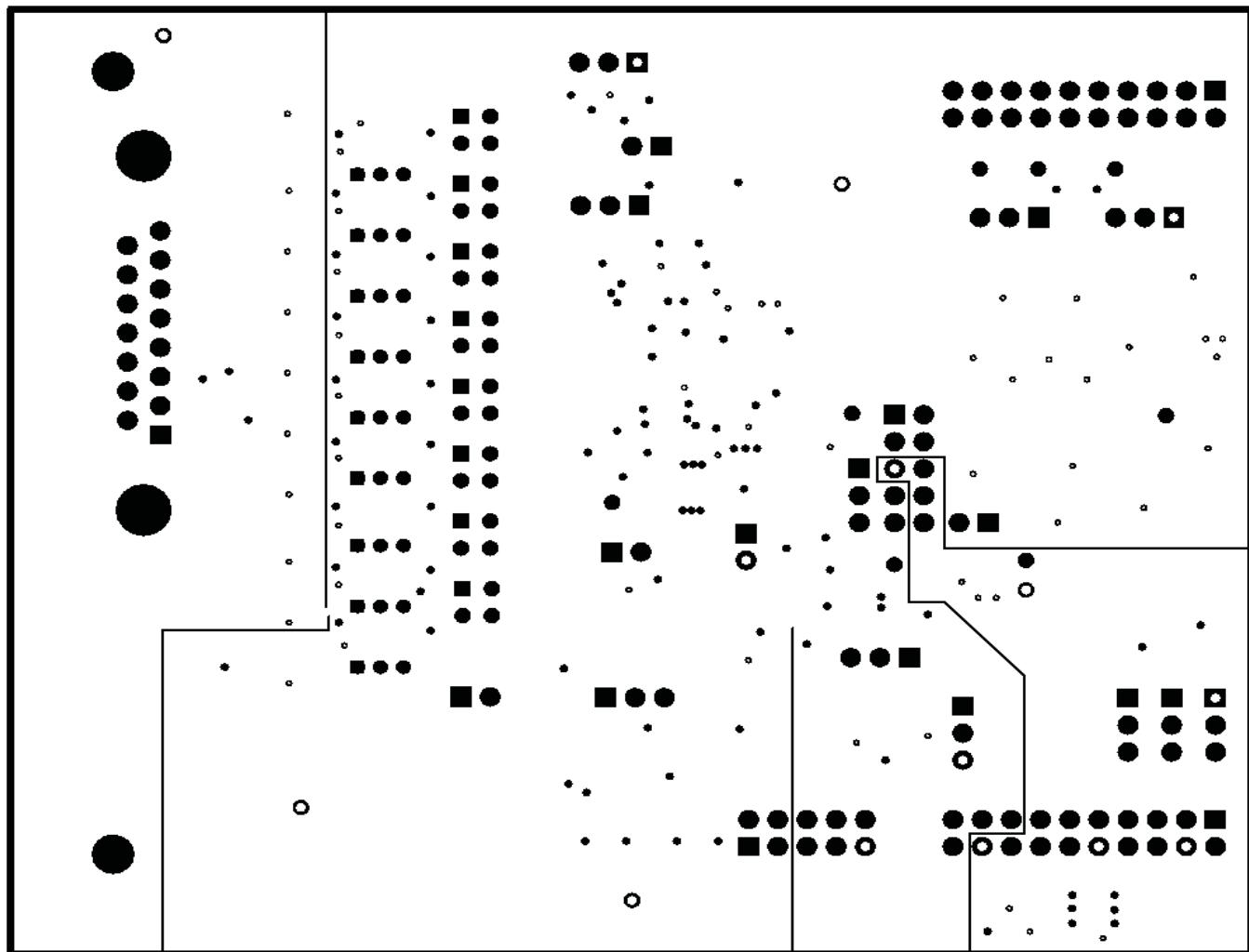


Figure 63. Internal Ground Plane (Layer 2)

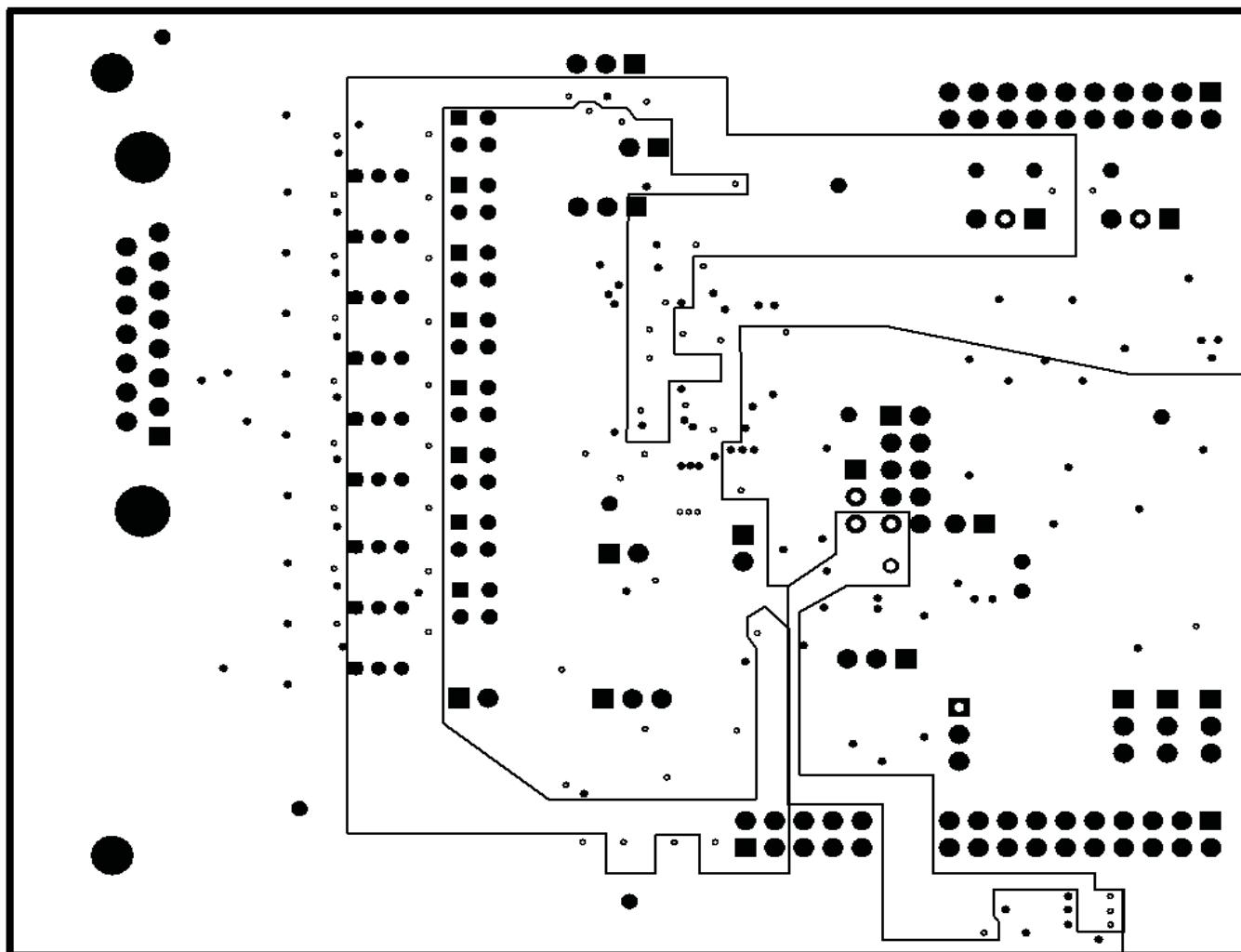


Figure 64. Internal Power Plane (Layer 3)

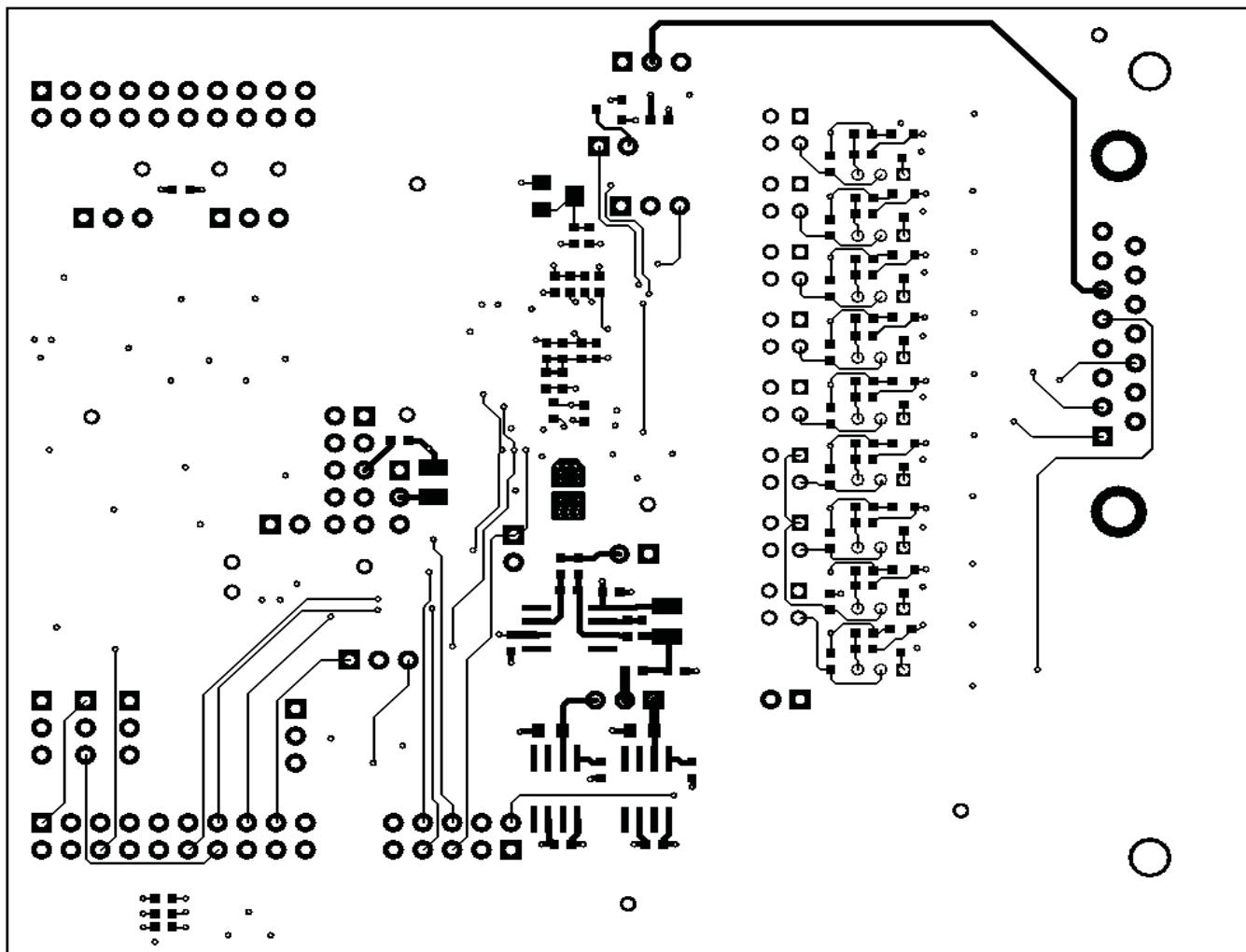


Figure 65. Bottom Layer

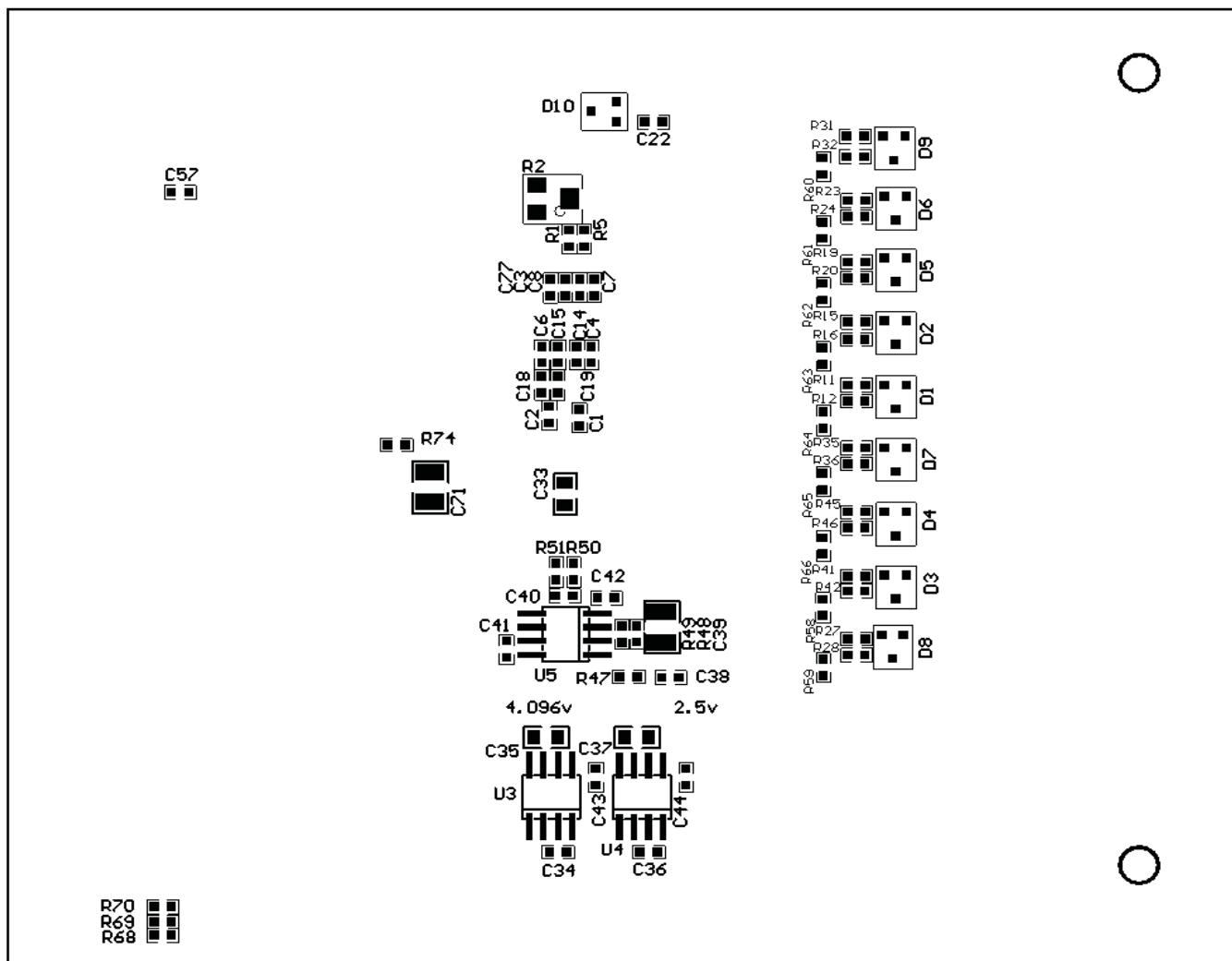


Figure 66. Bottom Component Placement

### 8.3 ECG Cable Details

Figure 67 shows the details of the recommended ECG cable.

#### Cable details:

- 10-lead ECG cable for Philips/HP-snap, button (Part No: 010302013);  
<http://www.biometriccables.com/index.php?productID=692>
- 10-lead ECG cable for Philips/HP-Clip-on type (Part No: 010303013A);  
<http://www.biometriccables.com/index.php?productID=693>

Another compatible cable for the ADS1198ECG-FE: HP/Philips/Agilent-compatible 10-lead ECG cable.

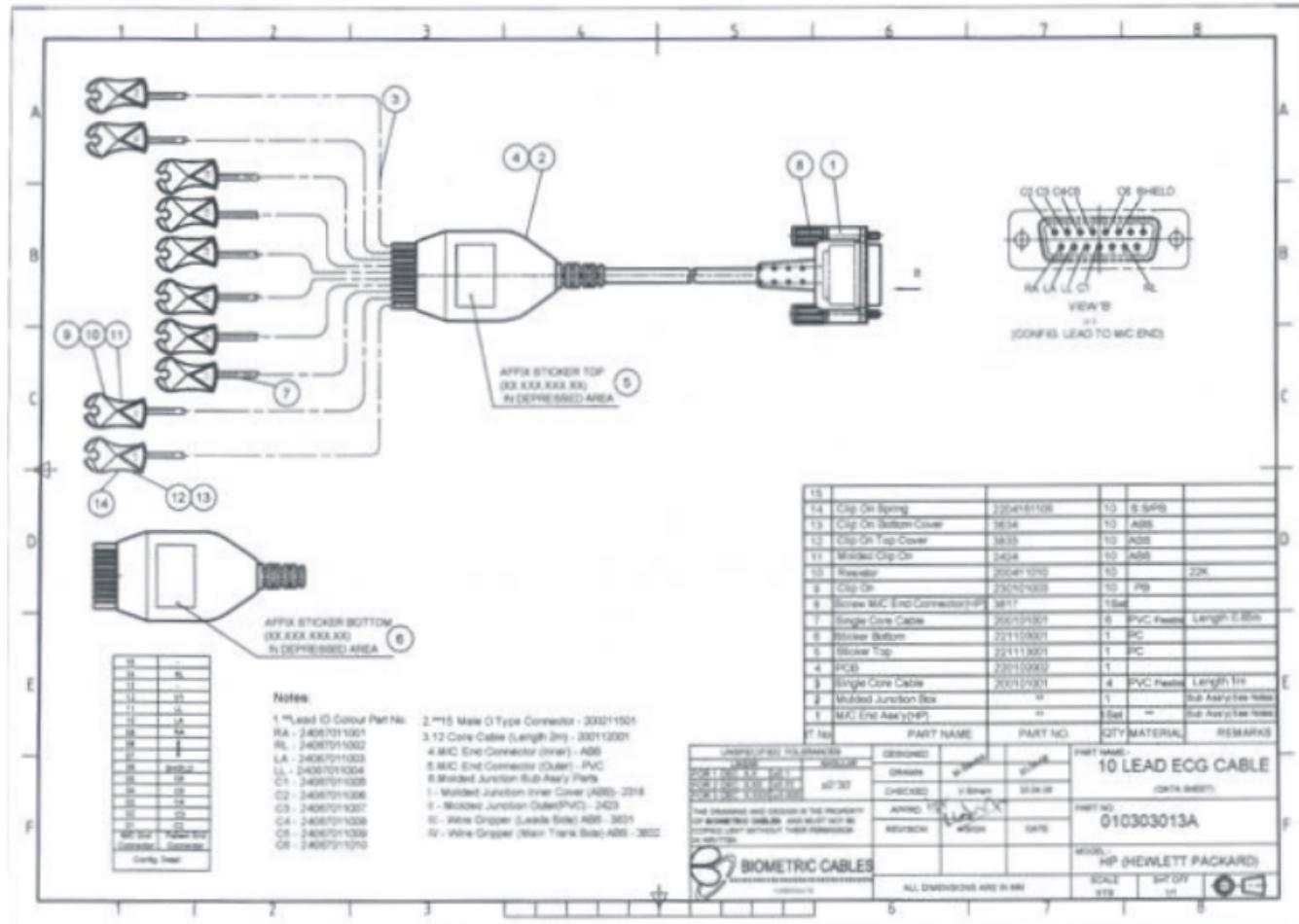


Figure 67. ECG Cable Schematic

## **8.4 Bill of Materials**

Table 29 lists the bill of materials for the ADS1198ECG-FE.

**Table 29. Bill of Materials: ADS1198ECG-FE**

Qty	Ref Des	Value	Description	MFR	Part Number
1	NA		Printed wiring board	TI	6514709
15	C1, C2, C3, C4, C5, C6, C11, C17, C47, C48, C49, C52, C58, C76, C77	1.0µF	Capacitor, ceramic 25V 10% X5R 0603	Murata	GRM188R61E105KA12D
0	C7, C8, C15, C19, C21, C22, C25, C27, C34, C36, C38, C40, C41, C42, C43, C44, C56, C62, C67, C78, C79, C81, C83, C85, C87, C89		Not Installed		
1	C9	22µF	Capacitor, ceramic 6.3V 10% X5R 0805	Taiyo Yuden	JMK212BJ226KG-T
11	C10, C45, C46, C50, C51, C54, C55, C60, C61, C65, C66	10µF	Capacitor, ceramic 10V 10% X5R 0805	Murata	GRM219R61A106KE44D
10	C12, C13, C14, C16, C18, C57, C69, C70, C94, C95	0.1µF	Capacitor, ceramic 50V 10% X7R 0603	Murata	GRM188R71H104KA93D
1	C20	10000pF	Capacitor, ceramic 50V 10% X7R 0603	Murata	GRM188R71H103KA01D
20	C23, C24, C26, C28, C29, C30, C31, C32, C72, C73, C74, C75, C80, C82, C84, C86, C88, C91, C92, C93	47pF	Capacitor, ceramic 50V 5% C0G 0603	Murata	GRM1885C1H470JA01D
0	C33, C35, C37		Not Installed		
0	C39		Not Installed		
4	C53, C59, C63, C64	2.2µF	Capacitor, ceramic 6.3V 10% X5R 0603	Murata	GRM185R60J225KE26D
2	C68, C71	100µF	Capacitor, ceramic 10V 20% X5R 1210	Taiyo Yuden	LMK325BJ107MM-T
1	C90	100pF	Capacitor, ceramic 50V 5% C0G 0603	Murata	GRM1885C1H101JA01D
0	D1 - D10		Not Installed		
1	J1		Connector, DSUB Rpct 15POS R/A PCB SLD	FCI	D15S13A4GV00LF
			Connector, DSUB Rpct R/A 15POS GOLD	Tyco	5747845-3
2	J2, J3		10x2x.1 female (installed from bottom side)	Samtec	SSW-110-21-FM-D
1	J4		5x2x.1 female (installed from bottom side)	Samtec	SSW-105-21-FM-D
0	J5		Not Installed		
4	JP1, JP4, JP5, JP16		2 Position Jumper _ 0.1" spacing	Samtec	TSW-102-07-T-S
0	JP3		Not Installed		
0	JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP17, JP25		Not Installed		
9	JP2, JP15, JP18, JP19, JP20, JP21, JP22, JP23, JP24		3-Position Jumper _ 0.1" spacing	Samtec	TSW-103-07-T-S
8	JP26, JP27, JP28, JP29, JP30, JP31, JP32, JP33		2x2x1, 2-Pin Dual Row Header	Samtec	TSW-102-07-T-D
5	L1 - L5		Ferrite Bead 470Ω 0805	Taiyo Yuden	BK2125HM471-T

**Table 29. Bill of Materials: ADS1198ECG-FE (continued)**

Qty	Ref Des	Value	Description	MFR	Part Number
0	R1, R4, R5, R11, R12, R15, R16, R19, R20, R23, R24, R27, R28, R31, R32, R35, R36, R41, R42, R45 - R51, R54, R55, R58 - R66, R68, R69, R70		Not Installed		
0	R2		Not Installed		
5	R3, R71, R72, R73, R74	0Ω	Resistor, 1/10W 5% 0603 SMD	Yageo	RC0603JR-070RL
14	R6, R7, R10, R14, R18, R22, R26, R30, R34, R38, R40, R44, R67, R75	10.0kΩ	Resistor, 1/10W 1% 0603 SMD	Yageo	RC0603FR-0710KL
1	R8	392kΩ	Resistor, 1/10W 1% 0603 SMD	Yageo	RC0603FR-07392KL
10	R9, R13, R17, R21, R25, R29, R33, R37, R39, R43	22.1kΩ	Resistor, 1/10W 1% 0603 SMD	Yageo	RC0603FR-0722K1L
1	R52	47.5kΩ	Resistor, 1/10W 1% 0603 SMD	Yageo	RC0603FR-0747K5L
1	R53	43.2kΩ	Resistor, 1/10W 1% 0603 SMD	Yageo	RC0603FR-0743K2L
1	R56	49.9kΩ	Resistor, 1/10W 1% 0603 SMD	Yageo	RC0603FR-0749K9L
1	R57	46.4kΩ	Resistor, 1/10W 1% 0603 SMD	Yageo	RC0603FR-0746K4L
5	TP1, TP2, TP8, TP11, TP12		Test Point PC Mini .040"D Black	Keystone	5001
8	TP3, TP4, TP5, TP6, TP7, TP9, TP10, TP13		Test Point PC Mini .040"D Red	Keystone	5000
1	U1		IC ADC 16-Bit SPI 8kSPS 64TQFP	TI	ADS1198CPAG
0	U2		Not Installed		
0	U3, U4, U5		Not Installed		
1	U6		IC Unreg Chrg Pump V INV SOT23-5	TI	TPS60403DBVR
1	U7		IC LDO Reg 250mA 3.0V SOT23-5	TI	TPS73230DBVR
1	U8		IC LDO Reg NEG 200mA ADJ SOT23-5	TI	TPS72301DBVT
1	U9		IC LDO Reg 250mA ADJ-V SOT23-5	TI	TPS73201DBV
1	U10		IC EEPROM 256kBit 400kHz 8TSSOP	Microchip	24AA256-I/ST
1	OSC1		OSC 2.0480 MHZ 3.3V HCMOS SMT	Fox	FXO-HC735-2.048MHZ
28	NA		Shunt	Samtec	SNT-100-BK-G-H

## 9 Appendix

### 9.1 Optional External Hardware (Not Included)

The input of the ADS1198ECG-FE requires a DB15 connector. [Figure 68](#) illustrates the most optimal cable connection to the ADS1198ECG-FE. [Figure 69](#) and [Figure 70](#) show two alternate ways that cables can be constructed to interface with the ADS1198ECG-FE. [Figure 71](#) shows an alternate testing tool to the instrument used in the tests for this user guide (refer to [Section 4.7.1](#)).



**Figure 68. 15-Pin, Shielded Connector from Biometric Cables**



Figure 69. 15-Pin, Twisted Wire Cable to Banana Jacks



Figure 70. 15-Pin, Twisted Wire Cable

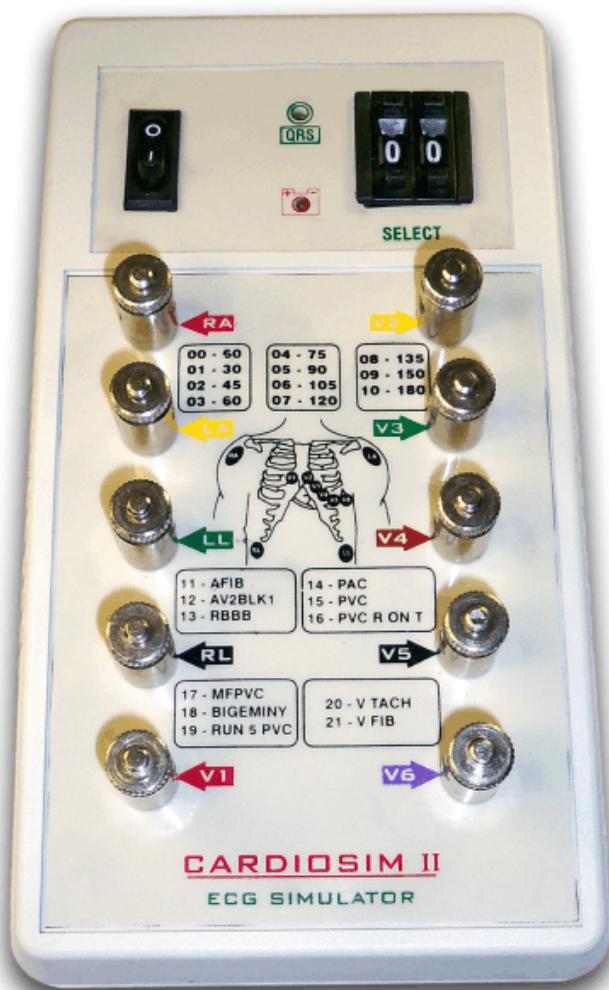


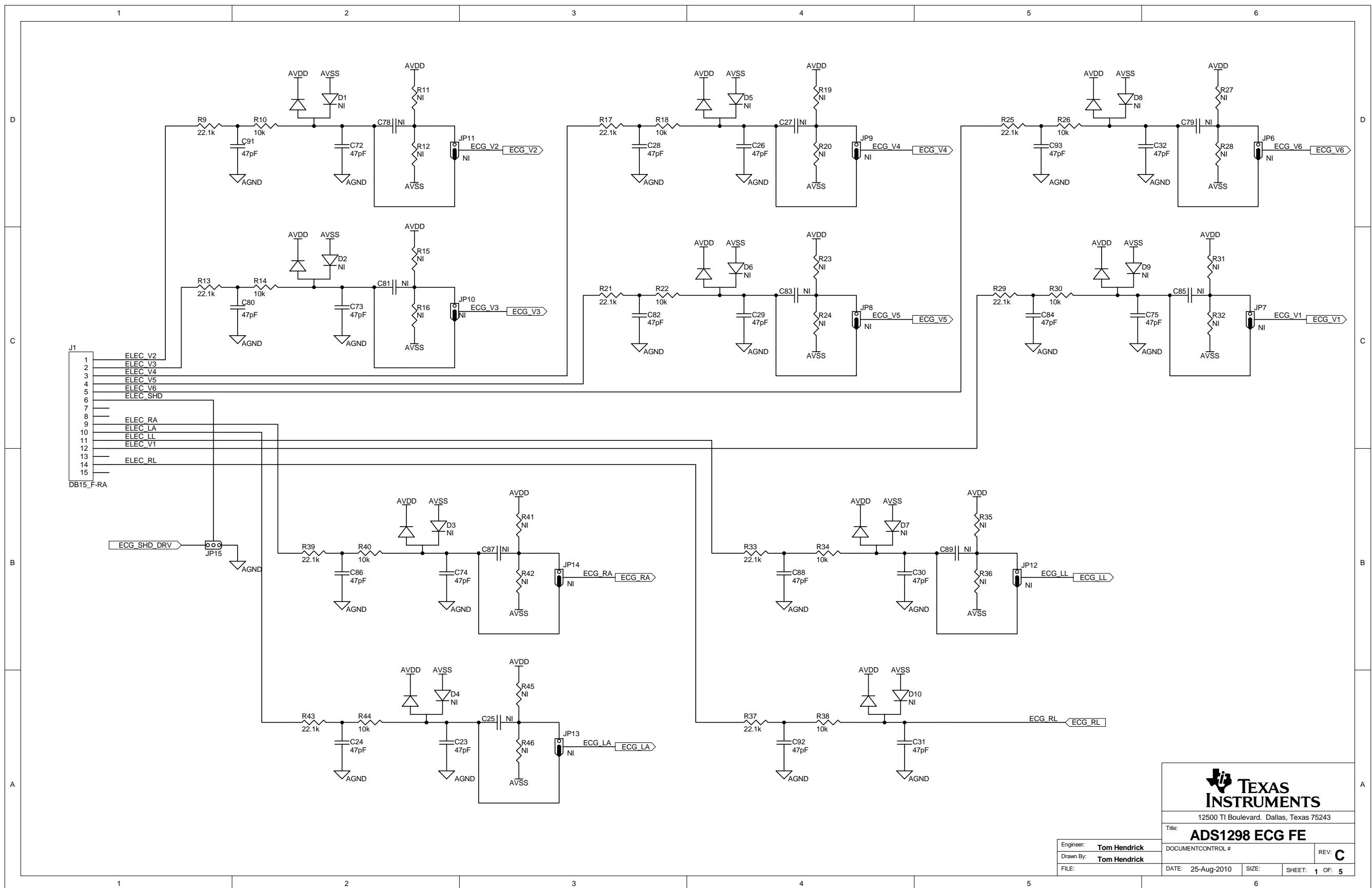
Figure 71. Cardiosim ECG Simulator Tool

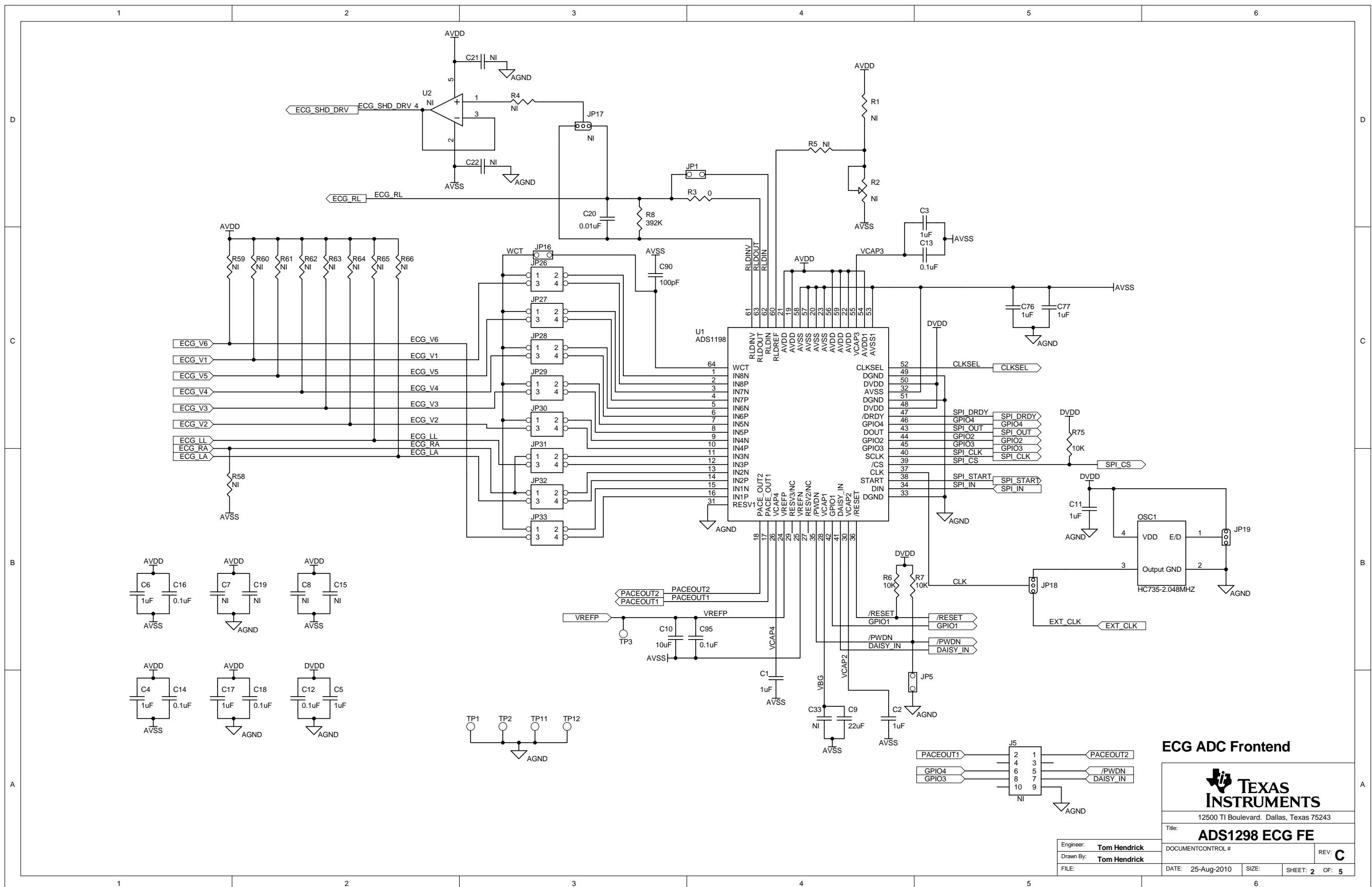
## 9.2 ADS1198ECG-FE Power-Supply Recommendations

Figure 72 shows a +6V power-supply cable (not provided in the EVM kit) connected to a battery pack with four 1.5V batteries connected in series. Connecting to a wall-powered source (provided in the EVM kit) makes the ADS1198ECG-FE more susceptible to 50Hz/60Hz noise pickup; therefore, for best performance, it is recommended to power the ADS1198ECG-FE with a battery source. This configuration minimizes the amount of noise pickup seen at the digitized output of the ADS1198.



Figure 72. Recommended Power Supply for ADS1198ECG-FE





D

D

C

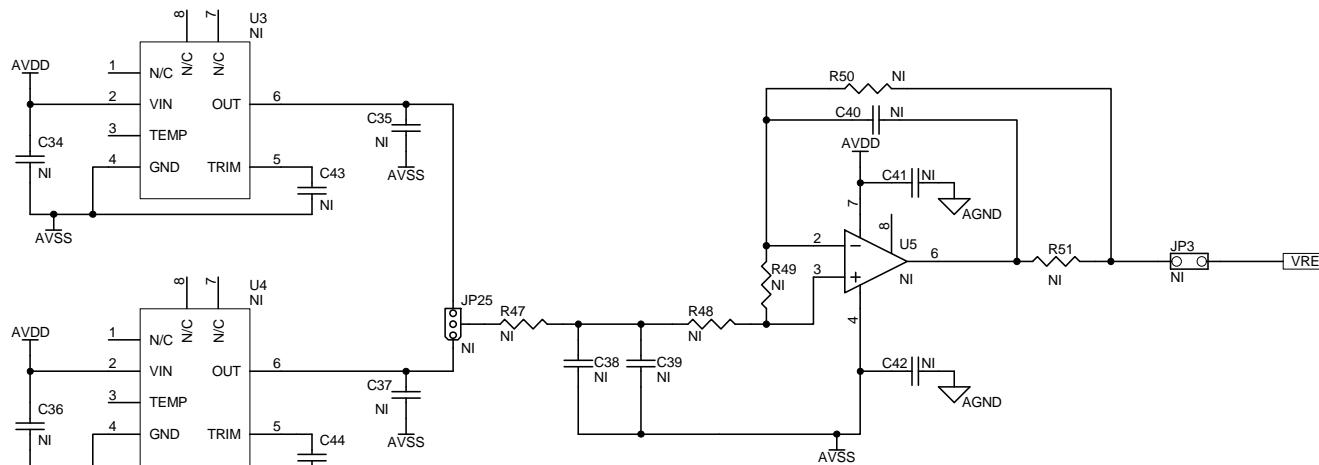
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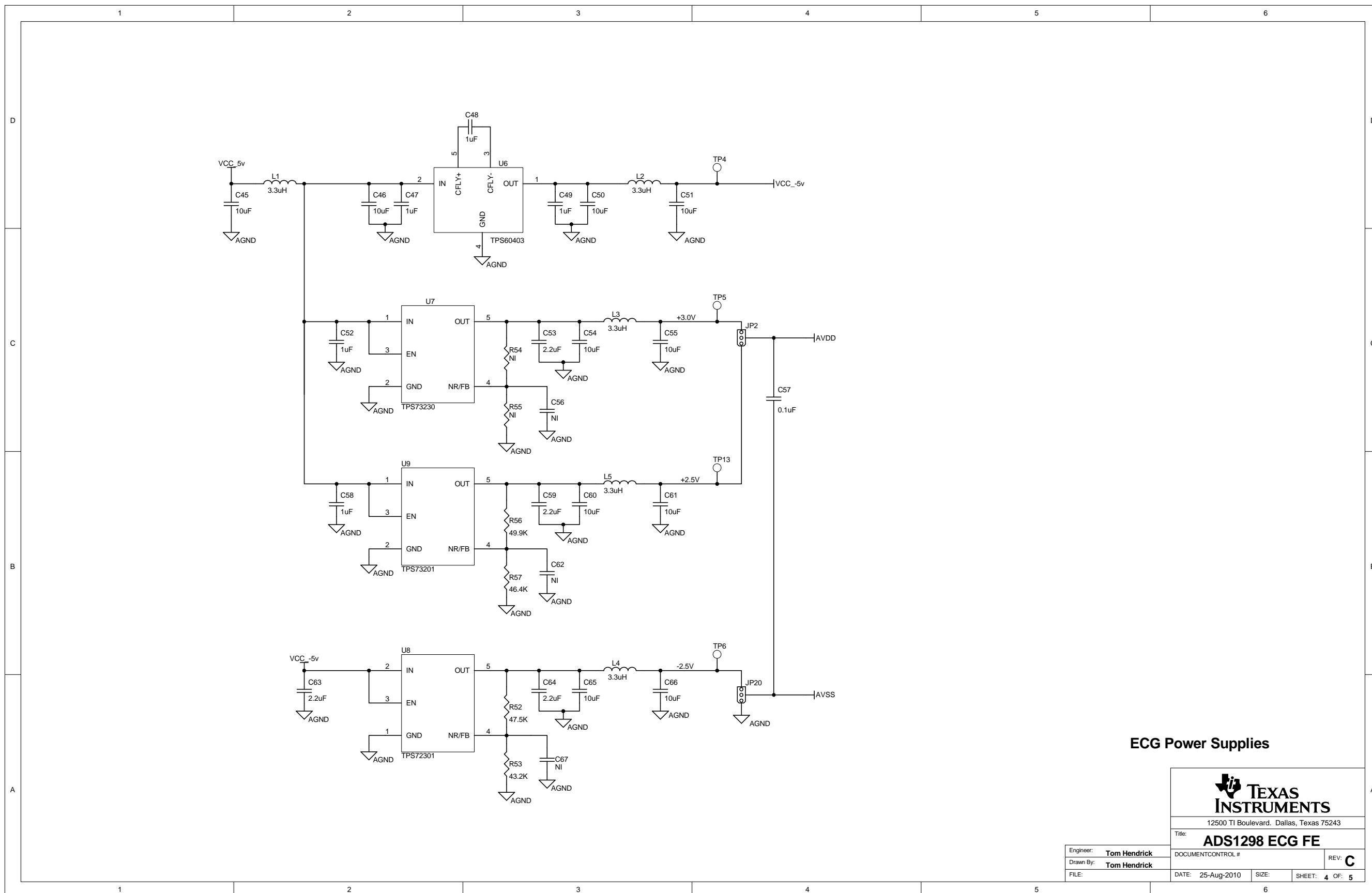
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A

A

**External Reference****External Reference Drivers****NOT INSTALLED**

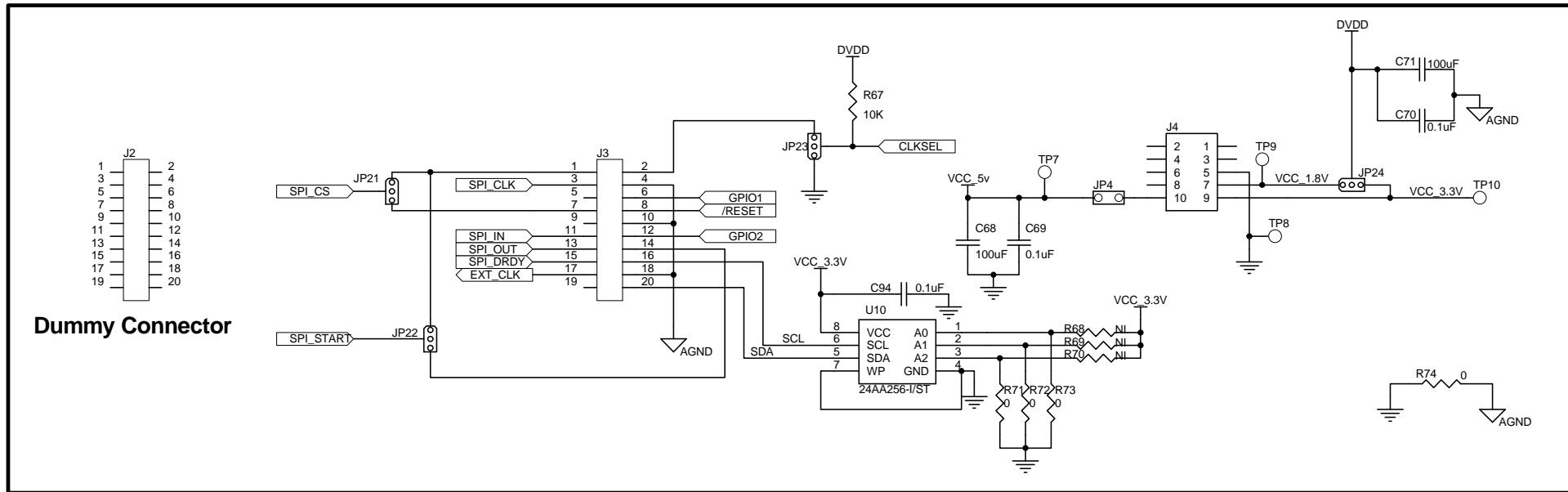
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	12500 TI Boulevard, Dallas, Texas 75243
Title:	<b>ADS1298 ECG FE</b>
Engineer:	<b>Tom Hendrick</b>
Drawn By:	<b>Tom Hendrick</b>
DOCUMENT CONTROL #	
FILE#	DATE: 25-Aug-2010 SIZE: SHEET: 3 OF 5
	REV: <b>C</b>



1 2 3 4 5 6

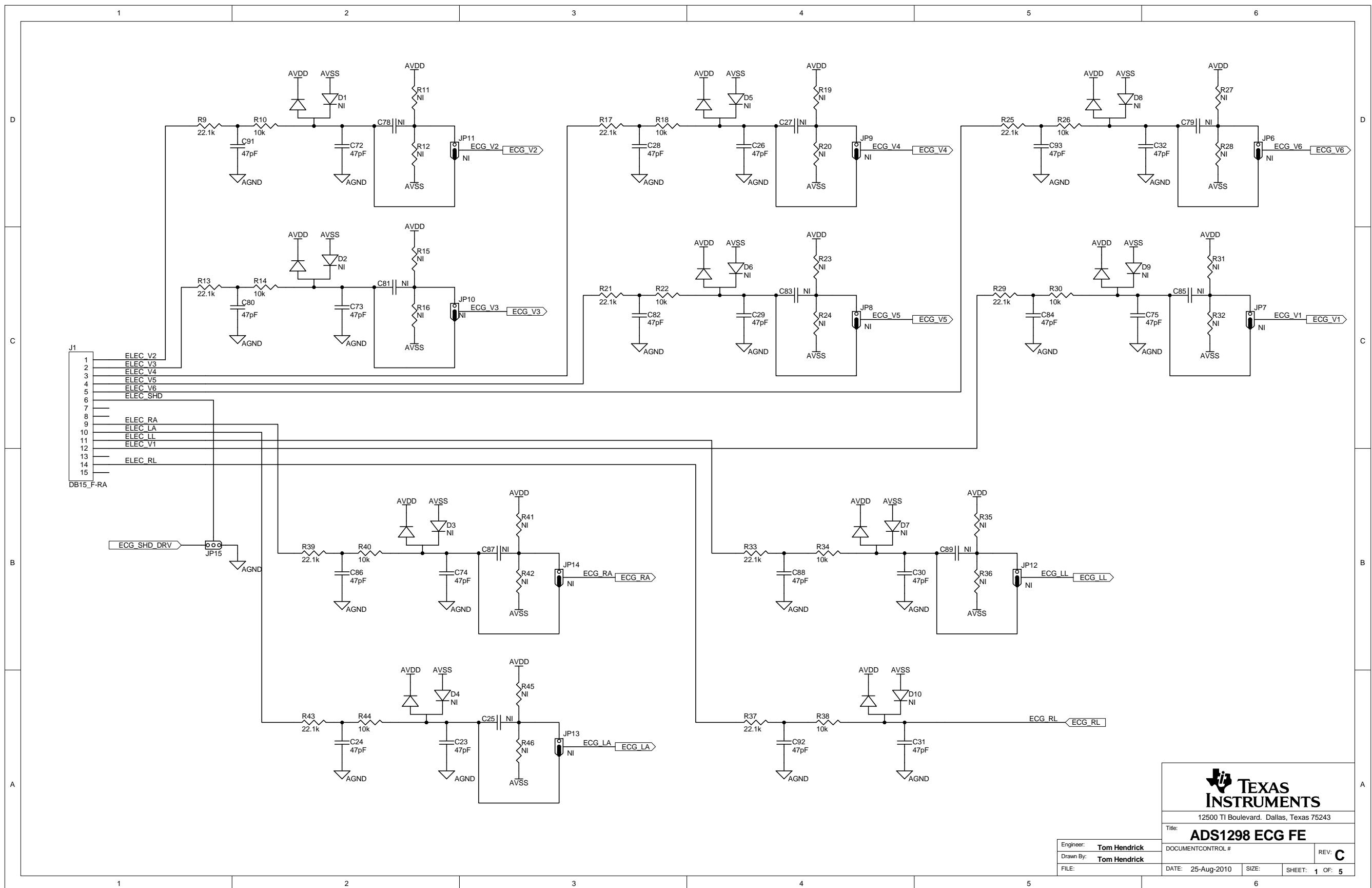
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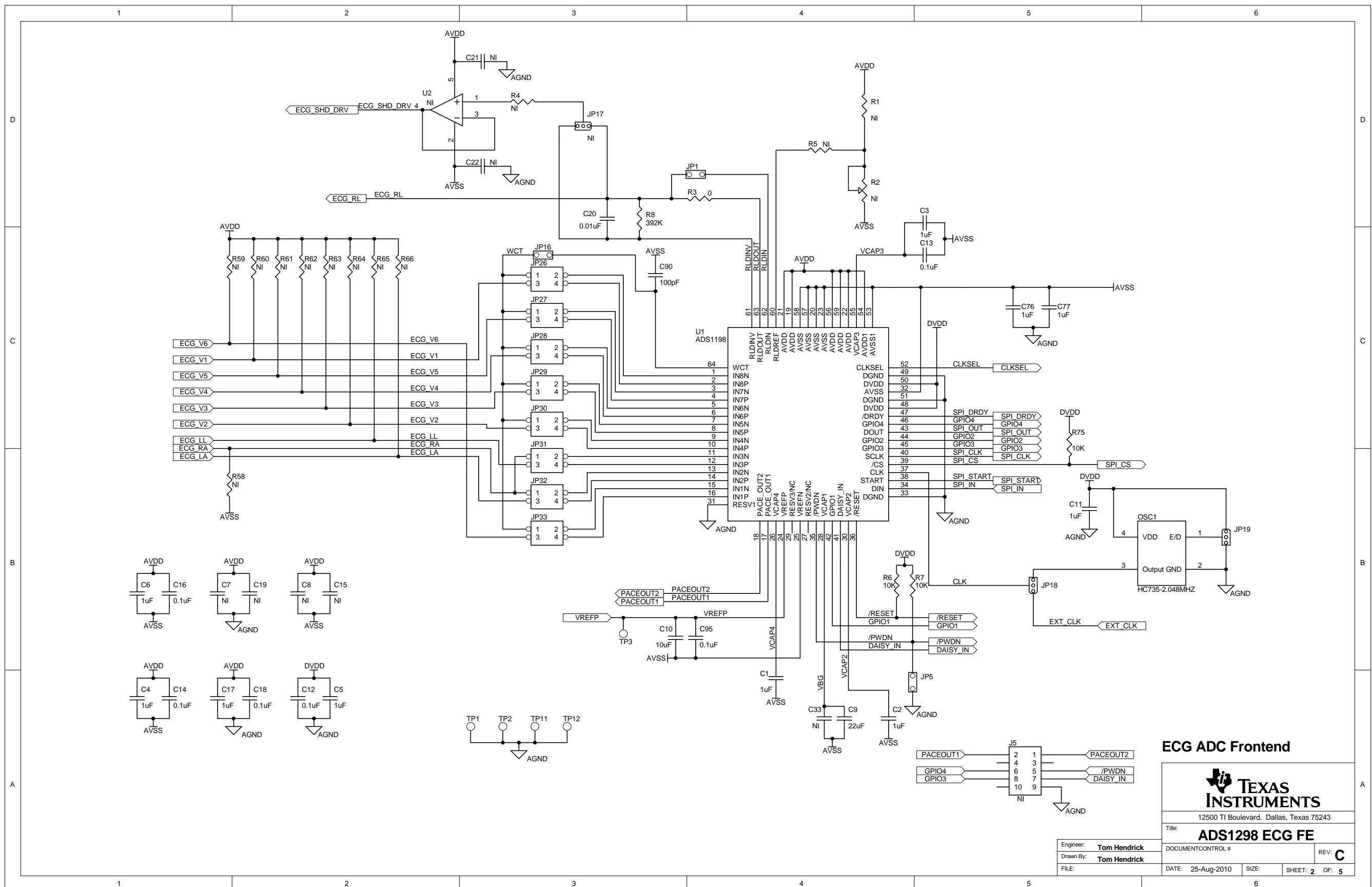
D

**MDK Interface Connectors****NOTE: J2, J3, J4 female connectors should be populated from the bottom side !****ECG MDK Board Interface Adapter**

	<b>TEXAS INSTRUMENTS</b>
	12500 TI Boulevard. Dallas, Texas 75243
Title:	<b>ADS1298 ECG FE</b>
Engineer:	<b>Tom Hendrick</b>
Drawn By:	<b>Tom Hendrick</b>
DOCUMENT CONTROL #	REV <b>C</b>
FILE#	DATE: 25-Aug-2010 SIZE: SHEET: 5 OF 5

1 2 3 4 5 6





D

D

C

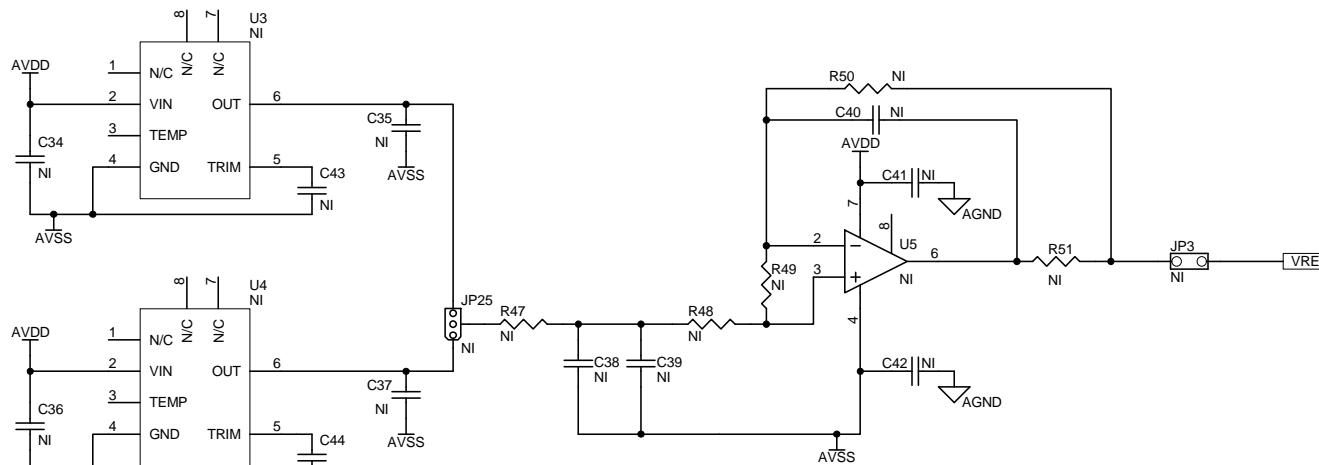
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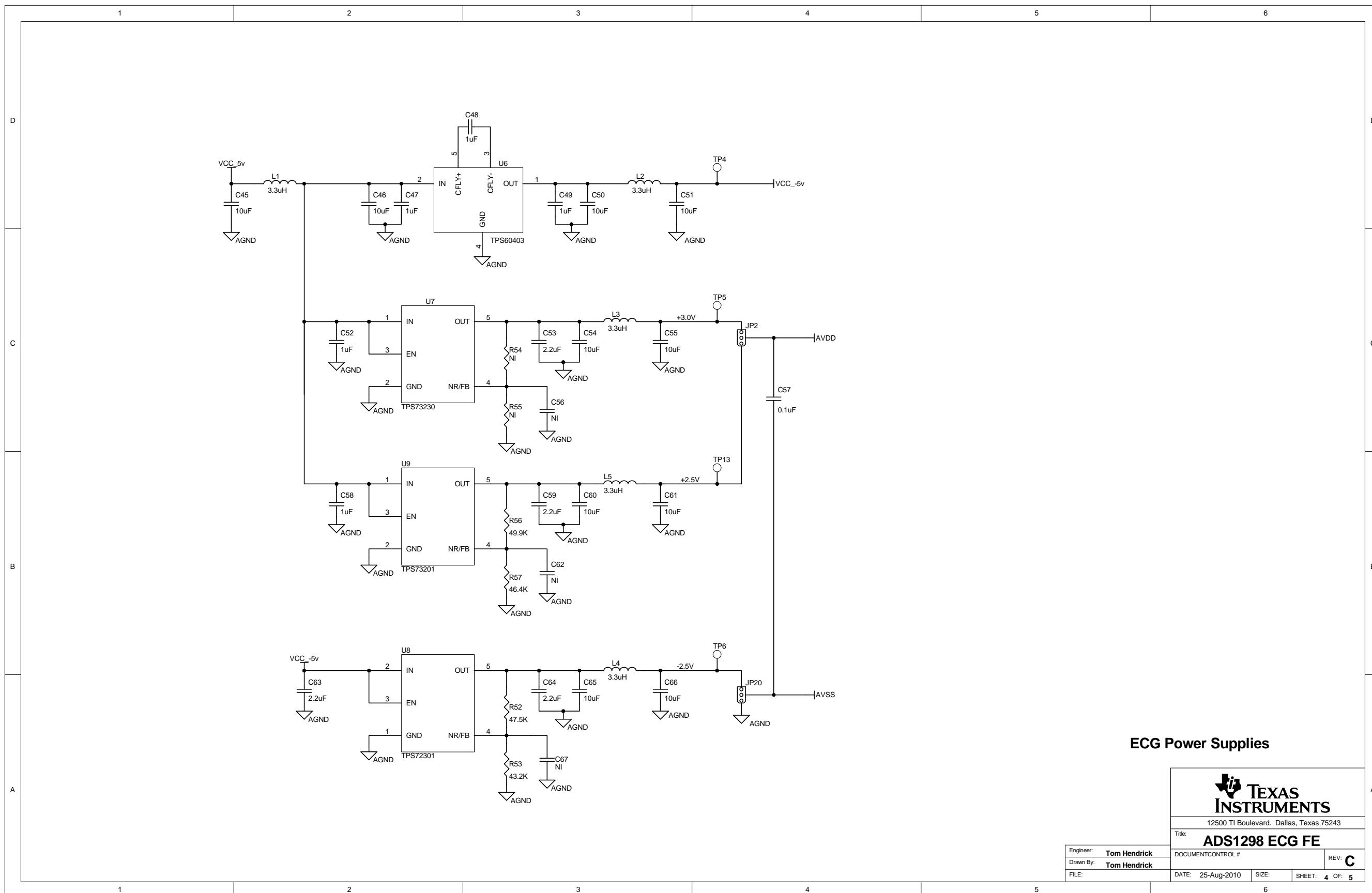
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A

**External Reference****External Reference Drivers****NOT INSTALLED**

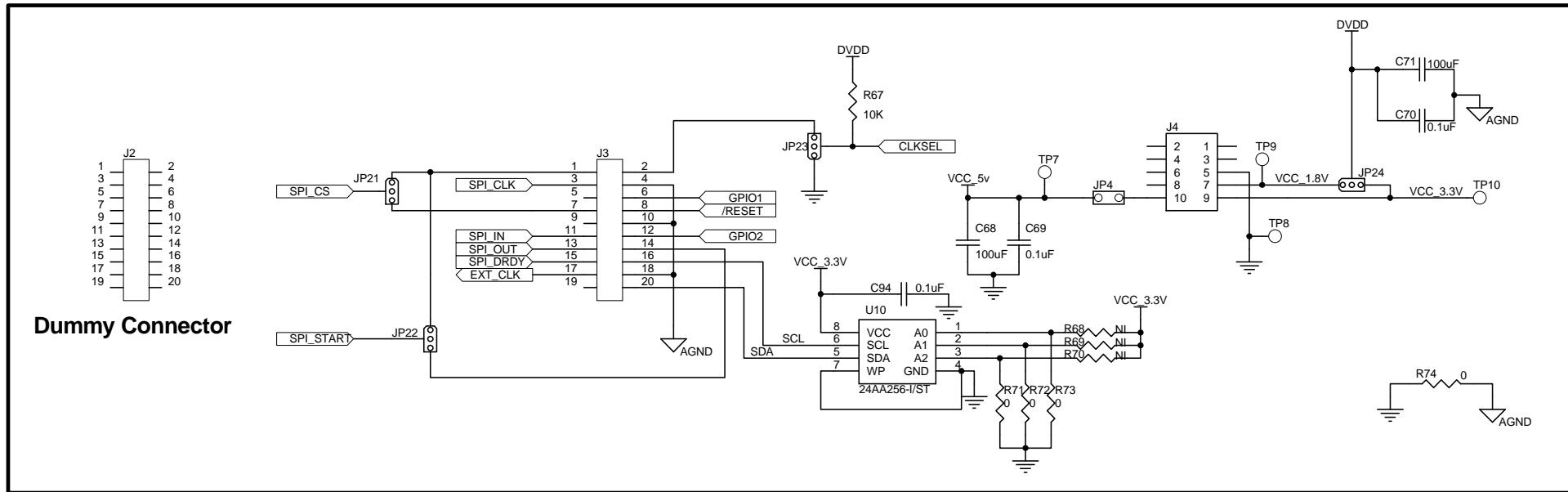
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	12500 TI Boulevard, Dallas, Texas 75243
Title:	<b>ADS1298 ECG FE</b>
Engineer:	<b>Tom Hendrick</b>
Drawn By:	<b>Tom Hendrick</b>
DOCUMENT CONTROL #	
FILE#	DATE: 25-Aug-2010 SIZE: SHEET: 3 OF: 5
	REV: <b>C</b>



1 2 3 4 5 6

D

D

**MDK Interface Connectors****NOTE: J2, J3, J4 female connectors should be populated from the bottom side !****ECG MDK Board Interface Adapter**

	<b>TEXAS INSTRUMENTS</b>
	12500 TI Boulevard. Dallas, Texas 75243
Title:	<b>ADS1298 ECG FE</b>
Engineer:	<b>Tom Hendrick</b>
Drawn By:	<b>Tom Hendrick</b>
DOCUMENT CONTROL #	REV <b>C</b>
FILE#	DATE: 25-Aug-2010 SIZE: SHEET: 5 OF 5

1 2 3 4 5 6

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It is important to operate this EVM within the input voltage range of -2.5V to +5V and the output voltage range of 0V to 5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30°C. The EVM is designed to operate properly with certain components above +30°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>