Keywords: chip scale package, flip chip, CSP, UCSP, U-CSP, BGA, WLCSP

May 01, 2008

APPLICATION NOTE 1891

Wafer-level packaging (WLP) and its applications

Abstract: This application note discusses Maxim's wafer-level package (WLP). Topics include: wafer construction, tape-and-reel packaging, PCB layout, assembly, reflow, thermal properties, and reliability.

Note: Ultimately, it is the responsibility of the end user and assembler to abide by their own design and the assembly document requirements of their industry standards. Industry standards documents can include, but are not limited to:

- Association Connecting Electronics Industries (IPC)
- Joint Electronic Device Engineering Council (JEDEC)
- Electronic Industries Alliance (EIA)
- International Electronics Manufacturing Initiative (iNEMI)
- International Electrotechnical Commission (IEC)
- American National Standards Institute (ANSI)
- Jisso International Council (JIC)
- Japan Printed Circuit Association (JPCA)
- Wiring and Harness Manufacturers Association (WHMA)

Introduction

The wafer-level package (WLP) is a type of chip-scale package (CSP), which enables the IC to be attached face down to the printed circuit board (PCB) using conventional SMT assembly methods. The chip's pads connect directly to the PCB pads through individual solder balls (**Figure 1**). WLP technology differs from other ball grid array, leaded, and laminate-based CSPs because no bond wires or interposer connections are required. In general, underfill material is not required for WLP. However, in certain applications such as mobile devices, underfill can enhance WLP mechanical robustness. The main advantages of the WLP are a small package size, a minimized IC-to-PCB inductance, and a shortened manufacturing cycle time.

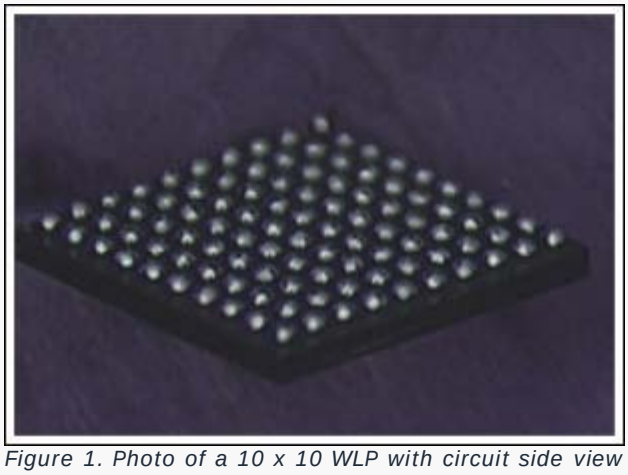

Figure 1. Photo of a 10 x 10 WLP with circuit side view

WLP construction

Maxim's WLP chips are manufactured by building up the package interconnect structure directly on the silicon circuit substrate. A dielectric repassivation polymer film is applied over the active wafer surface. This film provides both mechanical stress relief for the ball attachment, and electrical isolation on the die surface. Vias are imaged within the polymer film, providing electrical contact to the IC bond pad.

WLP ball arrays are configured based on a regular grid with an uniform grid pitch. The solder bump material is identified by the A1 indicator in the top mark (see **Figure 2** for the location of A1 in top mark). The A1 indicator for eutectic SnPb solder is a laser overlay of dual concentric circles, ⊙. For Pb-free solders, the lasered A1 indicator is a plus sign, ✚. Backside wafer lamination (protective polymer film) is used for all Pb-free WLP products. This polymer material is included for both mechanical and UV light protection of the backside silicon surface.

WLP area array designs and dimensions

Maxim's WLP packages are currently designed in both 0.5mm and 0.4mm pitch. Detailed WLP outline drawings are available on Maxim's

Package Outlines page.

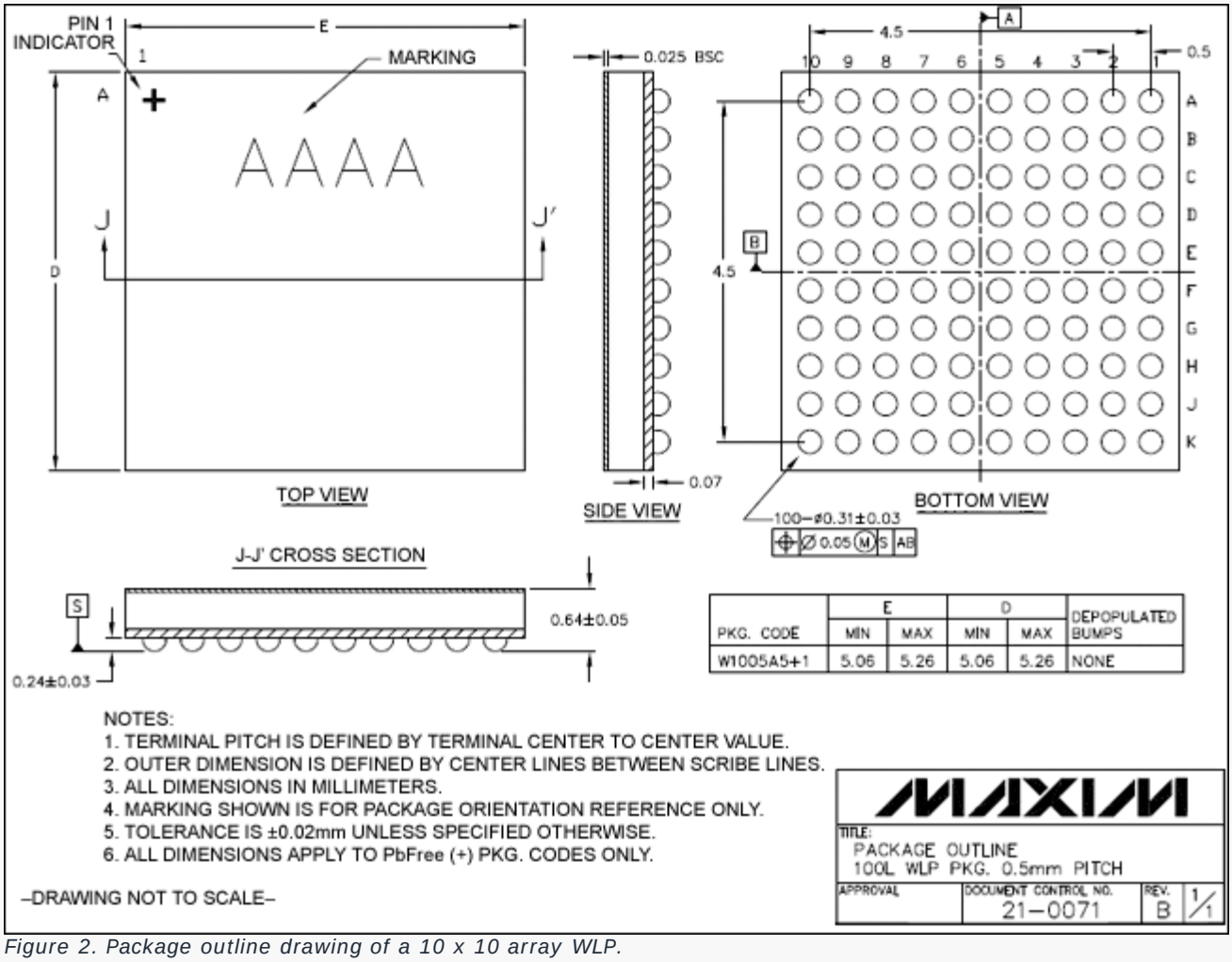

Figure 2. Package outline drawing of a 10 x 10 array WLP.

WLP carrier tape

Maxim ships all WLPs in the component carrier tape-and-reel (T&R) format only. WLP tape-and-reel requirements are based on the EIA-481 standard. Detailed tape-and-reel construction information is available on Maxim's SMD Tape & Reel Data page.

PCB assembly process design and implementation

Reference:

- IPC-7094 Design and Assembly Process Implementation for Flip-Chip and Die Size Components

PCB design criteria

References:

- IPC-A-600 Acceptability of Printed Boards
- IPC-6011 Generic Performance Specification for Printed Boards
- IPC-6012 Qualification and Performance Specification for Rigid Printed Boards
- IPC-6013 Qualification and Performance Specification for Flexible Printed Boards
- IPC-6016 Qualification and Performance Specification for High-Density Interconnect (HDI) Layers or Boards
- IPC-D-279 Design Guidelines for Reliable Surface-Mount Technology Printed Board Assemblies
- IPC-2221 Generic Standard on Printed Board Design
- IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards
- IPC-2223 Sectional Design Standard for Flexible Printed Boards
- IPC-2226 Design Standard for High-Density Array or Peripheral Leaded Component Mounting Structures

1. The design layout for the WLP component should be at the most neutral location of mechanical stress and strain; it should be shrouded by much taller adjacent components, wherever possible.
2. For all two-sided PCB assembly designs, align a much larger compliant package on the opposite side at the WLP centroid location.

Land pattern design

Reference:

- IPC-7351 Generic Requirements for Surface-Mount Design and Land Pattern Standard

Two types of land patterns are used for surface-mount packages (**Figure 3**):

1. **Solder Mask Defined (SMD)**
   - SMD pads are open metal surfaces with solder mask openings.
   - The solder mask opening is smaller than the metal pad.
   - Solder mask material used to define the opening is commonly LPI (liquid photoimageable) and must have suitable material properties to meet all SMT processing requirements.
2. **NonSolder Mask Defined (NSMD).**
   - NSMD pads are metal defined pads that have a solder mask clearance around the pad.
   - The solder mask opening is larger than the metal pad.
   - The solder mask material used to define the opening is commonly LPI (liquid photoimageable) and must have suitable material properties to meet all SMT processing requirements.

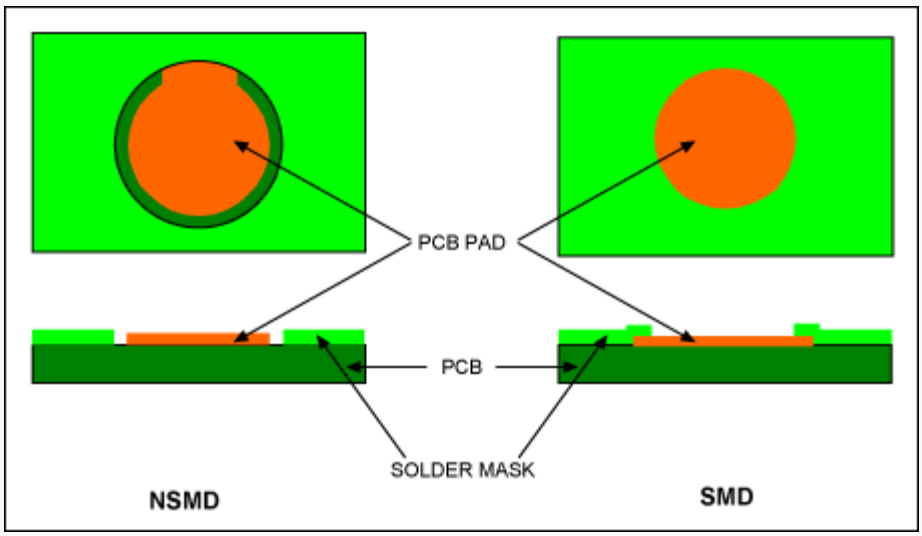

Figure 3. SMD vs. NSMD PCB land pad design for WLP.

To choose between NSMD and SMD pads, all power, ground, and signal-routing requirements must be considered.

For a given WLP pitch, the size of a NSMD pad is smaller than that of an SMD pad. Therefore, the NSMD board design allows better routability of Cu lines between pads. Also, micro-via design (i.e., "via in pad") can improve the routability of Cu lines between pads.

Use only one type of a pad layout (NSMD or SMD) and one type of pad surface finish (see below) for a given board design.

Solder mask is recommended between all pads.

The trace width connected to pads should be < 60% pad diameter.

Table 1. PCB pad size (in microns) for Maxim WLP

WLP Ball Pitch	Nominal Ball Size Diameter	Nominal Pad Size Diameter Used in Maxim Package Qualification	Recommended Pad Size Range
500	300	220	220 ±25
500	350	275	275 ±25
400	250	210	210 ±25

Metal surface coating

1. Organic Solderability Preservative (OSP): allowed.
2. Electroless Nickel/Immersion Gold (ENIG): allowed.
3. Immersion tin plating and Hot-Air Solder Level (HASL) tin plating: not recommended.

Pb-free assembly PCB material

Standard FR-4 is compatible with Maxim WLP. However, using higher glass transition (Tg) FR-4 with smaller thermal expansion coefficient (CTE) improves package reliability.

Solder paste print stencil aperture design

Reference:

- IPC-7525 Guidelines for Stencil Design

Aperture shape

1. Square is preferred to round for improved solder paste release from the stencil.
2. The stencil aperture shape should be trapezoidal with the bottom opening (at PCB side) larger than the opening at the top of the stencil.

Solder stencil fabrication

Stencils can be fabricated using either of the following processes:

1. Laser cut of stainless steel foil with subsequent electropolishing
2. Electroforming of nickel-based metal foil

SMT process flow

INCOMING WLP TAPE -AND -REEL INSPECTION
↓
SOLDER PASTE PRINTING ON BOARD
↓
CHIP PLACEMENT ON BOARD
↓
SOLDER REFLOW
↓
FLUX CLEANING (OPTIONAL)
↓
SOLDER JOINT INSPECTION
↓
PACK AND SHIP

Automated component placement

1. Standard pick-and-place equipment can be used for placing Maxim WLP; fine-pitch IC-packaging placement equipment is preferred for better accuracy.
2. Minimum force should be used for pick and place to avoid physical damage.
3. To have better reflow yield, it is recommended that bumps be dipped into solder paste on the PCB to greater than 20% of paste block height.

Solder paste reflow

1. All Maxim WLPs are compatible with industry-standard solder reflow processes. For a reflow profile, reference the Pb-free solder reflow requirement in J-STD-020, Rev D.1, and any other recommendation from the paste supplier.
2. Nitrogen inert-atmosphere reflow soldering is optional. However, the use of nitrogen inert-atmosphere reflow has demonstrated a better centering of the Pb-free WLP on the PCB pads than in the case of reflow in air.

Rework of WLP

Rework should only be performed using a controlled and qualified process which prevents mechanical and ESD damage of the silicon circuit and package.

Focused infrared (IR) technology is recommended for ball array package rework over traditional hot gas BGA rework systems. Focused IR allows for pin-point accuracy reflow removal and replacement of even the smallest WLP parts in a high-density circuit assembly without adjacent components heating.

Thermal performance of WLP

3-D thermal modeling has been performed to determine the junction-to-air thermal resistance, Θ_{JA}, and junction-to-board thermal resistance, Θ_{JB}, of Maxim WLP. See **Figures 4** and **5** for standard four-layer 2s2p boards (JESD51-9). Additional data for the 1s0p boards can be found on Maxim's internal WLP engineering site. Please ask your sales representative for access to AN1891_1.

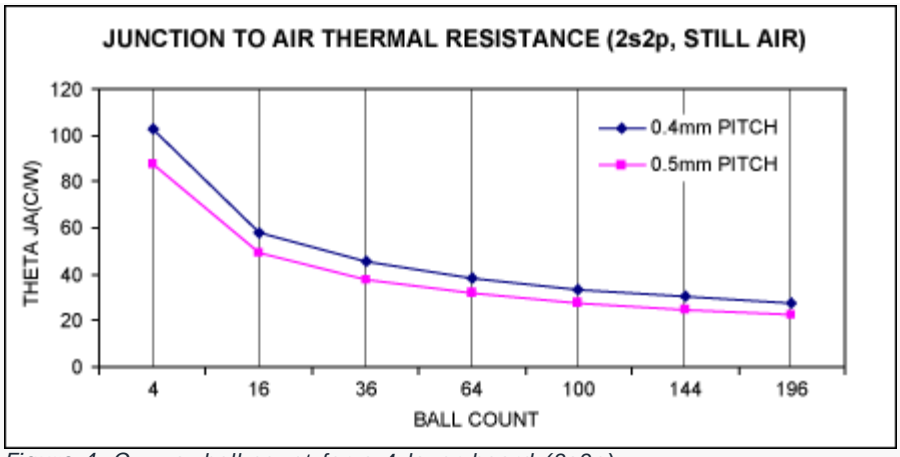

Figure 4. Θ_{JA} vs. ball count for a 4-layer board (2s2p).

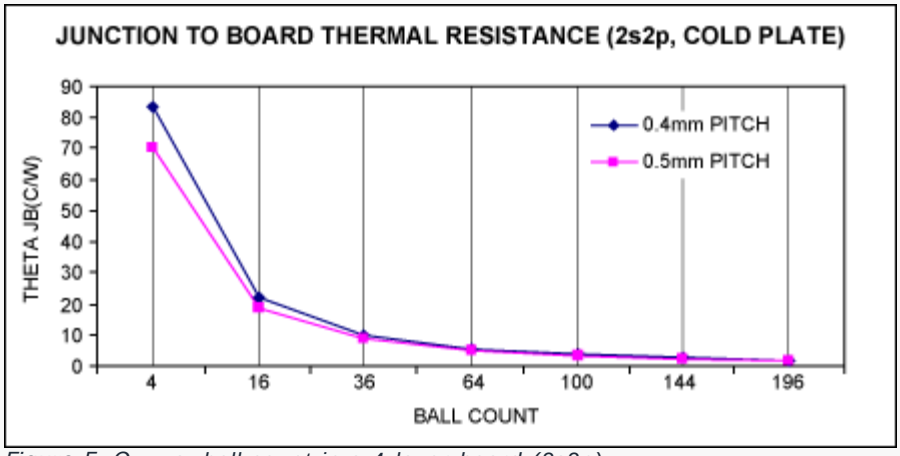

Figure 5. Θ_{JB} vs. ball count in a 4-layer board (2s2p).

Maxim WLP reliability

Reliability tests detailed in **Table 2** are performed to qualify Maxim WLP. Data for a 6 × 6 array WLP is given in **Table 3**. Data for other arrays can be found on Maxim's internal WLP engineering site. Please ask your sales representative for AN1891_1.

Table 2. Reliability qualification requirements

Test	Specification	Test Duration	Sampling Plan	Number of Lots
MSL 1 Solder Reflow (260°C peak)	J-STD 20C	3x	0/150	3
High-Temperature Storage	JESD22 A103	1000 hours	0/77	3
Temperature Cycle	JESD22 A104, Condition G (-40°C to + 125°C)	1000 cycles (array size < = 6 x 6)	77	3
		500 cycles (array size > 6 x 6)	77 (note)	3
Operating Life Test(Tj = 135°C)	JESD22 A108	1000 hours	0/77	3
Drop Test	JESD22 B111	150 cycles	60 (note)	1

Note: Less than 5% failure rate and more than 90% confidence level at the number of cycles specified for the reliability stress.

Table 3. 0.5mm pitch 6 x 6 array Pb-free WLP reliability test results

Stress Test	Duration	No. of Samples	No. of Failures
Solder Reflow	3x	150	0
Temp. Cycle	500x	77	0
	1000x	77	0
High-Temp. Storage	1000 hours	240	0
Drop Test*	150x	60	0

* Using WLP daisy chain.

Automatic Updates

Application note 1891: www.maxim-ic.com/an1891

More Information

For technical support: www.maxim-ic.com/support
For samples: www.maxim-ic.com/samples
Other questions and comments: www.maxim-ic.com/contact