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APPLICATION NOTE 4053

Setup and Hold Times for High-Speed Digital-to-Analog Converters (DACs) Demystified

Abstract: This application note defines setup and hold times for high-speed digital-to-analog converters (DACs) and identifies their proper interpretation. High-speed DACs often specify these two parameters as "signed" values, and interpreting them with regard to data transition can be challenging. The application presented in this article helps offset this challenge.

Introduction

Meeting the digital timing requirements for high-speed digital-to-analog converters (DACs) is critical for achieving maximum performance. As clock frequencies increase, setup and hold times for the data interface become significant concerns for the system designer. The goal of this application note is to thoroughly explain the setup and hold times as they pertain to Maxim's high-performance converter solutions.

Defining Setup and Hold Times

Setup time (t_S) describes the point in time data must be at a valid logic level relative to the DAC clock transition. Hold time (t_H), on the other hand, specifies when the data can change after it has been captured/sampled by the device. **Figure 1** shows setup and hold times with reference to a rising-edge clock signal. The active edge of the clock signal for a specific device may be the rising/falling edge or it may be user selectable, as in the MAX5895 16-bit, 500Msps interpolating and modulating dual DAC that has CMOS inputs.

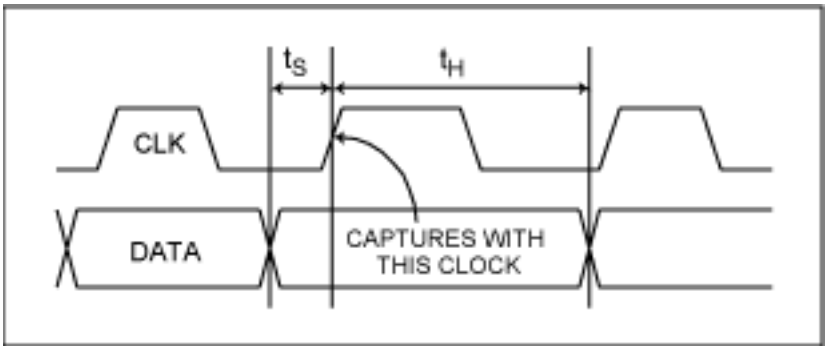

Figure 1. Setup and hold times in reference to a rising-edge clock signal.

Digital circuits designed in CMOS technologies typically switch at the voltage midway between the supply rails. Therefore, the time reference markers are positioned at the midpoint of the signal edges. The positions of the waveforms in Figure 1 demonstrate this typical condition for setup and hold times. Note that both parameters for this setting are positive in magnitude. Confusion can arise when the specified values for either setup or hold time are negative.

The MAX5891 600Msps, 16-bit DAC provides an excellent case study example for this midpoint condition. The setup time is specified for -1.5ns, and the hold time is 2.6ns. **Figure 2** illustrates the minimum setup time for the MAX5891. Note that, in reality, the data transition occurs after the capture clock has transitioned. **Figure 3** shows the minimum hold time for the same device.

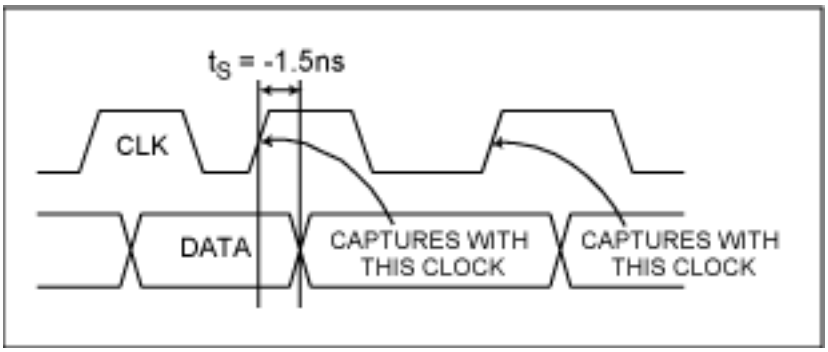

Figure 2. Minimum setup time for the MAX5891.

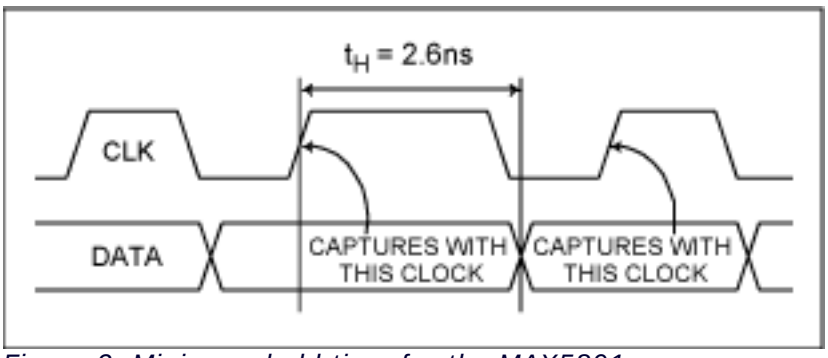

Figure 3. Minimum hold time for the MAX5891.

Meeting these timing specifications requires the user to analyze the data source's propagation delay and jitter specifications. The propagation delay determines the nominal timing requirements for the clock, while the jitter specification sets the available margin. To explain this relationship, consider a logic gate that has a propagation delay of 1.5ns. Using the same clock signal for the logic gate, the MAX5891 would just meet the setup time as shown in Figure 2. There would be no margin in this situation for temperature drift, clock or data jitter, or device-to-device variations.

Two of the techniques used to optimize the setup and hold times include adding clock delays and matching trace lengths. The addition of clock delays between the data source and the DAC helps to address the propagation-delay issue in the previous example. Matching the trace lengths between the digital source and the DAC input pins ensures that the effects of jitter and drift do not cause individual bits to slip into the next clock cycle. Remember that we are dealing with a high-speed digital data bus that is comprised of several data lines. The timing specifications must be met for all of these bits at all times.

Conclusion

There are many challenges with clocking high-frequency data. Overcoming these challenges requires a design or system-level engineer to fully understand the specifications for all devices in his/her signal chain. Failure to meet the requirements for any device in the chain will result in decreased system performance. Performance impairment may manifest itself as reduced DAC output accuracy or limited clock frequency.

Application Note 4053: www.maxim-ic.com/an4053

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