DIGITAL SYSTEMS AND MICROPROCESSORS (ELE2002M)

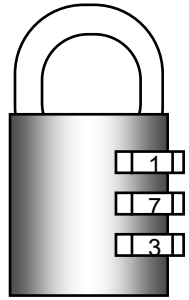
LECTURE 7 - SEQUENTIAL LOGIC

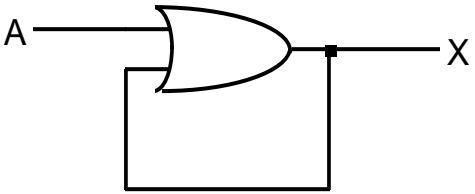
Instructor:

Assoc. Prof. Dr. Edmond Nurellari

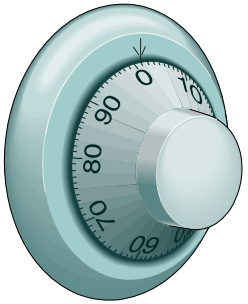
Sequential Logic Circuits

- So far we have only considered circuits where the output is purely a function of the inputs
- With sequential circuits the output is a function of the values of past and present inputs





$$X = X + A$$

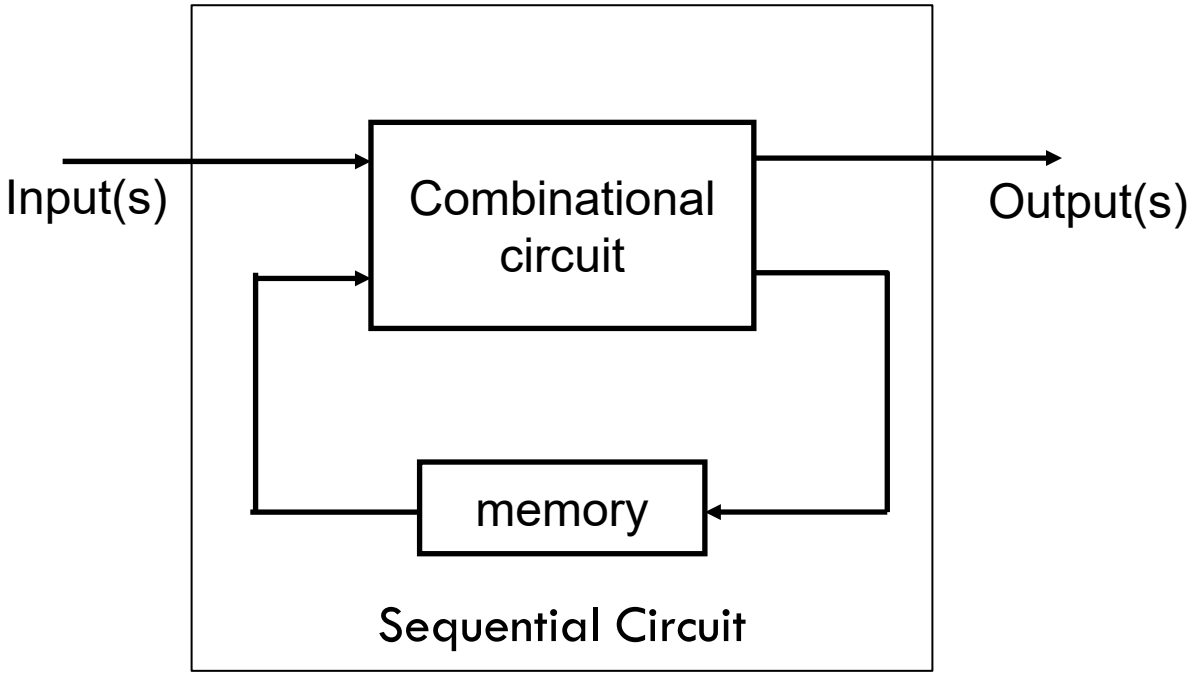


Sequential Circuits - Aims

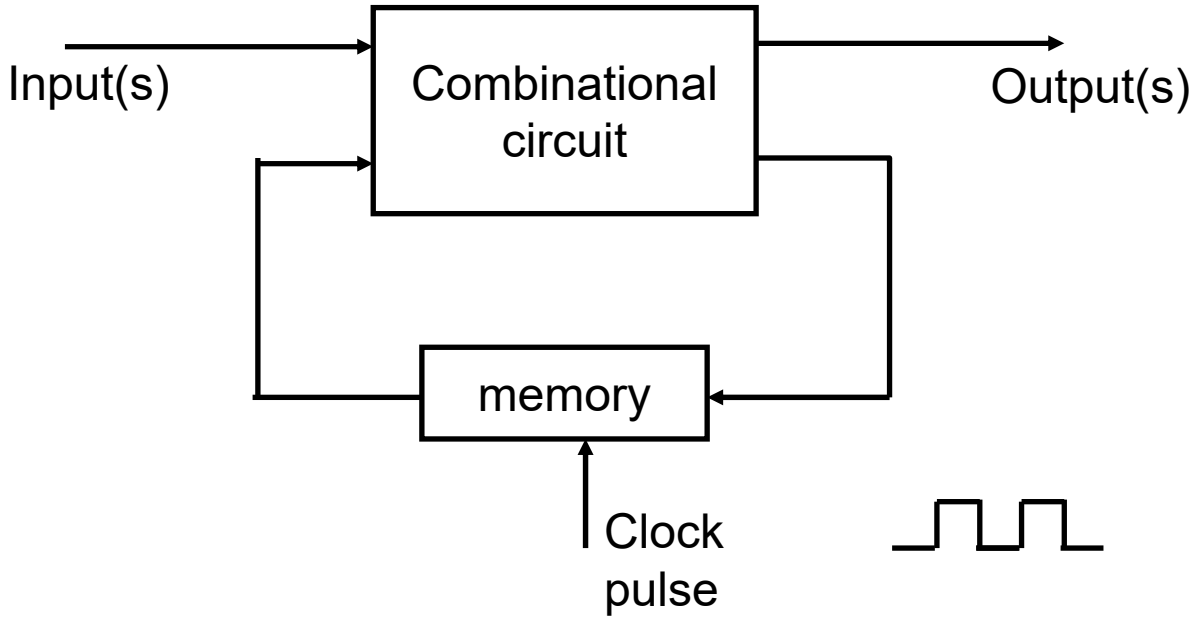
- To be able to differentiate between the various types of bistable circuits (and know when it is appropriate to use one type or another)
- To describe the structure and operation of simple registers, shift registers and binary counters
- To sketch and explain the features of a timing diagram for an n-bit register
- To generate a state transition diagram from the description of a problem, or to follow the flow of a given state transition diagram
- To apply the general sequential machine design method to sequential circuits such as counters

Sequential circuit concepts

The addition of a memory device to a combinational circuit allows the output to be fed back into the input:



Synchronous and Asynchronous

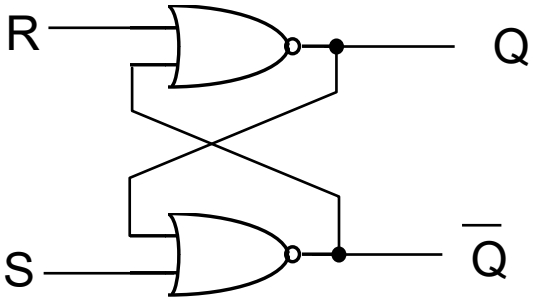


With synchronous circuits a clock pulse is used to regulate the feedback, input signal only enabled when clock pulse is high – acts like a "gate" being opened.

Latches and Flip Flops

- Latches (operate on signal levels)
  - SR latch
  - D Latch
- Flip flops (operate on clock transition)
  - Edge triggered D Flip-flop
  - JK Flip Flop
  - T Flip Flop

SR Latch



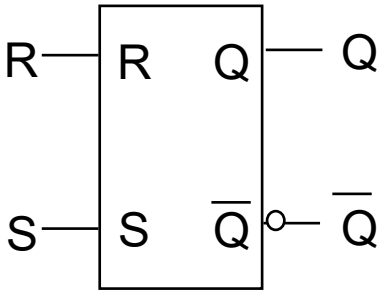
SR Latch with NOR gates

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	?

n+1 represents output at some future time

n represents current output.

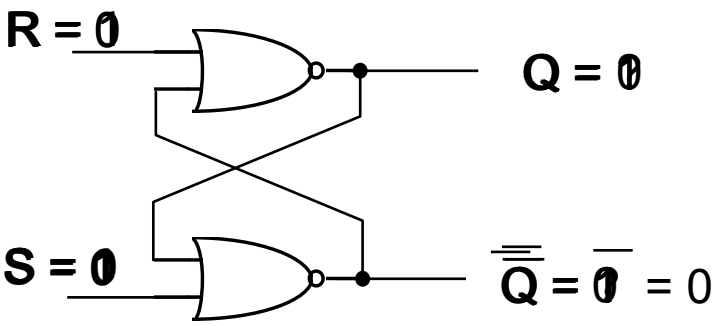
Function Table



Symbol

SR Latch operation

- Assume some previous operation has Q as a 1
- Assume R and S are initially inactive



SR Latch Circuit

Indicates a stable state at some future time (n+ = now plus)

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	?

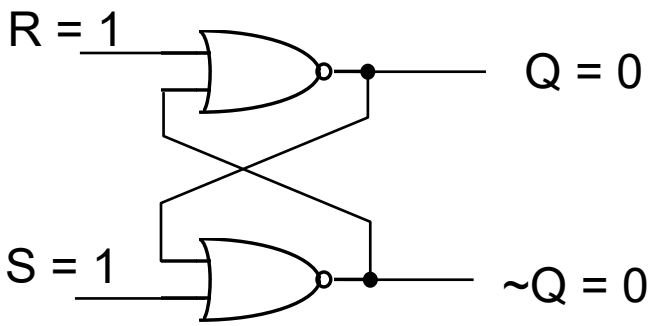
~Q = $\overline{Q}$, i.e. is the complement of Q.

Now assume R goes first to 1 then returns to 0, what happens:

Race Condition

Similar sequences can be followed to show that setting S to 1 then 0 – activating S – will set Q to a 1 stable state.

When R and S are activated simultaneously both outputs will go to a 0



When R and S now go inactive 0, both inputs at both gates are 0 and both gates output a 1.

This 1 fed back to the inputs drives the outputs to 0, again both inputs are 0 and so on and so on and so on and so on.

Metastable state

- In a perfect world of perfect electronic circuits the oscillation continues indefinitely.

- However, delays will not be consistent in both gates so the circuit will collapse into one stable state or another.

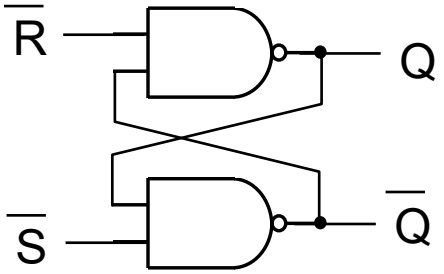
This collapse is unpredictable.

Thus our function table:

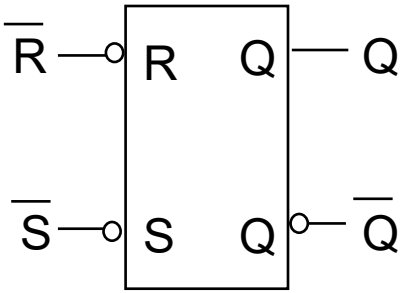
R	S	Q_{n+1}	
0	0	Q_n	Future output = present output
0	1	1	Set the latch
1	0	0	Reset the latch
1	1	?	Don't know

SR Latch

NAND Form of SR Latch produces similar result from inverted inputs



Circuit



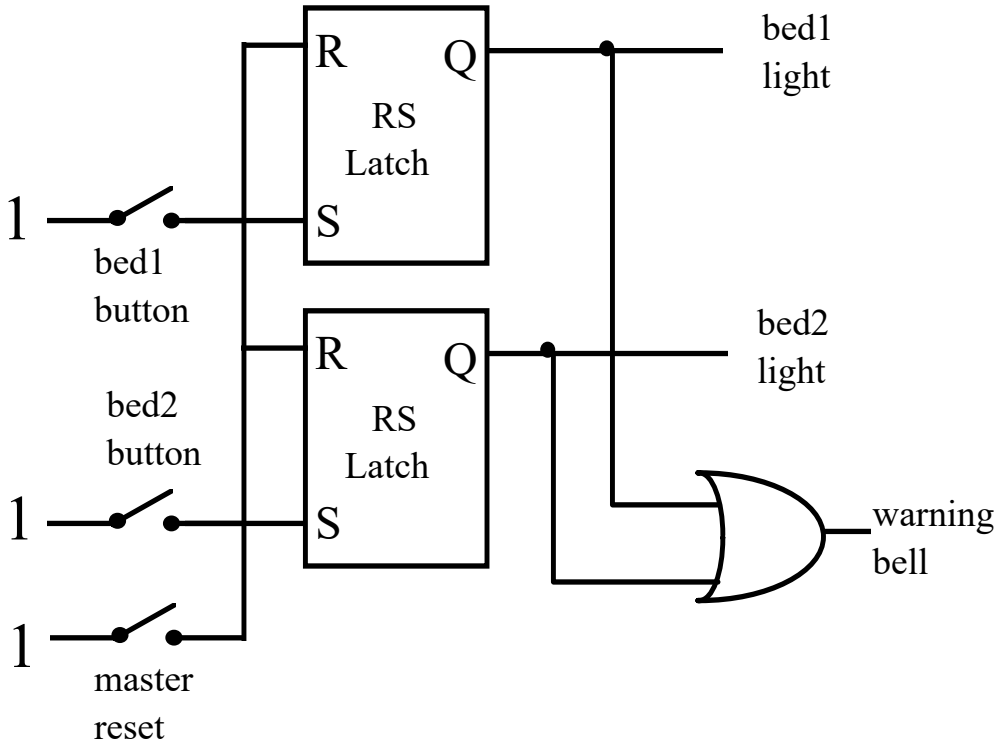
Symbol

$\overline{R}$	$\overline{S}$	Q_{n+1}
0	0	?
0	1	0
1	0	1
1	1	Q_n

Function Table

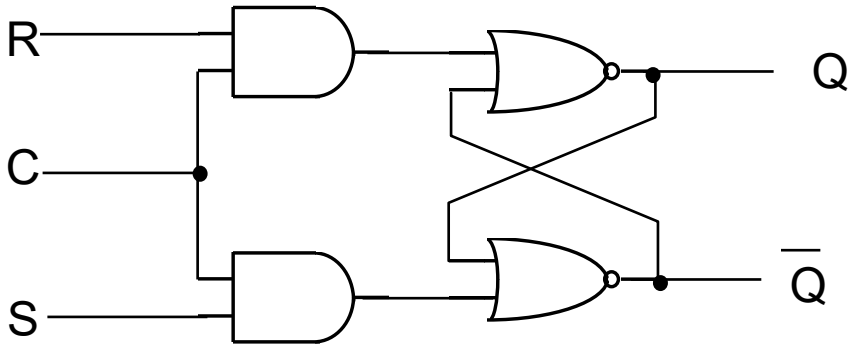
Application of the SR Latch

- An important application of SR latches is for recording short lived events
  - e.g. pressing an alarm bell in a hospital

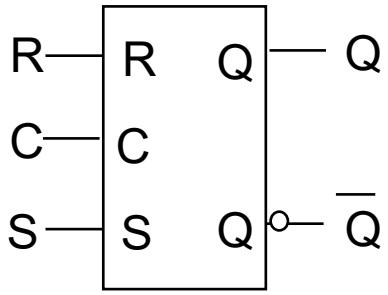


Clocked SR Latch

- In some cases it is necessary to disable the inputs to a latch
- This can be achieved by adding a **control** or **clock** input to the latch
  - When C = 0, R and S inputs cannot reach the latch
    - Holds its stored value
  - When C = 1, R and S inputs connected to the latch
    - Functions as before



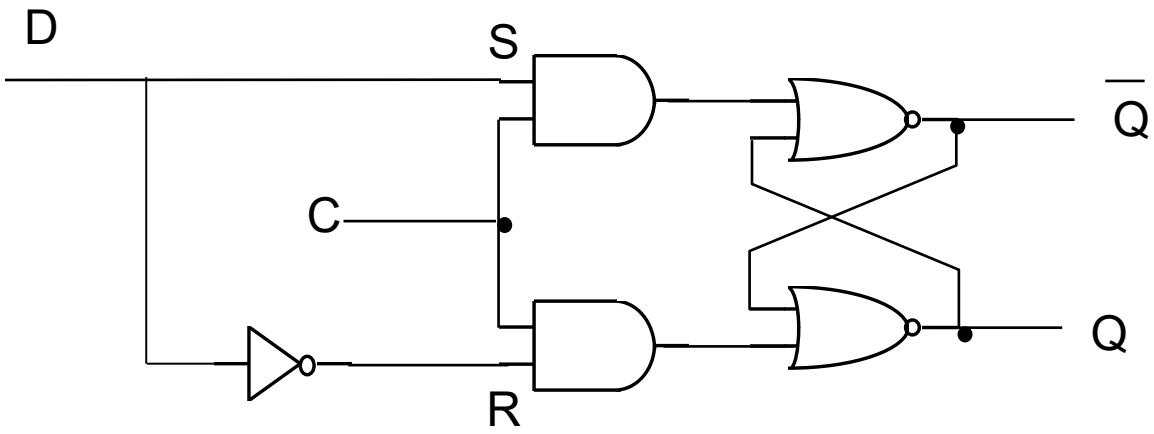
Clocked SR Latch



R	S	C	Q_{n+1}	
X	X	0	Q_n	Hold
0	0	1	Q_n	Hold
0	1	1	1	Set
1	0	1	0	Reset
1	1	1	?	Indeterminate

Clocked D Latch

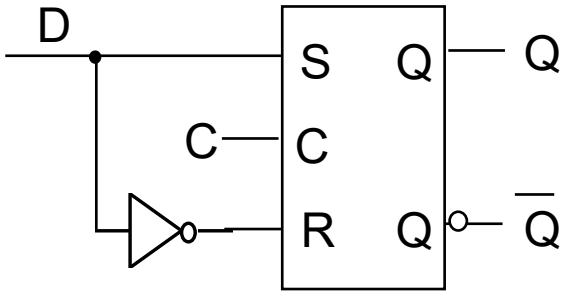
Simplest clocked latch of practical importance is the Clocked **D latch**



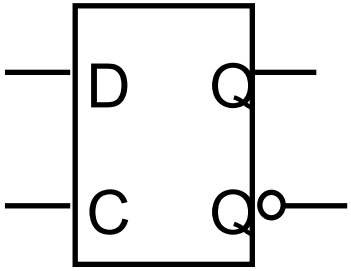
- It means that both active 1 inputs at R and S can't occur.
- Notice we've reversed S and R so when D is 1 Q is 1.

D Latch

- It removes the undefined behaviour of the SR latch
- Often used as a basic memory element for the short term storage of a binary digit applied to its input
- Symbols are often labeled data and enable/clock (D and C)



Circuit



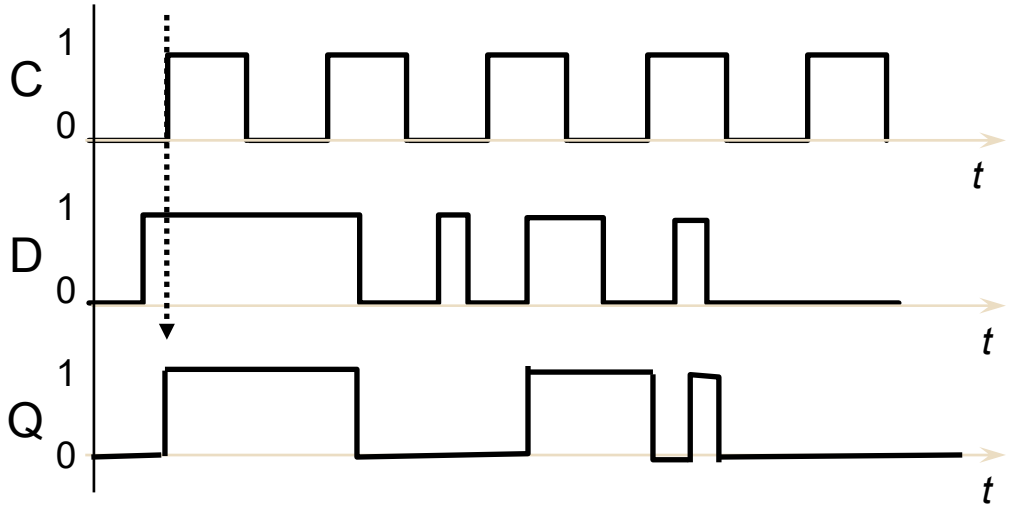
Symbol

D	C	Q_{n+1}	
X	0	Q_n	Hold
0	1	0	Reset
1	1	1	Set

Function Table

Transparency

- The devices that we have looked so far are transparent
  - That is when C = 1 the output follows the input
  - There will be a slight lag between them



When the clock "gate" opens, changes in input take effect at outputs – transparency. Also known as "level-triggered".

Propagation Delay, Setup and Hold time (for transparent circuits)

- Propagation delay:

Time taken for any change at inputs to affect outputs (change on D to change on Q).

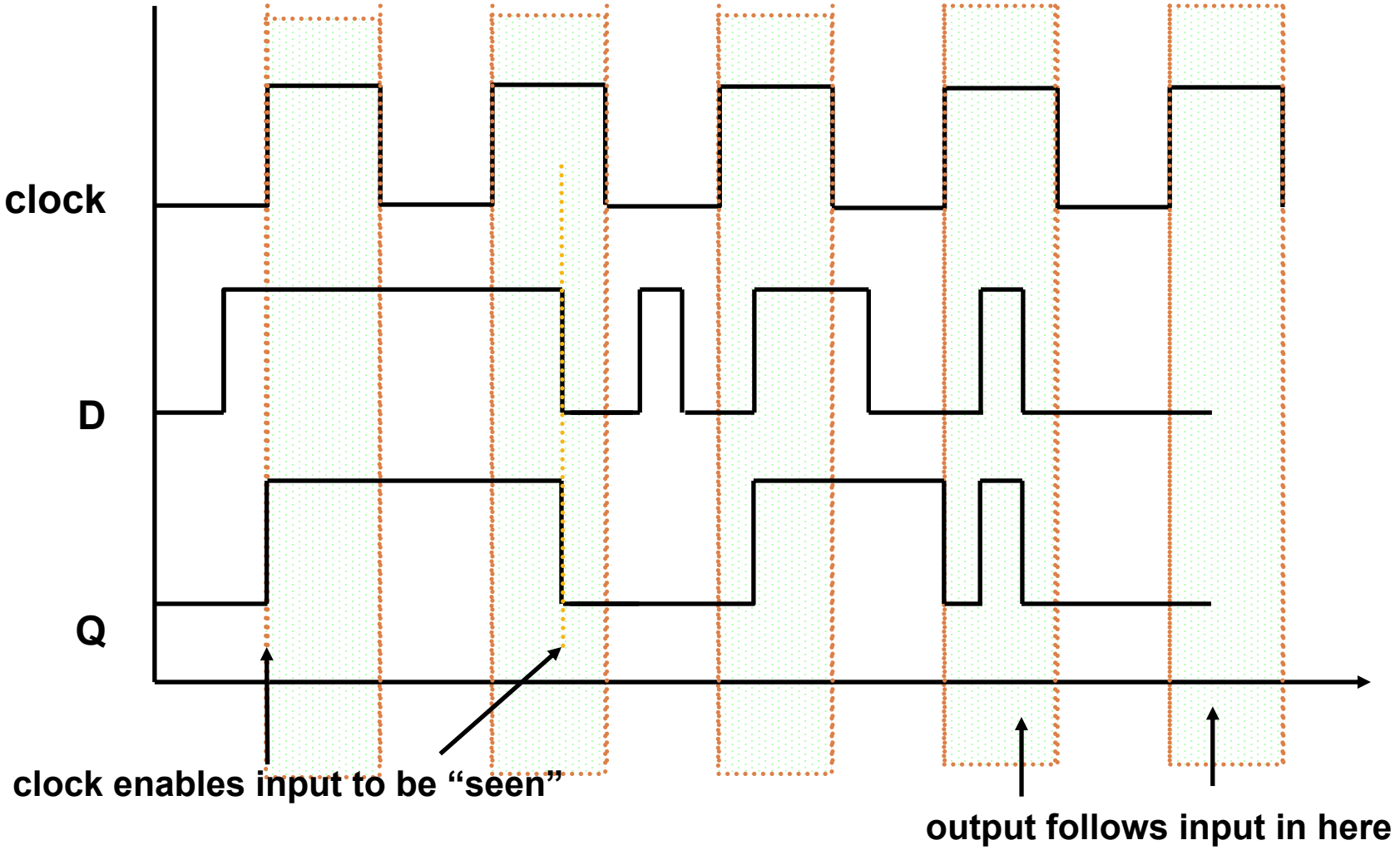
- Setup time:

Data on inputs D must be held steady for at least this time before the clock changes.

- Hold time:

Data on inputs D must be held steady for at least this time after the clock changes.

Clocked D Latch – Timing Diagram



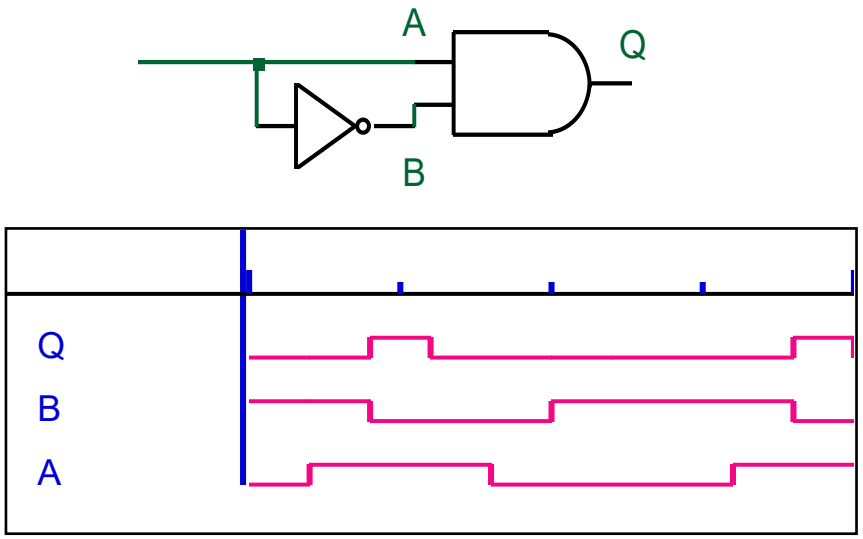
Latches - Summary

- Two cross-coupled NOR gates form an SR (set and reset) latch
- A clocked SR latch has an additional input that controls when setting and resetting can take place
- A D-latch has a single data input
  - the output is held when the clock input is a zero
  - the input is copied to the output when the clock input is a one
- The output of the clocked latches is transparent
- The output of the clocked D latch can be represented by the following behavior

D	C	Q_{n+1}	
X	0	Q_n	Hold
0	1	0	Reset
1	1	1	Set

Propagation Delay

Will the output of the following circuit ever be a 1?



The brief pulse or **glitch** in the output is caused by the propagation delay of the signals through the gates

Latches and Flip Flops

- Terms are sometimes used confusingly
- A latch is not clocked whereas a flip-flop is clocked.
- A clocked latch can therefore equally be referred to as a flip flop (SR flip flop, D flip flop).
- **However, as we shall see, all practical flip flops are edge-triggered on the clock pulse.**

Latches Vs Flip Flops

- Clocked latches are level triggered. While the clock is high, inputs and thus outputs can change.
- This is not always desirable.
- A Flip Flop is edge-triggered – either by the leading or falling edge of the clock pulse.
- Ideally, it responds to the inputs only at a particular instant in time.
- It is not transparent.