DIGITAL SYSTEMS AND MICROPROCESSORS (ELE2002M)

LECTURE - 8

SEQUENTIAL LOGIC – FLIP FLOPS

Instructor:

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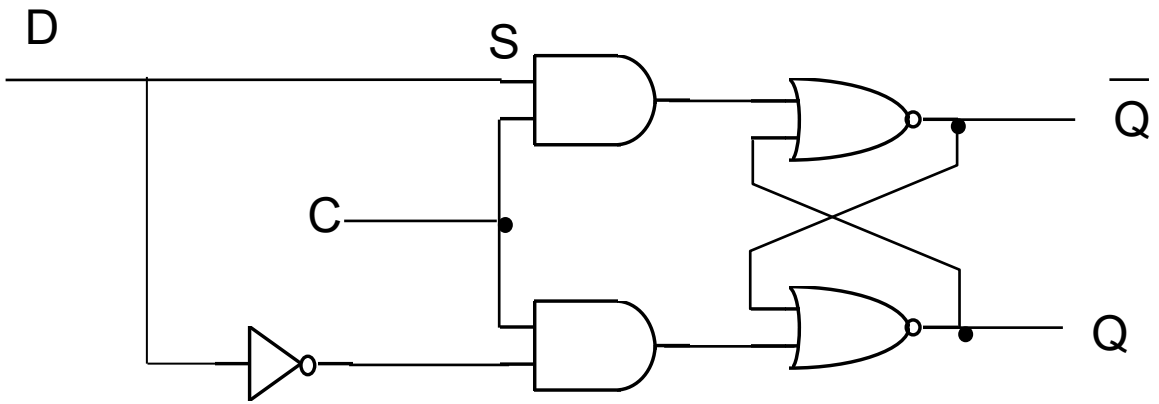
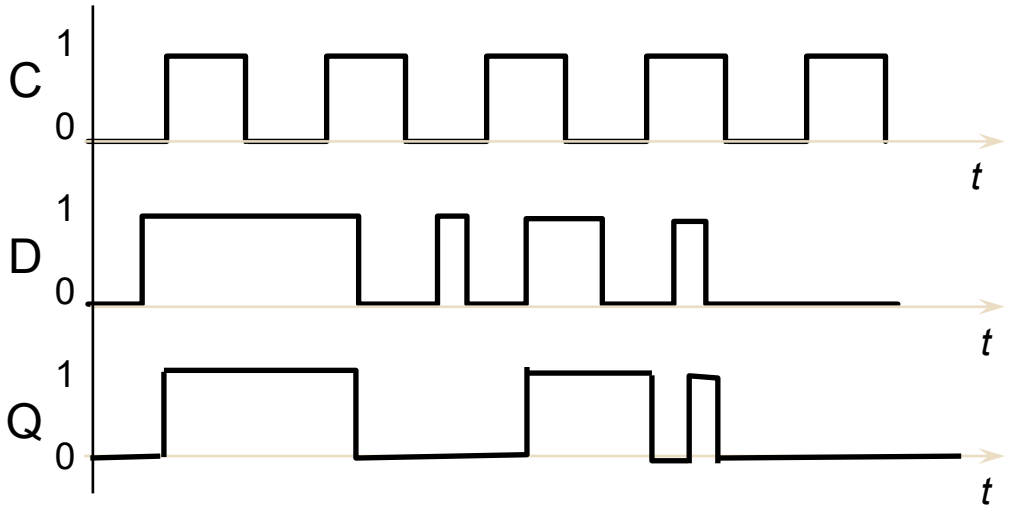
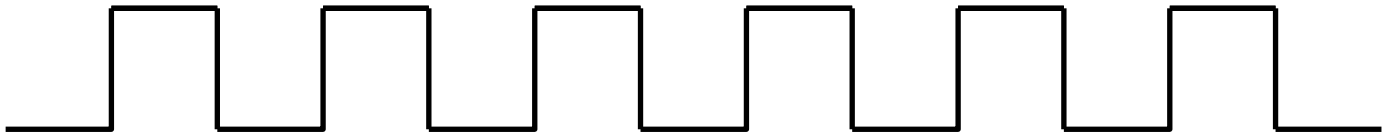
D-type Latch – Timing Review



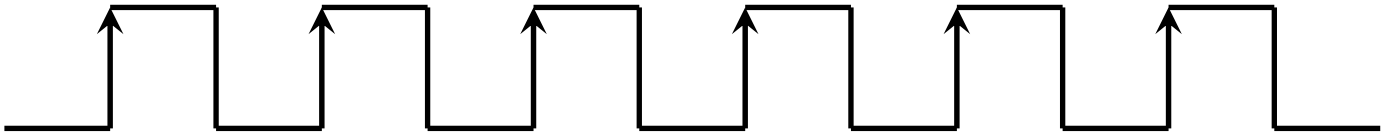
The high part represents active 1, the low part active 0.



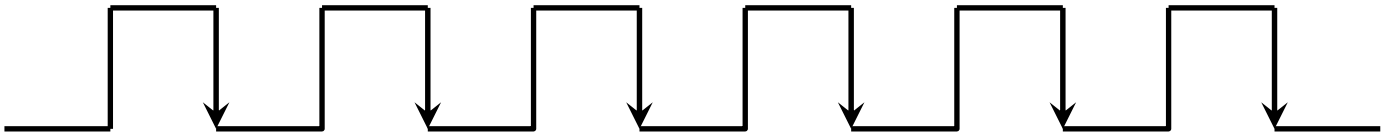
Clock Response in Latch and FFs



(a) Response to positive level

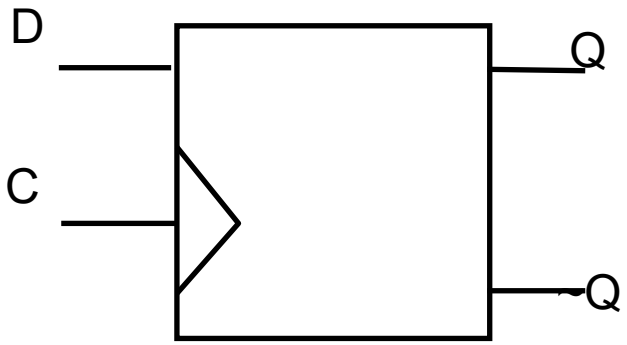


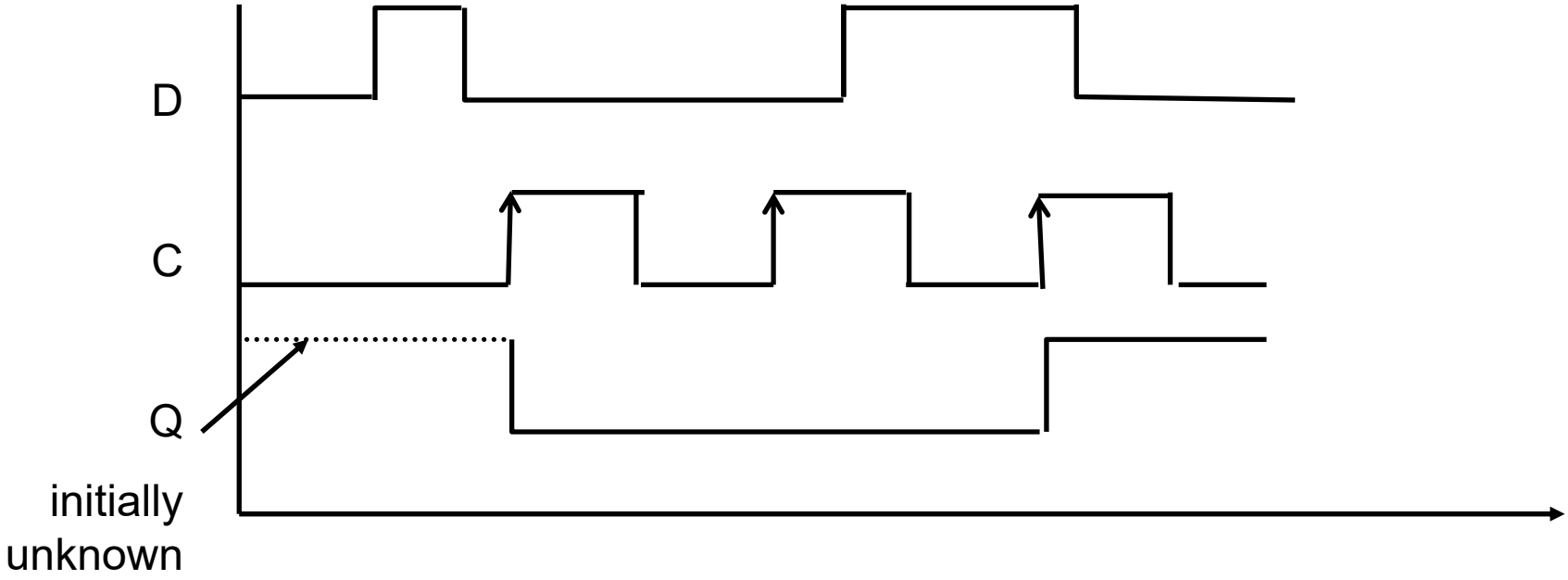
(b) Positive-edge response



(c) Negative-edge response

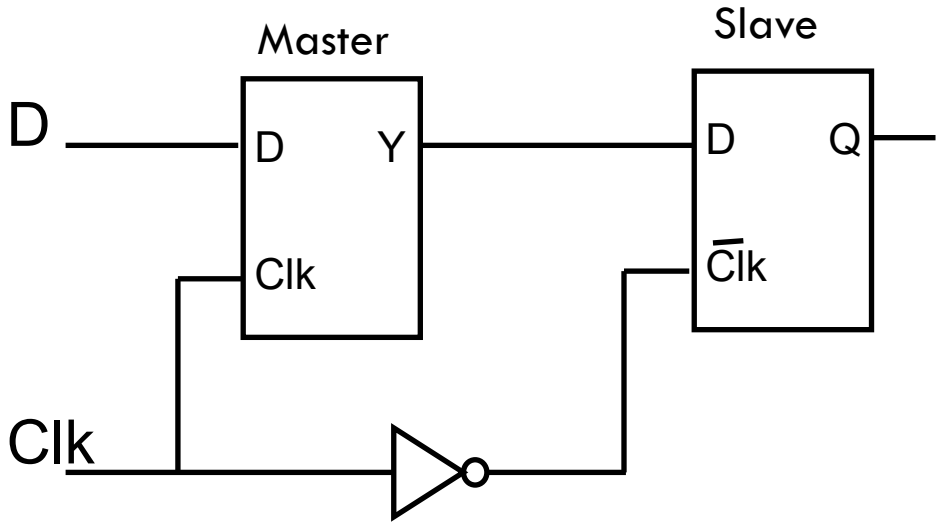
Positive edge-triggered D Flip-flop Timing





Master Slave D Flip-flop

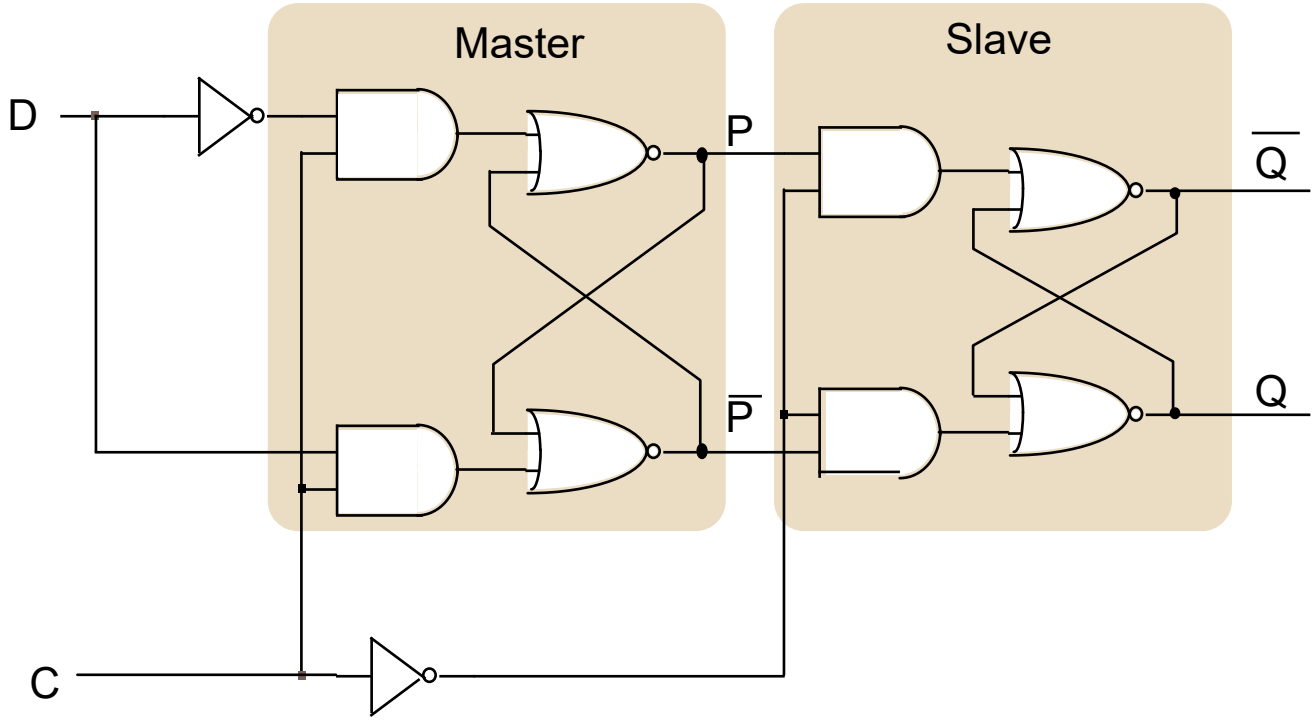
A negative edge triggered flip-flop using D-latches



On the negative edge of the clock, the master captures the D input and the slave outputs it.

A master-slave Flip-flop

No matter how long the clock pulse, both circuits cannot be active at the same time.

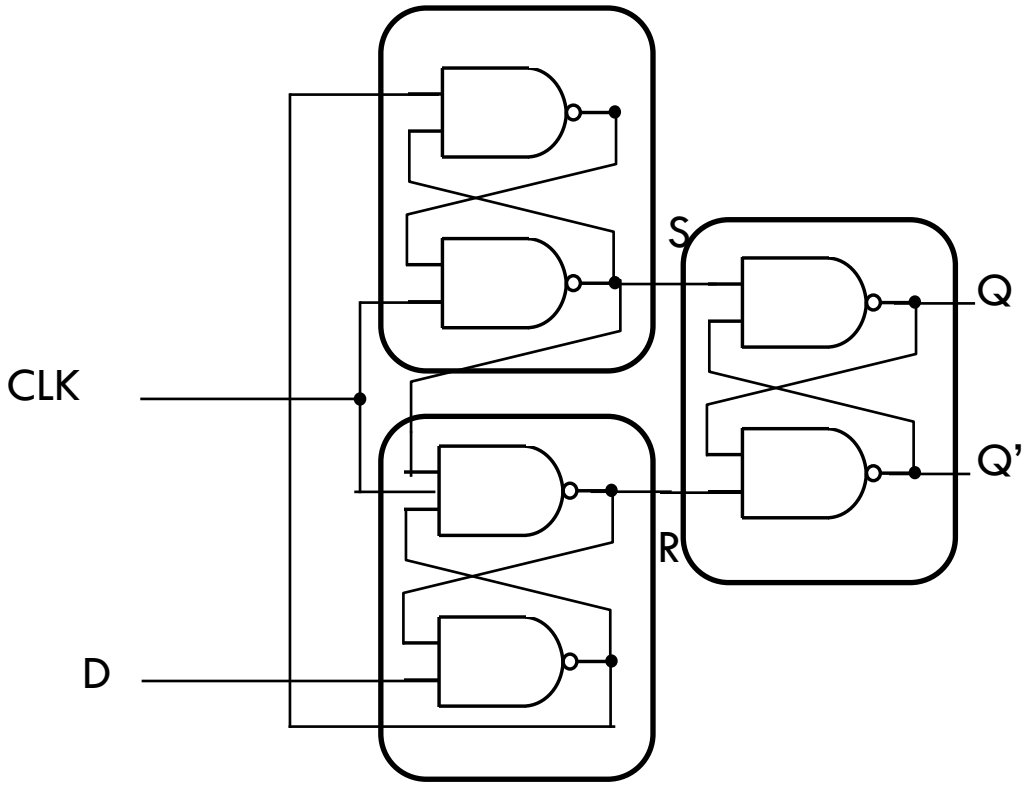


When C = 1 output of master (P) follows D input and because of inverted C input output of master unable to influence output of slave

When C = 1->0 master slave output influenced by master output - note masters inputs disabled at this time (i.e. Value of D just before negative clock edge copied to Q output - a negative edge triggered device)

Because of master-slave behavior transparency removed

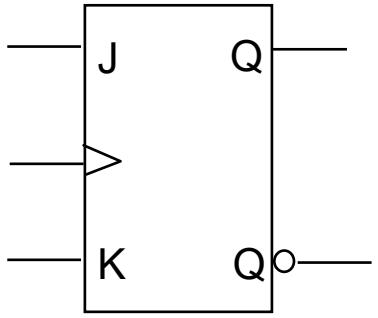
D-type Positive Edge Triggered Flip-flop



The most economical flip-flop - uses fewest gates

JK Flip-flop

- The most versatile of the flip-flops
- Has two data inputs (J and K)
- Do not have an undefined state like SR flip-flops
  - When J & K both equal 1 the output toggles on the active clock edge
- Most JK flip-flops based on the edge-triggered principle

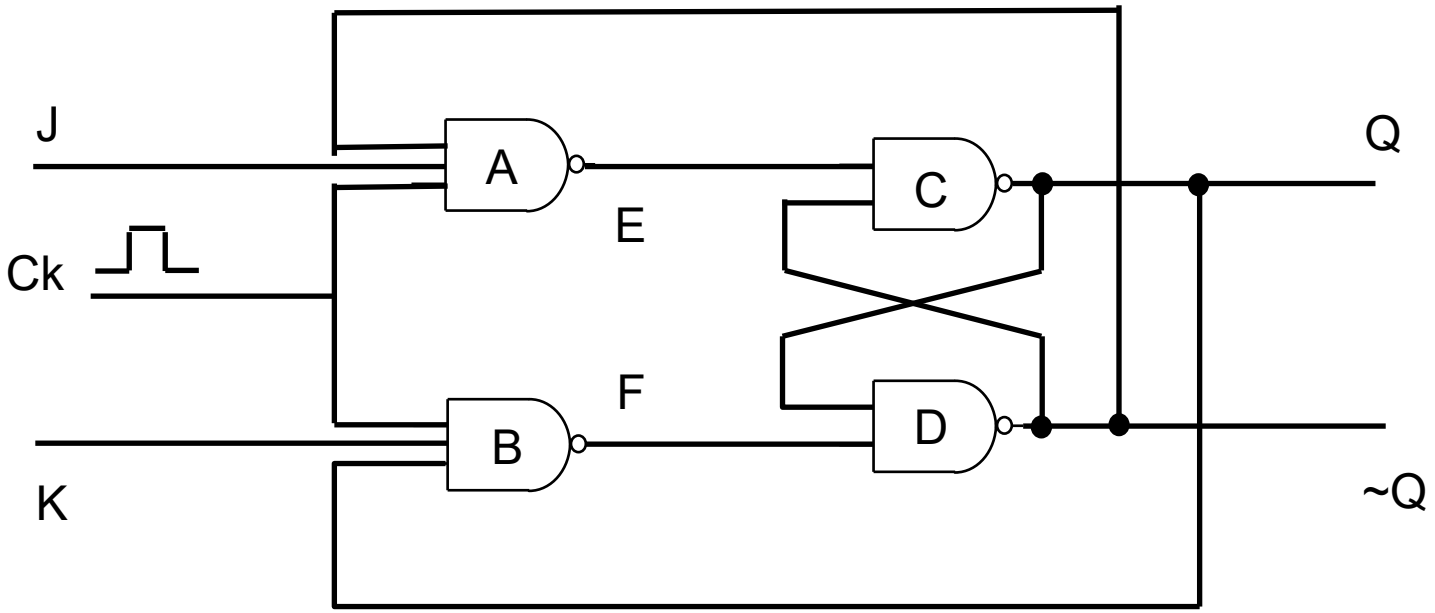


+ve edge triggered JK flip-flop

The C column indicates +ve edge triggering (usually omitted)

J	K	C	Q_{n+1}	
0	0		Q_n	Hold
0	1		0	Reset
1	0		1	Set
1	1		Q_n	Toggle
X	X	X	Q_n	Hold

Example JK circuit

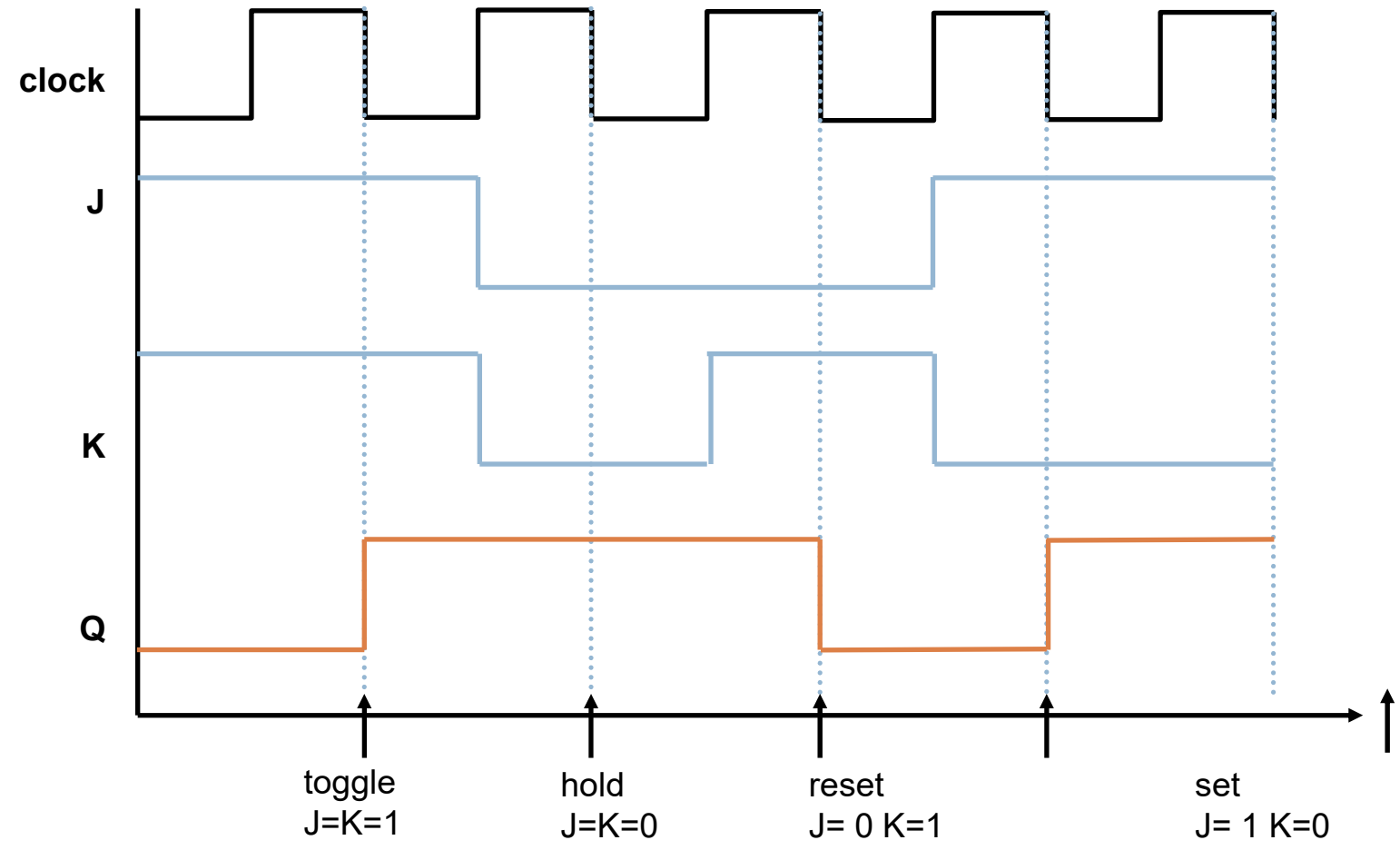


- Assume Q = 0, ~Q = 1, K = 1
- Gate B is disabled (Q = 0, F = 1)
- Make J = 1 to change circuit, when Ck = 1, all inputs to A = 1, E goes to 0, makes Q = 1
- Now Q and F are both 1 so ~Q = 0 and the circuit has toggled.

J	K	C	Q_{n+1}	
0	0		Q_n	Hold
0	1		0	Reset
1	0		1	Set
1	1		$\overline{Q_n}$	Toggle
X	X	X	Q_n	Hold

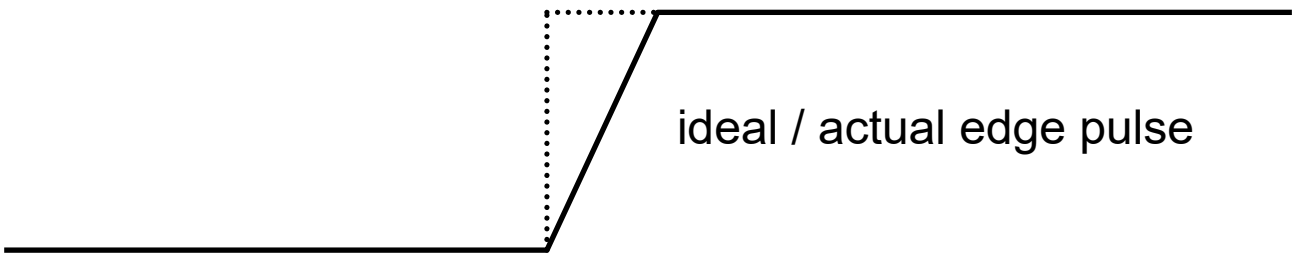
Timing diagram for JK Flip-flop

Negative Edge Triggered

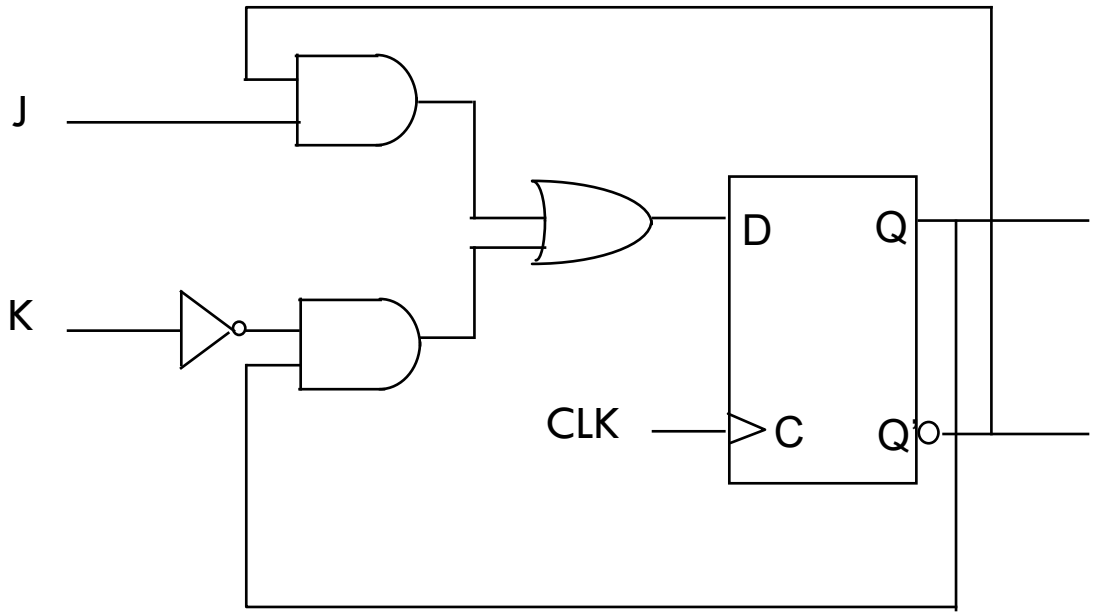


Clock Pulse

- The JK flip flop seems to solve all the problems associated with both inputs at 1.
- However the clock rise/fall is of finite duration.
- If the clock pulse takes long enough, the circuit can toggle.
- For the JK flip flop it is assumed the pulse is quick enough for the circuit to change only once.



JK from D Flip-flop

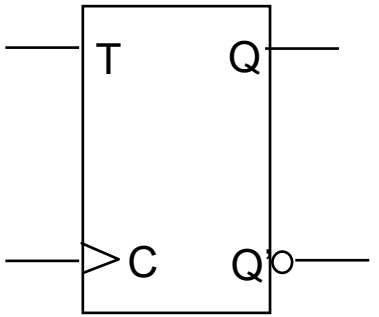


T Flip Flop (Toggle)

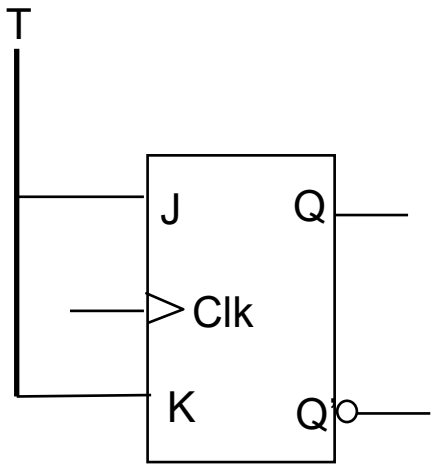
J	K	Q_{n+1}	
0	0	Q_n	Hold
0	1	0	Reset
1	0	1	Set
1	1	Q_n	Toggle

D	Q_{n+1}	
0	0	Reset
1	1	Set

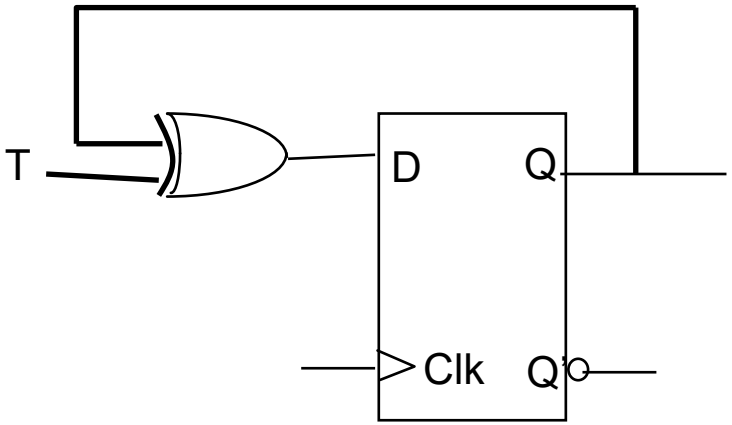
T	Q_{n+1}	
0	Q_n	Reset
1	Q'_n	Set



T Flip Flop from JK and DFF



(a) From JK Flip Flop



(a) From D Flip Flop

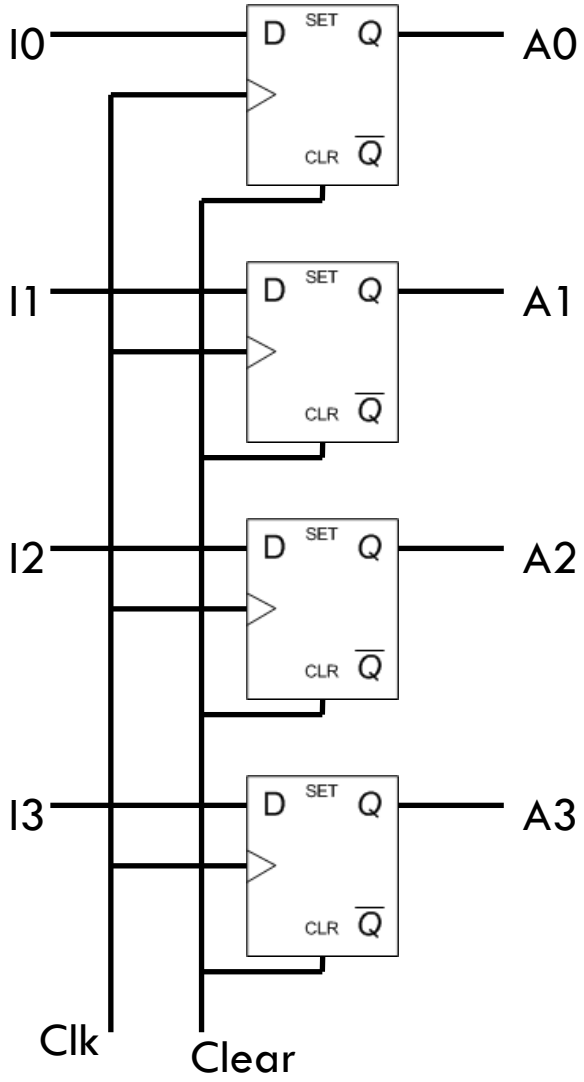
Summary of Flip Flops

- Flip flops are circuits controlled by a clock.
- Triggered on the edge of the pulse to avoid races with both inputs at 1 during the clock pulse.
- Because modern IC's have a small propagation delay races can still occur.
- The master-slave configuration solves this problem by having only master or slave active at any one time.

What you should be able to do

- Explain the difference between combinational and sequential circuits
- Explain the basic operation of SR and D latches.
- Explain the operation of SR and JK flip flops.
- Explain the operation of master-slave flip flops.
- Draw simple timing diagrams for clocked latches and edge-triggered flip flops.
- Define setup and hold times for a transparent latch.

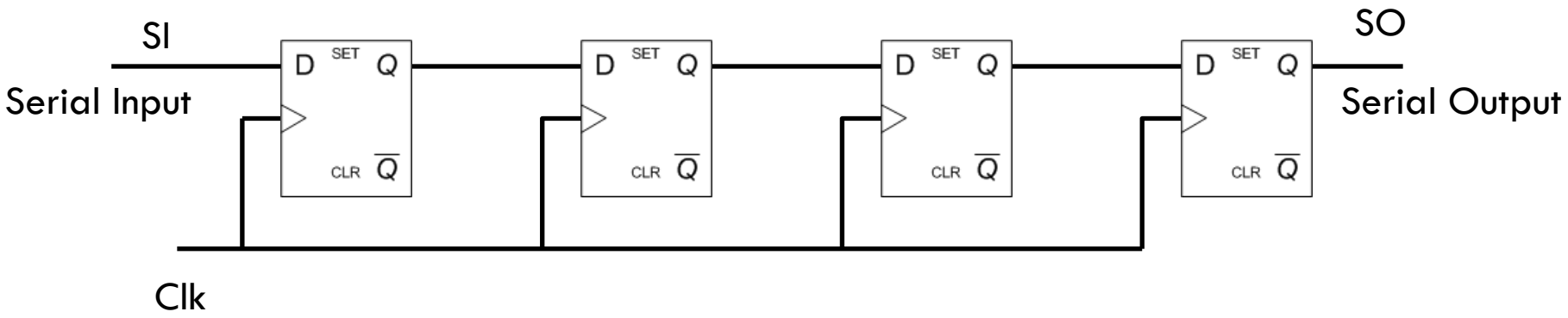
Registers



Parallel Loading

Shift Registers

Serial Input – Serial Output



Counters

Ripple Counters