DIGITAL SYSTEMS AND MICROPROCESSORS (ELE2002M)

LECTURE 2 - GATE LEVEL MINIMIZATION

Instructor:

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Gate Level Minimisation

- Covered earlier
  - Sum of products
  - Boolean algebra
- This Lecture
  - Karnaugh maps
  - Some more examples of algebra and truth tables=

Karnaugh Maps

- K-Maps are a convenient way to simplify Boolean Expressions.
- They can be used for up to 4 or 5 variables.
- They are a visual representation of a truth table.
- Expression are most commonly expressed in sum of products form.

K-map revision

Simplify the Boolean Expression:

$F(w,x,y,z) = \sum (1,3,7,11,15)$

Which has don't care conditions

$D(w,x,y,z) = \sum (0,2,5)$

Solution

K-map revision

$F(w,x,y,z) = \sum (1,3,10) + \sum_d (0,2,8,12)$

Simplified expression for F = ?

Solution

De Morgan again

- A NAND gate:

$$Y = \overline{A.B} = \overline{A} + \overline{B}$$

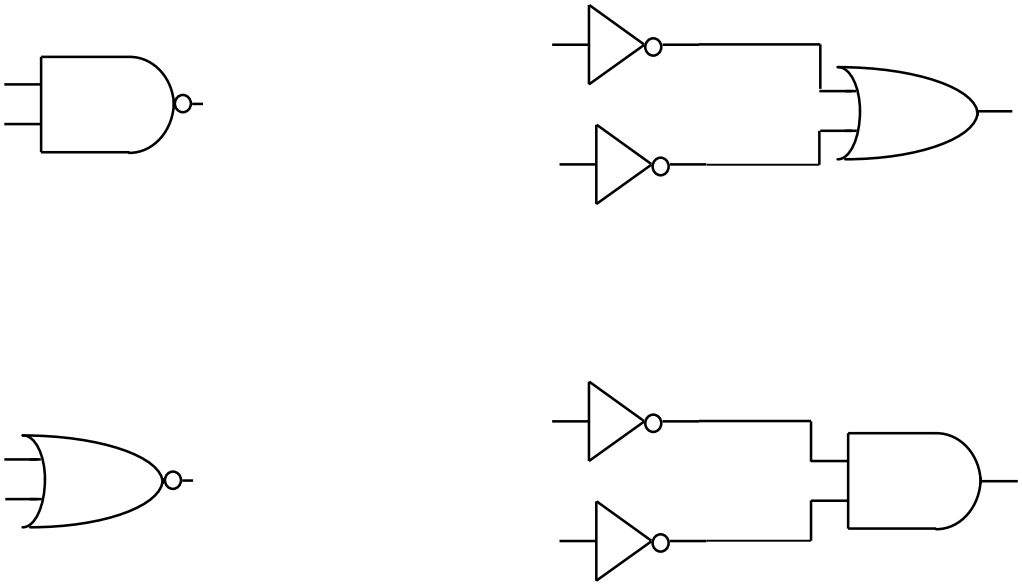
is the same as an OR gate with two NOT gates

- Similarly a NOR gate is the same as an AND gate with two inverters

$$Y = \overline{A + B} = \overline{A}.\overline{B}$$

- not the individual terms
- change the sign
- not the lot

Dual gates

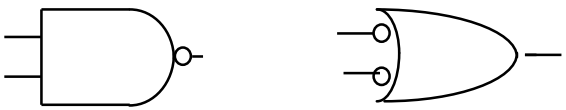


- **NOT the individual inputs**
- **Change the gate**
- **NOT the output**

Truth Tables and Boolean Notation

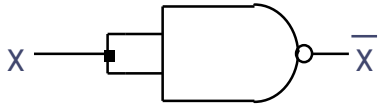
NAND Gate Representation

- It is possible to implement any Boolean expression using only NAND gates

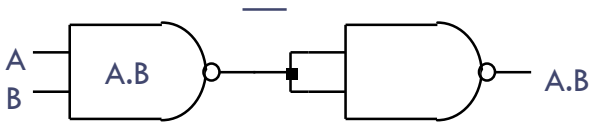


Two Graphic Symbols for NAND

NOT

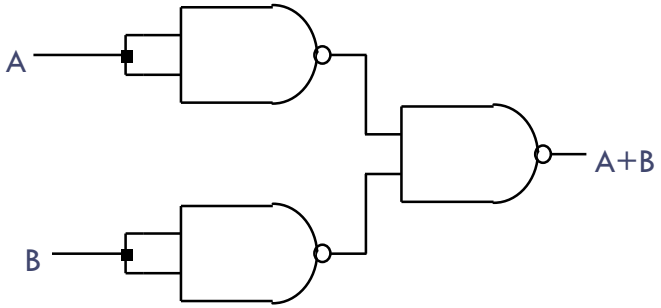


AND



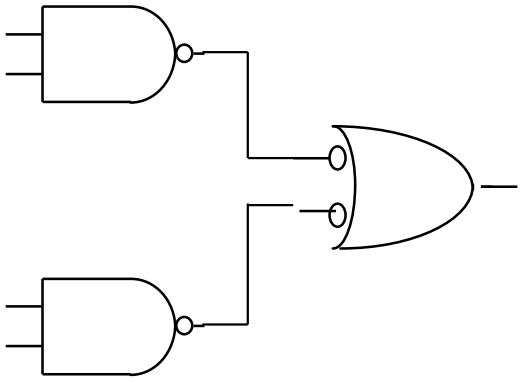
OR

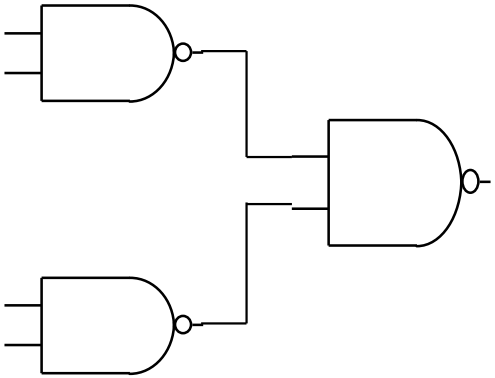
$$A + B = \overline{\overline{A}.\overline{B}}$$



Two Level Implementation using NAND

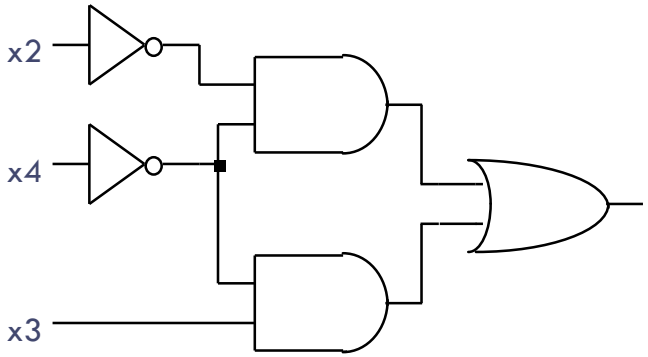
F = AB + CD





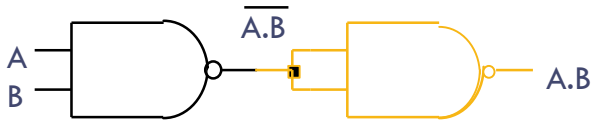
Truth Tables and Boolean Notation

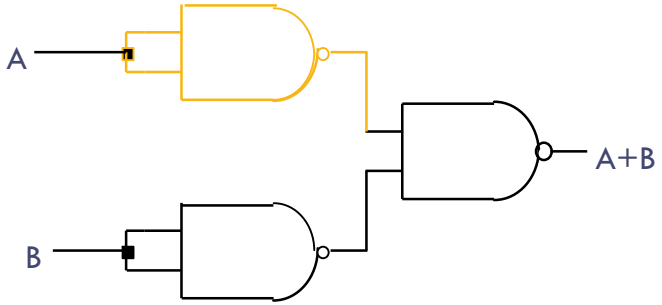
- NAND Gate representation
  - Implement the following circuit using only NAND gates

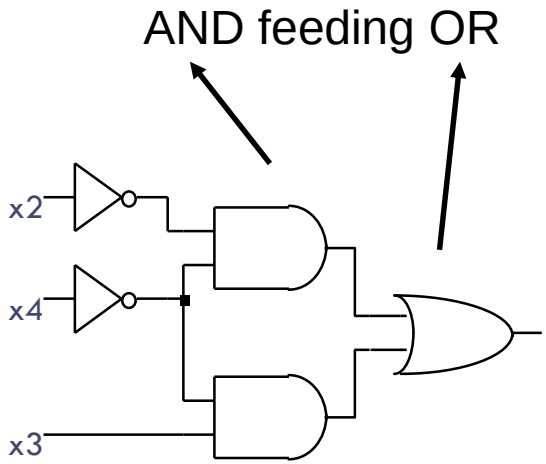


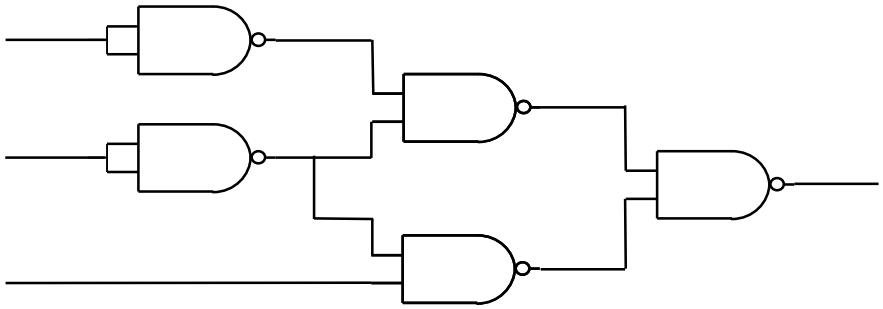
Solution

- Dual the gates, remember two NOTs together can be removed.









Example

Implement the following Boolean function using NAND gates

$F(x,y,z) = \sum (1,2,3,4,5,7)$

First reduce using K-map

F =

Multi-level NAND Gates

General Procedure for converting a multi-level AND-OR diagram into all-NAND diagram:

1. Convert all AND gates to NAND gates with AND-Invert symbol
2. Convert all OR gates to NAND gates with invert-OR symbol
3. Check all bubbles in the diagram. For each bubble that is not compensated by another circle along same line, insert an inverter (a one-input NAND gate) or complement the input literal.

Multi Level NAND Example

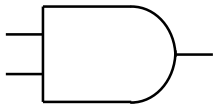
F = (AB’ + A’B) (C+D)

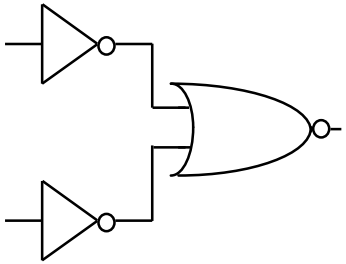
Solution

NOR Gates

- Implement NOT, AND and OR using NOR gates

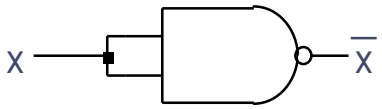
- Example AND gate dual circuit:



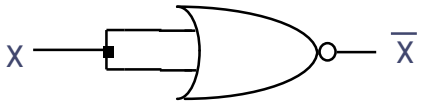


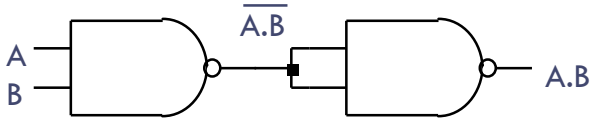
Solution

- Similar pattern to using NAND gates (not surprising)

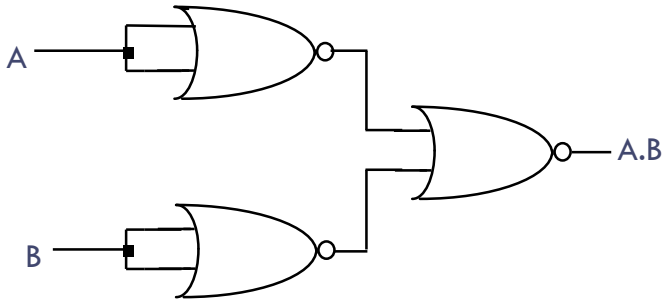


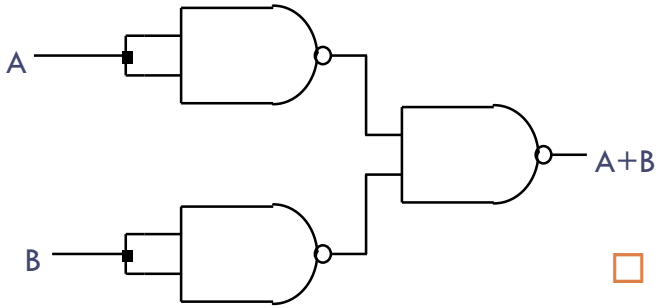
- NOT



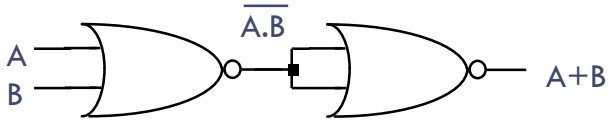


- AND





- OR



Homework Exercise

- NOR Gate representation
  - It is also possible to implement any Boolean expression using only NOR gates
  - Implement the following circuit using only NOR gates