DIGITAL SYSTEMS AND MICROPROCESSORS (ELE2002M)

LECTURE 5 - COMBINATIONAL LOGIC CONT…

Instructor:

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What we have covered so far?

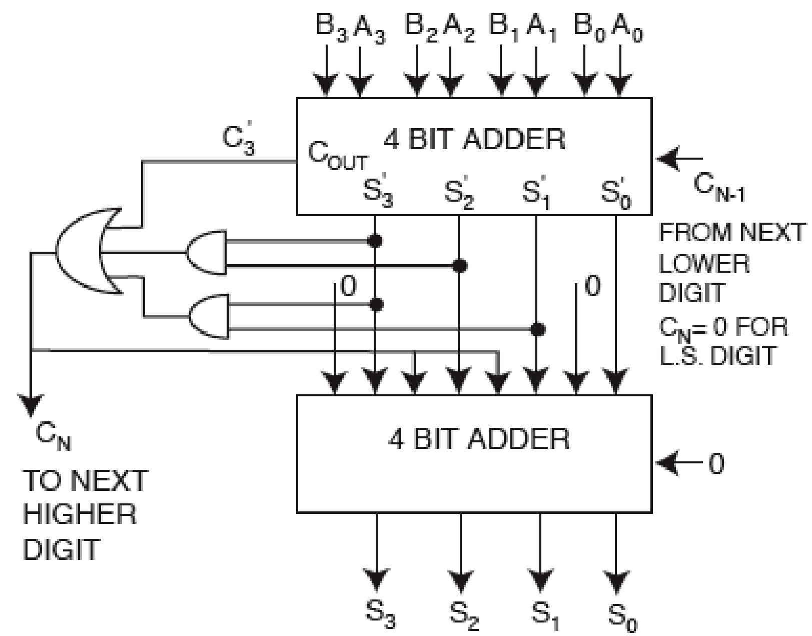
- Half Adders
- Full Adders
- Binary Adders (for multi-digit binary numbers)
- Half Subtractor
- Full Subtractor
- Binary Subtractor
- Adder-Subtractor Unit

Decimal Adder

Decimal		Binary Sum						BCD Sum				
		C3’	S3’	S2’	S1’	S0’		Cout	S3	S2	S1	S0
0		0	0	0	0	0		0	0	0	0	0
1		0	0	0	0	1		0	0	0	0	1
2		0	0	0	1	0		0	0	0	1	0
3		0	0	0	1	1		0	0	0	1	1
4		0	0	1	0	0		0	0	1	0	0
5		0	0	1	0	1		0	0	1	0	1
6		0	0	1	1	0		0	0	1	1	0
7		0	0	1	1	1		0	0	1	1	1
8		0	1	0	0	0		0	1	0	0	0
9		0	1	0	0	1		0	1	0	0	1
10		0	1	0	1	0		1	0	0	0	0
11		0	1	0	1	1		1	0	0	0	1
12		0	1	1	0	0		1	0	0	1	0
13		0	1	1	0	1		1	0	0	1	1
14		0	1	1	1	0		1	0	1	0	0
15		0	1	1	1	1		1	0	1	0	1
16		1	0	0	0	0		1	0	1	1	0
17		1	0	0	0	1		1	0	1	1	1
18		1	0	0	1	0		1	1	0	0	0
19		1	0	0	1	1		1	1	0	0	1

Decimal (BCD) Adder

- $C = C_3' + S_3S_2 + S_3S_1$



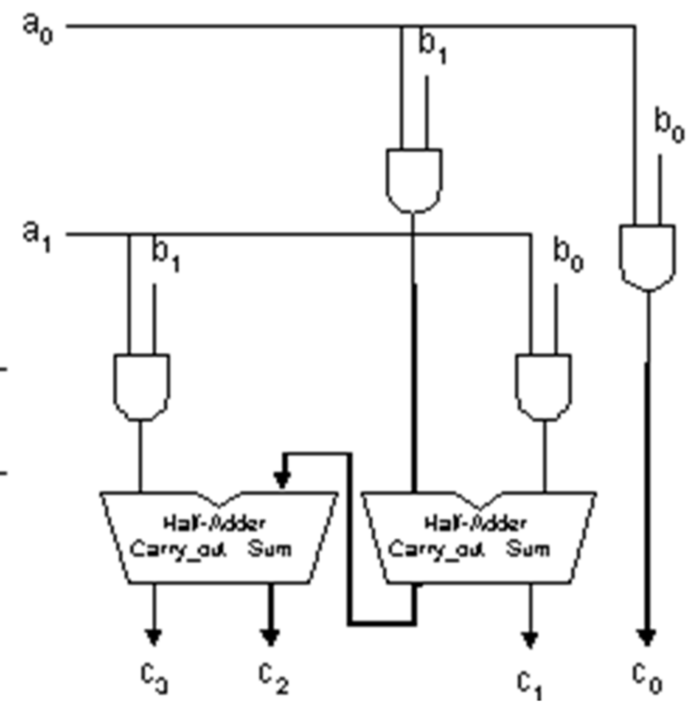
Binary Multiplier

- Work same way as multiplication of binary numbers.
- Multiplicand is multiplied by each bit of the multiplier
- Each multiplication forms a partial product
- Successive partial products are shifted one position to the left.
- Final product Is obtained from the sum of the partial products.

- Example:

  2-bit binary multiplication

$$
\begin{array}{ccccc}
 & & & b_1 & b_0 \\
 & & \times & a_1 & a_0 \\
\hline
 & & & a_0b_1 & a_0b_0 \\
+ & & a_1b_1 & a_1b_0 & \\
\hline
c_3 & & c_2 & c_1 & c_0
\end{array}
$$



4x3 Binary Multiplier

- For J multiplier bits and K multiplicand bits we need
  - (JxK) AND gates
  - (J-1) K-bit adders
  - to produce J+K bits

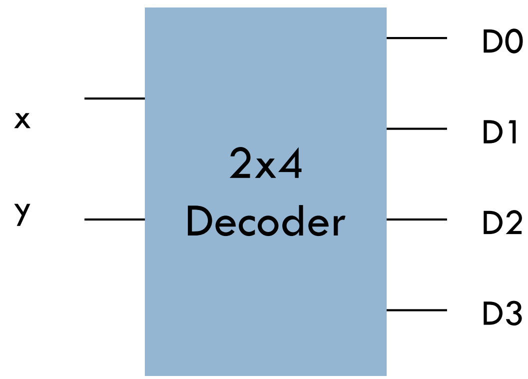
- Let multiplicand be $B = B_3B_2B_1B_0$
- Let multiplier be $A = A_2A_1A_0$

Comparator

- Compare two 4-bit binary numbers $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$
- Two numbers are equal if $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$, $A_0 = B_0$
- Let x_i be the XNOR function AiBi + Ai'Bi' for I = 0,1,2,3
- So x_i is 1only if the pair of bits at position i is equal (A=B).
- What about A>B and A<B?

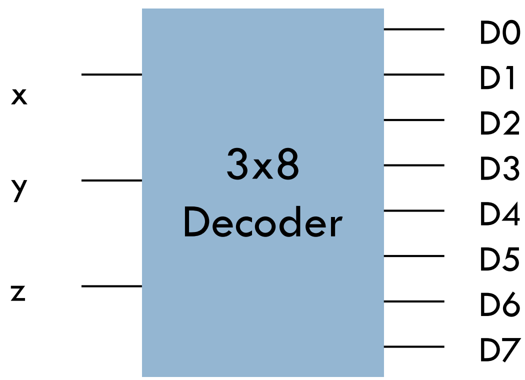
Decoder

- A n-bit binary code is capable of representing 2^n distinct elements of coded information.
- A decoder is a combinational circuit that converts binary information from n input lines to a *maximum* of 2^n outputs.
- A decoder presented here is called n-to-m-line decoder. Where $m <= 2^n$



Inputs			Outputs			
x	y		D0	D1	D2	D3
0	0		1	0	0	0
0	1		0	1	0	0
1	0		0	0	1	0
1	1		0	0	0	1

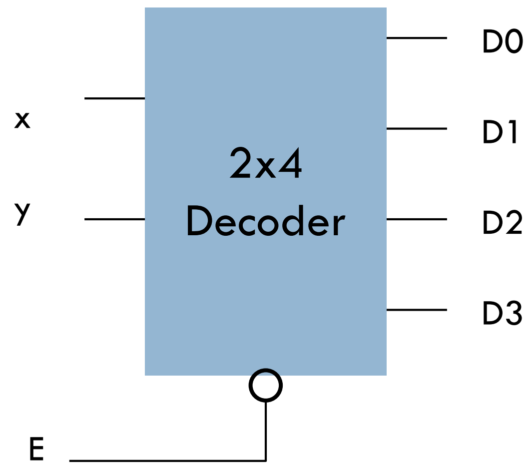
3x8 Decoder



Inputs				Outputs							
x	y	z		D0	D1	D2	D3	D4	D5	D6	D7
0	0	0		1	0	0	0	0	0	0	0
0	0	1		0	1	0	0	0	0	0	0
0	1	0		0	0	1	0	0	0	0	0
0	1	1		0	0	0	1	0	0	0	0
1	0	0		0	0	0	0	1	0	0	0
1	0	1		0	0	0	0	0	1	0	0
1	1	0		0	0	0	0	0	0	1	0
1	1	1		0	0	0	0	0	0	0	1

Complemented 2x4 Line Decoder

E	x	y		D0	D1	D2	D3
1	X	X		1	1	1	1
0	0	0		0	1	1	1
0	0	1		1	0	1	1
0	1	0		1	1	0	1
0	1	1		1	1	1	0



Combinational Logic Implementation

- Implement a Full adder using a 3x8 Decoder.

- Implement a 4x16 Decoder using 2 3x8 Decoders