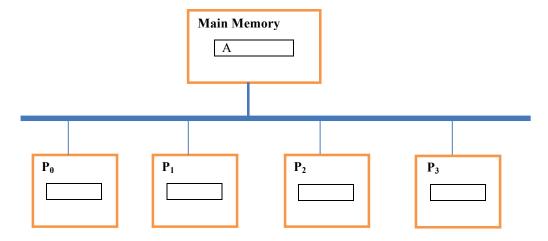
Name SUID#	
------------	--

CIS655/CSE661: Advanced Computer Architecture Mock Exam. Spring 2017

- 1. First, write down your name and SUID on the top of all pages.
- 2. Check the number of pages; if it is smaller than 14 pages, report.
- 3. Close the exam and wait until the exam starts.

Problem 1. [20 points] Cache Coherence

In a shared memory, a snooping protocol is implemented among four processors (P_0 , P_1 , P_2 , P_3). Consider just one memory block in this problem. Initially, the block is of value A.



(A)[10 points] Suppose the **MSI** protocol is being used, and the instruction sequence to access block is illustrated in the following table ordered in time. Fill the rest of table with the value and state (M, S or I) of the cached copy of block *right after* the instruction is being executed.

	Time	Instruction	CPU P ₀	P_1	P ₂	P ₃
,	t_0	P ₀ : read	S/A (means: state 'S' and value 'A')	NA (Not Applicable)	NA	NA
Time-line	t_1	P ₃ : write A'				
ne l	t_2	P ₁ : write A"				
	t ₃	P ₂ : read				

(B) [3 points] Suppose the **MESI** protocol is being used, and the instruction sequence to access block is illustrated in the following table ordered in time. Fill the rest of table with the value and state (M, E, S or I) of the cached copy of block *right after* the instruction is being executed.

Time-line	
e	

Time	Instruction	P ₀	P_1	P ₂	P ₃
t_0	P ₀ : read	E/A	NA	NA	NA
t_1	P ₃ : write A'				
t_2	P ₁ : write A"				
t_3	P ₂ : read				

Name SUID#

Problem 2. [20 points] Parallel Processing

A shared-memory system with two processors is executing the following two code fragments in parallel (one on each processor). All variables are shared and are initially zeros. The system uses sequential consistency.

Processor P0	Processor P1
A=10;	Btmp=B;
Atmp=A;	C=Btmp;
B=Atmp-2;	if(C==0)
while $(C==0)$;	C=3;
C=6;	A=3;
<pre>printf("%d %d %d\n",A,B,C);</pre>	

(A) [6 points] Is it possible for the printout in P0 to be "10 8 6". If yes, show the execution interleaving that produces this printout. If no, explain why not.

(B) [6 points] Is it possible for P0 to get stuck and never print out anything? If yes, show the execution interleaving that produces this situation. If no, explain why not.

Name	SUID#
------	-------

(C) [8 points] Is it possible for P0 to print 3 as the value of C? If yes, show the execution interleaving that produces this printout. If no, explain why not.

Problem 3. [20 points] Disks and RAID

A 6,000RPM disk drive has 5 double-surface platters, with 100,000 tracks per surface, 1,000 sectors per tracks, and 512 data bytes per sector. Each sector also has a 128-bit error detection code that can detect all errors in its sector but cannot correct any errors. The head can takes one microsecond (one millionth of a second) to move from one cylinder to an adjacent cylinder, and multi-cylinder movements are done at the same speed (one cylinder per microsecond). The disk controller is very fast (assume zero latency for everything it does) and the I/O bus has very large (assume infinite) bandwidth.

(A) [2 point] How many heads does the disk drive have?

Name	SUID#
------	-------

(B) [4 points] Assuming that the disk controller and the drive itself are not servicing any other requests, what is the worst-case time needed to read a sector from the disk?

Name	SUID#	
•		

Problem 5. [20 points] Single-choice questions

- 1. [1 point] Which cache write mechanism allows out of date data in the memory?
 - A) Write back
 - B) Write allocate
 - C) Write through
 - D) Non-write allocate
- 2. [1 point] Which of the following is TRUE for the WSC?
 - A) WSC is built upon a large number of high-end servers.
 - B) WSC is built upon a small number of low-end servers.
 - C) WSC is built upon a large number of low-end servers.
 - D) In WSC, local disk access is commonly faster than remote memory access.
- 3. [2 points] Which of the following statements is FALSE?
 - A) Memory-mapped IO maps device control registers directly to physical address space.
 - B) DMA can move data away from physical memory without CPU's involvement.
 - C) In disk IO, there are multiple data copies before the application can read the data.
 - D) In disk IO, polling outperforms interrupt.
- 4. [2 points] Which of the following statements is TRUE?
 - A) Cache coherence is about multiple memory locations.
 - B) Consistency is about one memory location.
 - C) MSI snoopy protocol requires 3 bits to store states for each memory block.
 - D) In the write-update cache coherence, there may be out-to-date cached copy.
 - E) None of the above is TRUE.
- 5. [1 point] For optimizing memory access, the size of the cache needs to be large and close to the processor.
 - A) True
 - B) False
- 6. [1 point] In a 32-bit address space, with 4K(4096) pages and a page table entry of 8 bytes, what is the page-table size?
 - A) 32 MB
 - B) 8 MB
 - C) 800 KB
 - D) 32 KB

Name	SUID#

Name	SUID#

Name	SUID#

Name	SUID#

Name	SUID#