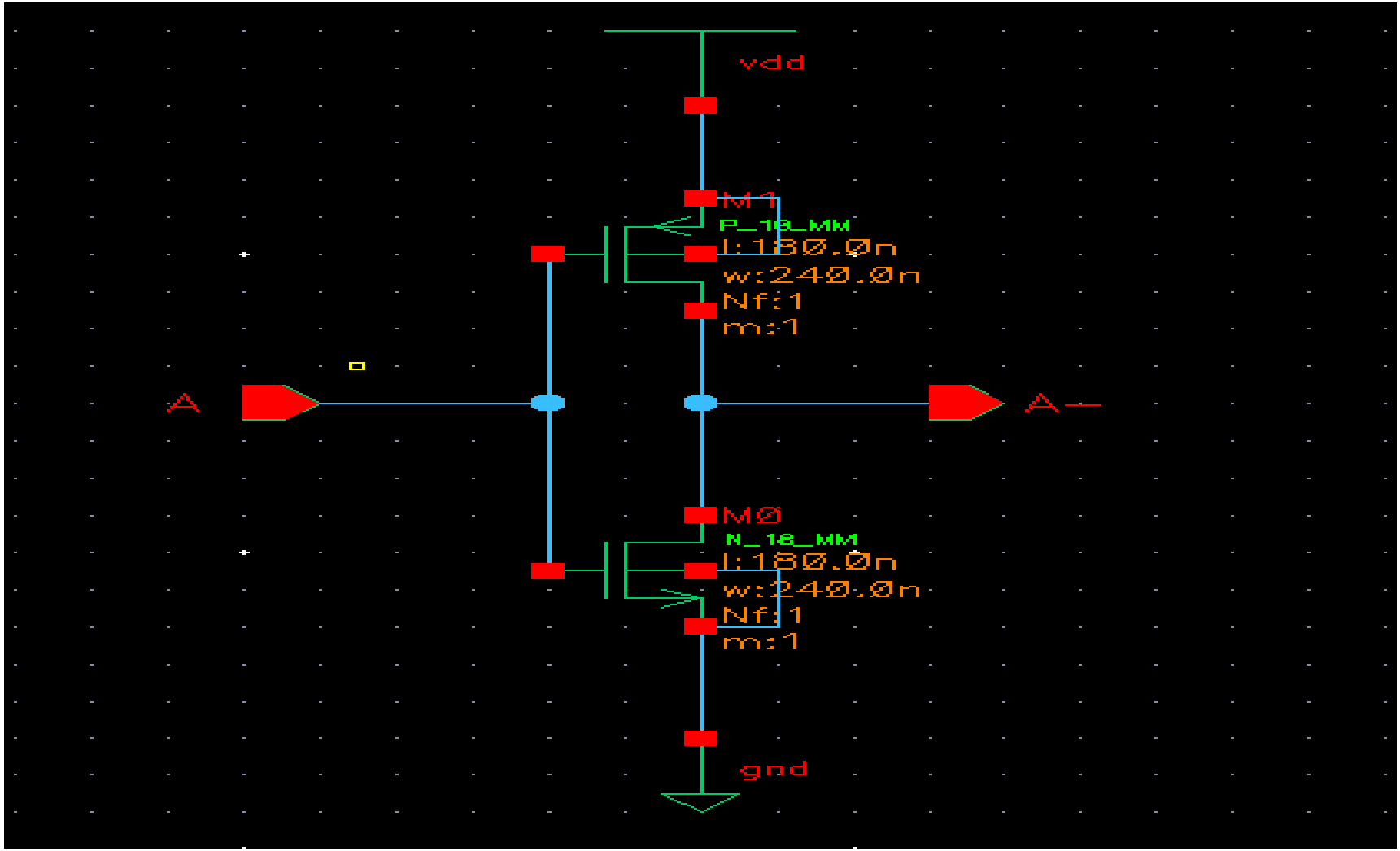
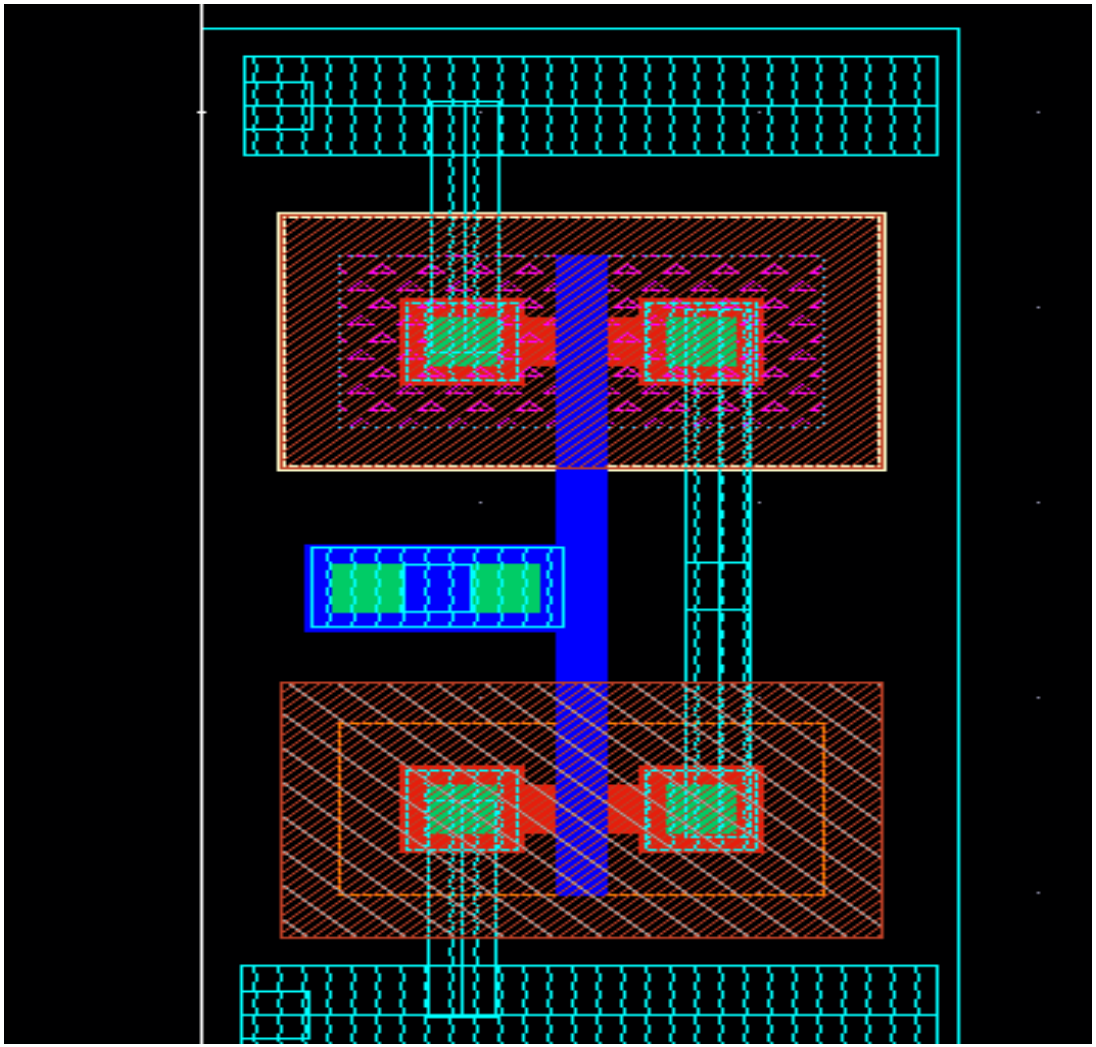
# Layout in Virtuoso - Flow

IIITH

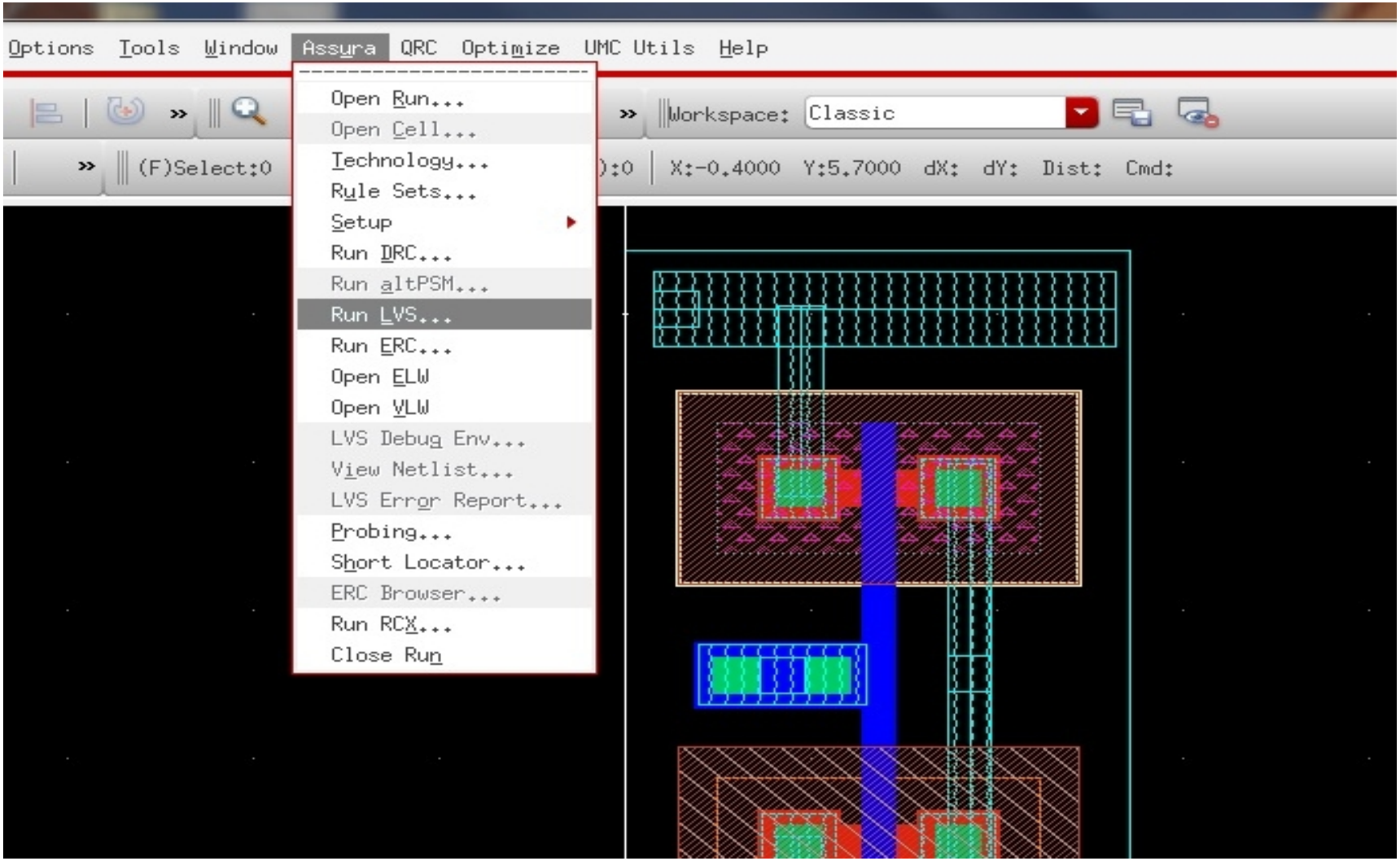
# Create Schematic



# Create Layout



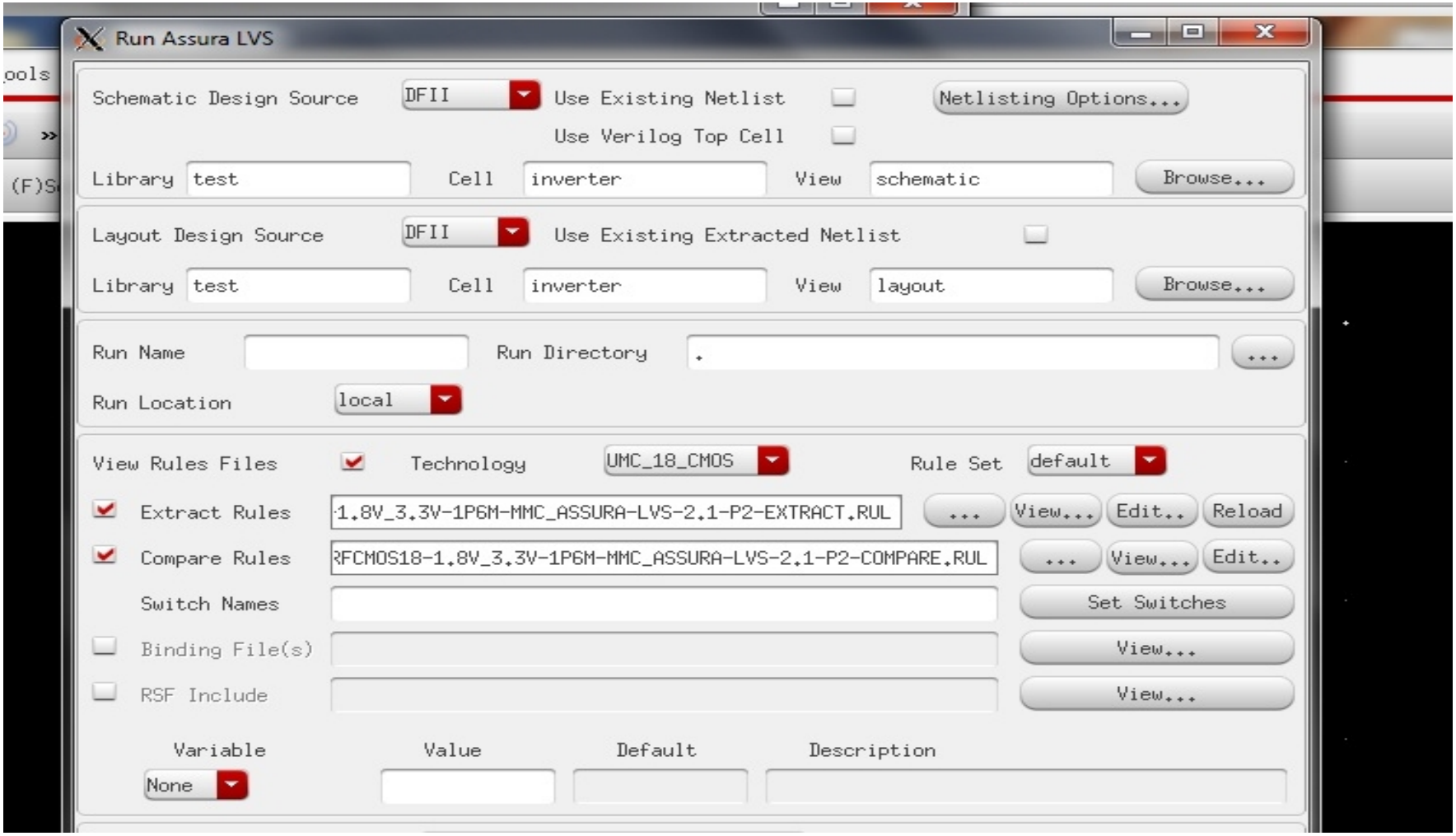
# RUNNING LVS


Options Tools Window Assura QRC Optimize UMC Utils Help
Open Run...
Open Cell...
Technology...
Rule Sets...
Setup
Run DRC...
Run altPSM...
Run LVS...
Run ERC...
Open ELW
Open VLW
LVS Debug Env...
View Netlist...
LVS Error Report...
Probing...
Short Locator...
ERC Browser...
Run RCX...
Close Run
Workspace: Classic
(F)Select:0
X:-0.4000 Y:5.7000 dX: dY: Dist: Cmd:

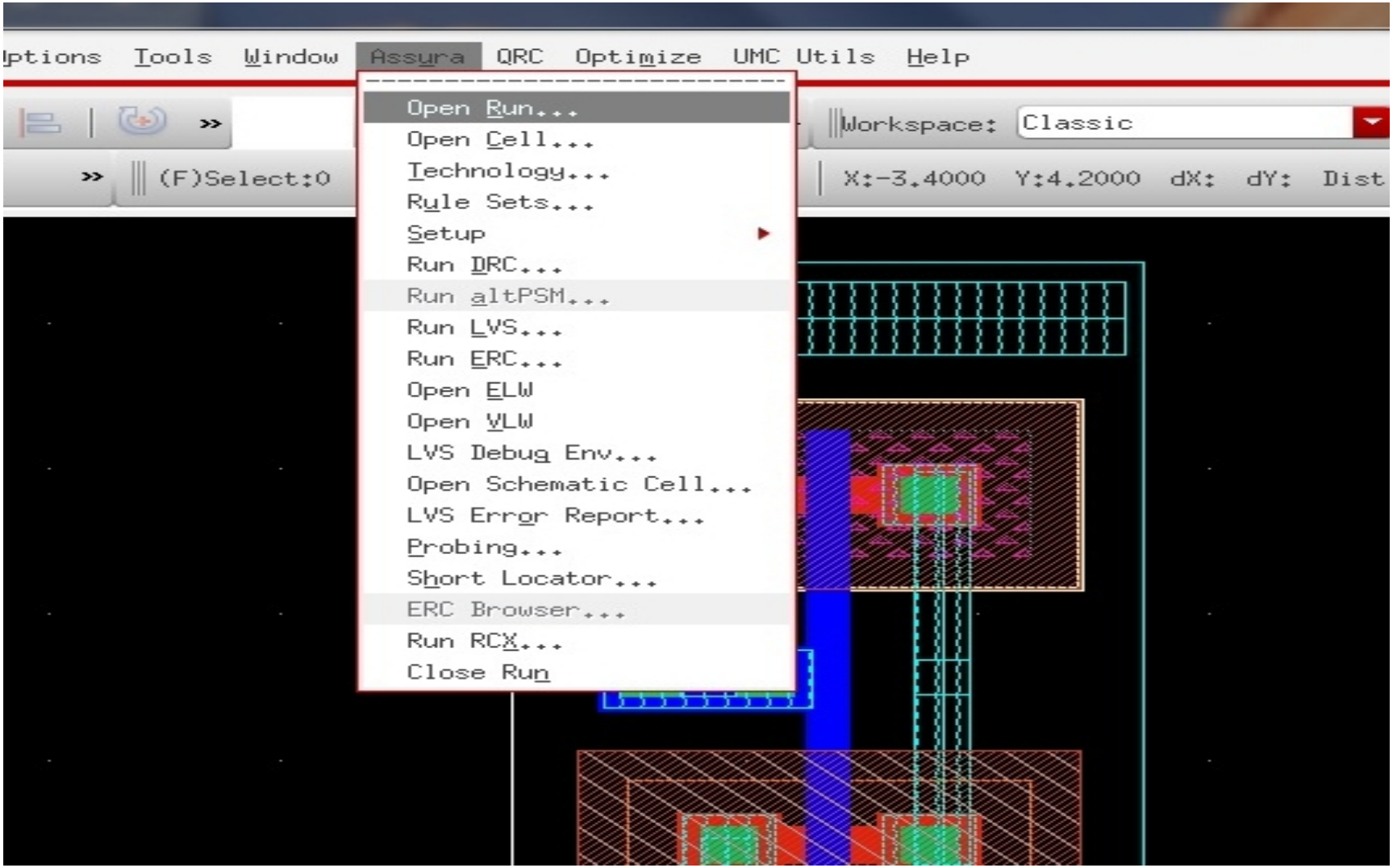
# RUNNING LVS

- Asuura --- > Run LVS
- Check Schematic and Layout cell Names
- Provide proper paths for Extraction and Compare rule decks
- Then Click “ok” or “apply” option to run LVS

# RUNNING LVS


Run Assura LVS
Schematic Design Source
DFII
Use Existing Netlist
Netlisting Options...
Use Verilog Top Cell
Library
test
Cell
inverter
View
schematic
Browse...
Layout Design Source
DFII
Use Existing Extracted Netlist
Library
test
Cell
inverter
View
layout
Browse...
Run Name
Run Directory
.
Run Location
local
View Rules Files
Technology
UMC_18_CMOS
Rule Set
default
Extract Rules
1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-EXTRACT.RUL
View...
Edit..
Reload
Compare Rules
RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-COMPARE.RUL
View...
Edit..
Switch Names
Set Switches
Binding File(s)
View...
RSF Include
View...
Variable
Value
Default
Description
None

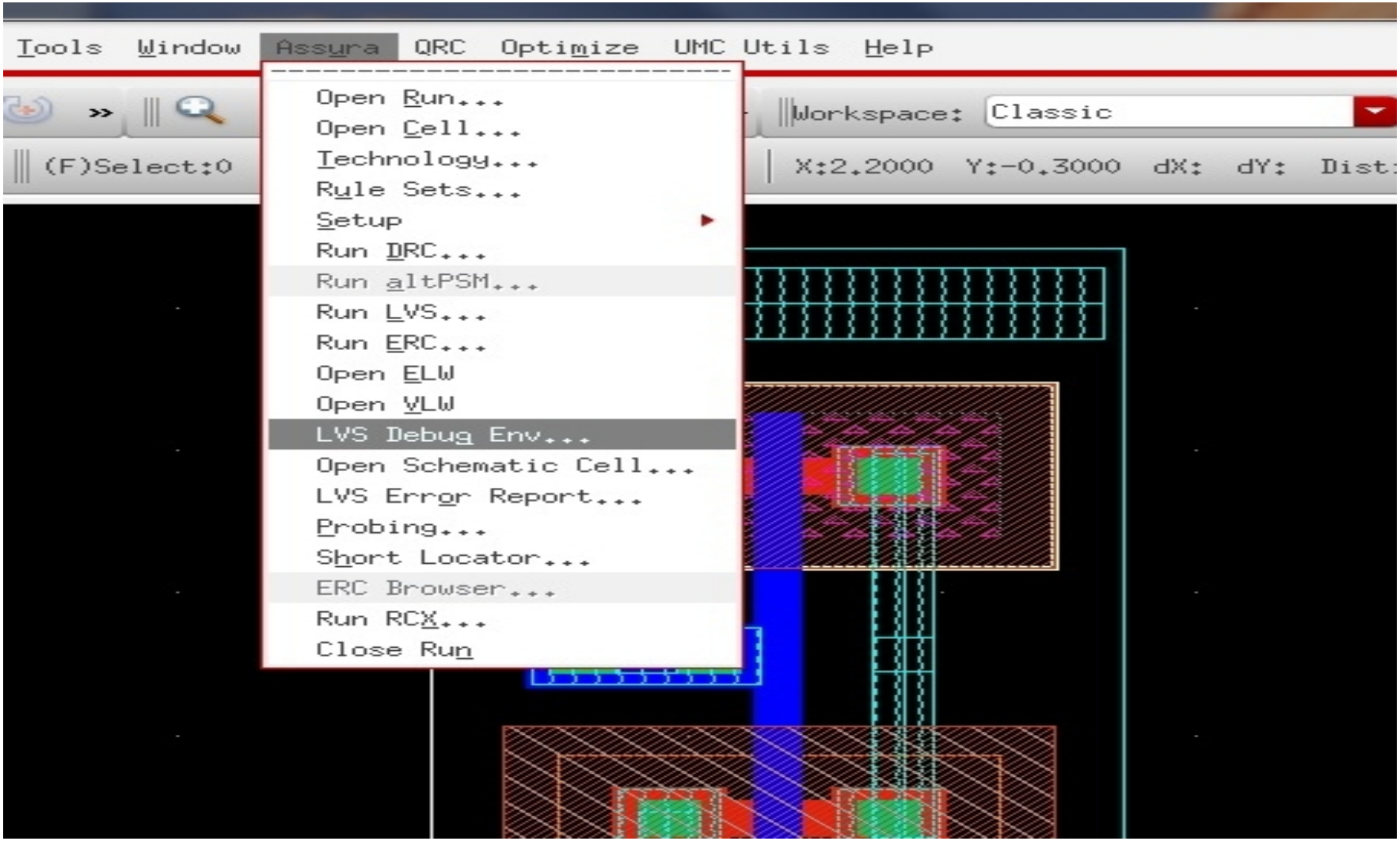
# LVS Debugging



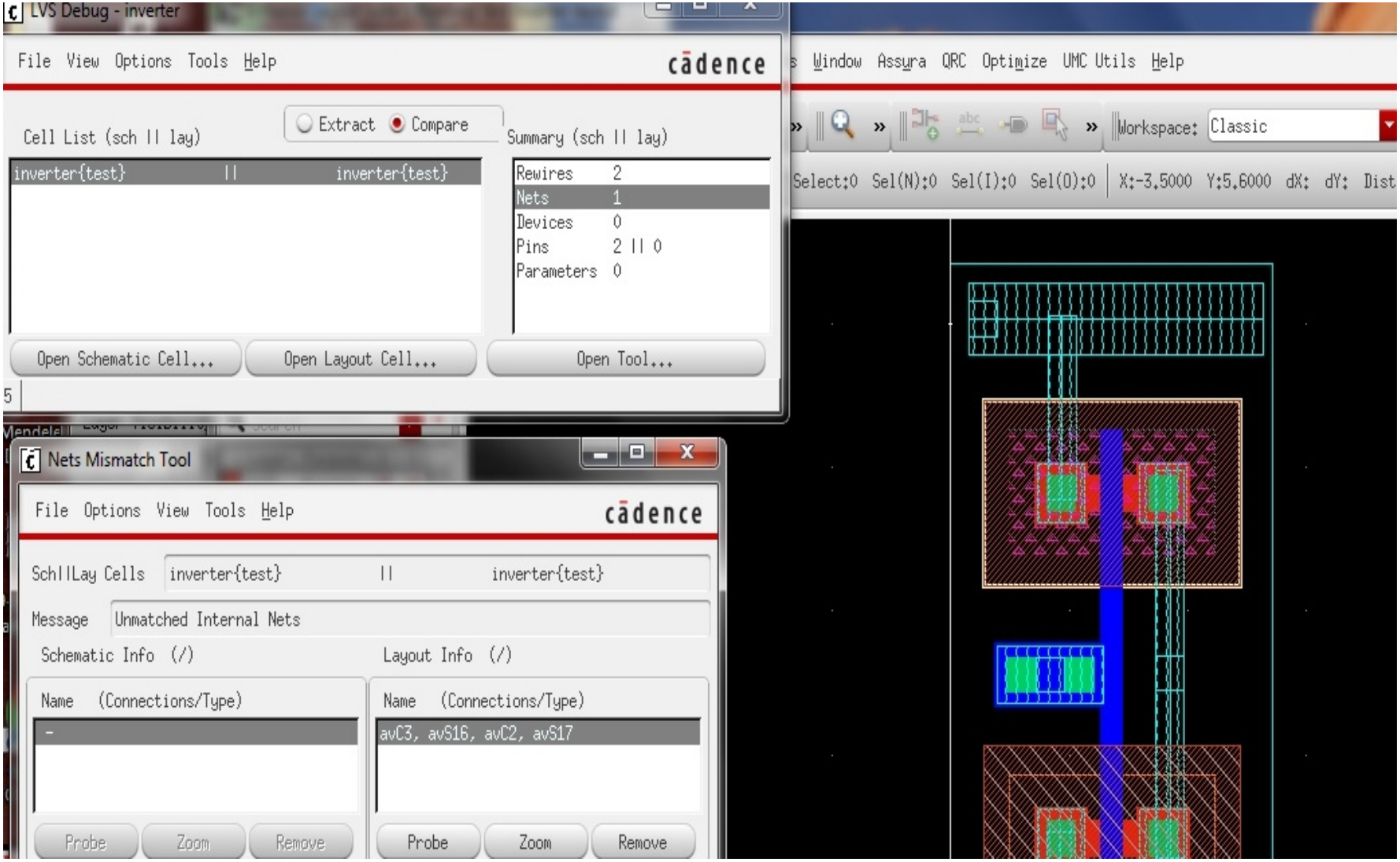
# LVS Debugging

- To debug LVS errors
- Assura --→ Open Run --→ Select the LVS run of the cell --- > Ok
- Assura --→ Lvs Debug Env
- This will pop up results and mismatch window
- Probe mismatch Nets or Devices or Pins and clean them and the run LVS again

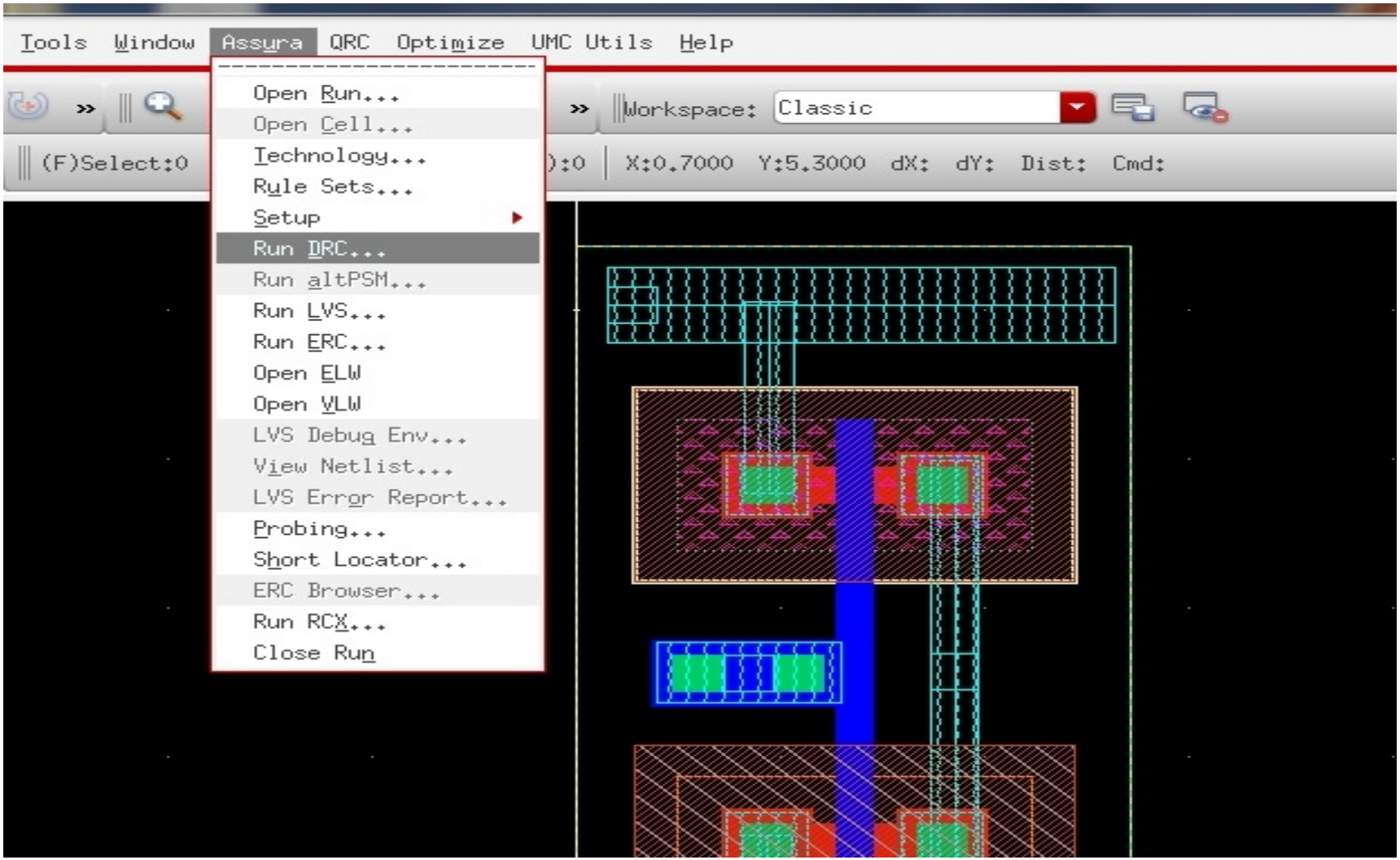
# LVS Debugging



# LVS Debugging



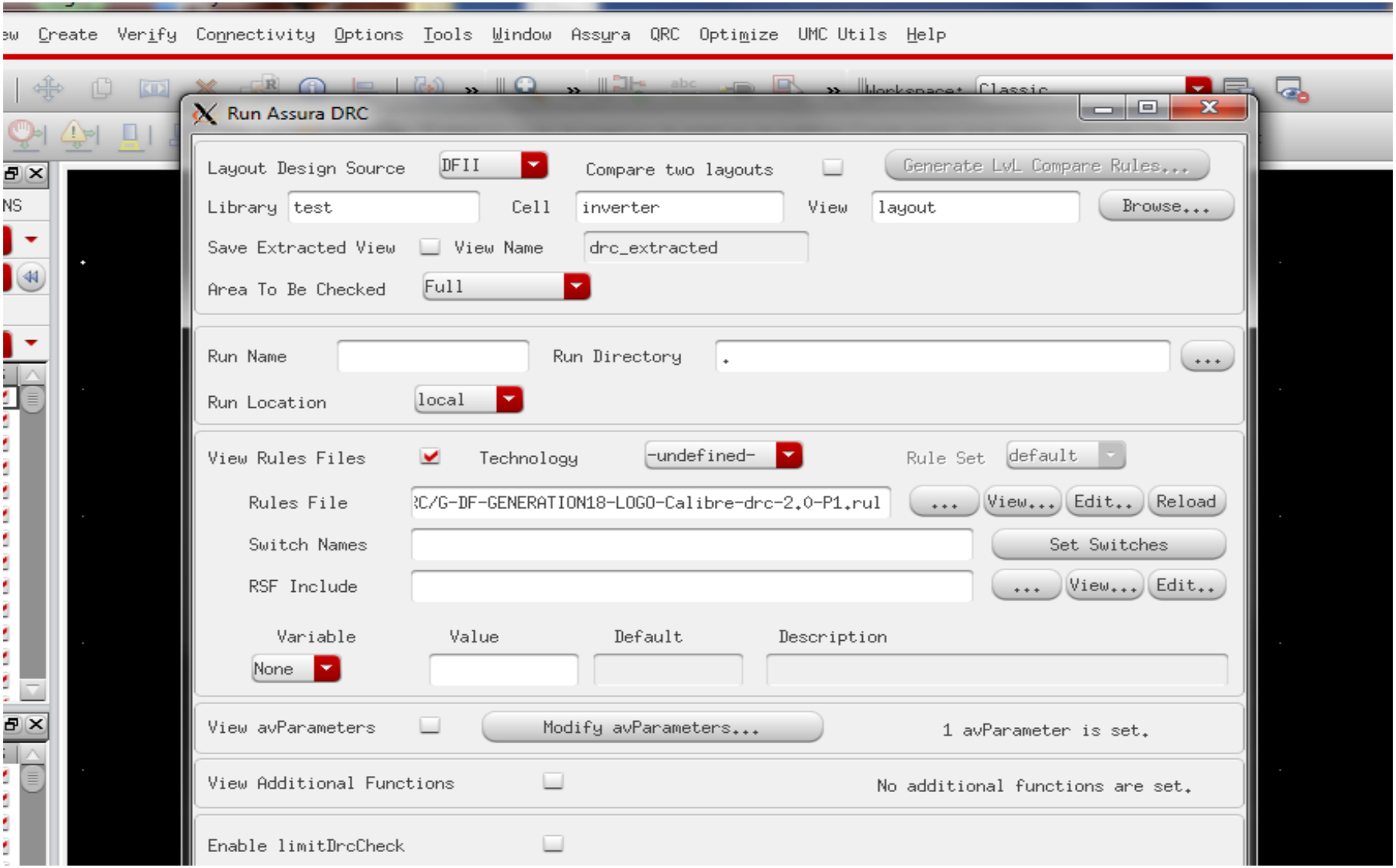
# RUNNING DRC


Tools
Window
Assura
QRC
Optimize
UMC Utils
Help
Open Run...
Open Cell...
Technology...
Rule Sets...
Setup
Run DRC...
Run altPSM...
Run LVS...
Run ERC...
Open ELW
Open VLW
LVS Debug Env...
View Netlist...
LVS Error Report...
Probing...
Short Locator...
ERC Browser...
Run RCX...
Close Run
Workspace: Classic
(F)Select:0
X:0.7000 Y:5.3000 dX: dY: Dist: Cmd:

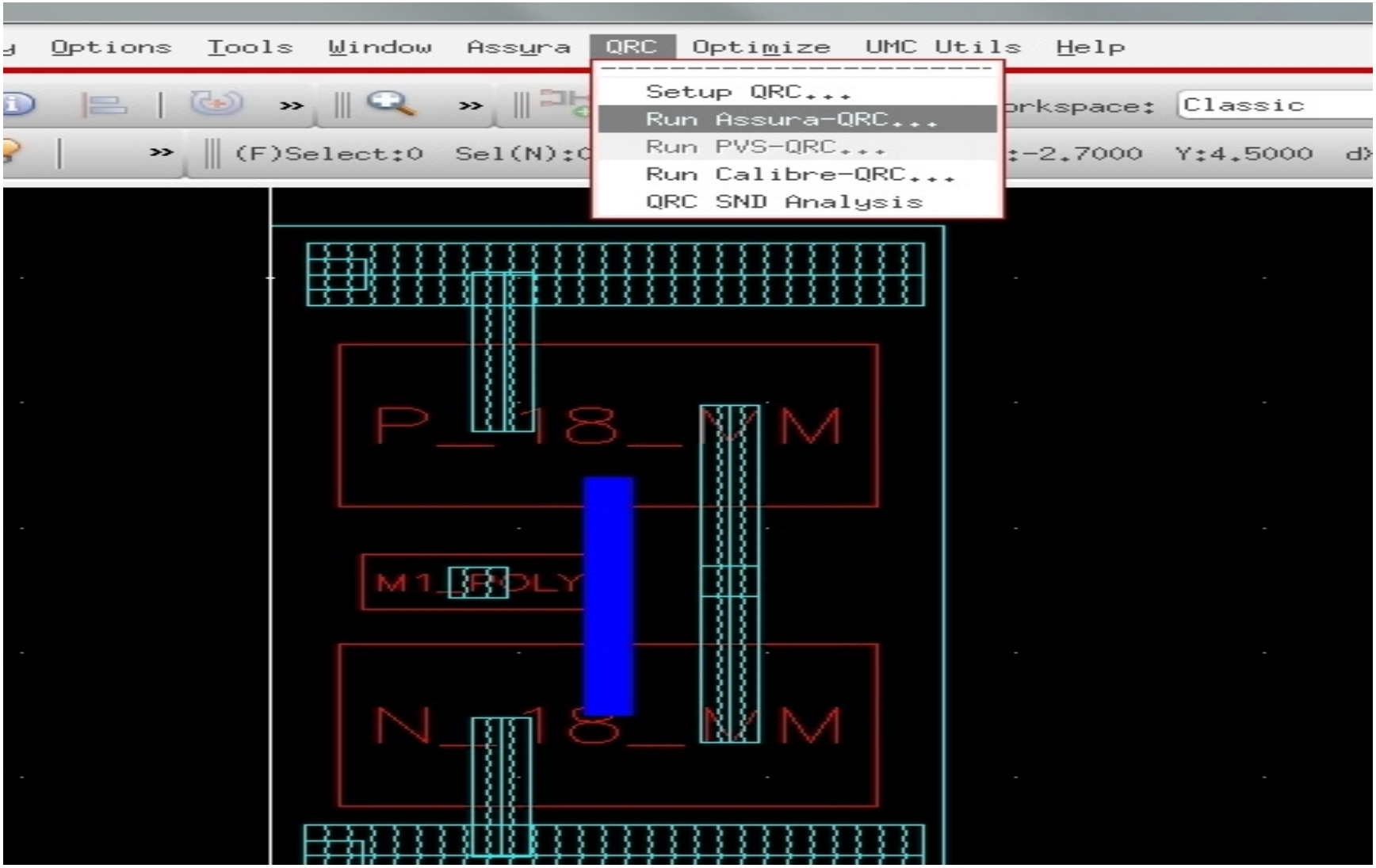
# RUNNING DRC

- Assura ---- > Run DRC
- Select the proper layout cell
- Provide path for proper DRC rule file
- Click “ok” or “apply” to run DRC
- Once the Run is finished it will pop up drc debugging window by itself

# RUNNING DRC


Create Verify Connectivity Options Tools Window Assura QRC Optimize UMC Utils Help
Run Assura DRC
Layout Design Source
DFII
Compare two layouts
Generate LvL Compare Rules...
Library
test
Cell
inverter
View
layout
Browse...
Save Extracted View
View Name
drc_extracted
Area To Be Checked
Full
Run Name
Run Directory
.
Run Location
local
View Rules Files
Technology
-undefined-
Rule Set
default
Rules File
RC/G-DF-GENERATION18-LOGO-Calibre-drc-2.0-P1.rul
View...
Edit..
Reload
Switch Names
Set Switches
RSF Include
Variable
Value
Default
Description
None
View avParameters
Modify avParameters...
1 avParameter is set.
View Additional Functions
No additional functions are set.
Enable limitDrcCheck

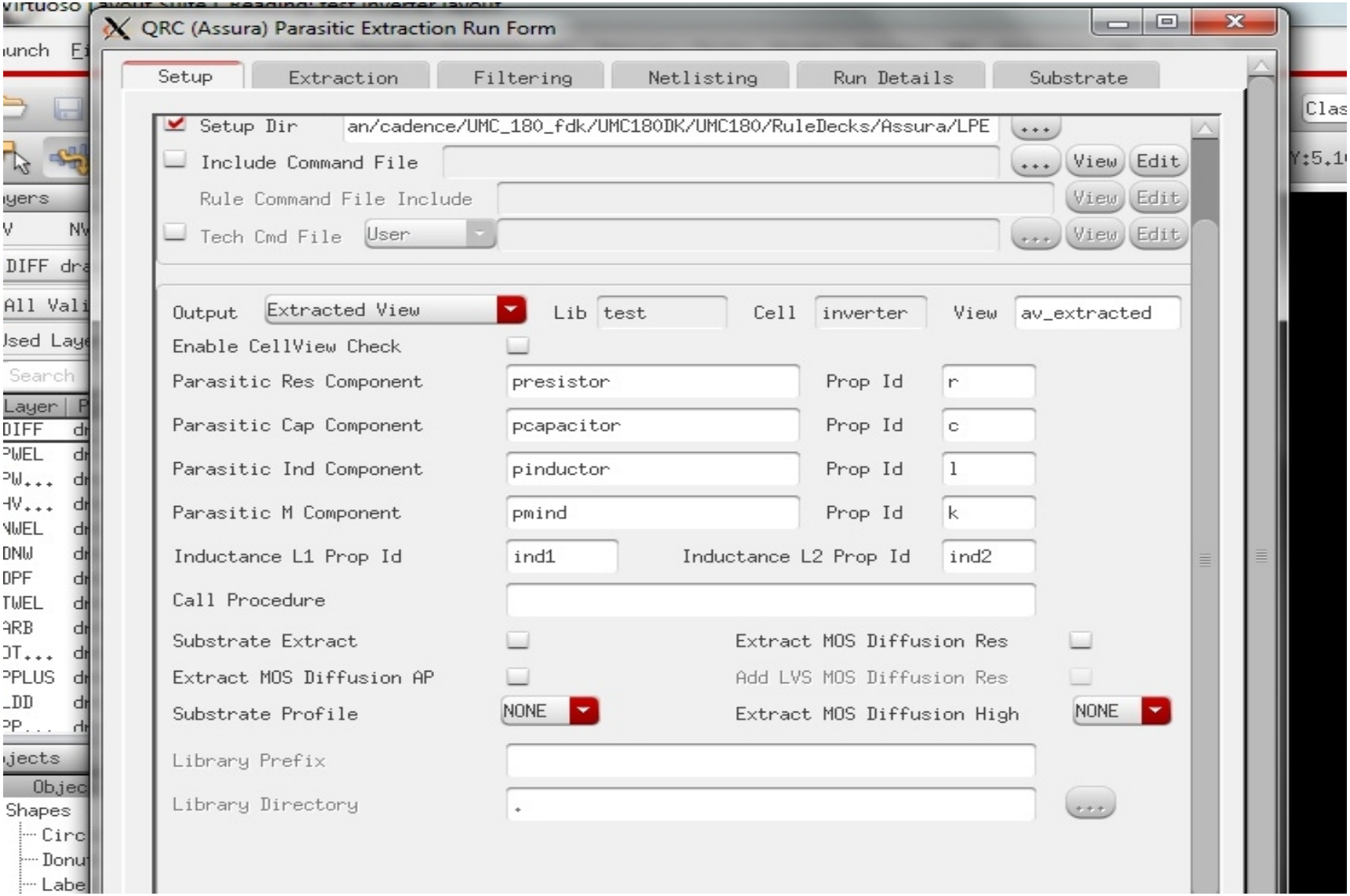
# RUNNING QRC


Options
Tools
Window
Assura
QRC
Optimize
UMC Utils
Help
Setup QRC...
Run Assura-QRC...
Run PVS-QRC...
Run Calibre-QRC...
QRC SND Analysis
Classic
(F)Select:0
Sel(N):0
X:-2.7000
Y:4.5000
P_18_M
M1_POLY
N_18_M

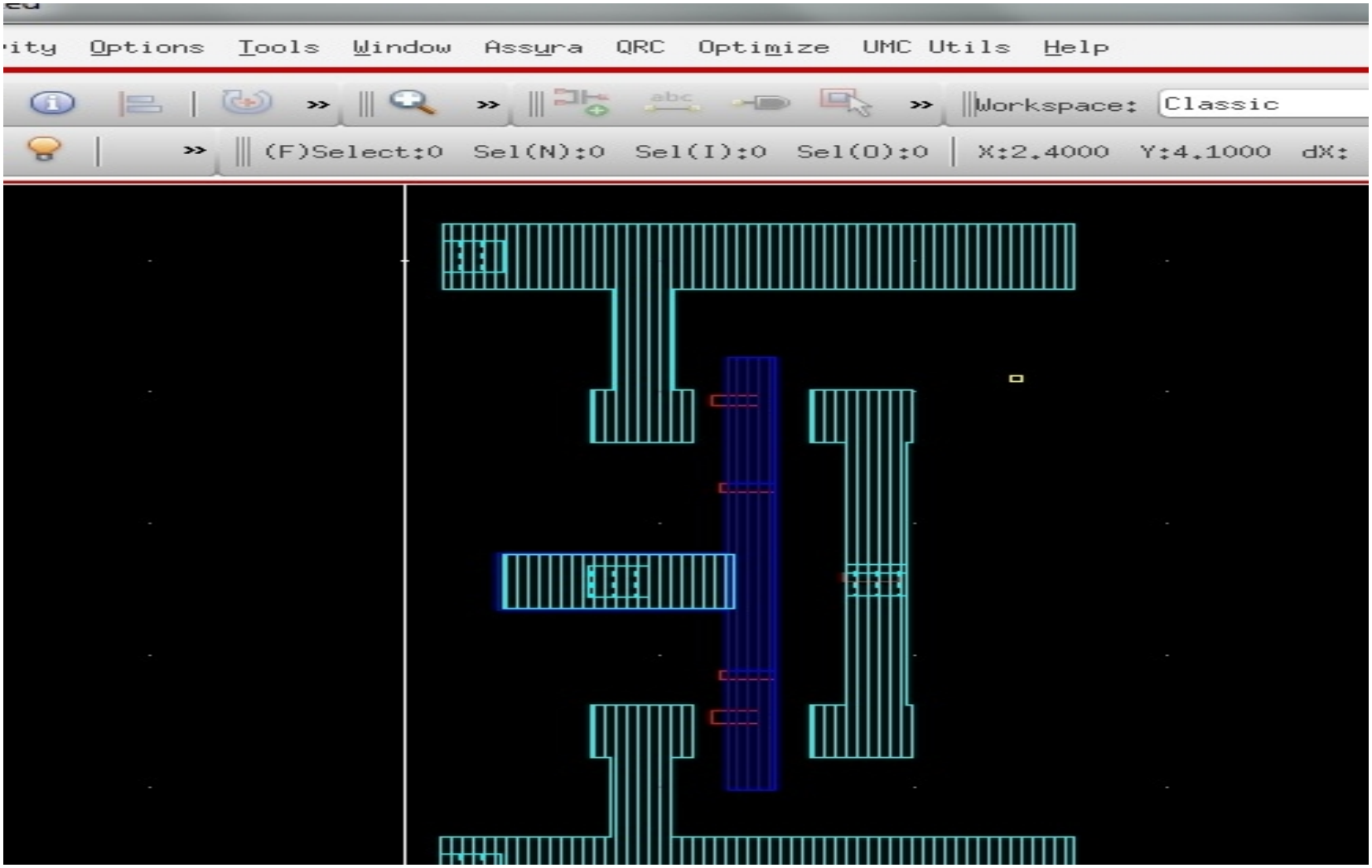
# RUNNING QRC

- Once the LVS is clean
- QRC ---→ Assura QRC -→ Select run
- Select Av extrated view or any other o/p netlist based on requirement
- Click ok to Run

# RUNNING QRC


QRC (Assura) Parasitic Extraction Run Form
Setup
Extraction
Filtering
Netlisting
Run Details
Substrate
Setup Dir
an/cadence/UMC_180_fdk/UMC180DK/UMC180/RuleDecks/Assura/LPE
Include Command File
View
Edit
Rule Command File Include
Tech Cmd File
User
Output
Extracted View
Lib
test
Cell
inverter
View
av_extracted
Enable CellView Check
Parasitic Res Component
presistor
Prop Id
r
Parasitic Cap Component
pcapacitor
c
Parasitic Ind Component
pinductor
l
Parasitic M Component
pmind
k
Inductance L1 Prop Id
ind1
Inductance L2 Prop Id
ind2
Call Procedure
Substrate Extract
Extract MOS Diffusion Res
Extract MOS Diffusion AP
Add LVS MOS Diffusion Res
Substrate Profile
NONE
Extract MOS Diffusion High
NONE
Library Prefix
Library Directory

# Av Ext View


ity Options Tools Window Assura QRC Optimize UMC Utils Help
Workspace: Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:2.4000 Y:4.1000 dX: