

Process Variations

Devices parameters vary between runs and even on the same die!

Variations in the process parameters, such as impurity concentration densities, oxide thicknesses, and diffusion depths. These are caused by non-uniform conditions during the deposition and/or the diffusion of the impurities. This introduces variations in the sheet resistances and transistor parameters such as the threshold voltage.

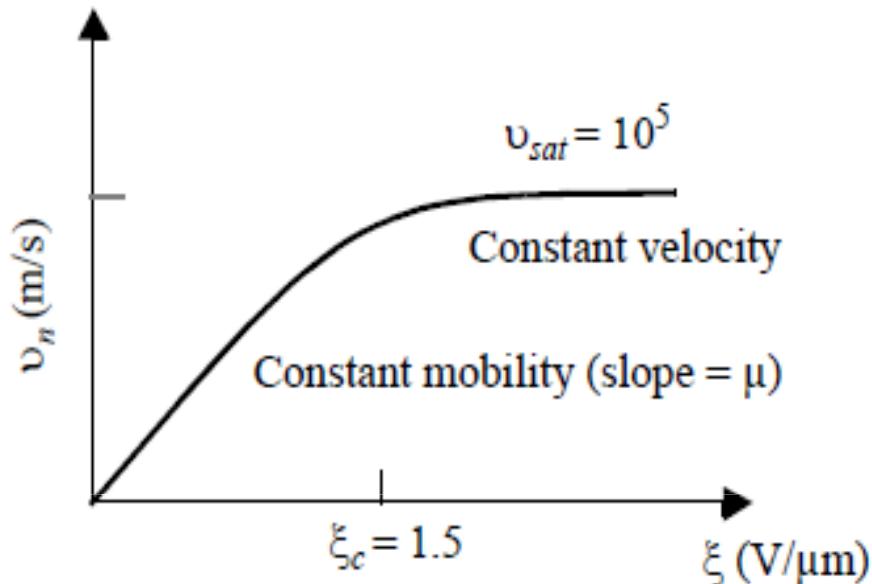
Variations in the dimensions of the devices, mainly resulting from the limited resolution of the photolithographic process. This causes (W/L) variations in MOS transistors and mismatches in the emitter areas of bipolar devices.



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Velocity Saturation



$$v_n = -\mu_n \xi(x) = \mu_n \frac{dV}{dx}$$

scattering effects (collisions suffered by the carriers)

For *p*-type silicon, the critical field at which electron saturation occurs is 1.5 V/ μ m

saturation velocity v_{sat} approximately equals 10⁵ m/s

$$v = \begin{cases} \frac{\mu_n \xi}{1 + \xi/\xi_c} & \text{for } \xi \leq \xi_c \\ v_{sat} & \text{for } \xi \geq \xi_c \end{cases}$$

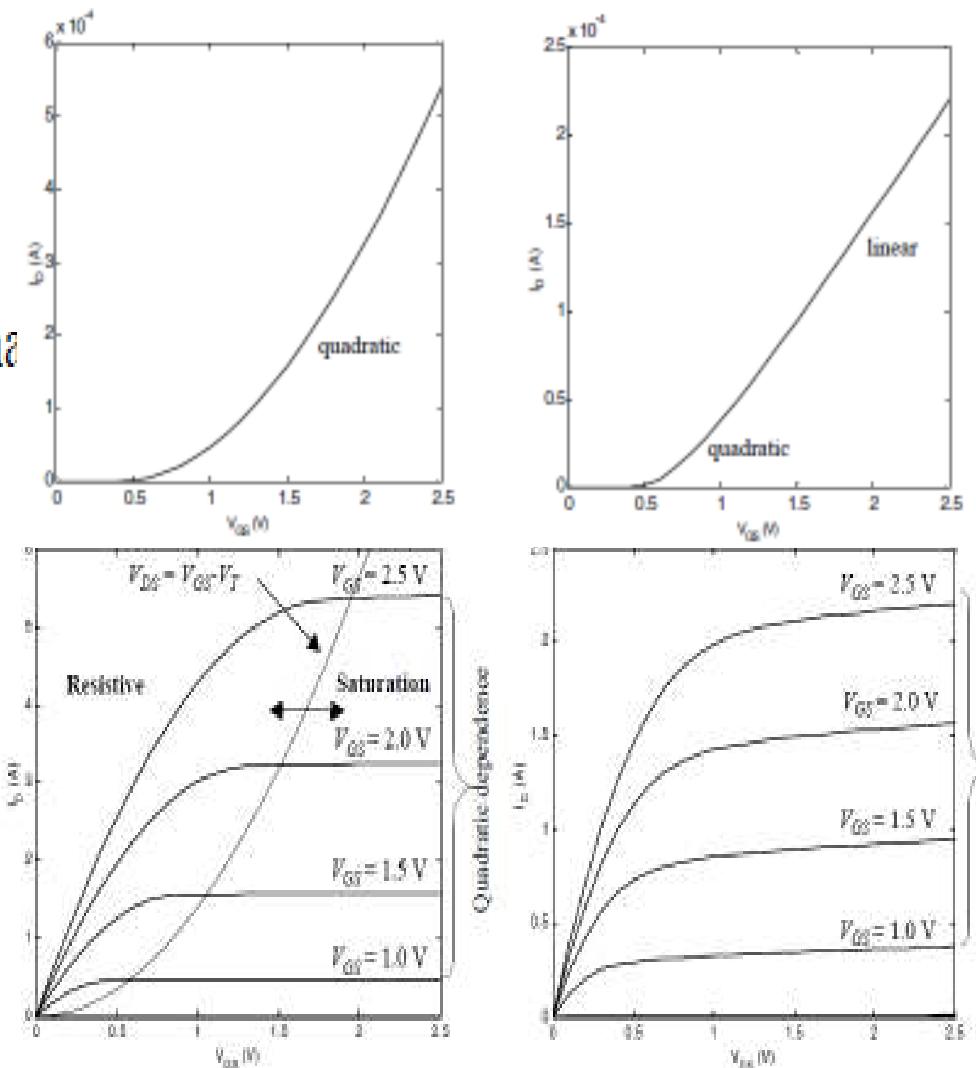
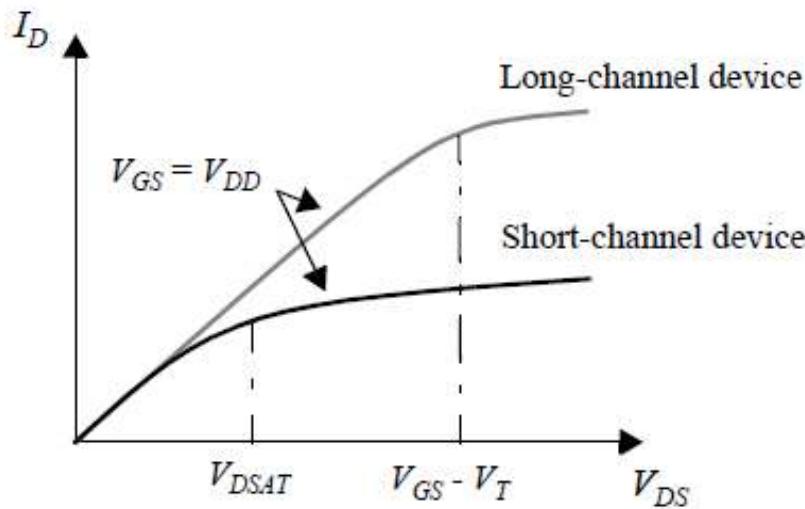


drain current in the resistive region

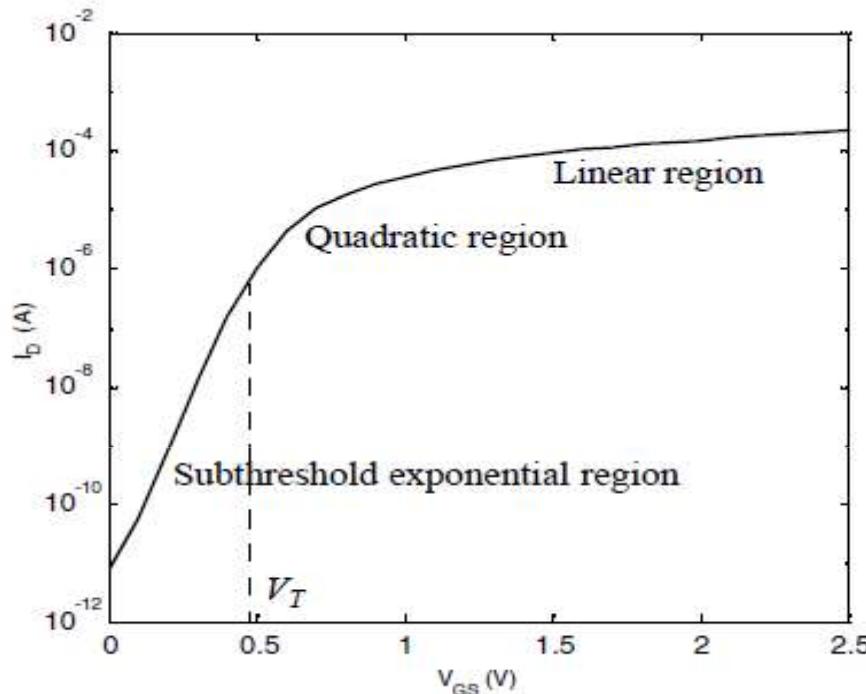
$$I_D = \kappa(V_{DS})\mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right]$$

For short-channel devices, κ is smaller than

$$\kappa(V) = \frac{1}{1 + (V/\xi_c L)}$$



Subthreshold Conduction



$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}} \right)$$

measures by how much V_{GS} has to be reduced for the drain current to drop by a factor $S = n \left(\frac{kT}{q} \right) \ln(10)$



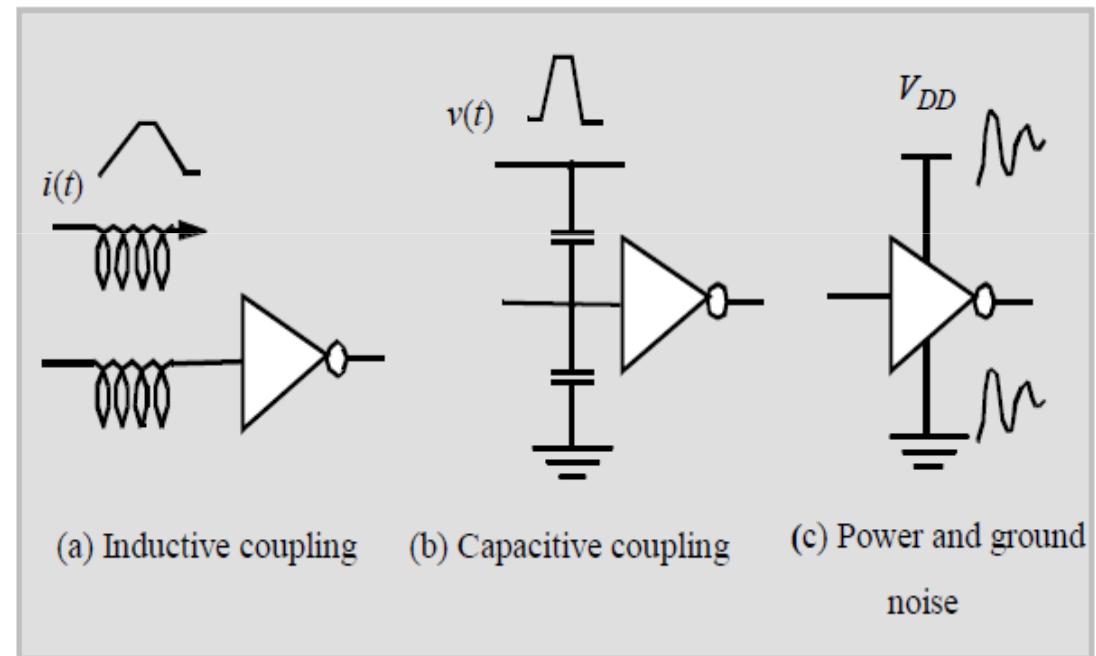
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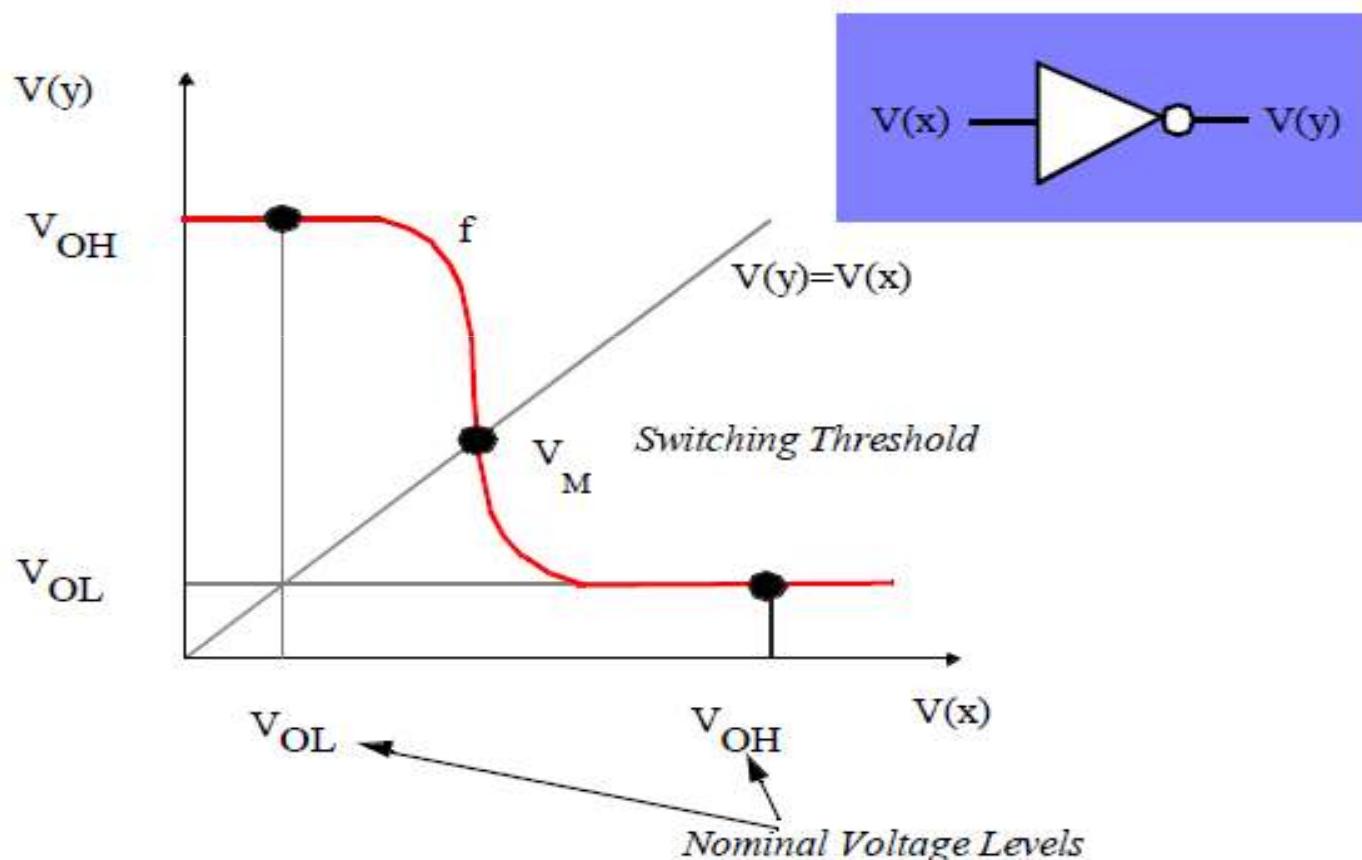
DIGITAL GATES Fundamental Parameters

- Functionality
- Reliability, Robustness
- Area
- Performance
 - » Speed (delay)
 - » Power Consumption
 - » Energy

Noise in Digital Integrated Circuits



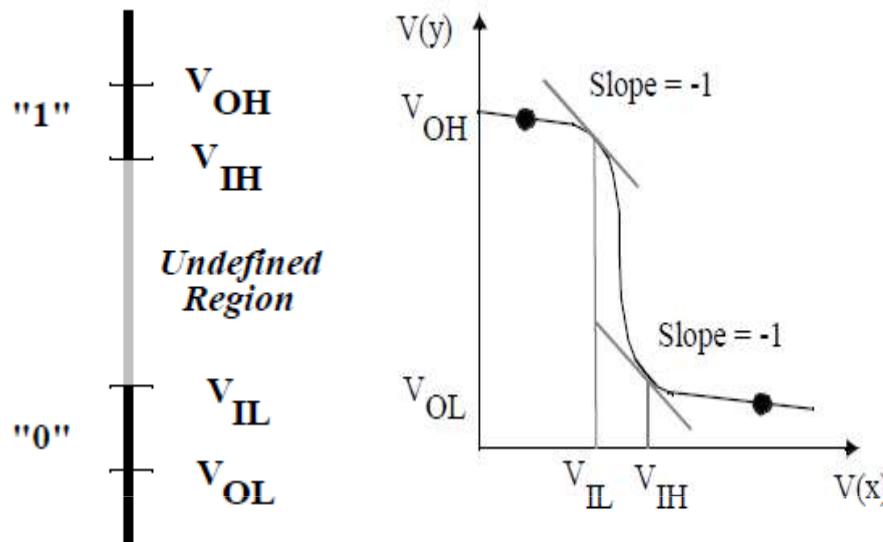
DC Operation: Voltage Transfer Characteristic



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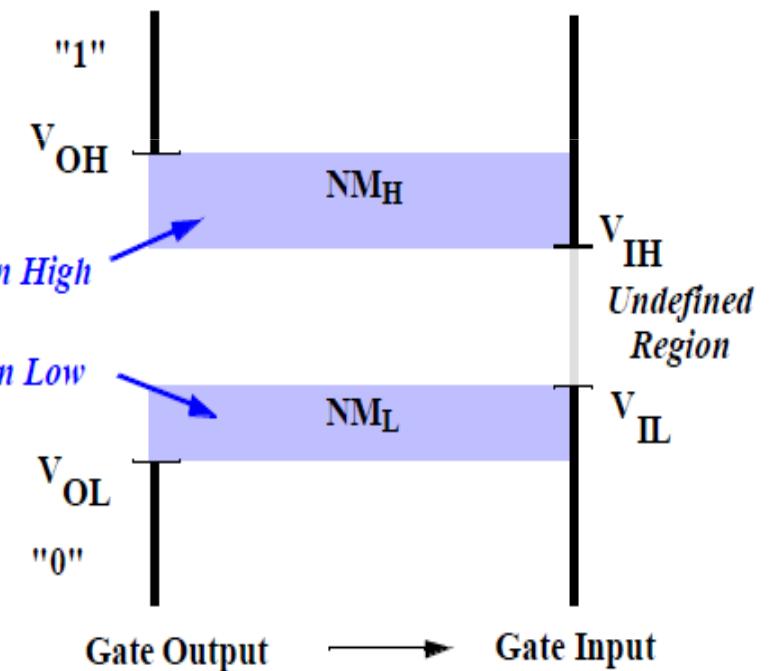
Mapping between analog and digital signals



Definition of Noise Margins

$$NM_L = V_{IL} - V_{OL}$$

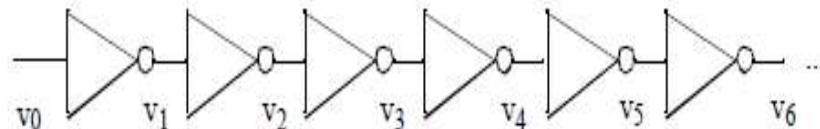
$$NM_H = V_{OH} - V_{IH}$$



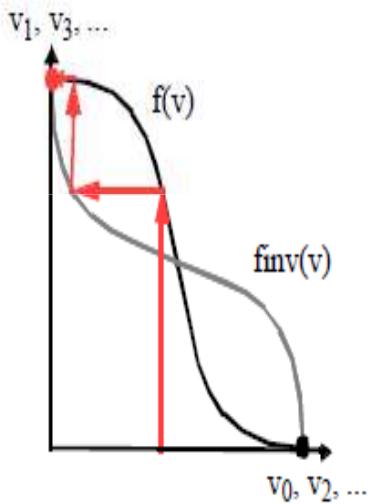
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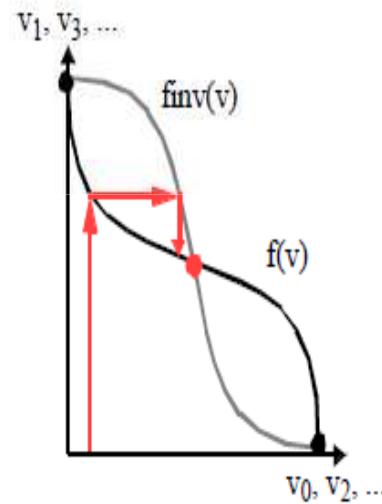
The Regenerative Property



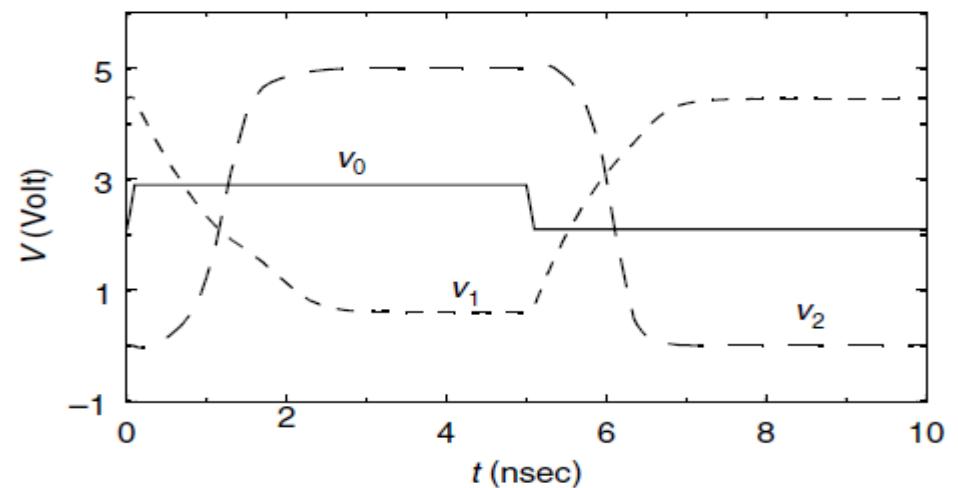
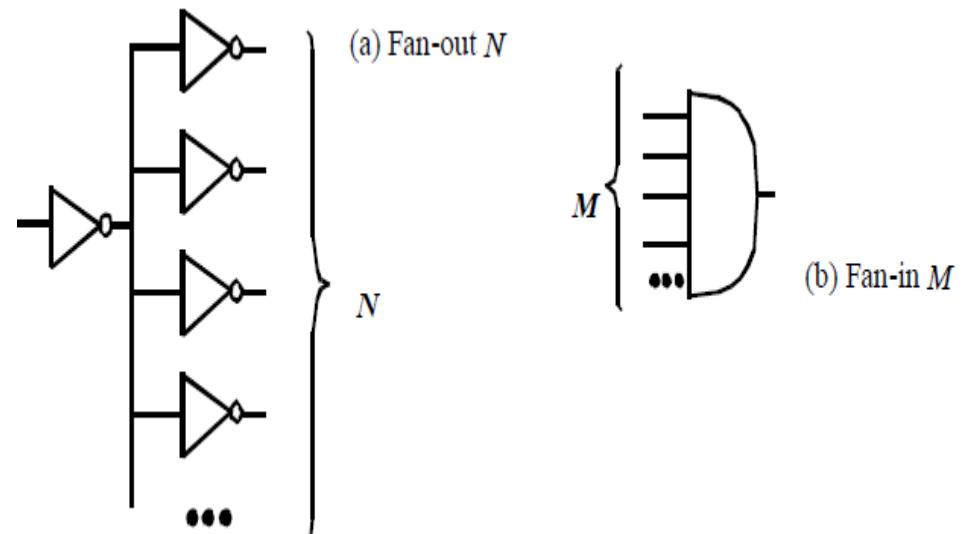
(a) A chain of inverters.



(b) Regenerative gate



(c) Non-regenerative gate



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Noise Immunity

- proportional to the signal swing V_{sw} . The impact on the signal node is expressed as $g V_{sw}$.
- fixed. The impact on the signal node equals $f V_{nf}$, with V_{nf} the amplitude of the noise source, and f the transfer function from noise to signal node.

$$V_{NM} = \frac{V_{sw}}{2} \geq \sum_i f_i V_{Nfi} + \sum_j g_j V_{sw}$$

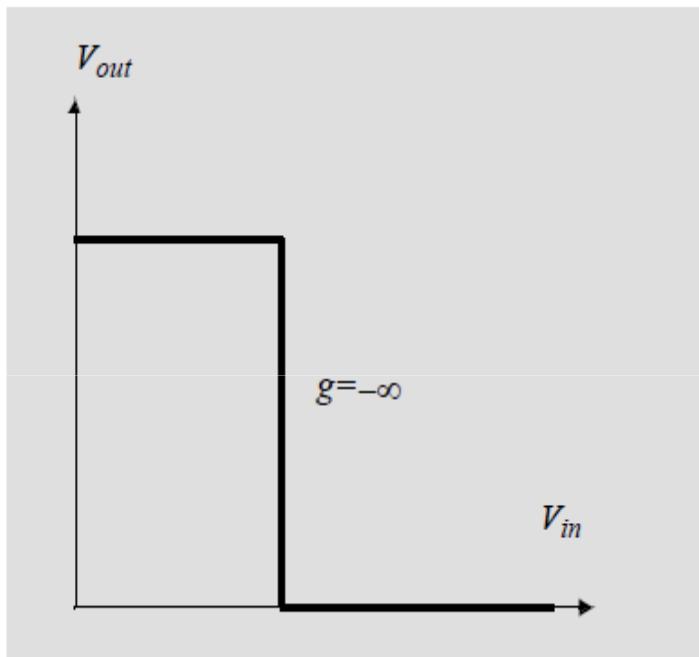
$$V_{sw} \geq \frac{2 \sum_i f_i V_{Nfi}}{1 - 2 \sum_j g_j}$$



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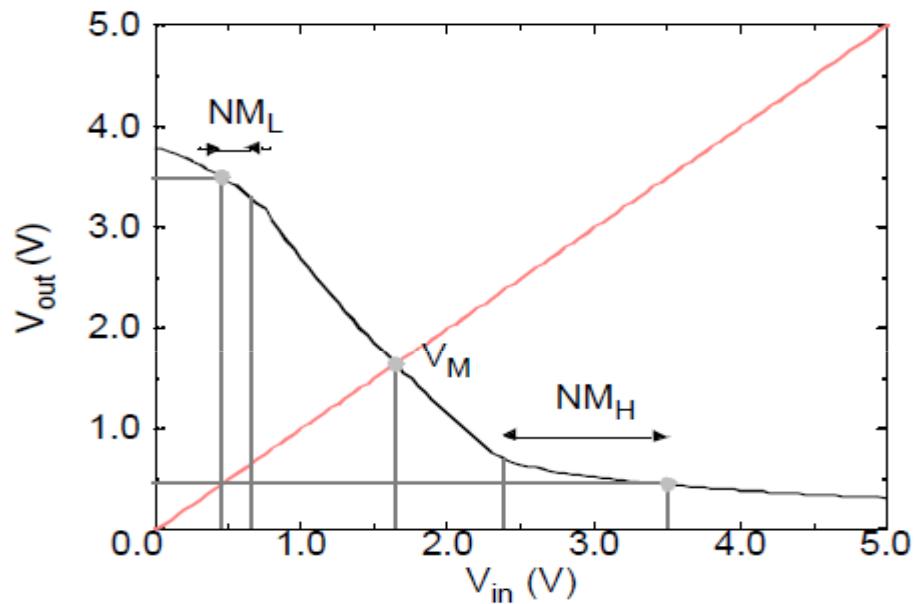
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The Ideal Gate



$$R_i = \infty$$
$$R_o = 0$$

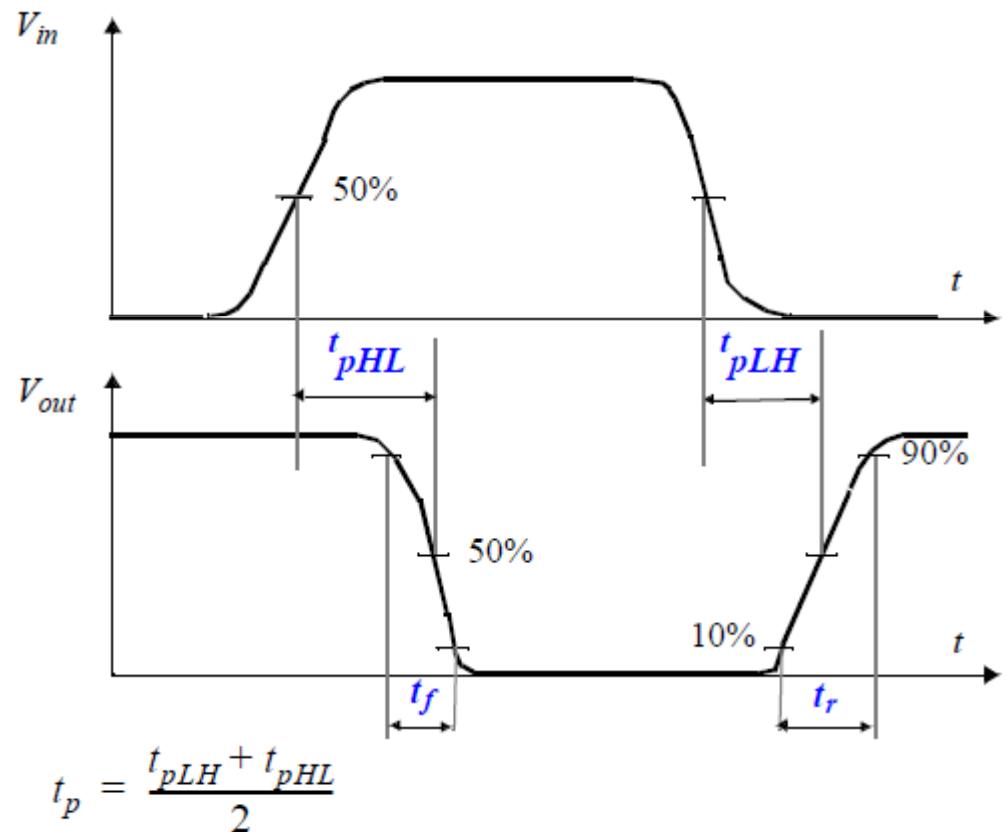
VTC of Real Inverter



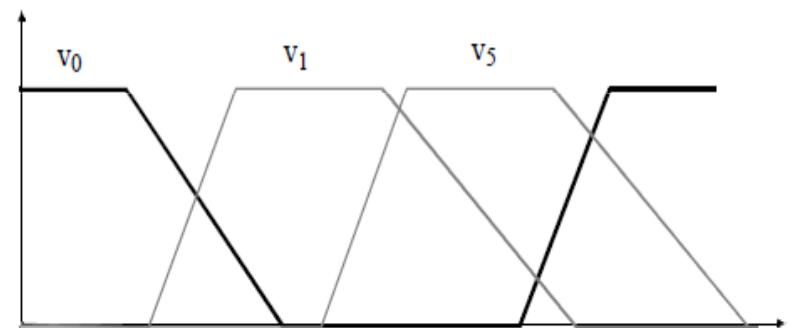
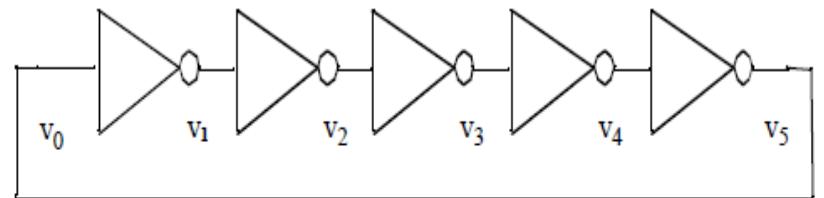
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Delay Definitions



Ring Oscillator



$$T = 2 \times t_p \times N$$

$$2Nt_p \gg t_f + t_r$$



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Power Dissipation

$$P_{peak} = i_{peak} V_{supply} = \max(p(t)))$$

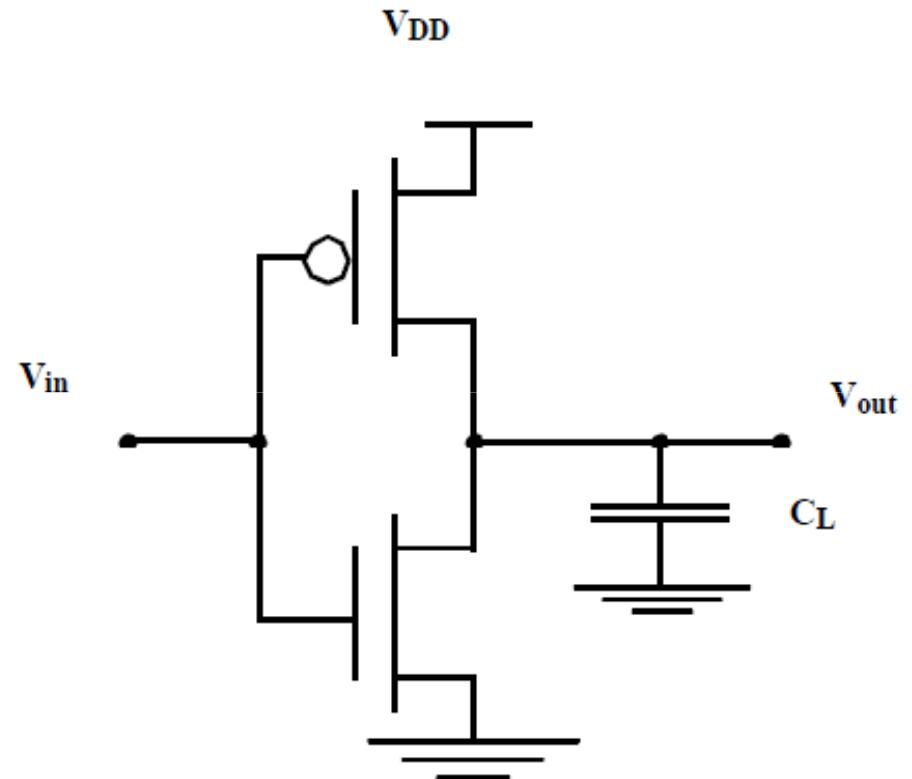
$$P_{av} = \frac{1}{T} \int_0^T p(t) dt = \frac{V_{supply}}{T} \int_0^T i_{supply}(t) dt$$

Power-Delay Product

$$PDP = t_p \times P_{av}$$

= Energy dissipated per operation

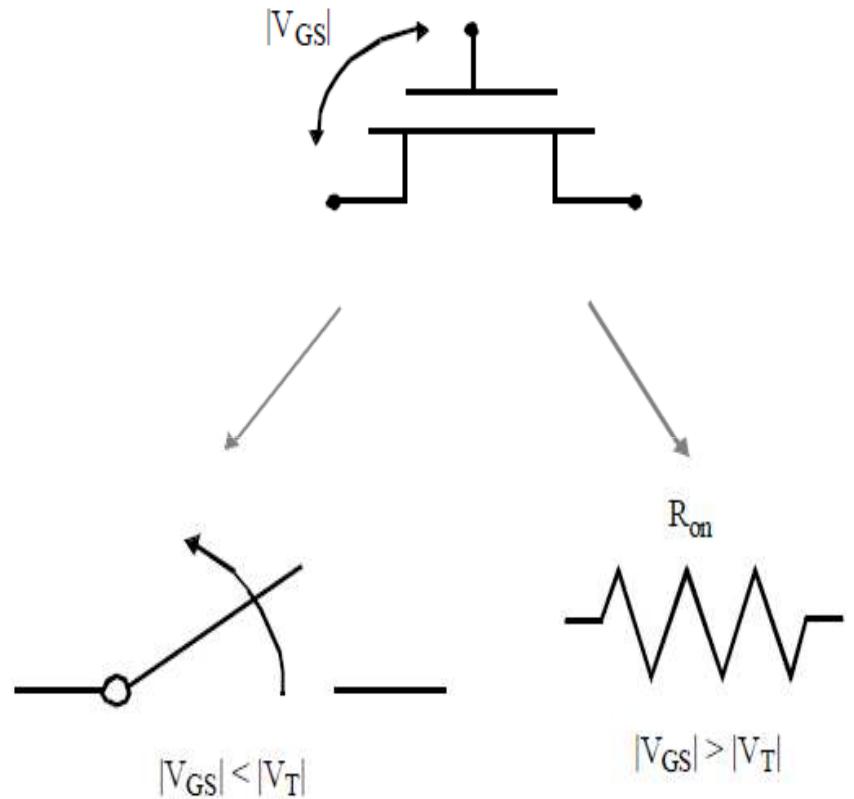
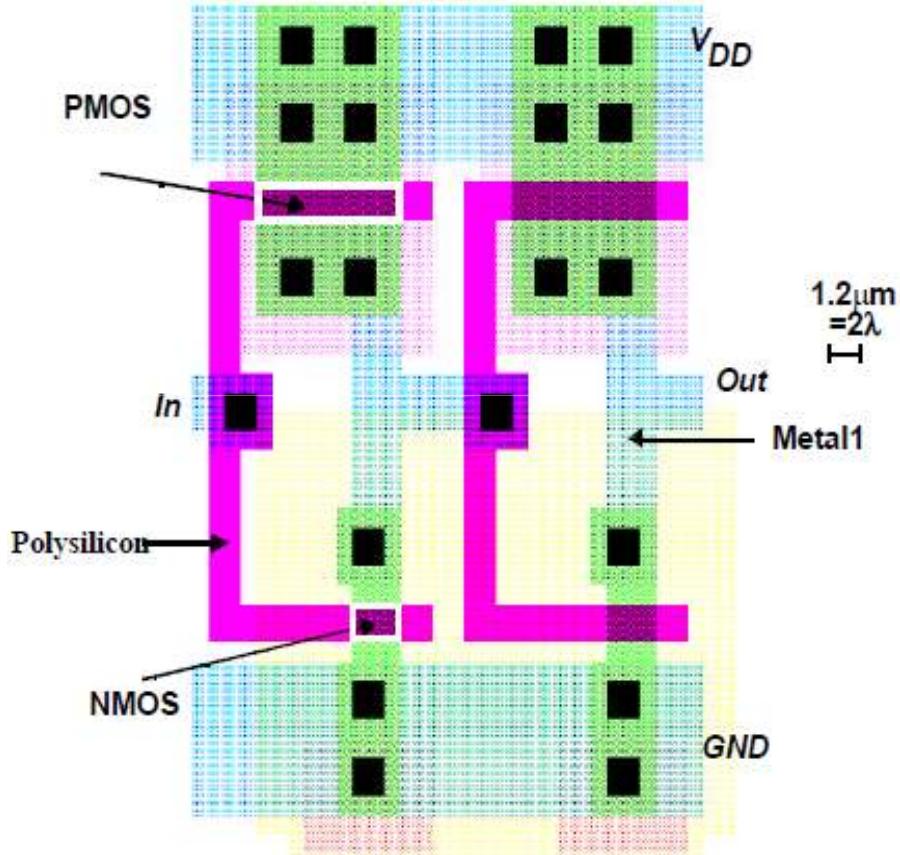
The CMOS Inverter



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CMOS Inverters



Switch Model of CMOS Transistor



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Some points to note

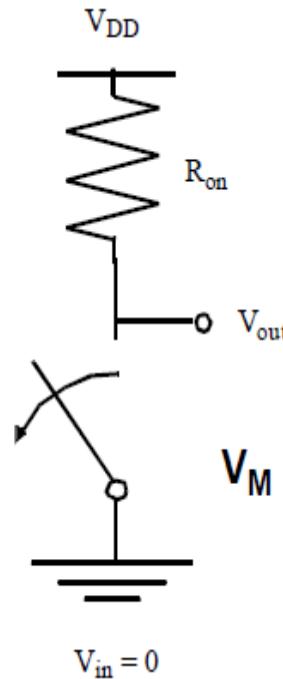
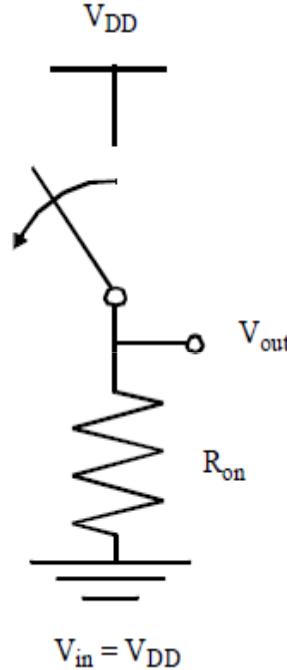
- The high and low output levels equal V_{DD} and GND , respectively; in other words, the voltage swing is equal to the supply voltage. This results in high noise margins.
- The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size. Gates with this property are called *ratioless*. This is in contrast with *ratioed logic*, where logic levels are determined by the relative dimensions of the composing transistors.
- In steady state, there always exists a path with finite resistance between the output and either V_{DD} or GND . A well-designed CMOS inverter, therefore, has a *low output impedance*, which makes it less sensitive to noise and disturbances. Typical values of the output resistance are in $k\Omega$ range.
- The *input resistance* of the CMOS inverter is extremely high, as the gate of an MOS transistor is a virtually perfect insulator and draws no dc input current. Since the input node of the inverter only connects to transistor gates, the steady-state input current is nearly zero. A single inverter can theoretically drive an infinite number of gates (or have an infinite fan-out) and still be functionally operational; however, increasing the fan-out also increases the propagation delay, as will become clear below. So, although fan-out does not have any effect on the steady-state behavior, it degrades the transient response.



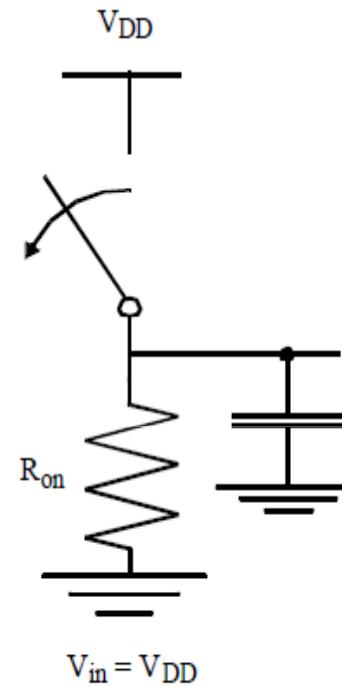
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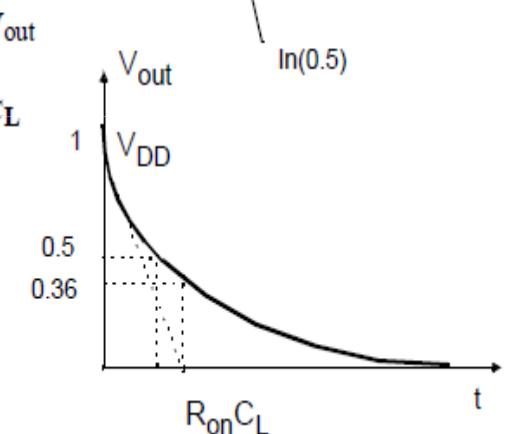
CMOS Inverter: Steady State Response



$$V_{OH} = V_{DD}$$
$$V_{OL} = 0$$
$$V_M = f(R_{onn}, R_{onp})$$



$$t_{pHL} = f(R_{on} \cdot C_L)$$
$$= 0.69 R_{on} C_L$$



CMOS Inverter: Transient Response



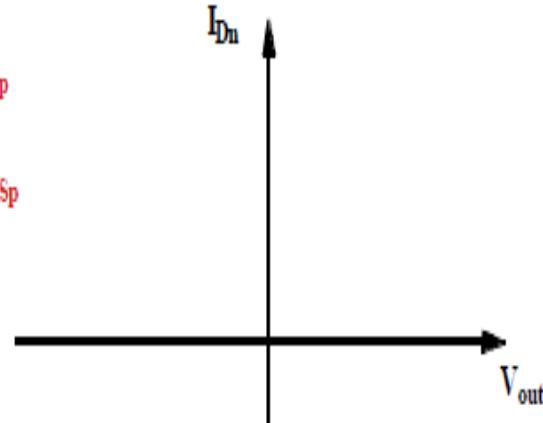
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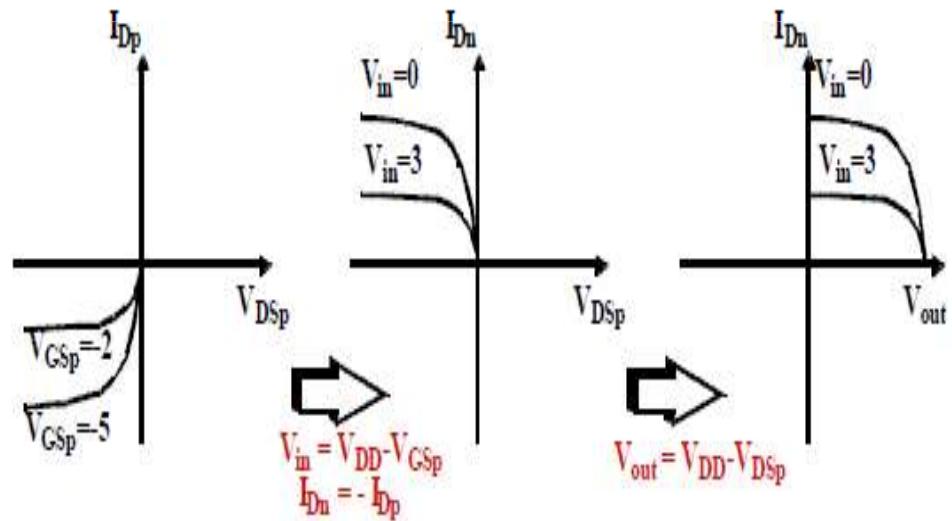
CMOS Properties

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

$$V_{in} = V_{DD} - V_{GSp}$$
$$I_{Dn} = - I_{Dp}$$
$$V_{out} = V_{DD} - V_{DSp}$$



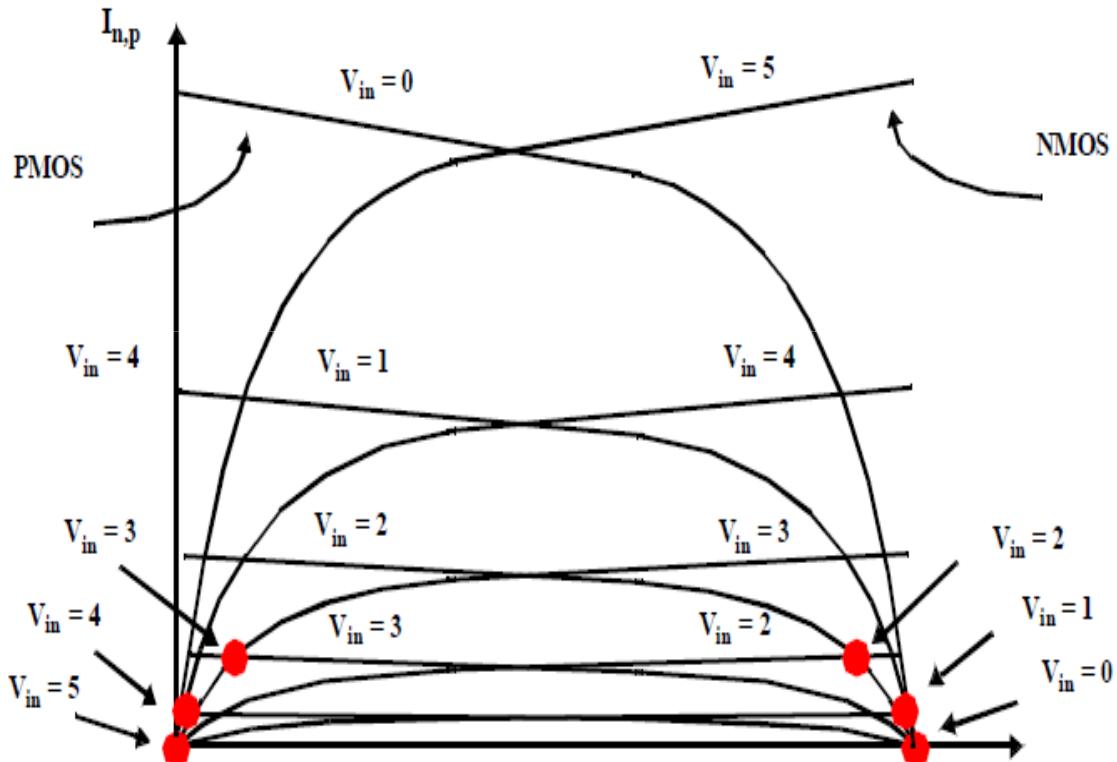
PMOS Load Lines



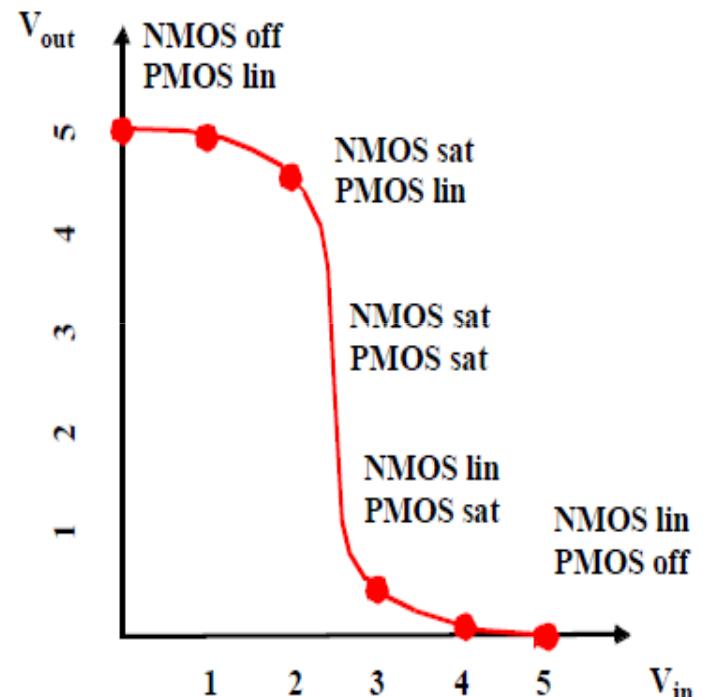
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CMOS Inverter Load Characteristics



CMOS Inverter VTC



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CMOS Inverter: The Static Behavior

The switching threshold, V_M , is defined as the point where $V_{in} = V_{out}$

$$k_n V_{DSATn} \left(V_M - V_{Tn} - \frac{V_{DSATn}}{2} \right) + k_p V_{DSATp} \left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2} \right) = 0$$

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2} \right) + r \left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2} \right)}{1 + r} \quad \text{with } r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{v_{satp} W_p}{v_{satn} W_n}$$

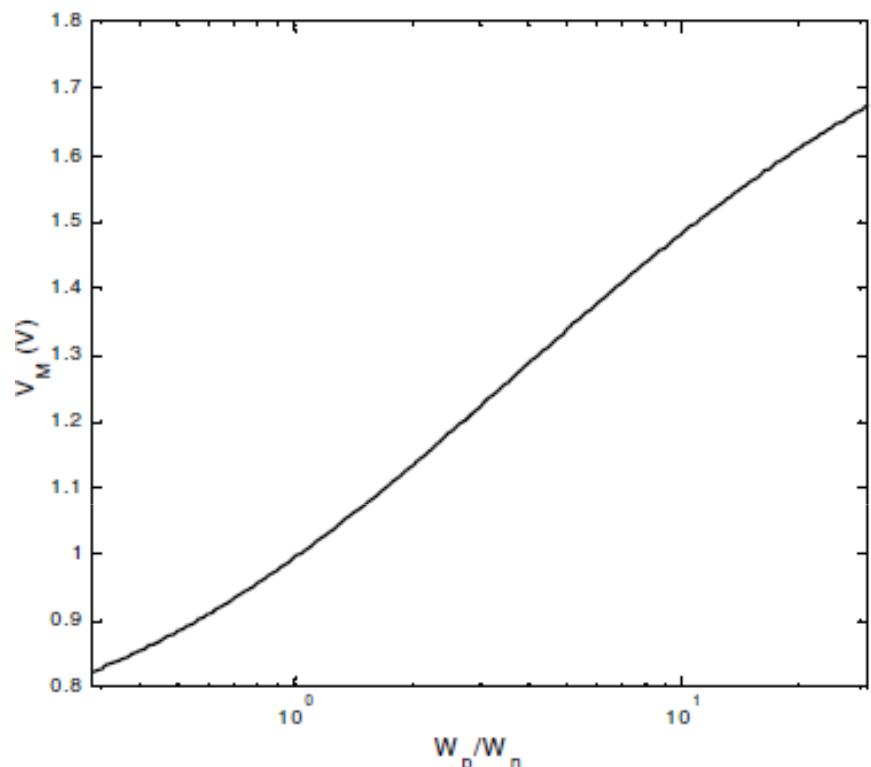
$$V_M \approx \frac{r V_{DD}}{1 + r} \quad (W/L)_p = (W/L)_n \times (V_{DSATn} k'_n) / (V_{DSATn} k'_p)$$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSATn} (V_M - V_{Tn} - V_{DSATn}/2)}{k'_p V_{DSATp} (V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)}$$

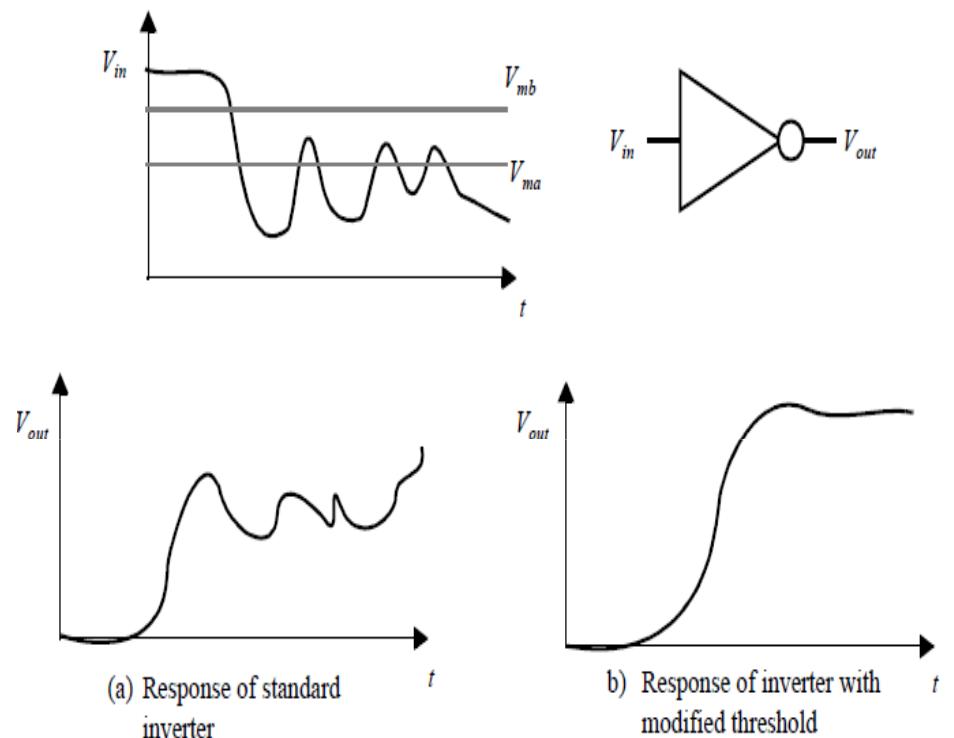


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Changing the inverter threshold can improve the circuit reliability



V_M is relatively insensitive to variations in the device ratio

The effect of changing the W_p/W_n ratio is to shift the transient region of the VTC



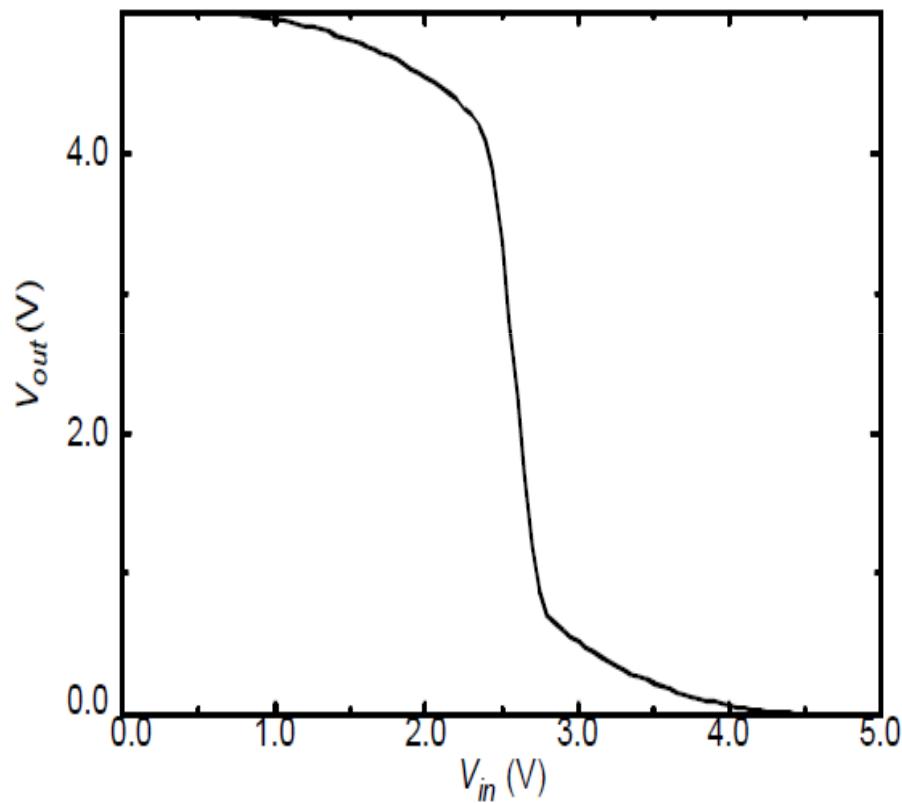
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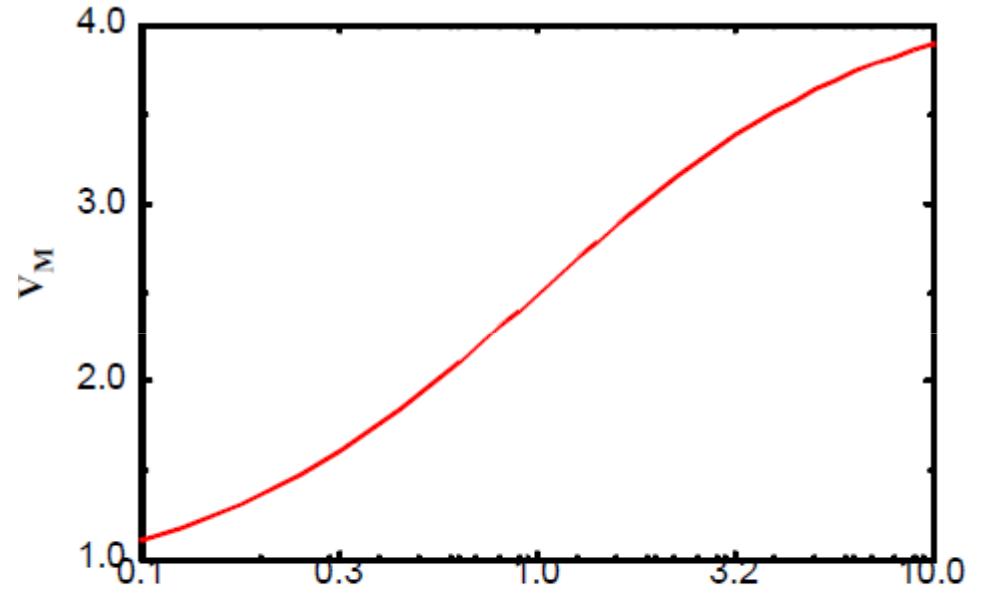




Simulated VTC



Gate Switching Threshold



$$V_M = \frac{r(V_{DD} - |V_{Tp}|) + V_{Tn}}{1+r} \quad \text{with} \quad r = \sqrt{\frac{k_p}{k_n}}$$



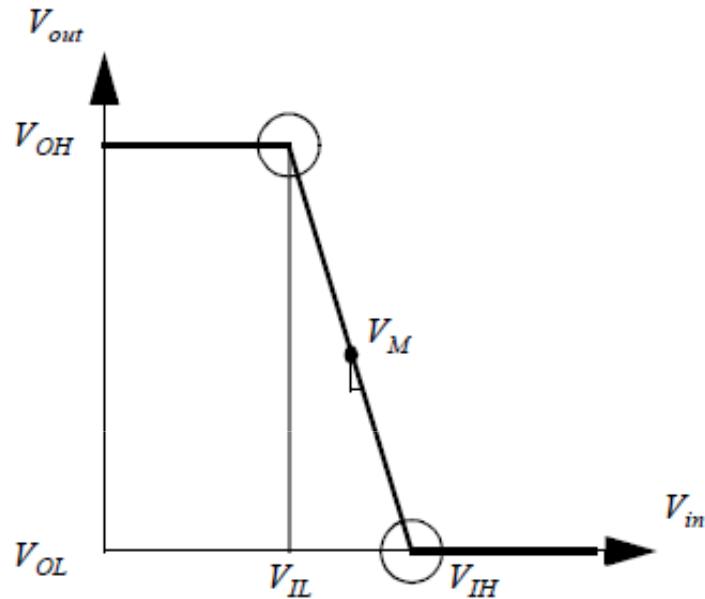
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Noise Margins

V_{IH} and V_{IL} are the operational points of the inverter where $\frac{dV_{out}}{dV_{in}} = -1$



$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \quad NM_L = V_{IL}$$

$$k_n V_{DSATn} \left(V_{in} - V_{Tn} - \frac{V_{DSATn}}{2} \right) (1 + \lambda_n V_{out}) +$$

$$k_p V_{DSATp} \left(V_{in} - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2} \right) (1 + \lambda_p V_{out} - \lambda_p V_{DD}) = 0$$

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n V_{DSATn} (1 + \lambda_n V_{out}) + k_p V_{DSATp} (1 + \lambda_p V_{out} - \lambda_p V_{DD})}{\lambda_n k_n V_{DSATn} (V_{in} - V_{Tn} - V_{DSATn}/2) + \lambda_p k_p V_{DSATp} (V_{in} - V_{DD} - V_{Tp} - V_{DSATp}/2)}$$

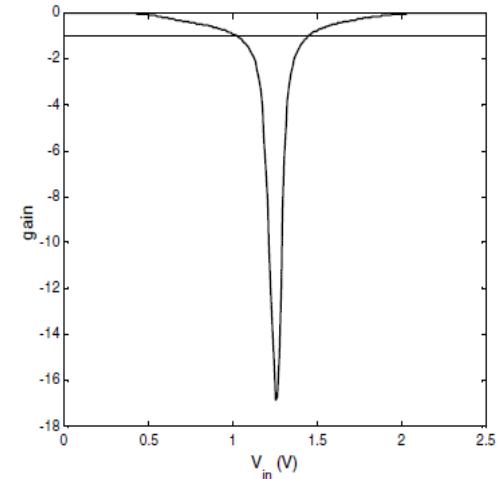
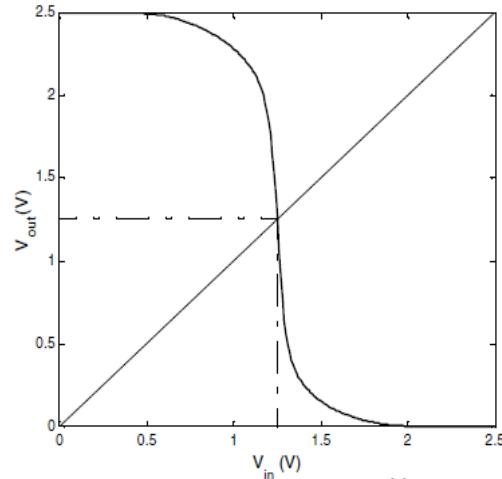


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$$g = -\frac{1}{I_D(V_M)} \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$

$$\approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$



Assume an inverter in the generic 0.25 μm CMOS technology designed with a PMOS/NMOS ratio of 3.4 and with the NMOS transistor minimum size ($W = 0.375 \mu\text{m}$, $L = 0.25 \mu\text{m}$, $W/L = 1.5$). We first compute the gain at V_M ($= 1.25 \text{ V}$),

$$I_D(V_M) = 1.5 \times 115 \times 10^{-6} \times 0.63 \times (1.25 - 0.43 - 0.63/2) \times (1 + 0.06 \times 1.25) = 59 \times 10^{-6} \text{ A}$$

$$g = -\frac{1}{59 \times 10^{-6}} \frac{1.5 \times 115 \times 10^{-6} \times 0.63 + 1.5 \times 3.4 \times 30 \times 10^{-6} \times 1.0}{0.06 + 0.1} = -27.5$$

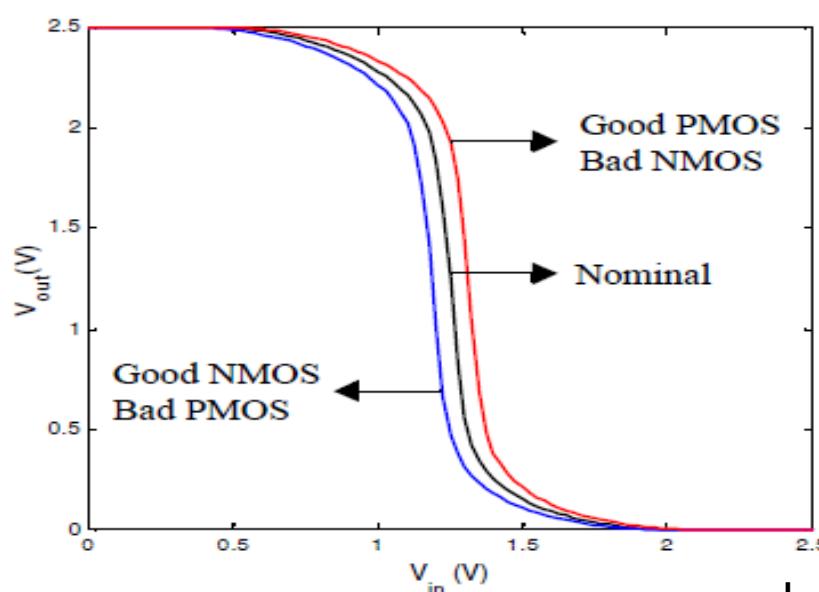
This yields the following values for V_{IL} , V_{IH} , NM_L , NM_H :

$$V_{IL} = 1.2 \text{ V}, V_{IH} = 1.3 \text{ V}, NM_L = NM_H = 1.2.$$

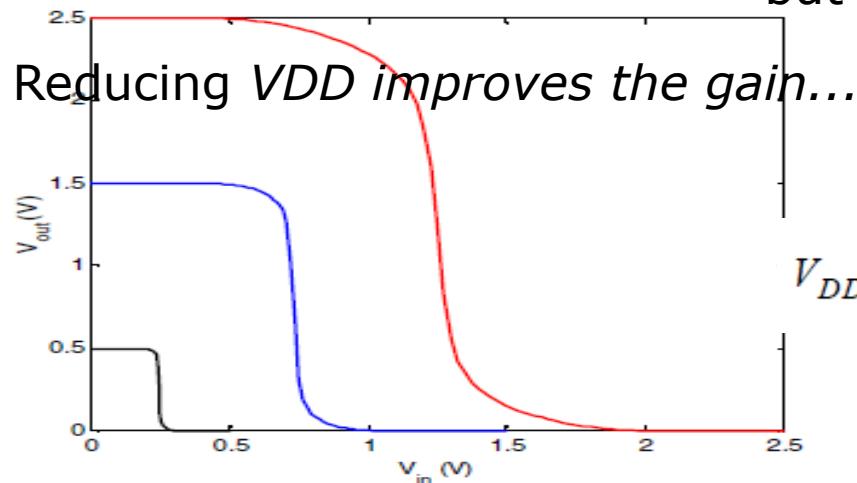


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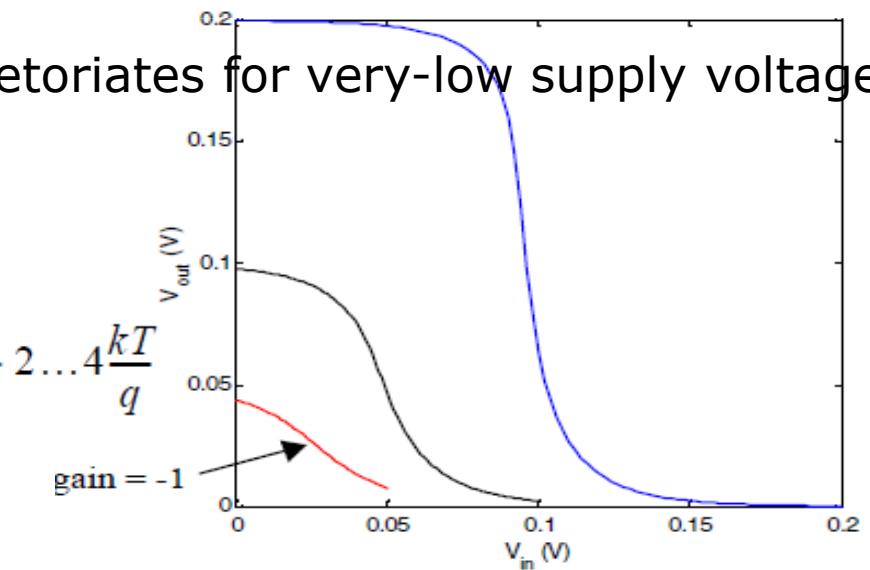
Impact of device variations on static CMOS inverter VTC. The “good” device has a smaller oxide thickness (- 3nm), a smaller length (-25 nm), a higher width (+30 nm), and a smaller threshold (-60 mV). The opposite is true for the “bad” transistor.



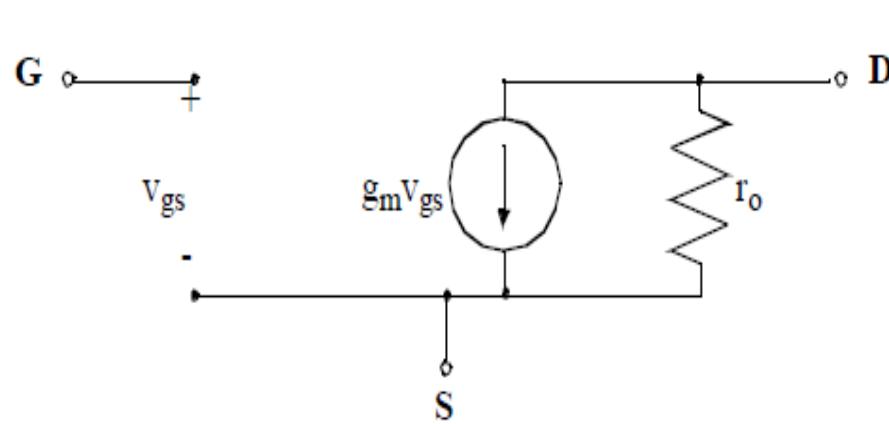
but it deteriorates for very-low supply voltages

$$V_{DDmin} > 2 \dots 4 \frac{kT}{q}$$

$$\text{gain} = -1$$

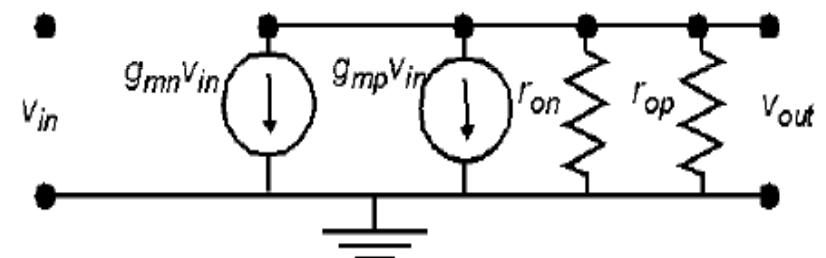


MOS Transistor Small Signal Model



At V_{IH} (V_{IL}): $\frac{\partial V_{out}}{\partial V_{in}} = -1$

small-signal model of inverter

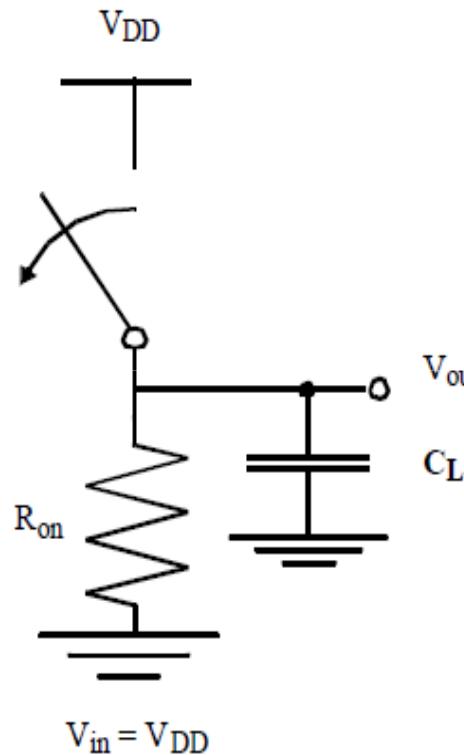


	g_m	r_o
linear	kV_{DS}	$[k(V_{GS}V_T V_{DS})]^{-1}$
saturation	$k(V_{GS}V_T)$	$1/N_D$

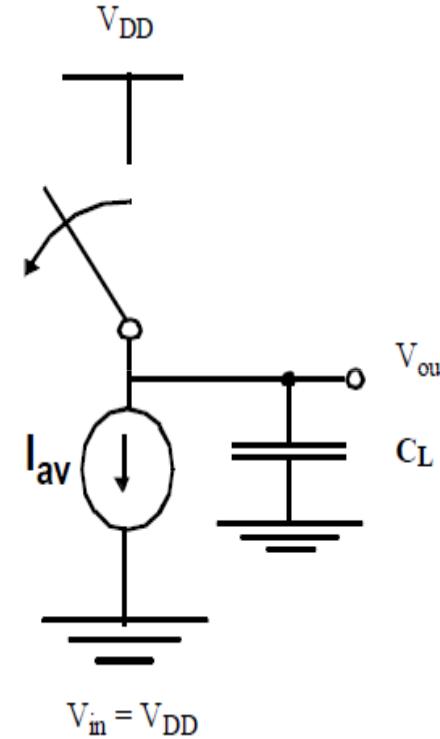
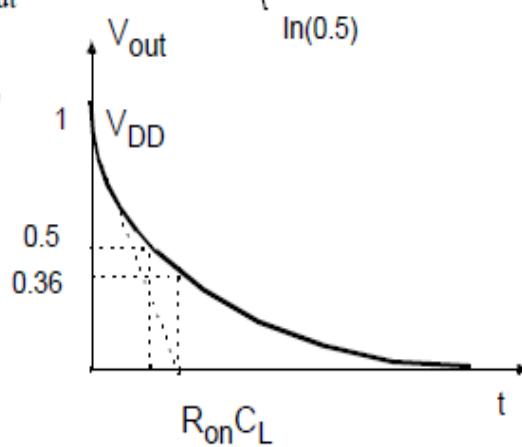
$$g = \frac{v_{out}}{v_{in}} = -(g_{mn} + g_{mp}) \times (r_{on} \parallel r_{op}) = -1$$

Determining V_{IH} and V_{IL}

CMOS Inverter: Transient Response



$$t_{pHL} = f(R_{on}, C_L) \\ = 0.69 R_{on} C_L$$



$$t_{pHL} = \frac{C_L V_{swing}}{I_{av}}$$

$$\sim \frac{C_L}{k_n V_{DD}}$$

CMOS Inverter Propagation Delay

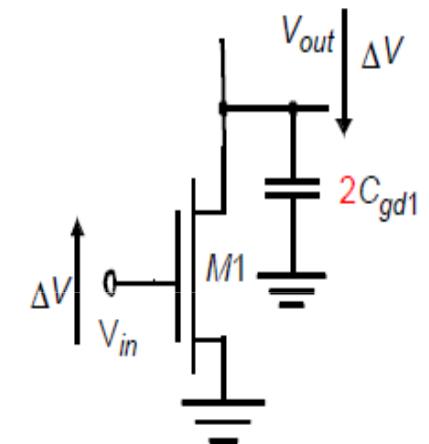
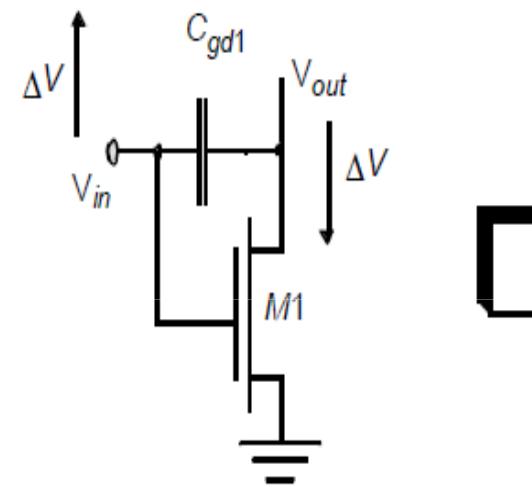
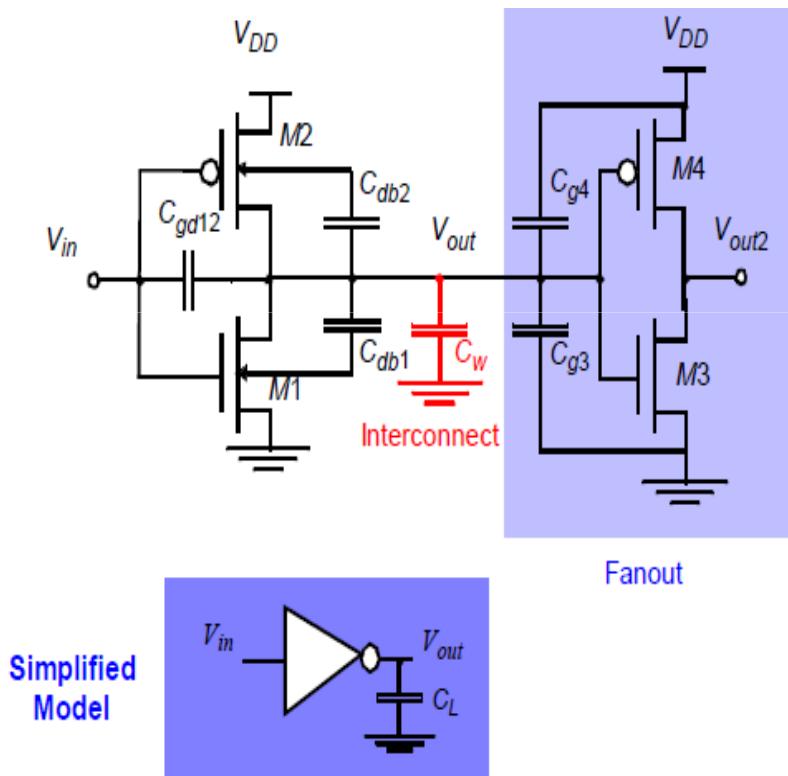


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Computing the Capacitances

The Miller Effect

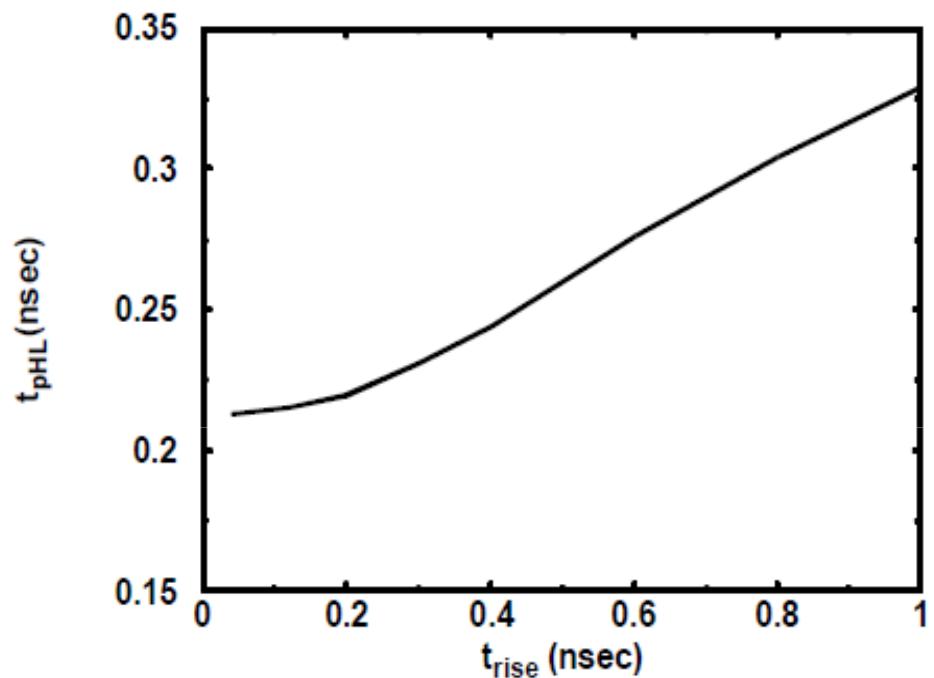


"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."



Computing the Capacitances

Capacitor	Expression
C_{gd1}	$2 \text{ CGD0 } W_n$
C_{gd2}	$2 \text{ CGD0 } W_p$
C_{db1}	$K_{eqn} (AD_n CJ + PD_n CJSW)$
C_{db2}	$K_{eqp} (AD_p CJ + PD_p CJSW)$
C_{g3}	$C_{ox} W_n L_n$
C_{g4}	$C_{ox} W_p L_p$
C_w	From Extraction
C_L	Σ



$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/12)^2}$$

Impact of Rise Time on Delay

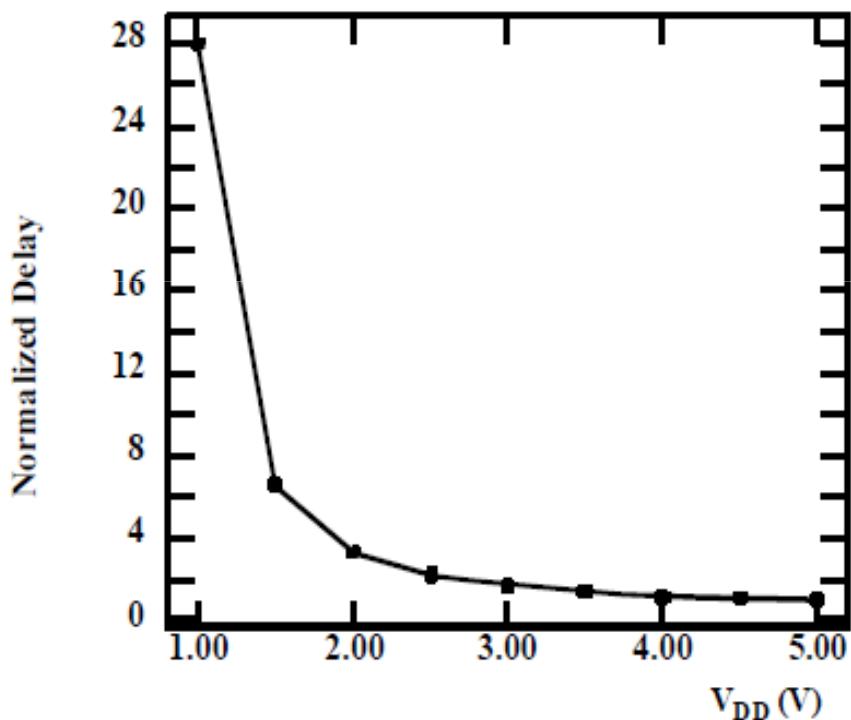


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Delay as a function of V_{DD}



Where Does Power Go in CMOS?

- Dynamic Power Consumption
Charging and Discharging Capacitors
- Short Circuit Currents
Short Circuit Path between Supply Rails during Switching
- Leakage
Leaking diodes and transistors

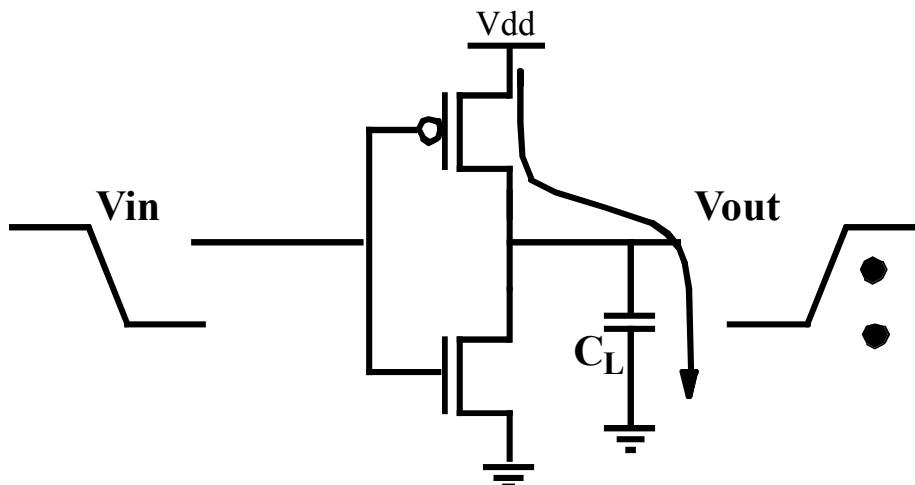


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Dynamic Power Dissipation

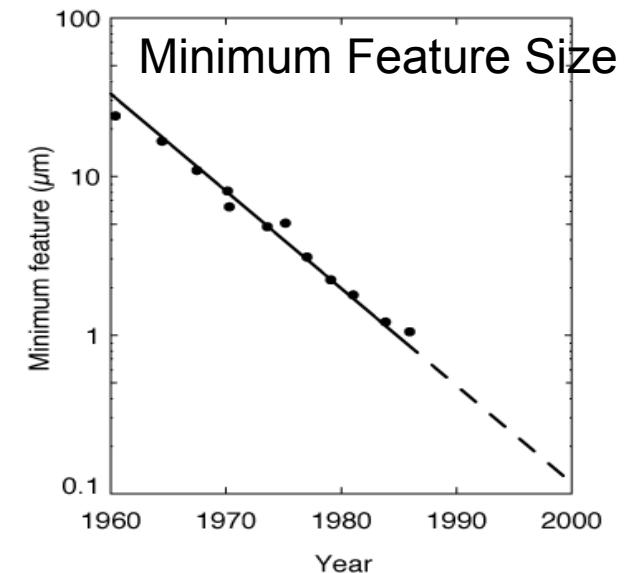


$$\text{Energy/transition} = C_L * V_{dd}^2$$

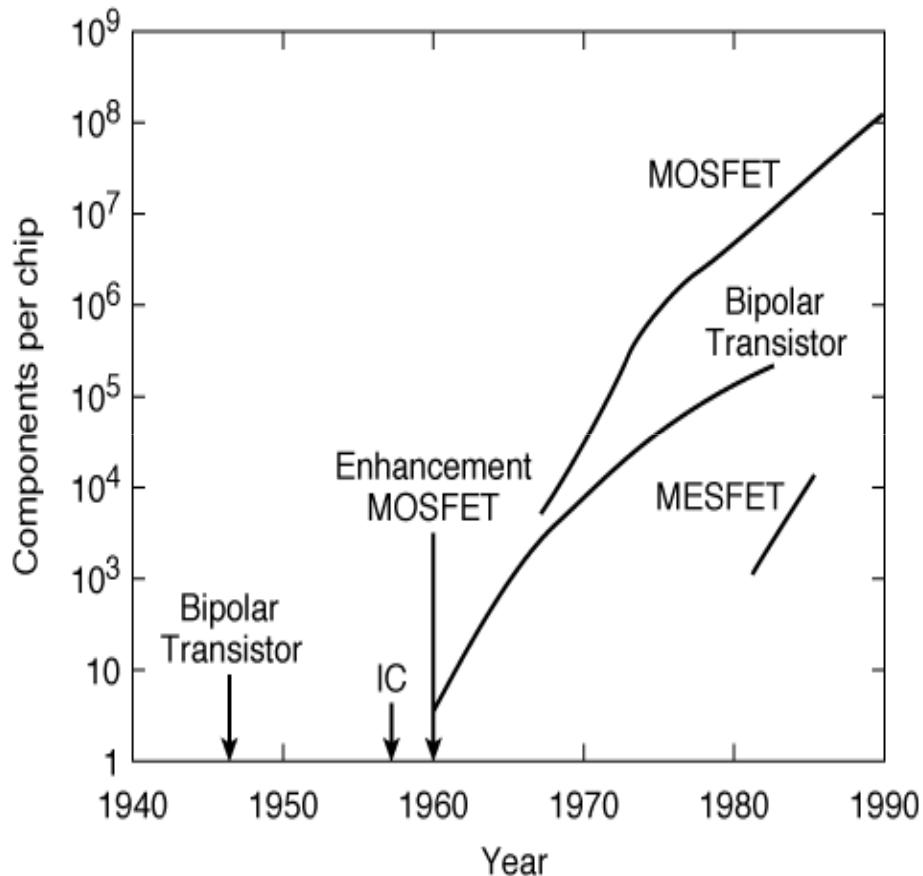
$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- Not a function of transistor sizes!
- Need to reduce C_L , V_{dd} , and f to reduce power.

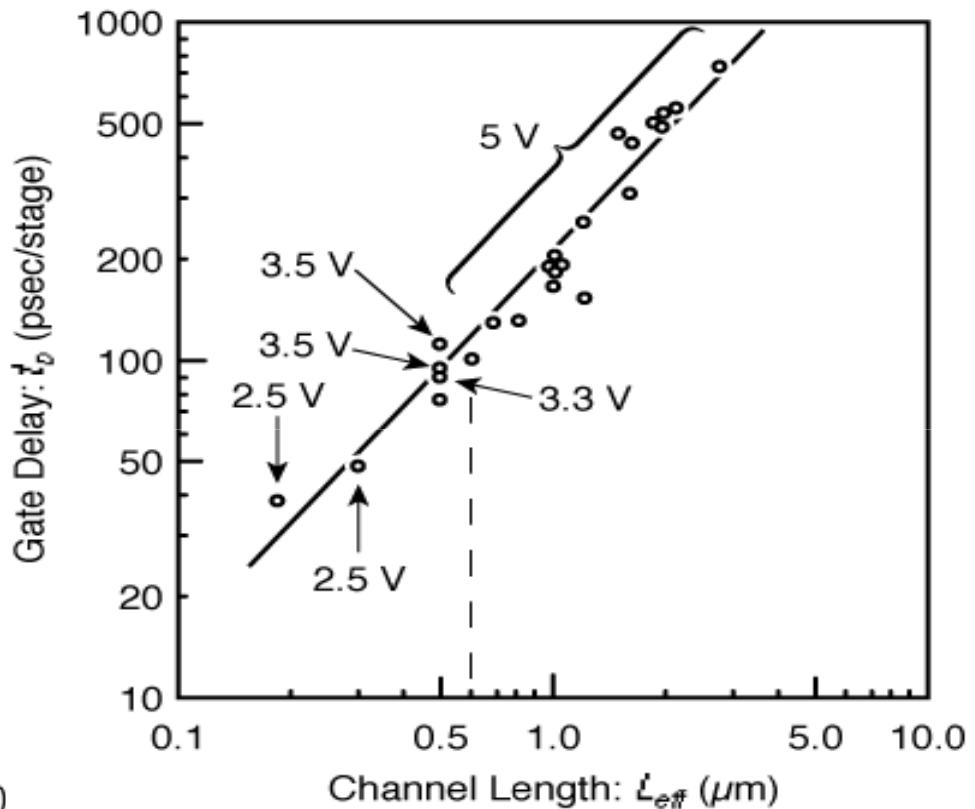
Year of Introduction	1994	1997	2000	2003	2006	2009
Channel length (μm)	0.4	0.3	0.25	0.18	0.13	0.1
Gate oxide (nm)	12	7	6	4.5	4	4
V_{DD} (V)	3.3	2.2	2.2	1.5	1.5	1.5
V_T (V)	0.7	0.7	0.7	0.6	0.6	0.6
NMOS I_{Dsat} (mA/ μm) (@ $V_{GS} = V_{DD}$)	0.35	0.27	0.31	0.21	0.29	0.33
PMOS I_{Dsat} (mA/ μm) (@ $V_{GS} = V_{DD}$)	0.16	0.11	0.14	0.09	0.13	0.16



Number of components per chip



Propagation Delay Scaling



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Technology Scaling Models

- **Full Scaling (Constant Electrical Field)**

ideal model — dimensions and voltage scale together by the same factor S

- **Fixed Voltage Scaling**

most common model until recently — only dimensions scale, voltages remain constant

- **General Scaling**

most realistic for todays situation — voltages and dimensions scale with different factors



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Scaling Relationships for Long Channel Devices

Parameter	Relation	Full Scaling	General Scaling	Fixed Voltage Scaling
W, L, t_{ox}		$1/S$	$1/S$	$1/S$
V_{DD}, V_T		$1/S$	$1/U$	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
Area/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_L	$C_{ox}WL$	$1/S$	$1/S$	$1/S$
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{av}	$k_{n,p} V^2$	$1/S$	S/U^2	S
t_p (intrinsic)	$C_L V / I_{av}$	$1/S$	U/S^2	$1/S^2$
P_{av}	$C_L V^2 / t_p$	$1/S^2$	S/U^3	S
PDP	$C_L V^2$	$1/S^3$	$1/SU^2$	$1/S$

Table 3.1 : Scaling Relationships for Long Channel Devices



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Scaling of Short Channel Devices

Parameter	Relation	Full Scaling	General Scaling	Fixed Voltage Scaling
I_{av}	$C_{ox}WV$	$1/S$	$1/U$	1
J_{av}	I_{av}/Area	S	S^2/U	S^2
t_p (intrinsic)	$C_L V / I_{av}$	$1/S$	$1/S$	$1/S$
P_{av}	$C_L V^2 / t_p$	$1/S^2$	$1/U^2$	1



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Propagation Delay from a Design Perspective

NMOS/PMOS Ratio

$$C_L = (C_{dp1} + C_{dn1}) + (C_{gp2} + C_{gn2}) + C_W$$

PMOS devices are made β times larger than the NMOS ones ($\beta = (W/L)_p / (W/L)_n$)

$$C_{dp1} \approx \beta \ C_{dn1} \text{ and } C_{gp2} \approx \beta \ C_{gn2}.$$

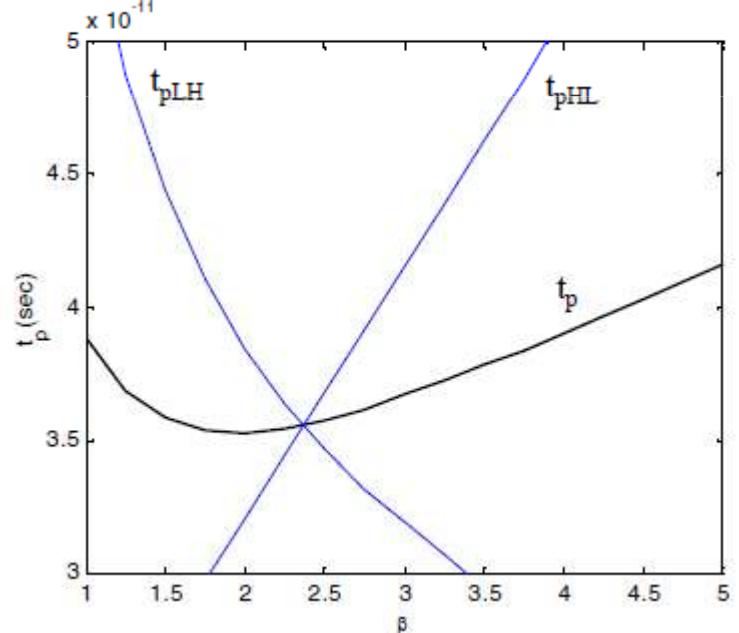
$$C_L = (1 + \beta)(C_{dn1} + C_{gn2}) + C_W$$

$$t_p = \frac{0.69}{2}((1 + \beta)(C_{dn1} + C_{gn2}) + C_W) \left(R_{eqn} + \frac{R_{eqp}}{\beta} \right)$$

$$= 0.345((1 + \beta)(C_{dn1} + C_{gn2}) + C_W)R_{eqn} \left(1 + \frac{r}{\beta} \right)$$

$$\beta_{opt} = \sqrt{r \left(1 + \frac{C_w}{C_{dn1} + C_{gn2}} \right)}$$

$$r (= R_{eqp}/R_{eqn})$$



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Sizing Inverters for Performance

$$t_p = 0.69 R_{eq} (C_{int} + C_{ext})$$

$$C_{int} = S C_{iref}$$

$$= 0.69 R_{eq} C_{int} (1 + C_{ext}/C_{int}) = t_{p0} (1 + C_{ext}/C_{int})$$

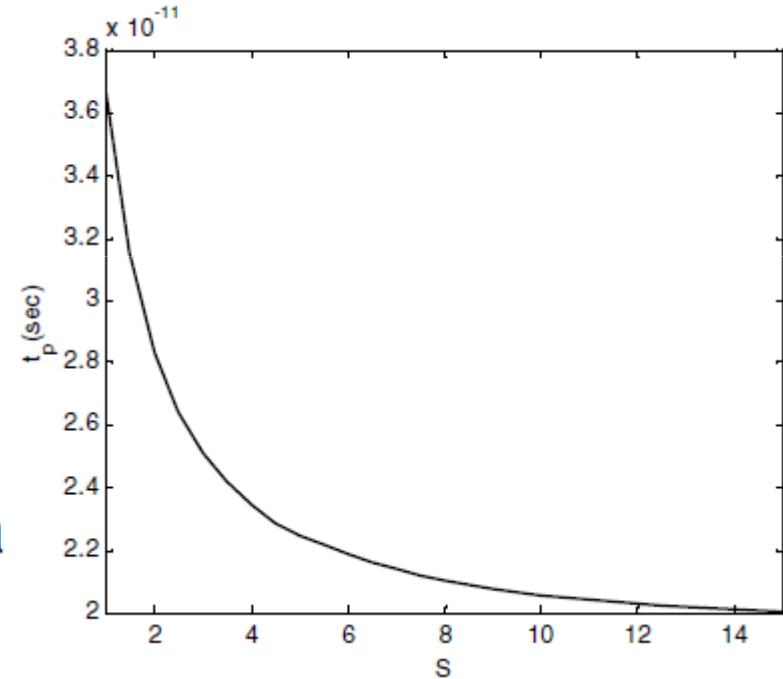
$$R_{eq} = R_{ref}/S.$$

$$t_p = 0.69 (R_{ref}/S) (S C_{iref}) (1 + C_{ext}/(S C_{iref}))$$

$$= 0.69 R_{ref} C_{iref} \left(1 + \frac{C_{ext}}{S C_{iref}}\right) = t_{p0} \left(1 + \frac{C_{ext}}{S C_{iref}}\right)$$

- The intrinsic delay of the inverter t_{p0} is independent of the sizing of the gate
- Making S infinitely large yields the maximum obtainable performance gain

intrinsic or unloaded delay. $t_{p0} = 0.69 R_{eq} C_{int}$



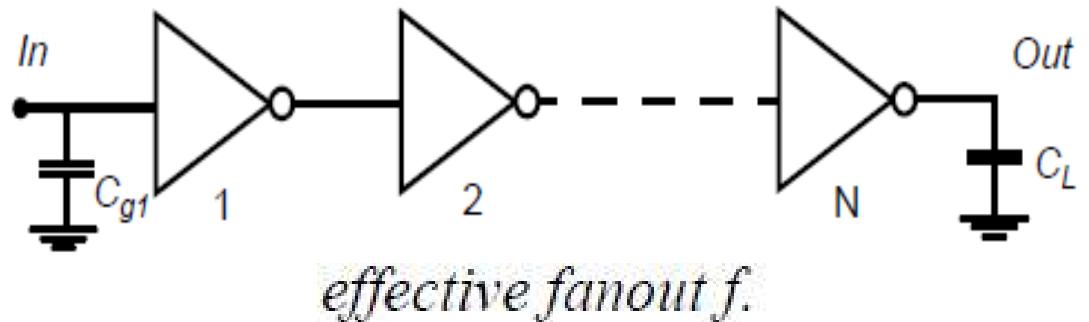
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Sizing A Chain of Inverters

$$C_{int} = \gamma C_g$$

$$t_p = t_{p0} \left(1 + \frac{C_{ext}}{\gamma C_g} \right) = t_{p0} (1 + f/\gamma)$$



$$t_{p,j} = t_{p0} \left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}} \right) = t_{p0} (1 + f_j/\gamma)$$

$$t_p = \sum_{j=1}^N t_{p,j} = t_{p0} \sum_{j=1}^N \left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}} \right), \text{ with } C_{g,N+1} = C_L$$

$$C_{g,j} = \sqrt{C_{g,j-1} C_{g,j+1}}. \quad f = \sqrt[N]{C_L / C_{g,1}} = \sqrt[N]{F} \quad t_p = N t_{p0} (1 + \sqrt[N]{F}/\gamma).$$



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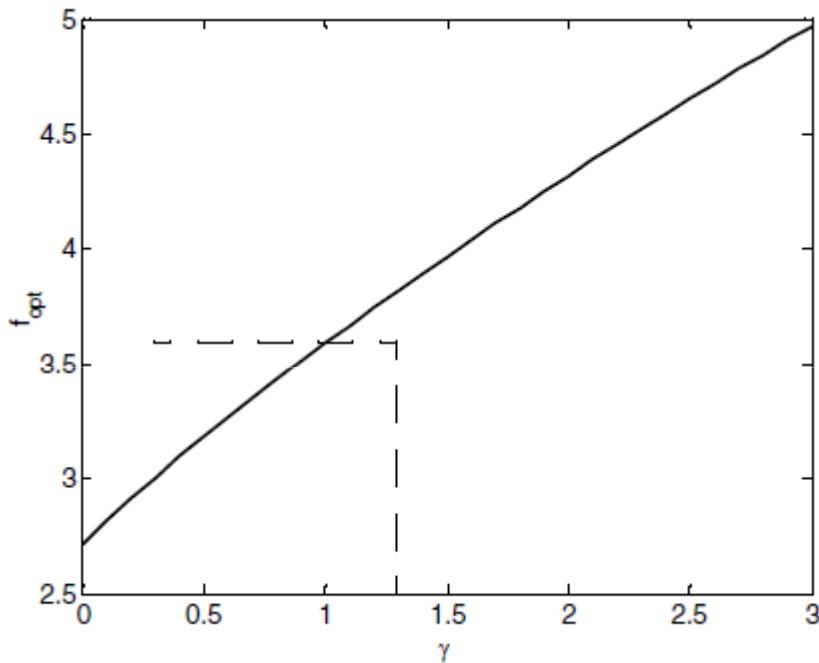
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Optimizing the number of stages in an inverter chain.

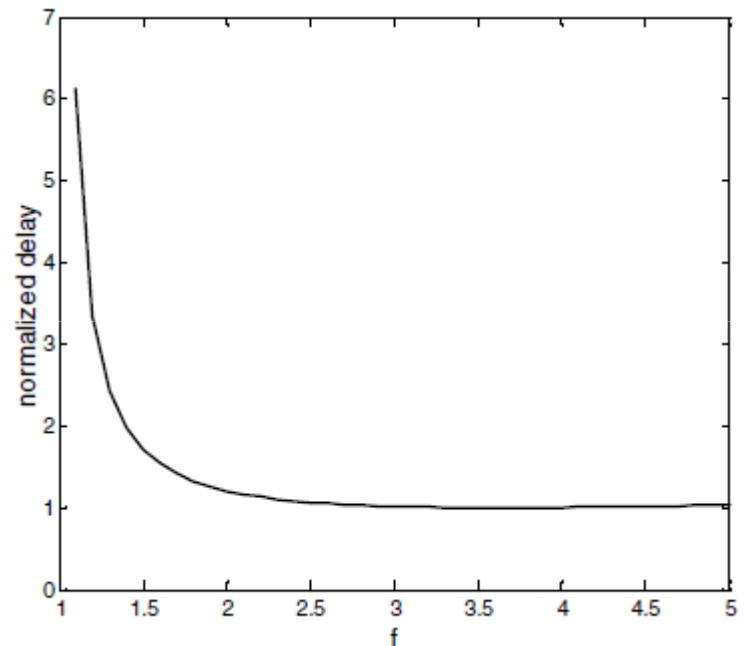
$$f = e^{(1 + \gamma/f)}$$

$$N = \ln(F)$$

$$f = 2.71828 = e$$



Optimum effective fanout f (or inverter scaling factor) as a function of the self-loading factor g in an inverter chain.



Normalized propagation delay ($tp/(tp_{opt})$) as a function of the effective fanout f for $g=1$.

Reducing V_{DD} has a quadratic effect

A reduction in the switching activity

Lowering the physical capacitance minimal size

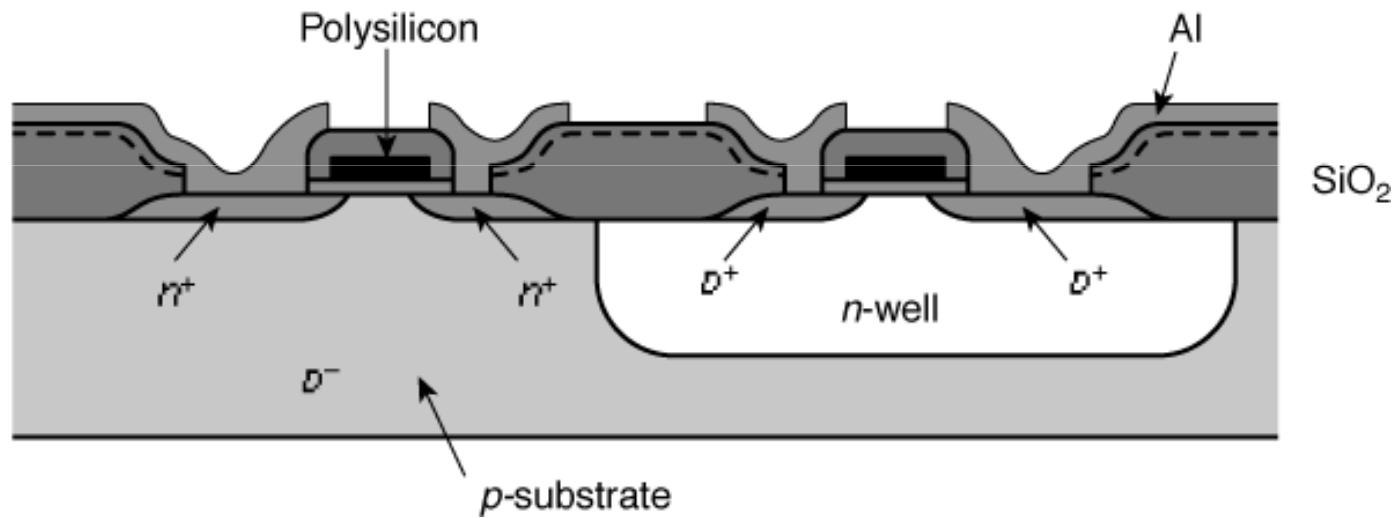
Device sizing, combined with supply voltage reduction, is a very effective approach in reducing the energy consumption of a logic network.



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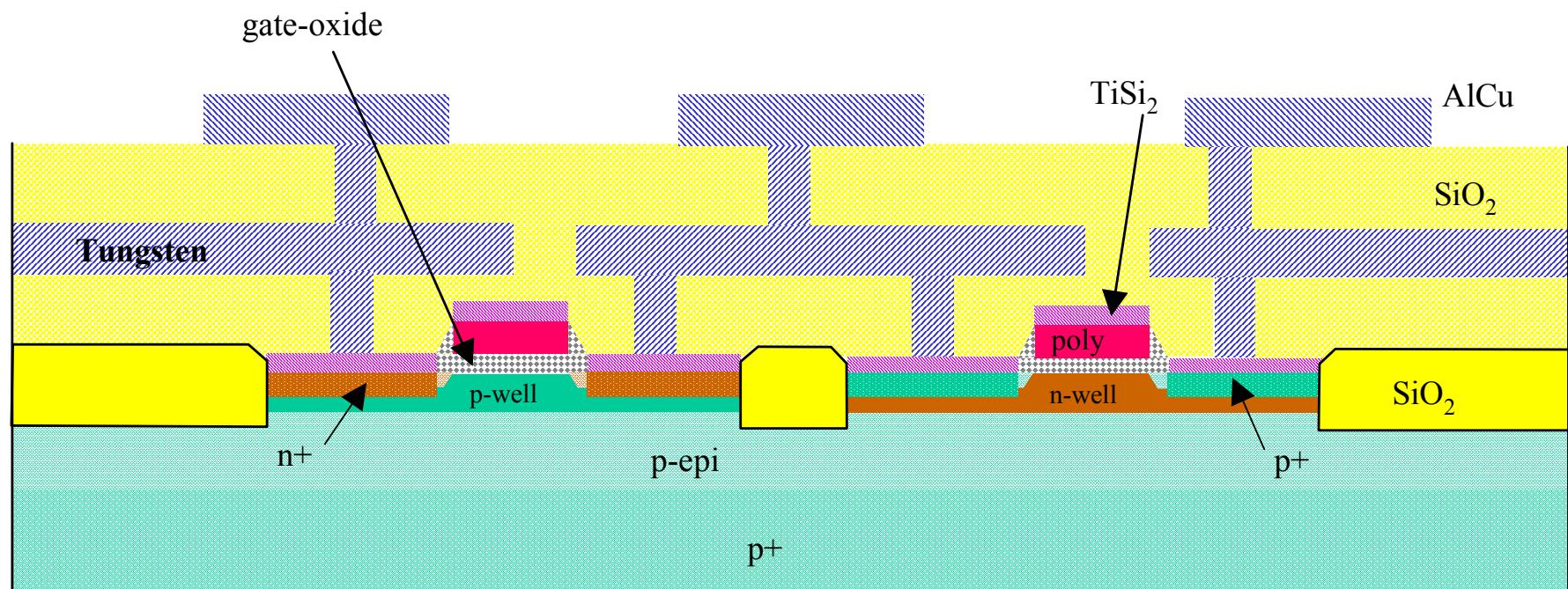
CMOS Process



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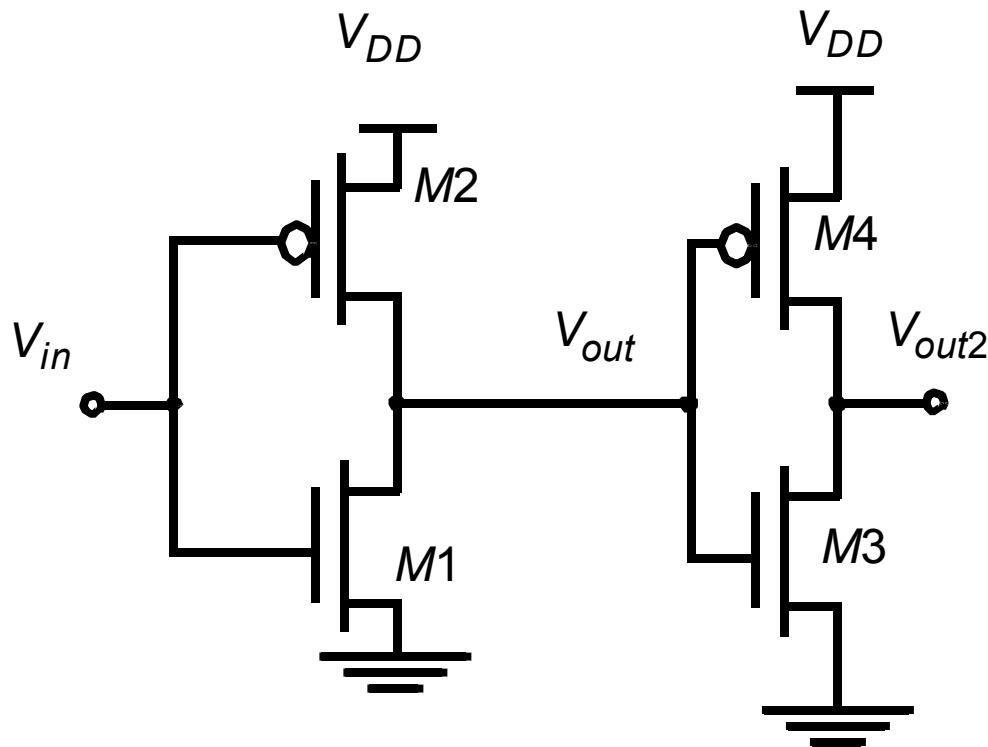
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A Modern CMOS Process



Dual-Well Trench-Isolated CMOS Process

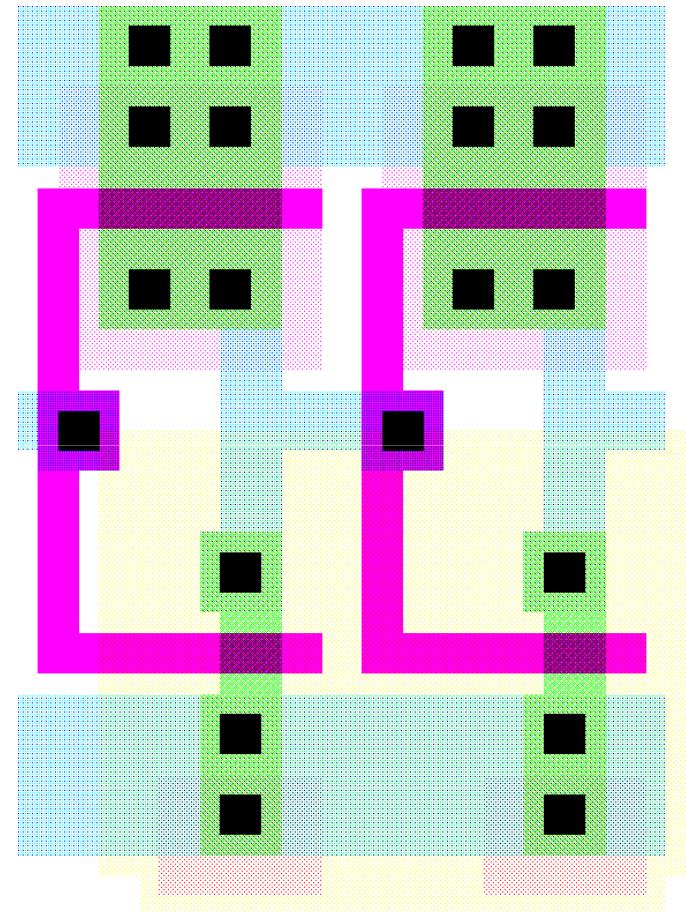
Circuit Under Design



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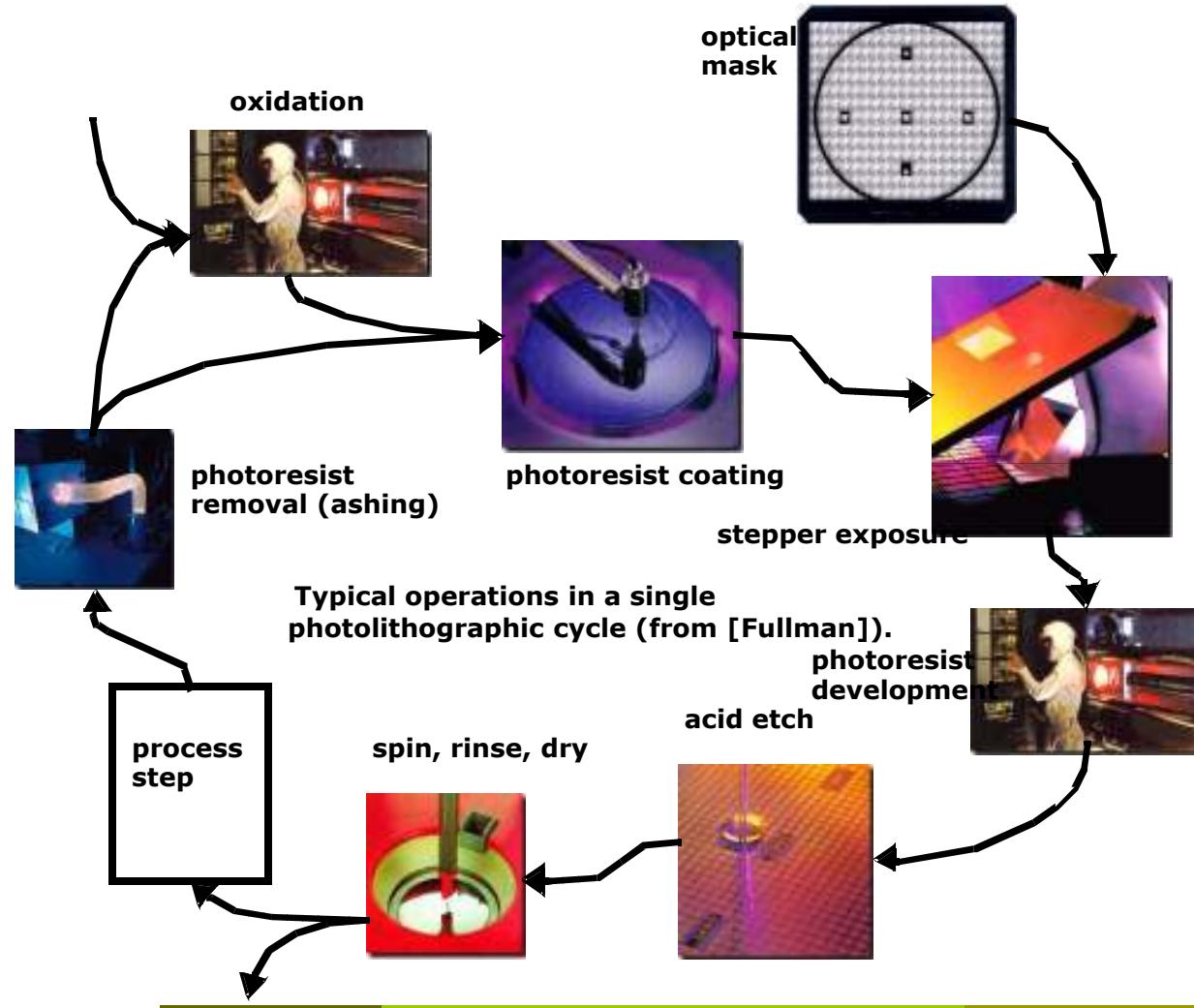
Its Layout View



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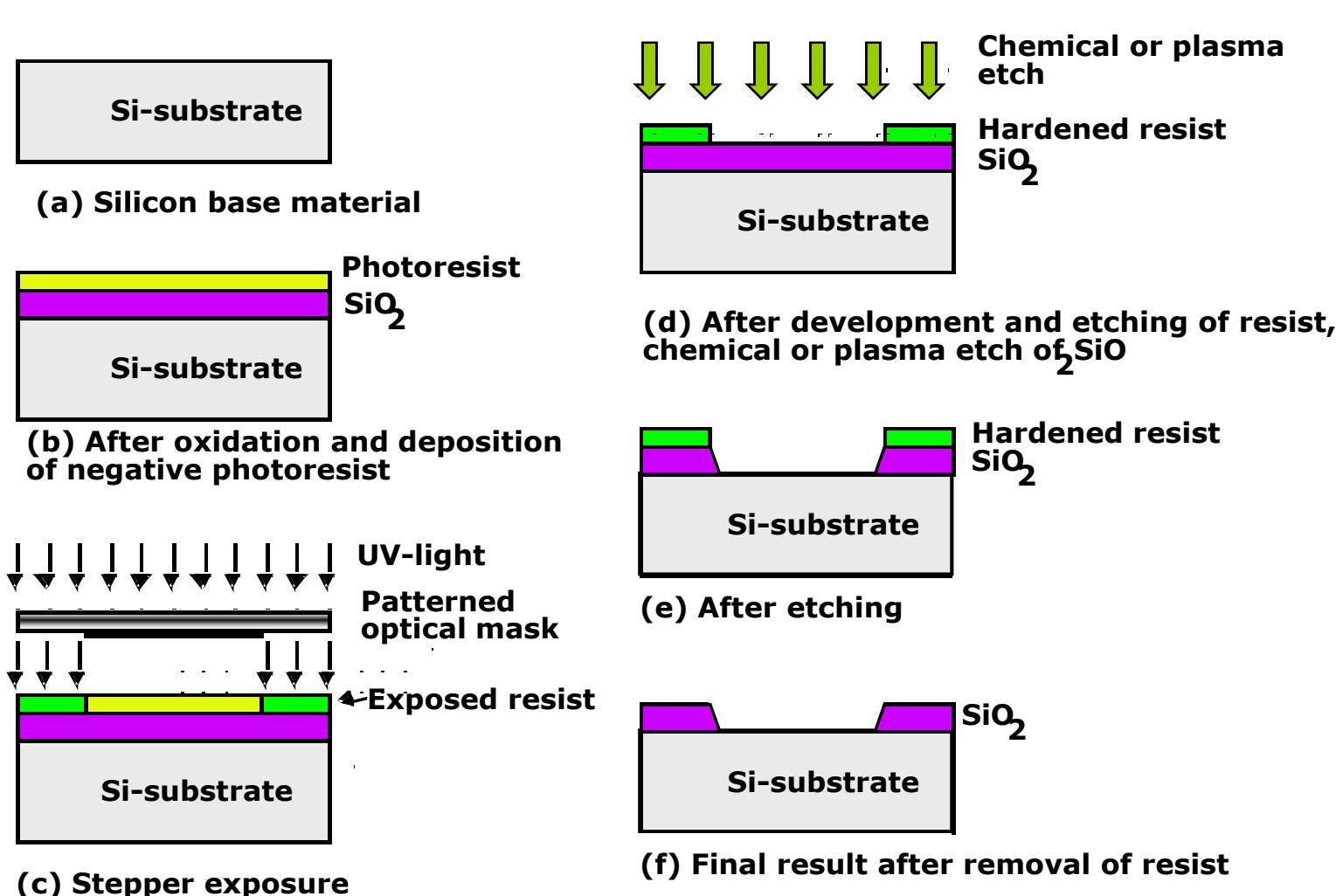
Photo-Lithographic Process



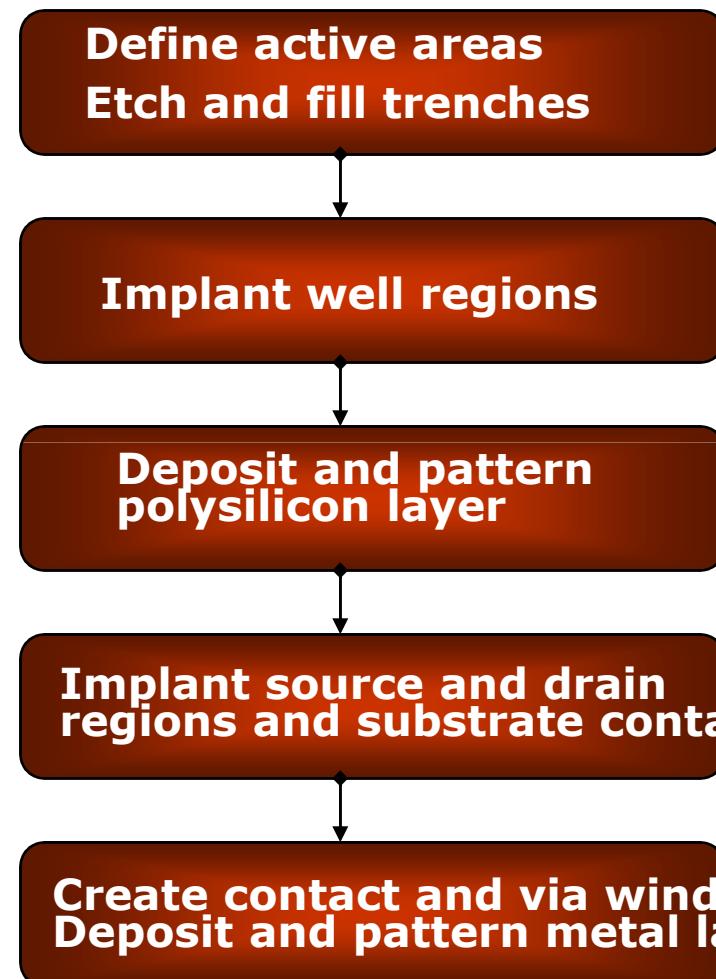
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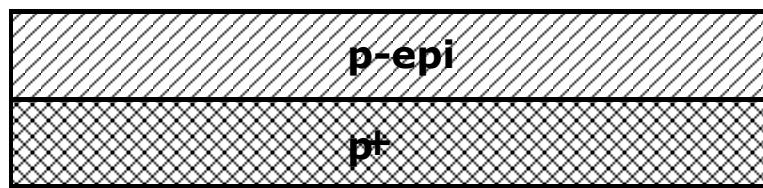
Patterning of SiO₂



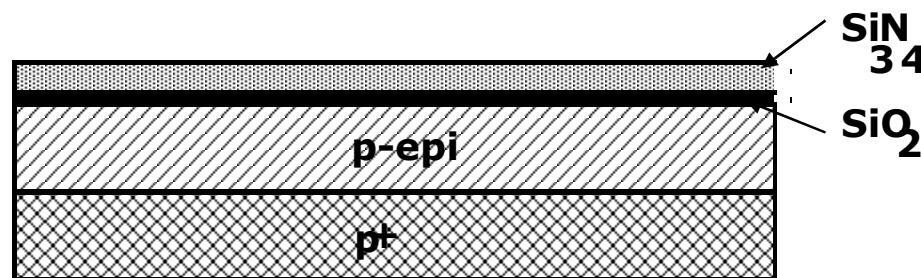
CMOS Process at a Glance



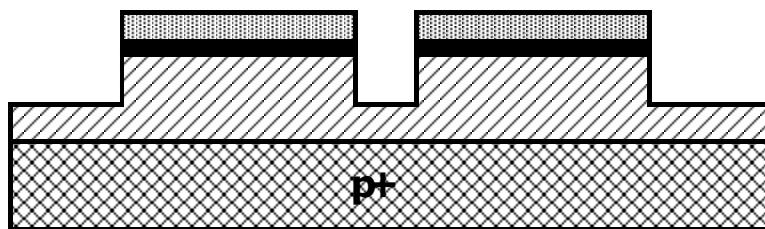
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer



(b) After deposition of gate-oxide sacrificial nitride (acts as a buffer layer)



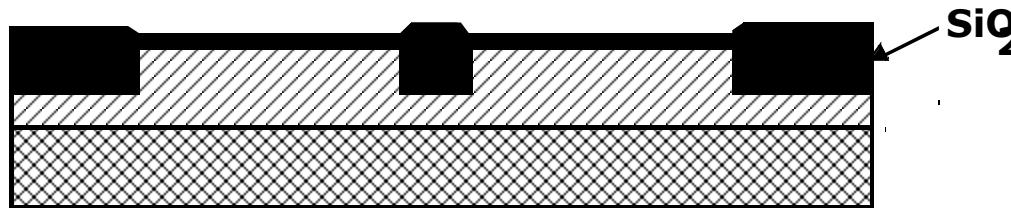
(c) After plasma etch of insulating trenches using the inverse of the active area mask



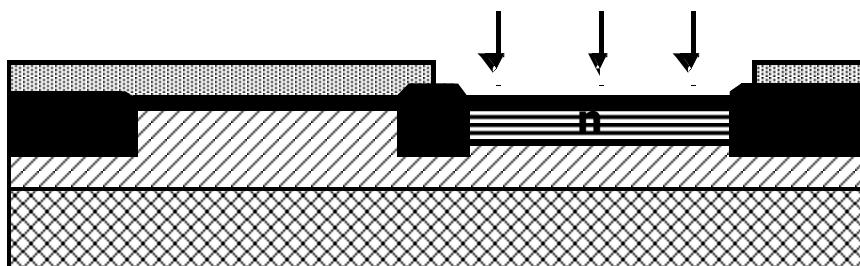
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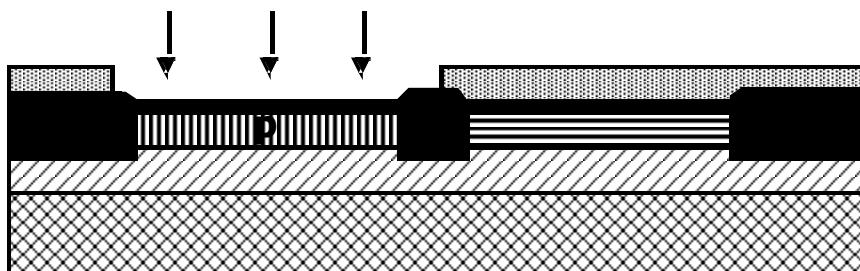
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride



(e) After n-well and V_{TP} adjust implants



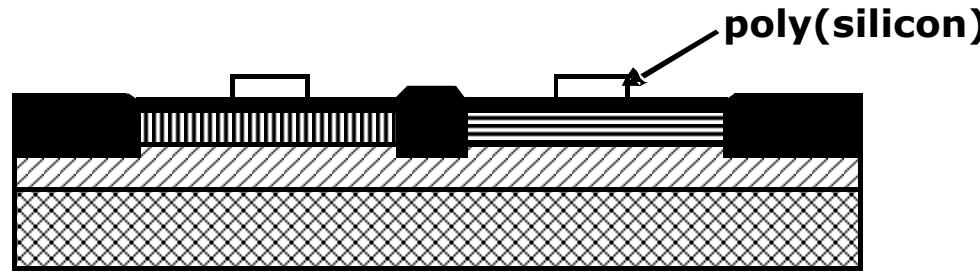
(f) After p-well and V_{TN} adjust implants



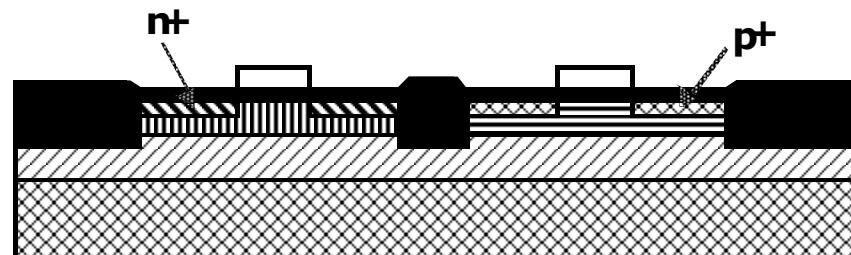
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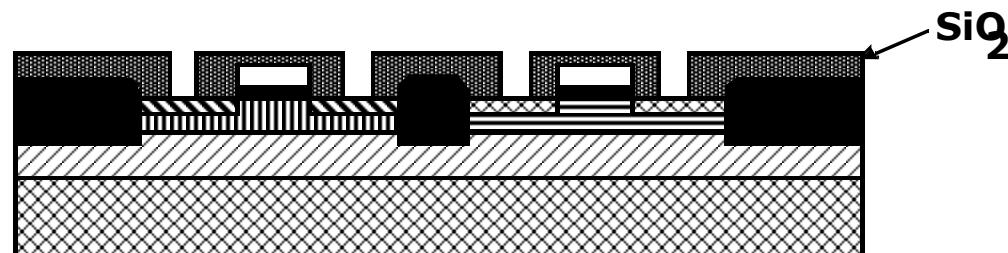
CMOS Process Walk-Through



(g) After polysilicon deposition and etch



(h) After $n+$ source/drain and $p+$ source/drain implants. These steps also dope the polysilicon.



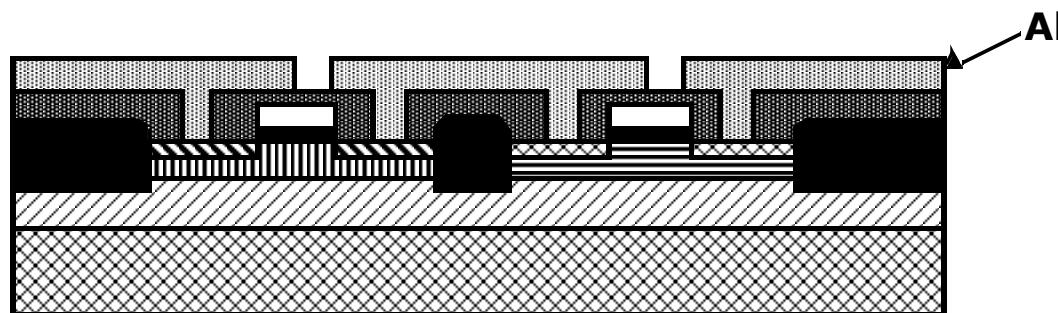
(i) After deposition of SiO_2 insulator and contact hole etch.



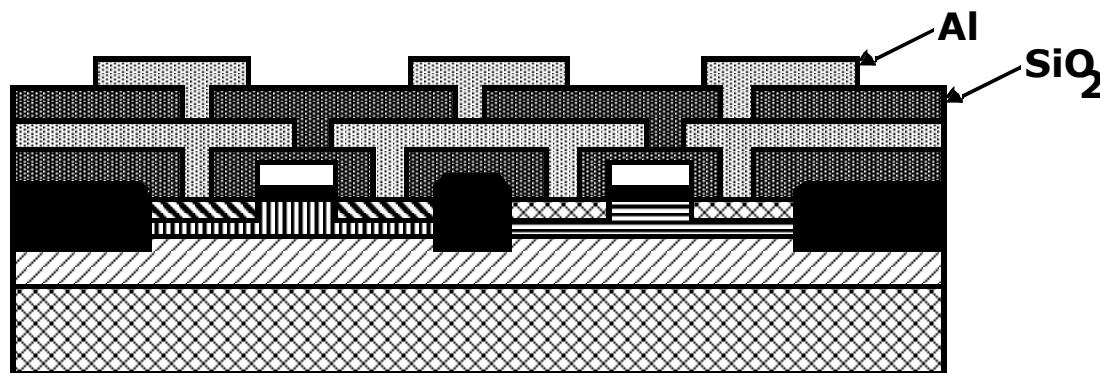
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CMOS Process Walk-Through



(j) After deposition and patterning of first Al layer.



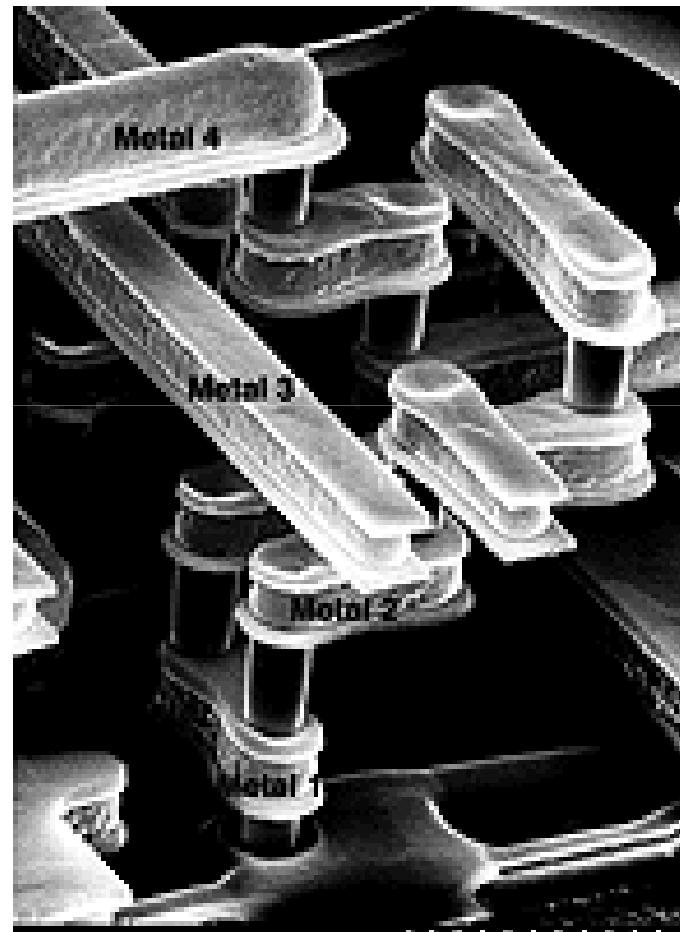
(k) After deposition of SiO₂ insulator, etching of via's, deposition and patterning of second layer of Al.



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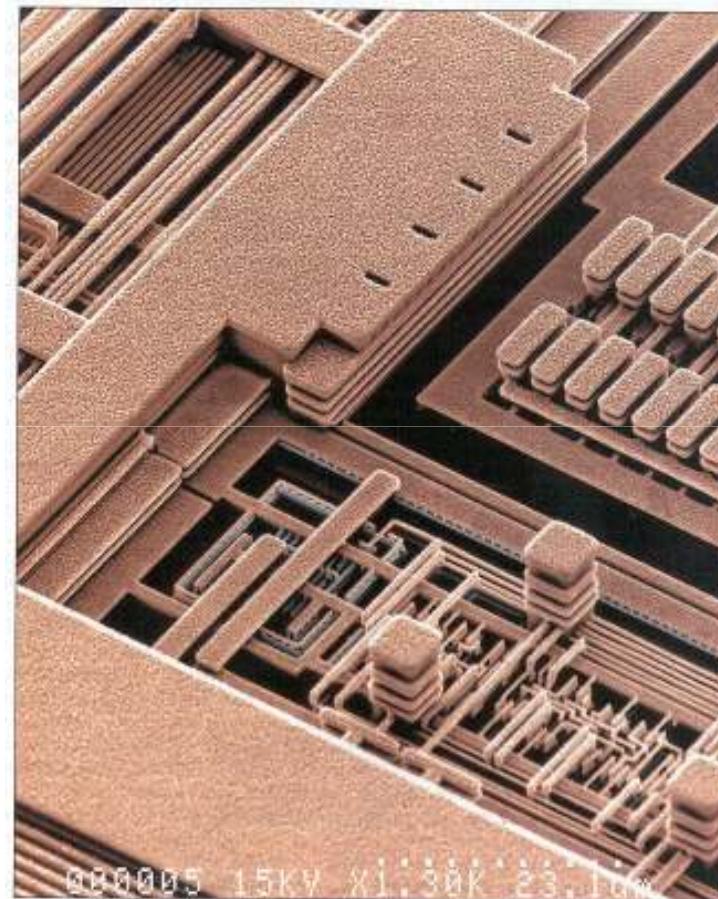
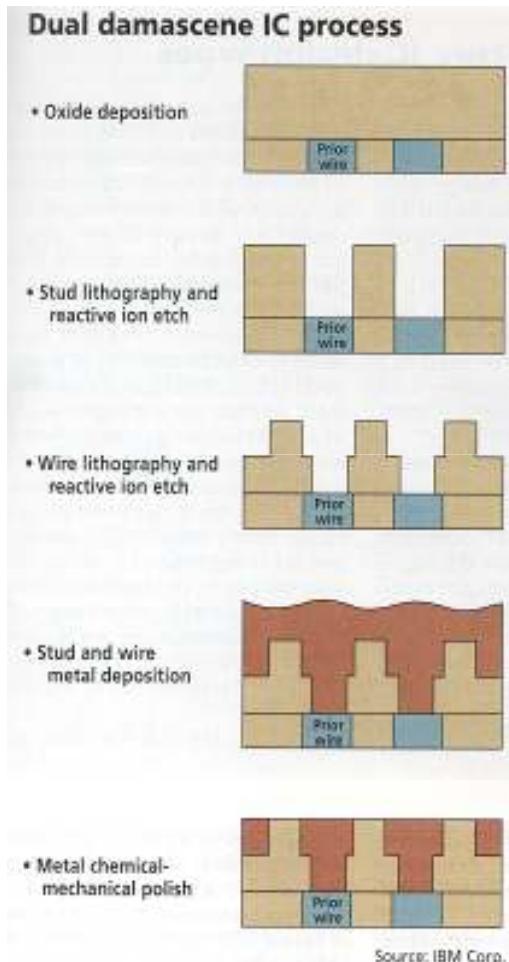
Advanced Metallization



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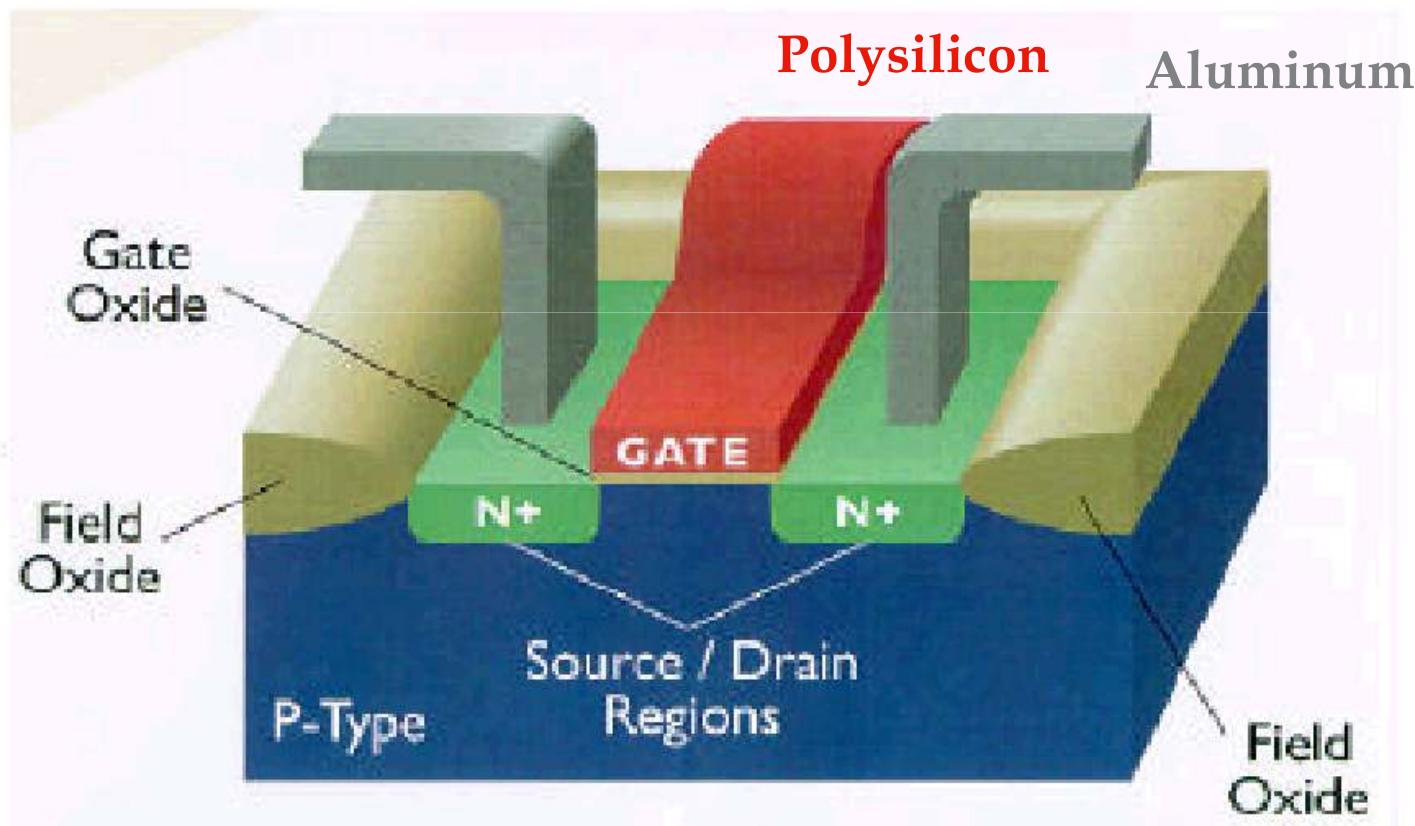
Advanced Metallization



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3D Perspective



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Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
 - scalable design rules: lambda parameter
 - absolute dimensions (micron rules)



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CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	



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Layers in 0.25 μm CMOS process

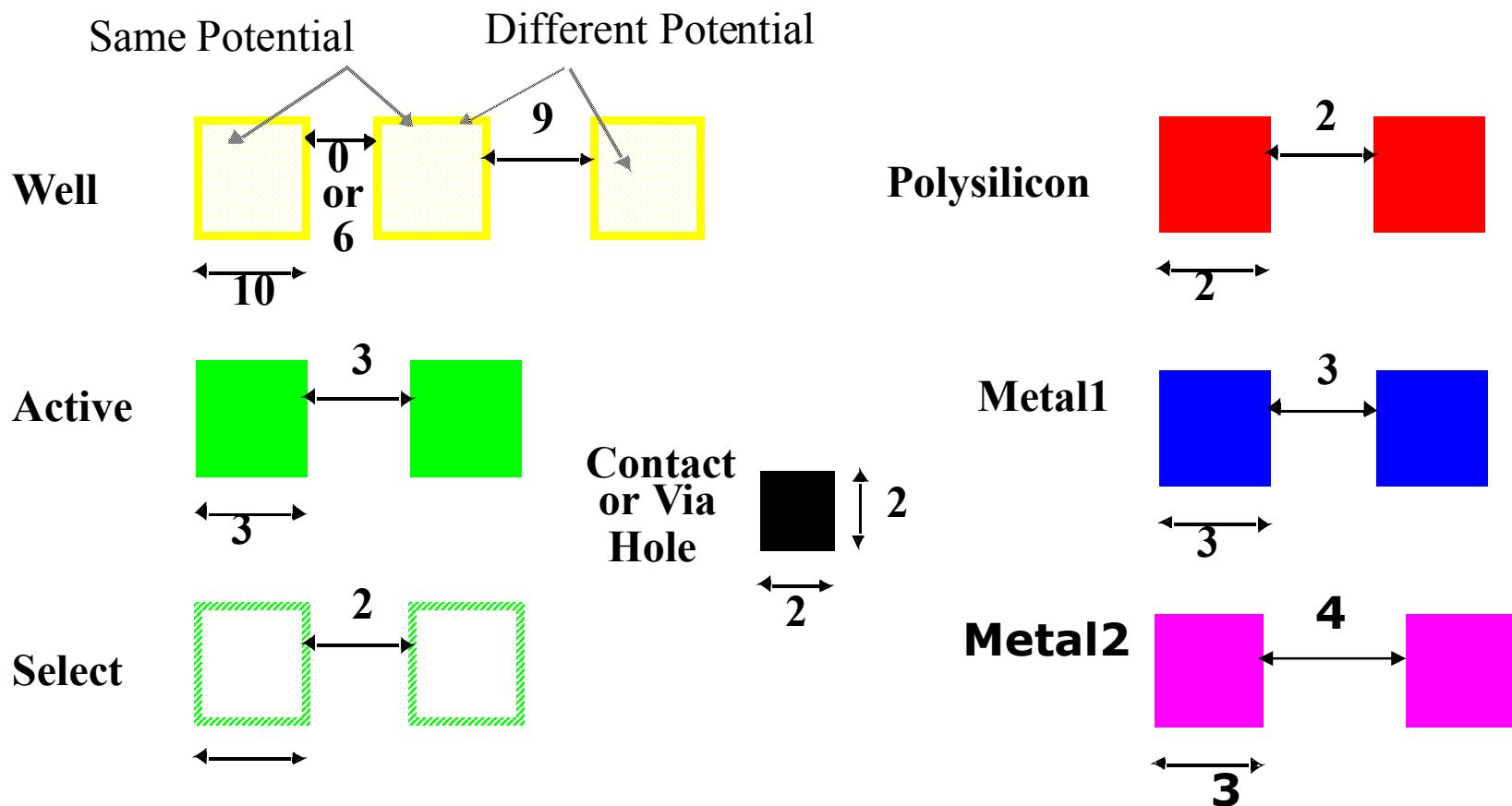
Layer Description	Representation				
metal					
well					
polysilicon					
contacts & vias					
active area and FETs					
select					



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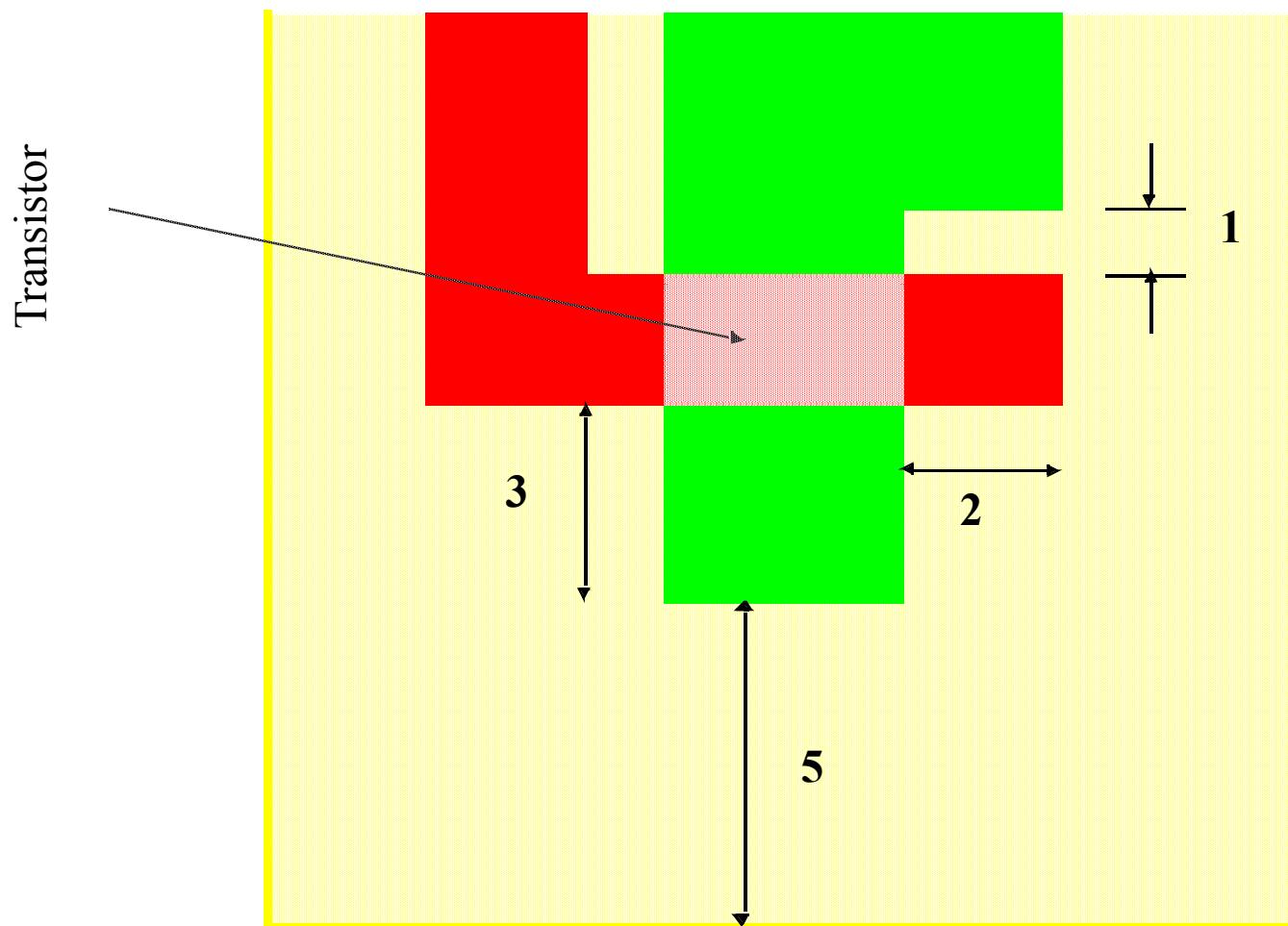
Intra-Layer Design Rules



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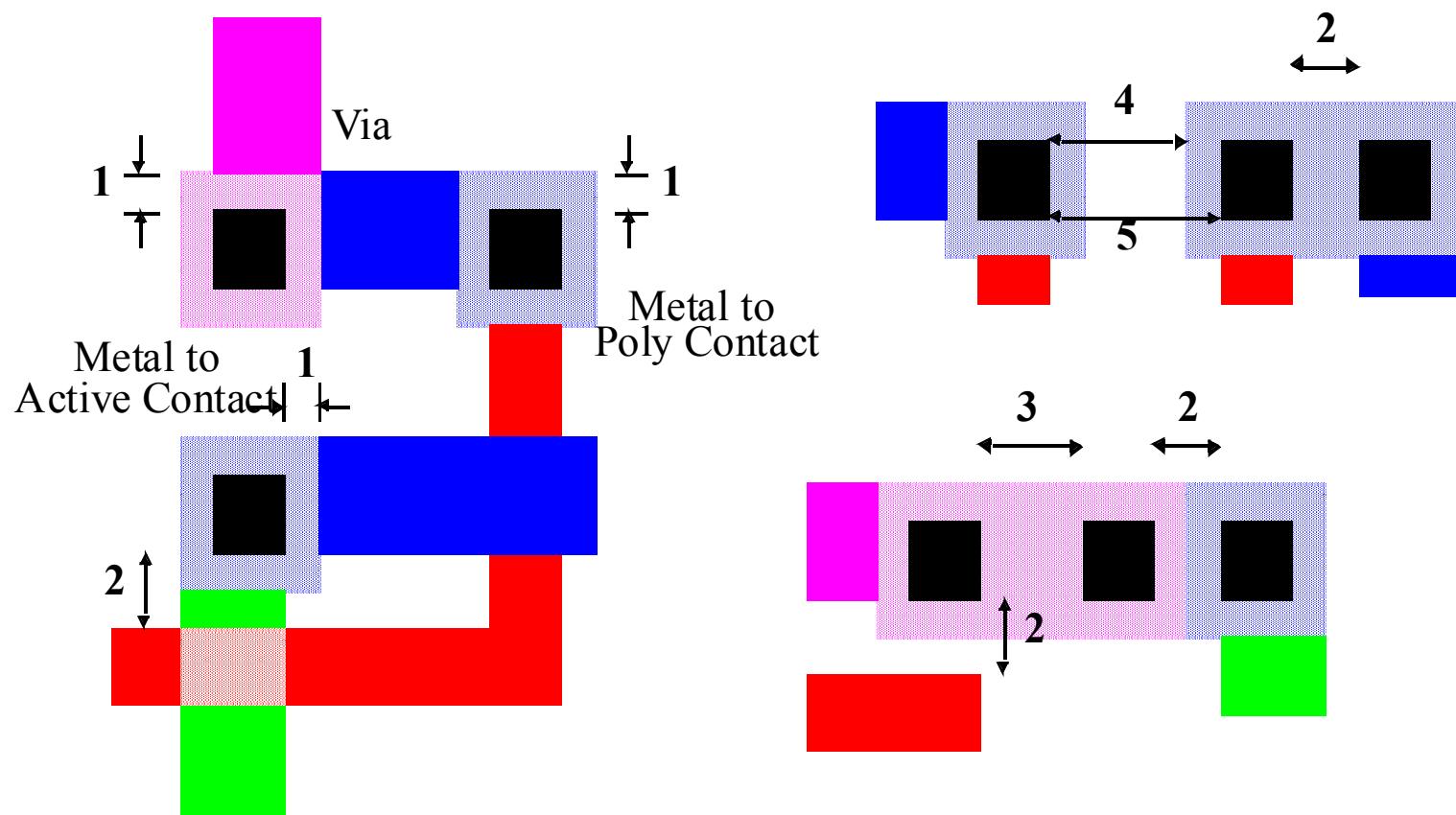
Transistor Layout



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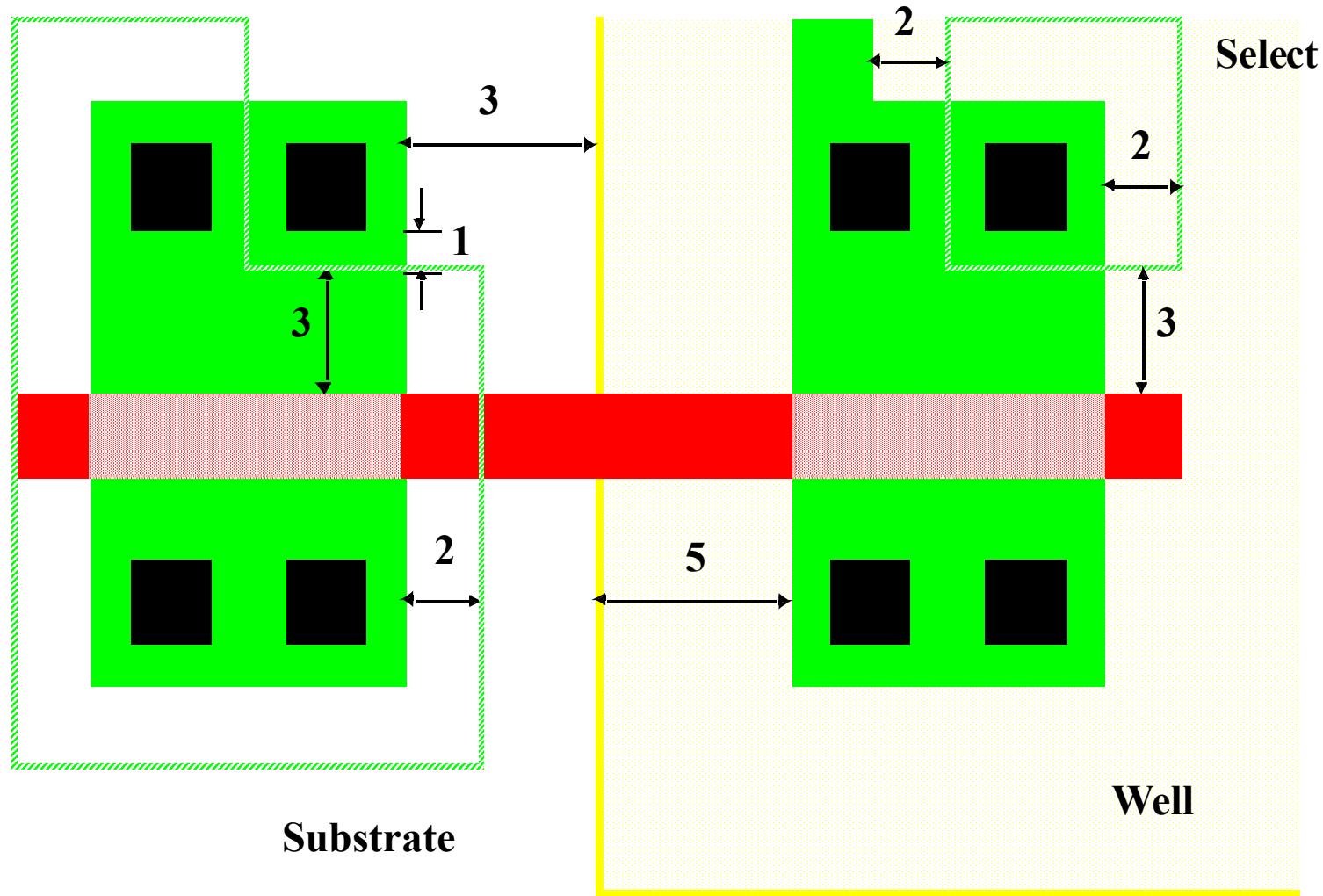
Vias and Contacts



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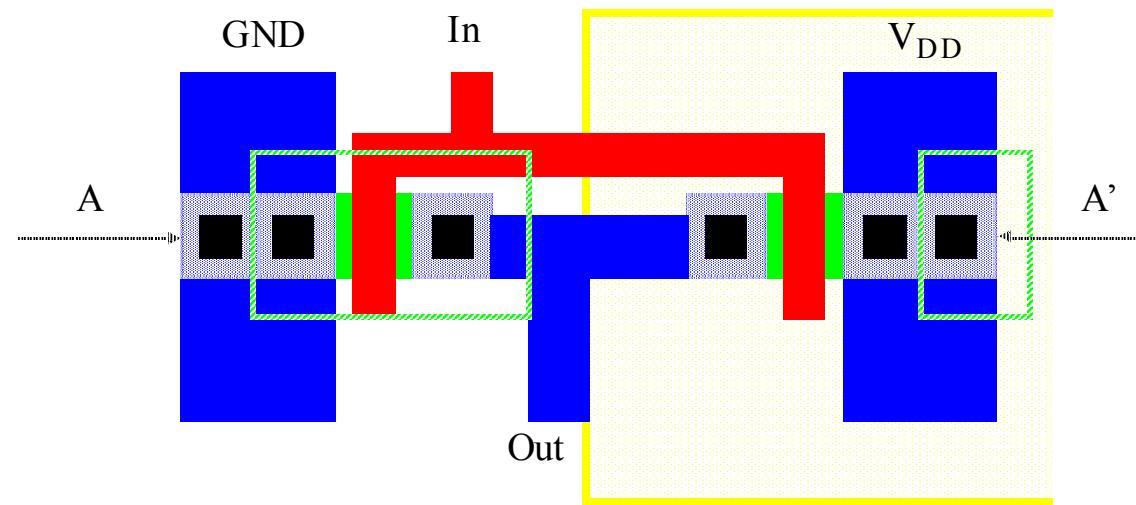
Select Layer



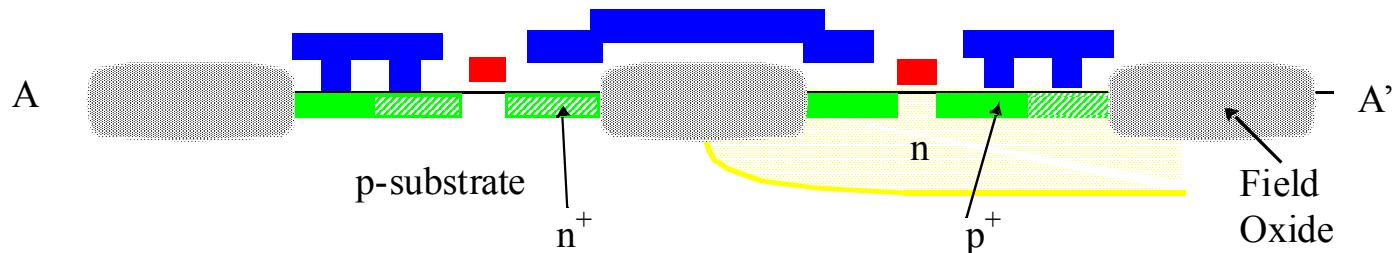
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CMOS Inverter Layout



(a) Layout



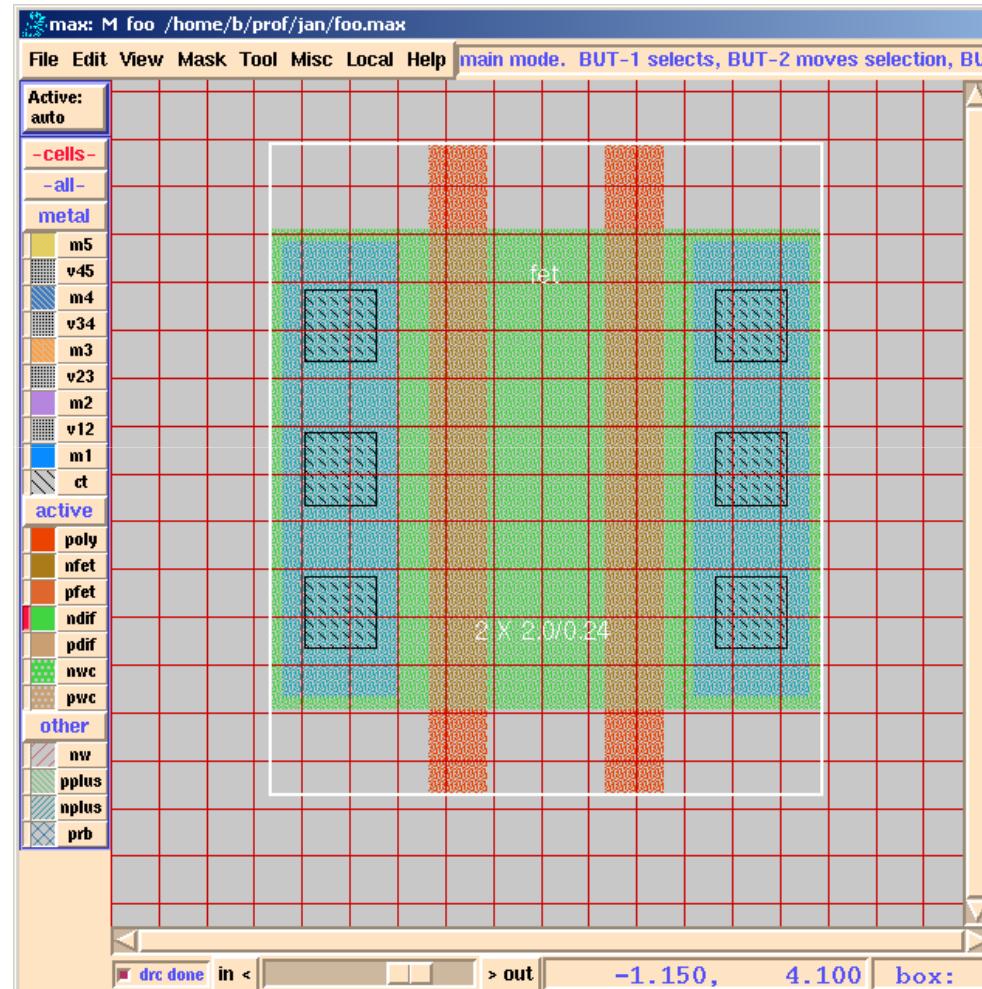
(b) Cross-Section along A-A'



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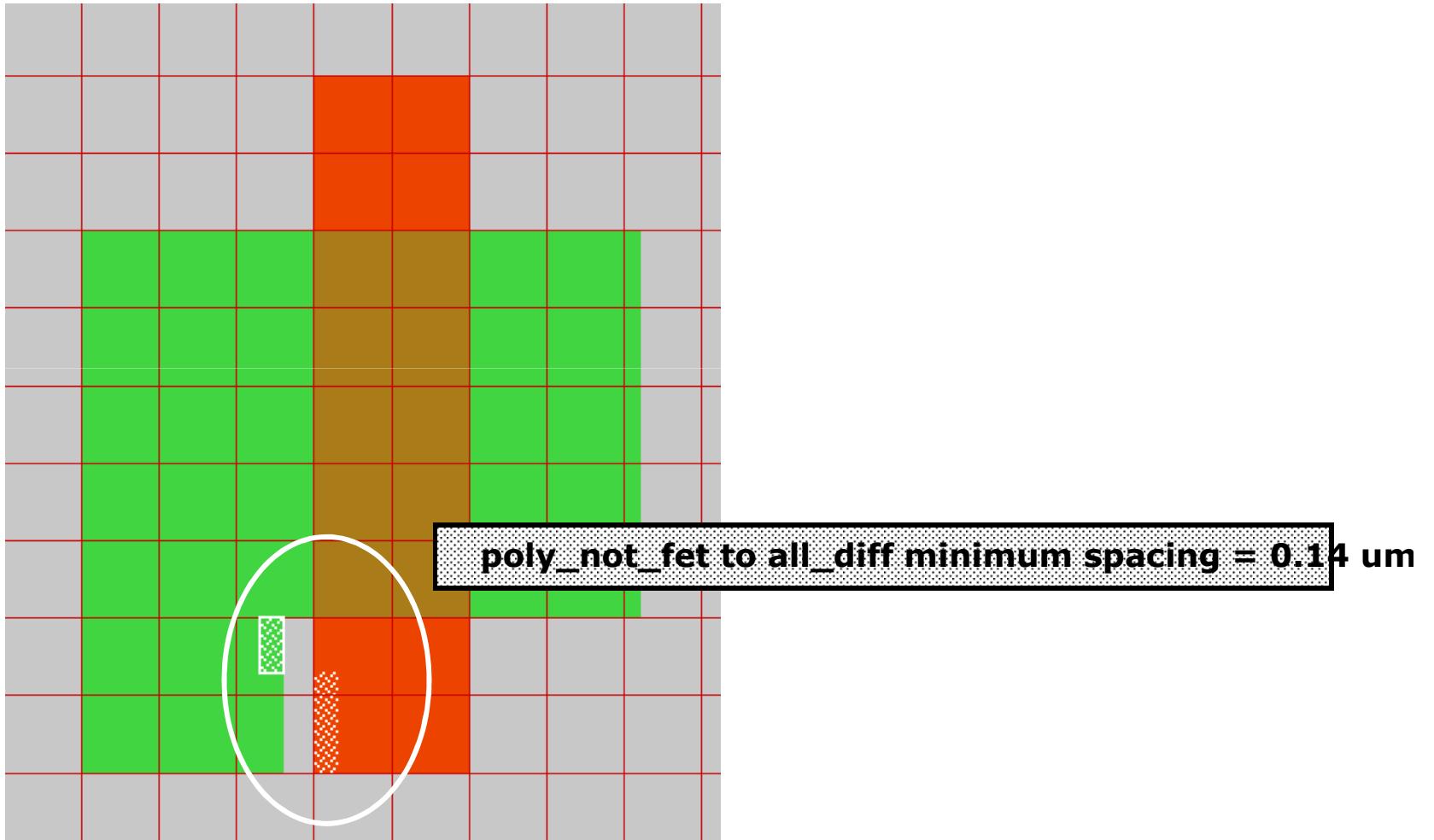
Layout Editor



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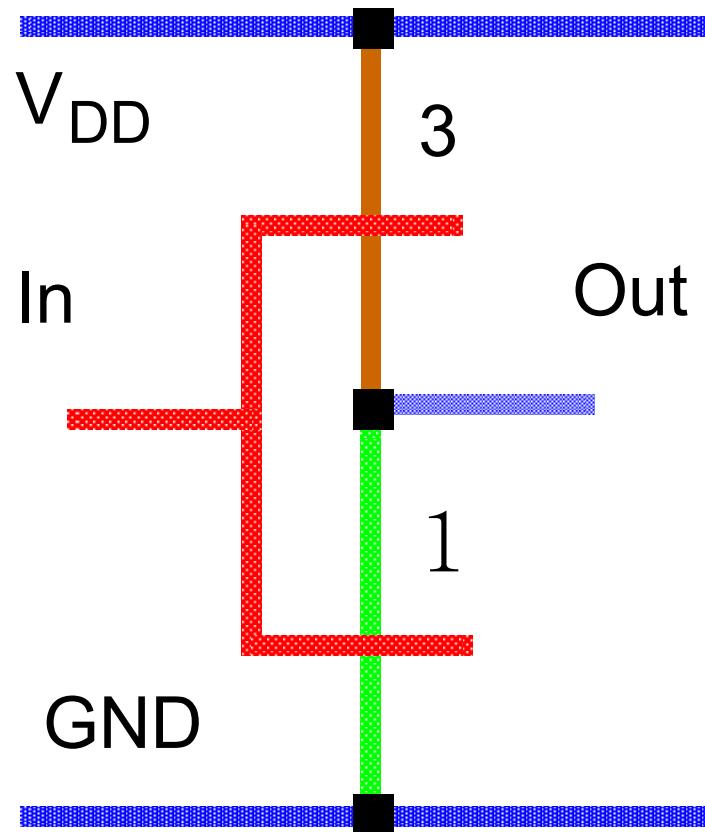
Design Rule Checker



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Sticks Diagram



- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program

Stick diagram of inverter



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Packaging Requirements

- **Electrical: Low parasitics**
- **Mechanical: Reliable and robust**
- **Thermal: Efficient heat removal**
- **Economical: Cheap**

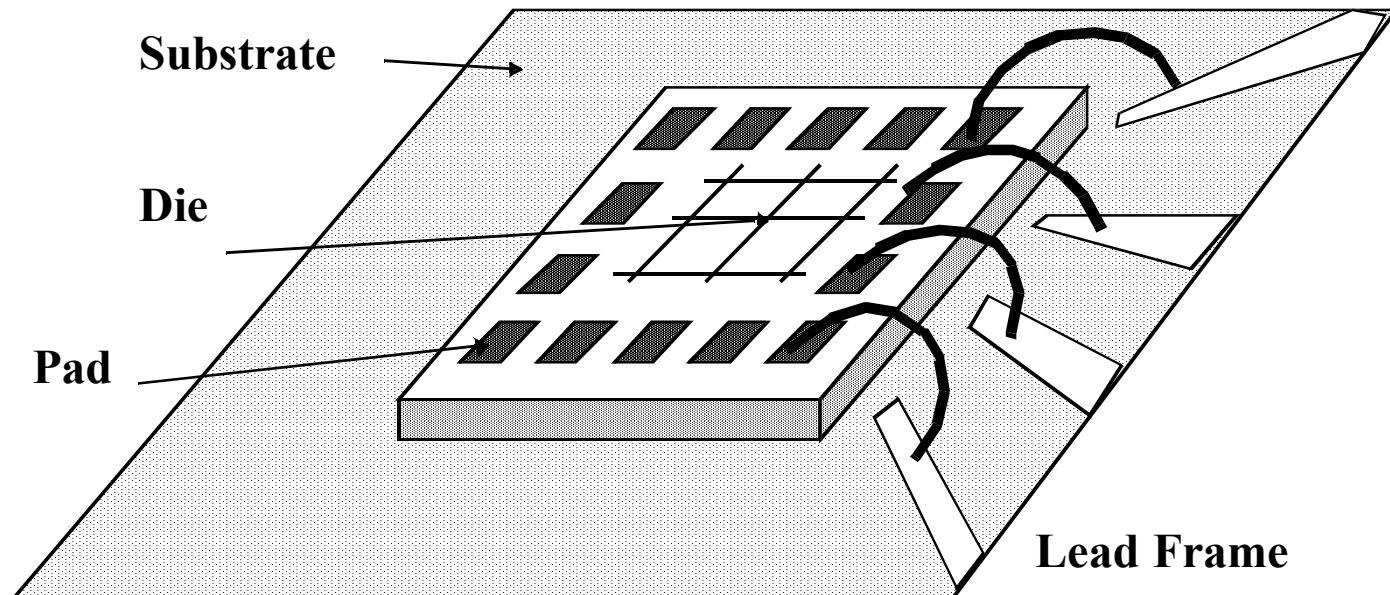


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Bonding Techniques

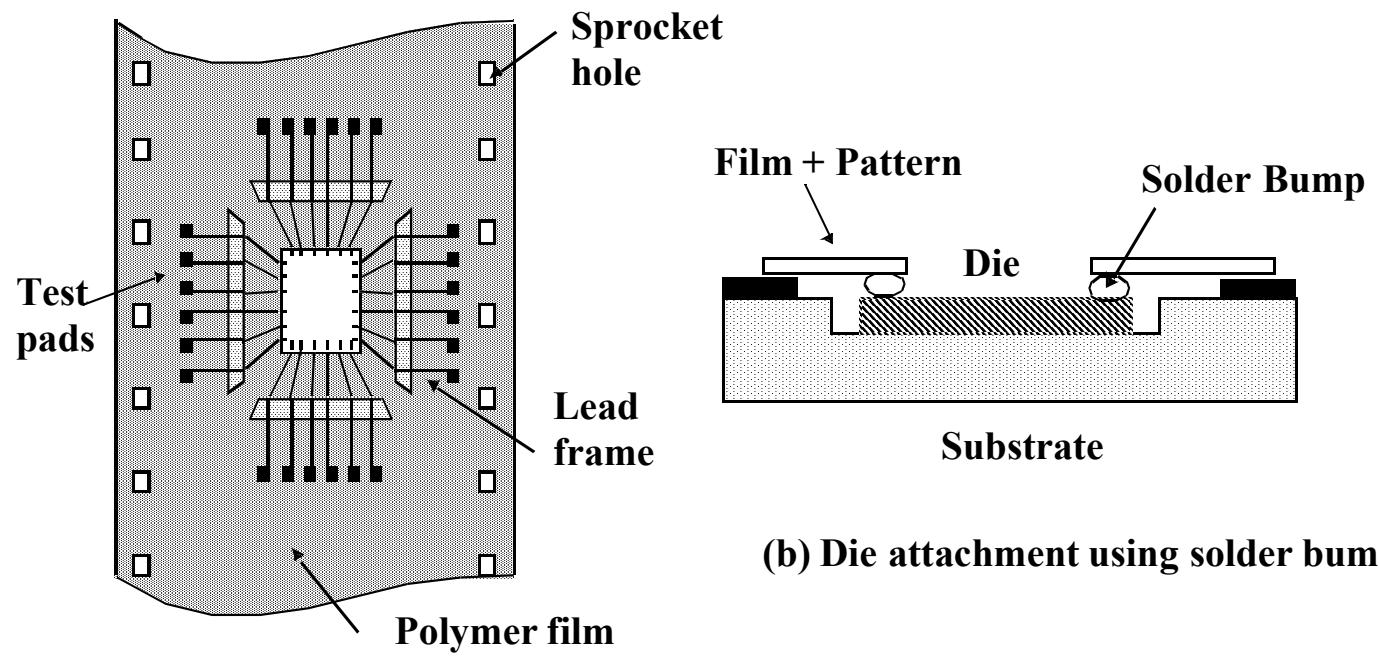
Wire Bonding



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Tape-Automated Bonding (TAB)



(a) Polymer Tape with imprinted
wiring pattern.

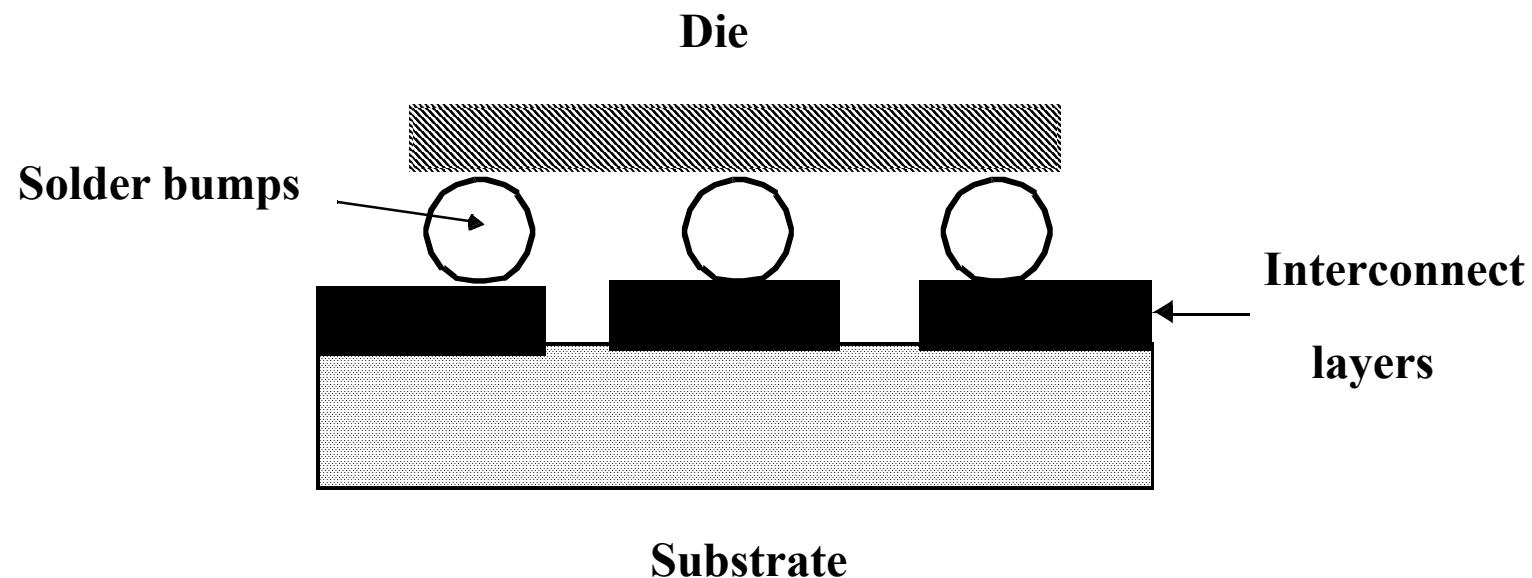
(b) Die attachment using solder bumps.



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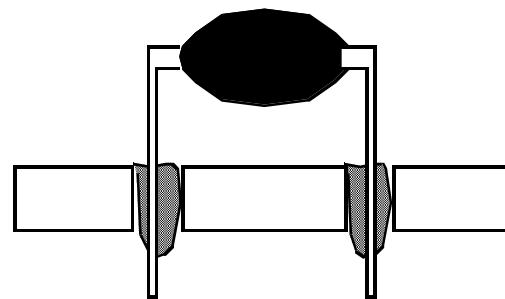
Flip-Chip Bonding



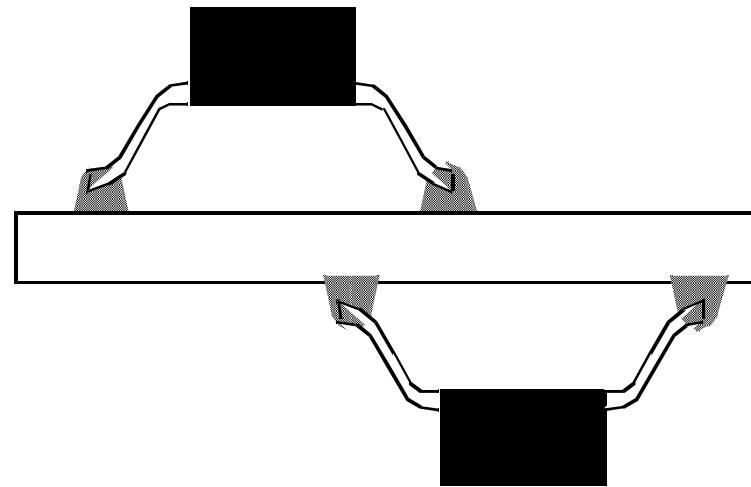
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Package-to-Board Interconnect



(a) Through-Hole Mounting



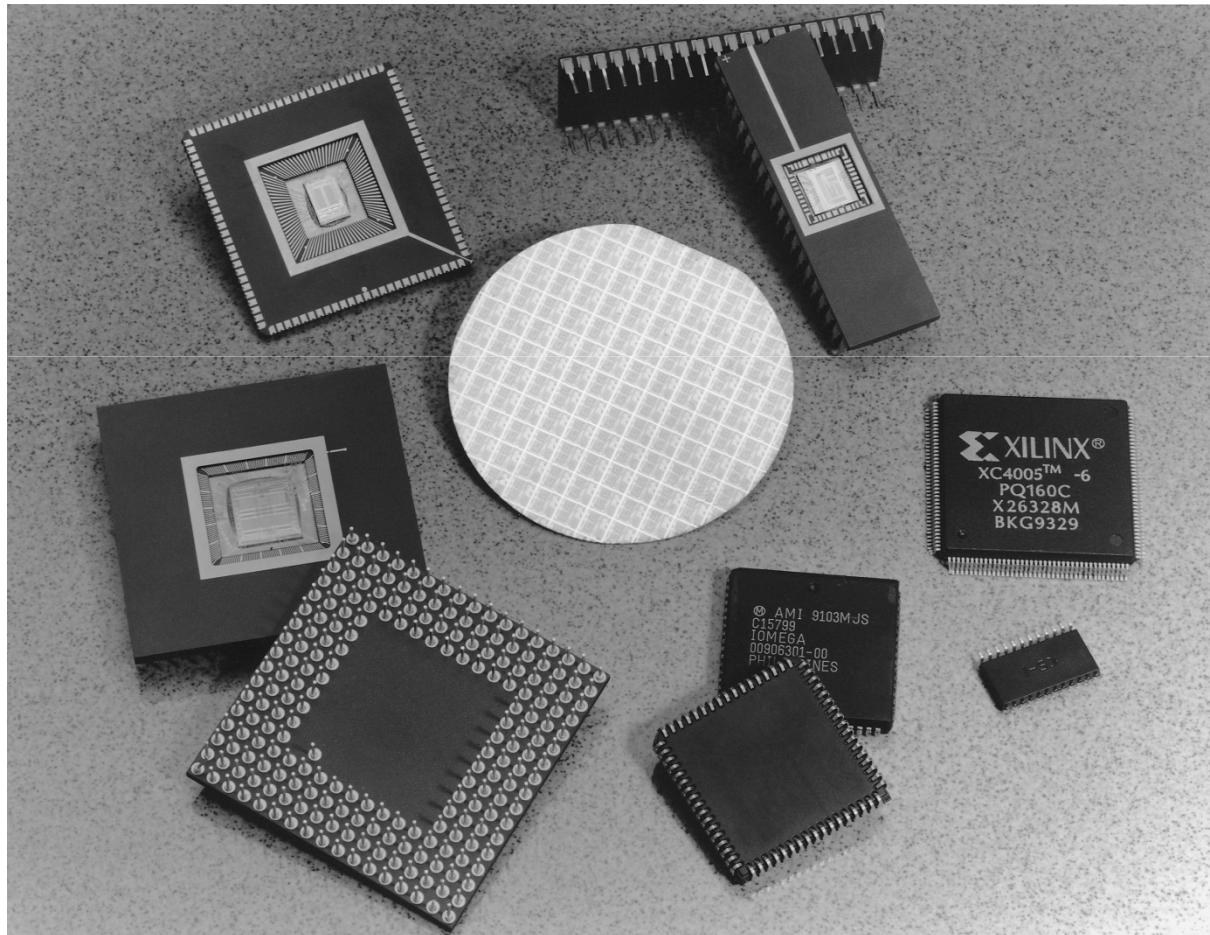
(b) Surface Mount



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Package Types



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Package Parameters

Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

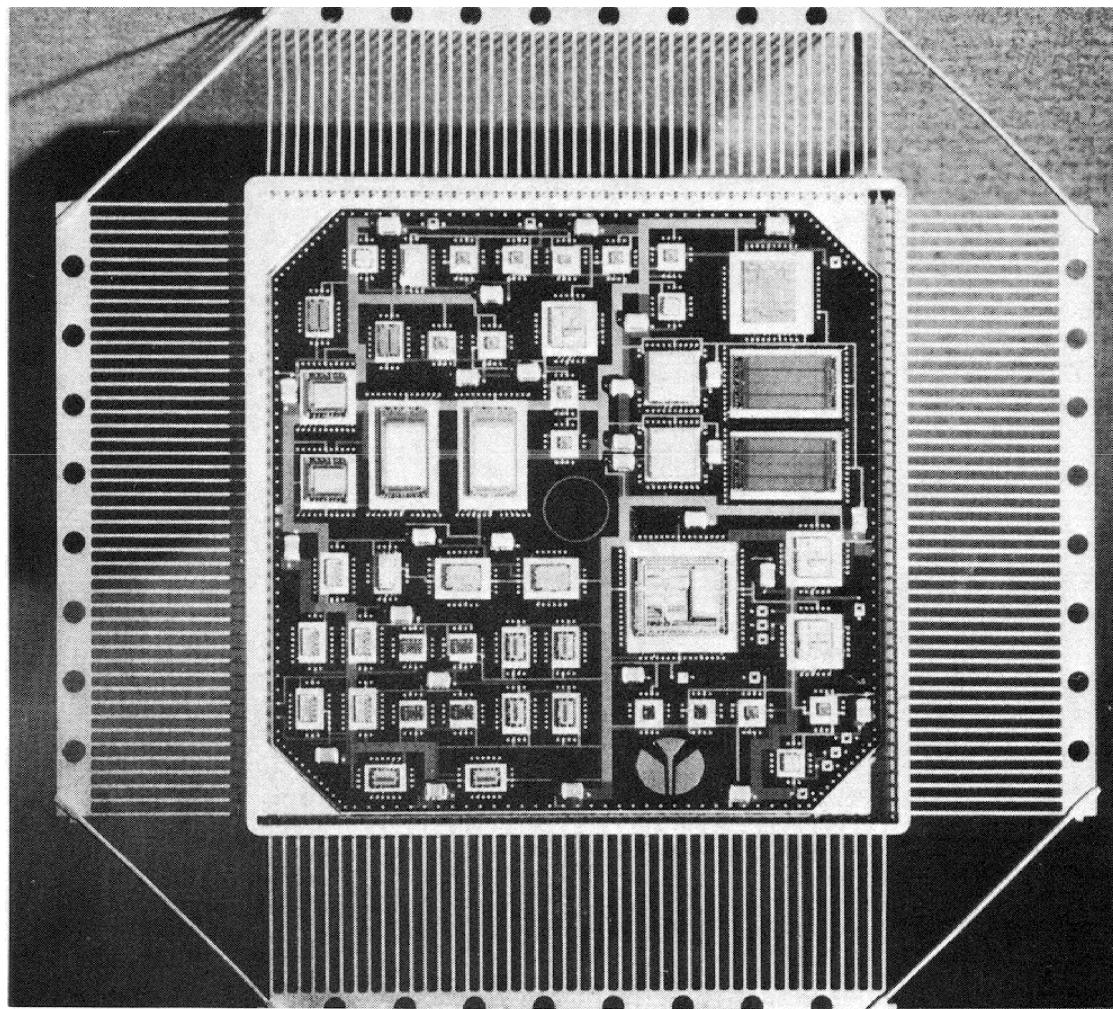
Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])



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Multi-Chip Modules



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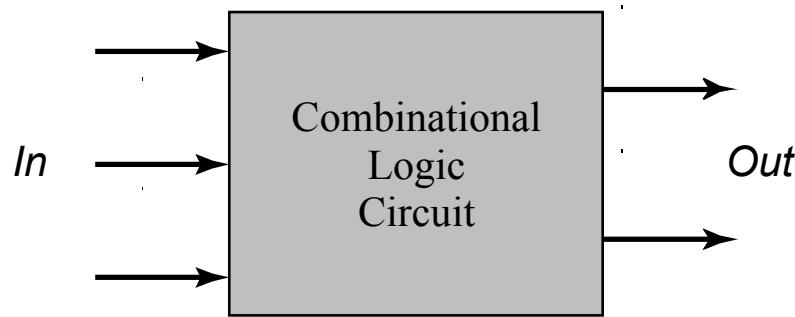
Designing Combinational Logic Circuits



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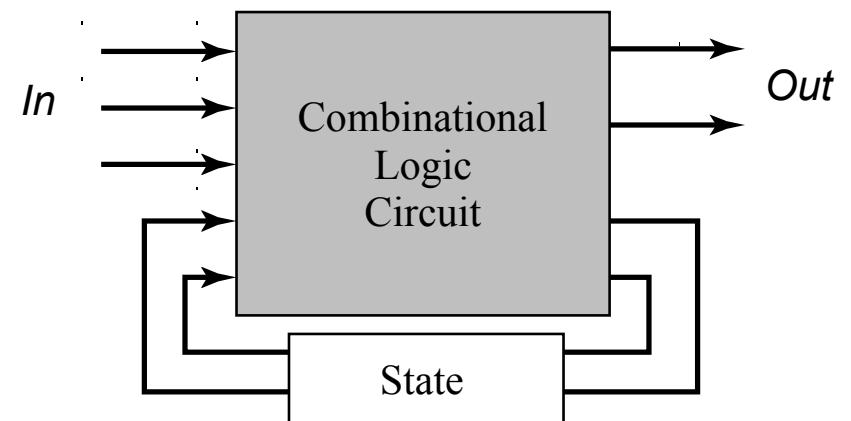
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Combinational vs. Sequential Logic



Combinational

$$\text{Output} = f(\text{In})$$



Sequential

$$\text{Output} = f(\text{In}, \text{Previous In})$$



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Static CMOS Circuit

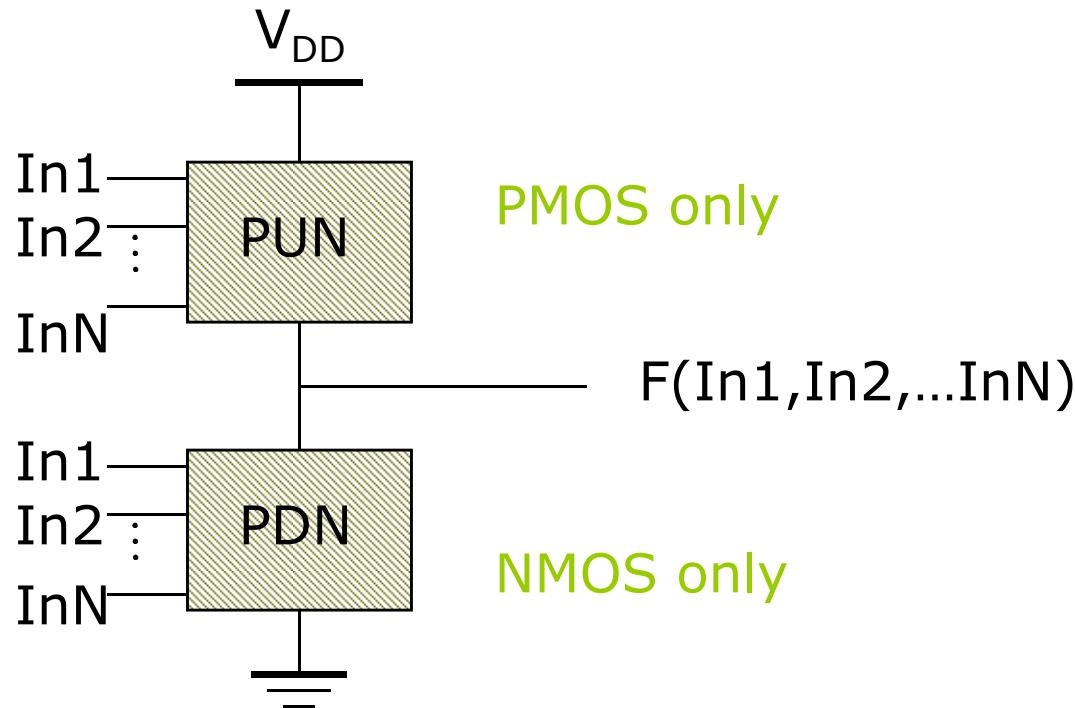
At every point in time (except during the switching transients) each **gate output is connected to either V_{DD} or V_{SS}** via a low-resistive path.

The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again, the transient effects during switching periods).

This is in contrast to the **dynamic** circuit class, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.



Static Complementary CMOS

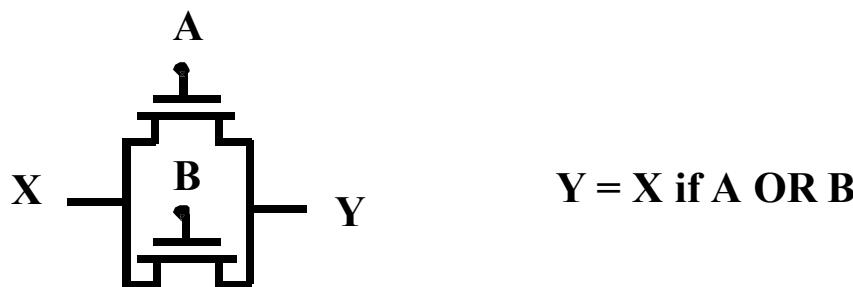


PUN and PDN are **dual** logic networks

NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



NMOS Transistors pass a “strong” 0 but a “weak” 1



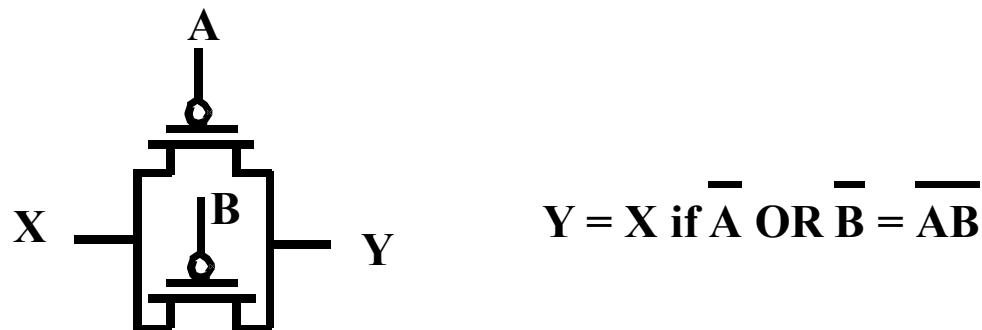
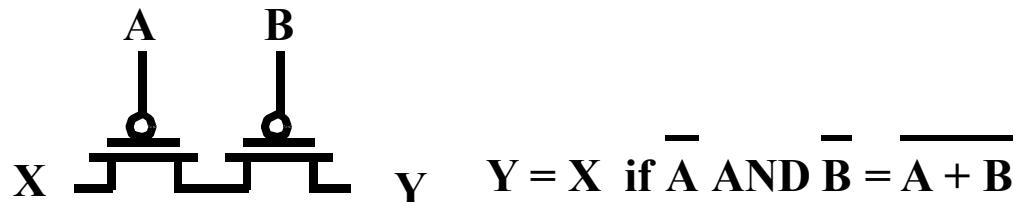
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PMOS Transistors

in Series/Parallel Connection

PMOS switch closes when switch control input is low



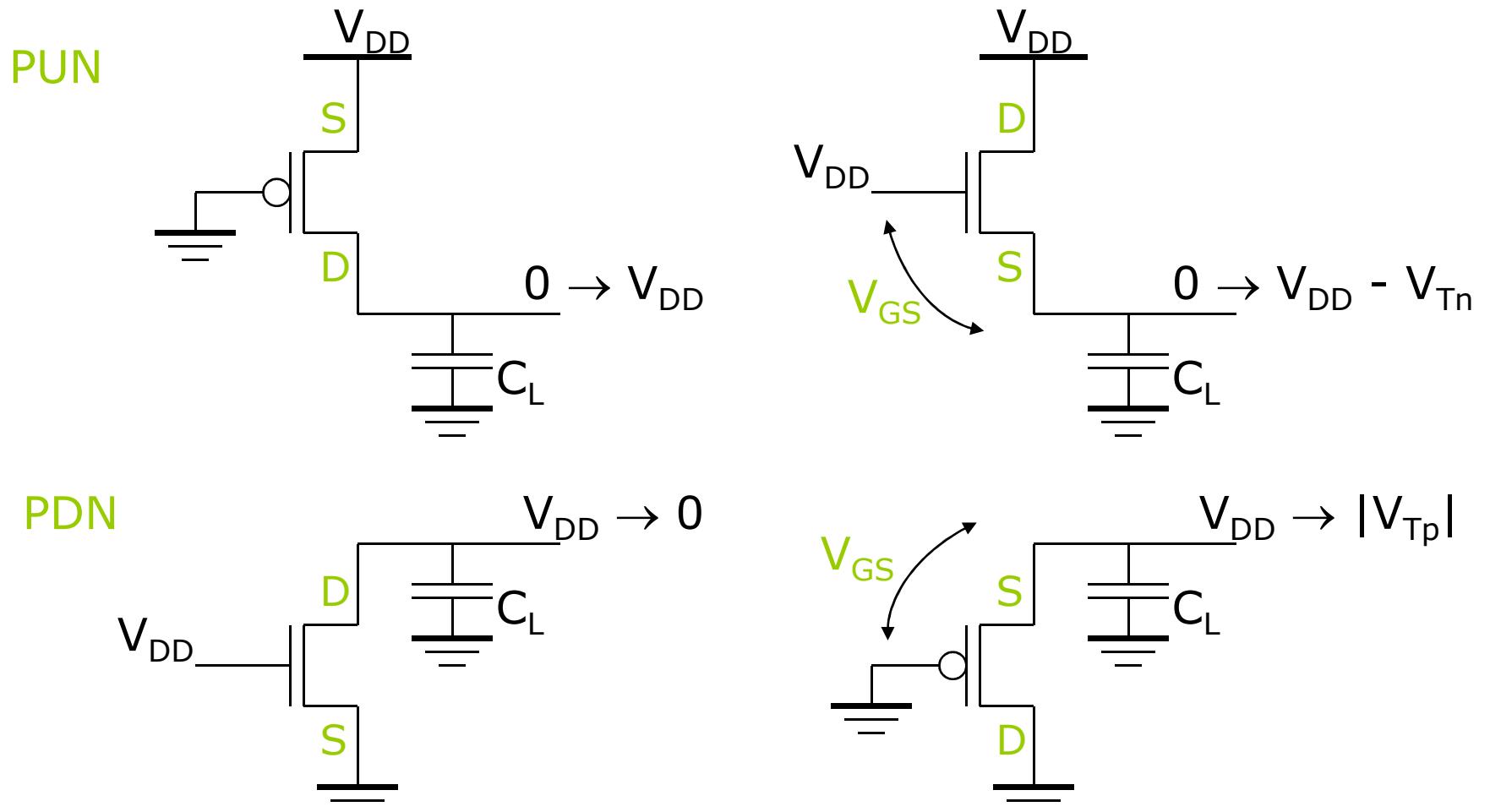
PMOS Transistors pass a “strong” 1 but a “weak” 0



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Threshold Drops



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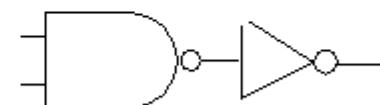
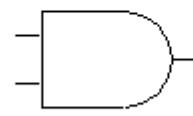
Complementary CMOS Logic Style

- PUP is the DUAL of PDN
(can be shown using DeMorgan's Theorem's)

$$\overline{A + B} = \bar{A}\bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

- The complementary gate is inverting



AND = NAND + INV



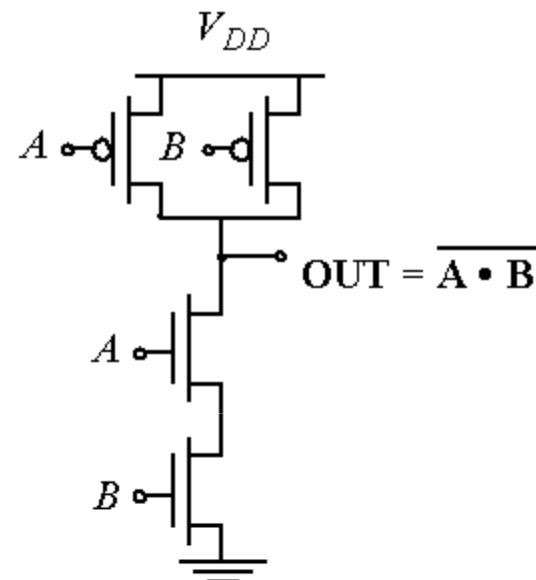
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Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: $G = A \cdot B \Rightarrow$ Conduction to GND

PUN: $F = \overline{\overline{A} + \overline{B}} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$G(\overline{In_1}, \overline{In_2}, \overline{In_3}, \dots) \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \dots)$$



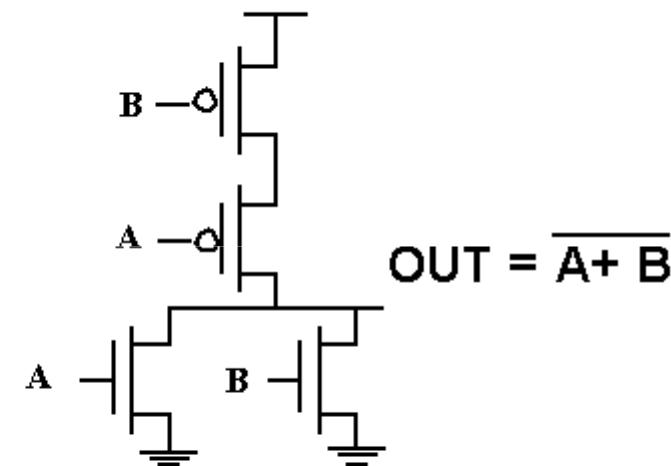
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Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

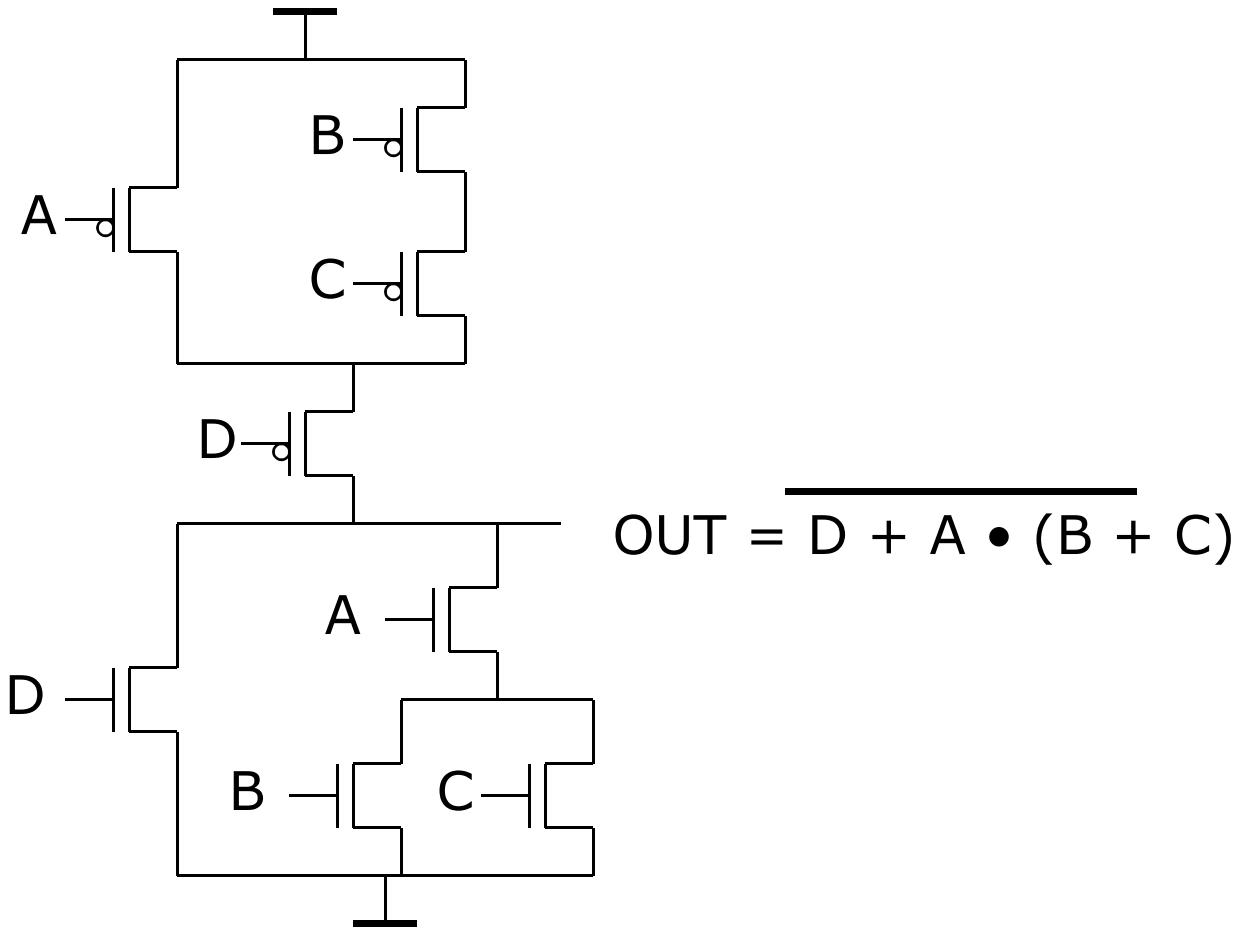
Truth Table of a 2 input NOR gate



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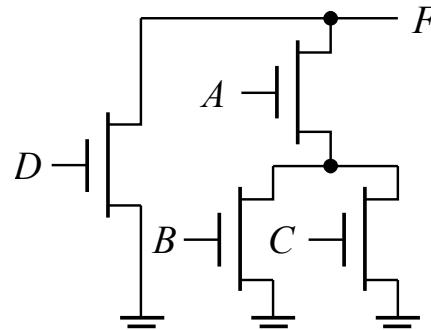
Complex CMOS Gate



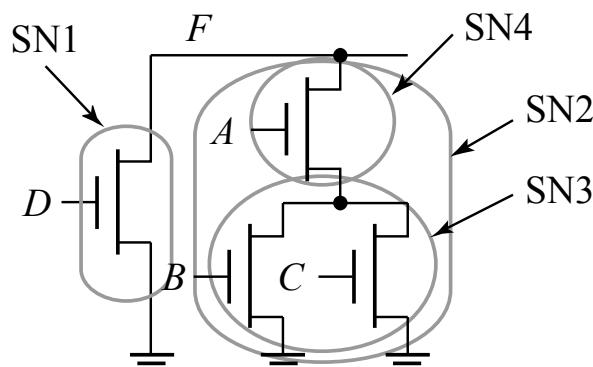
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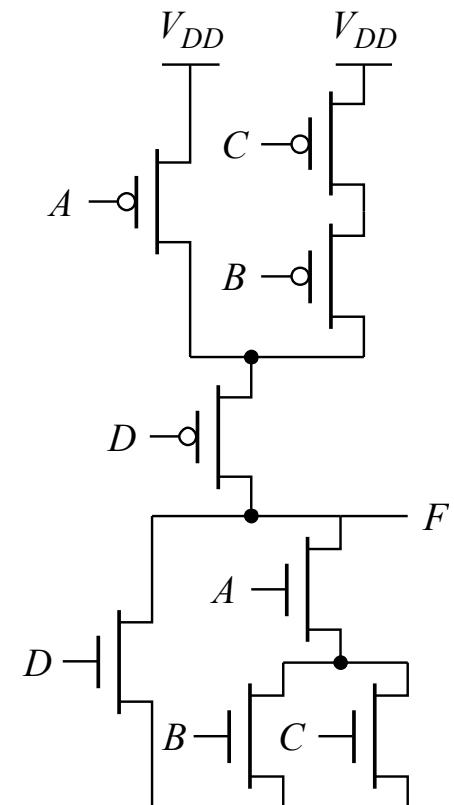
Constructing a Complex Gate



(a) pull-down network



(b) Deriving the pull-up network hierarchically by identifying sub-nets



(c) complete gate



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Cell Design

□ Standard Cells

- General purpose logic
- Can be synthesized
- Same height, varying width

□ Datapath Cells

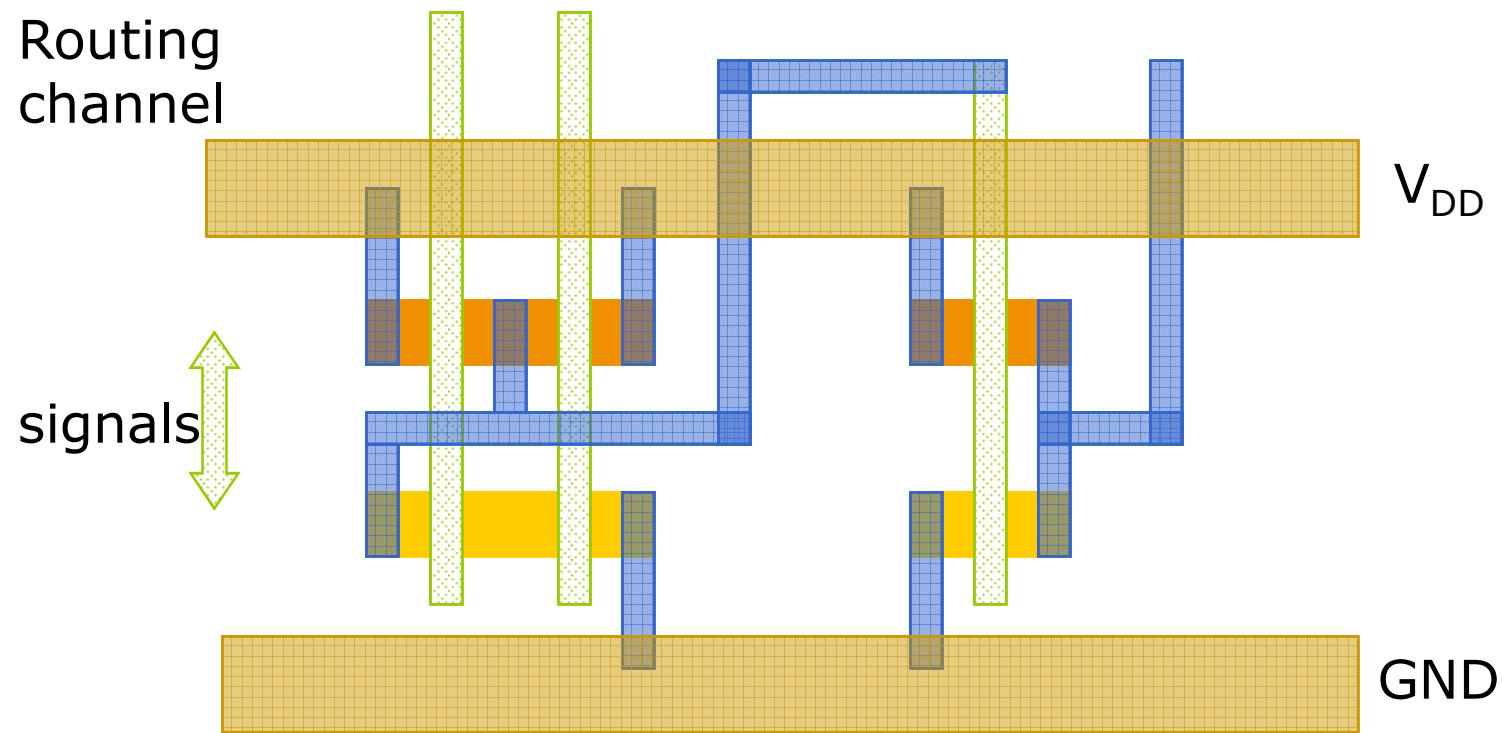
- For regular, structured designs (arithmetic)
- Includes some wiring in the cell
- Fixed height and width



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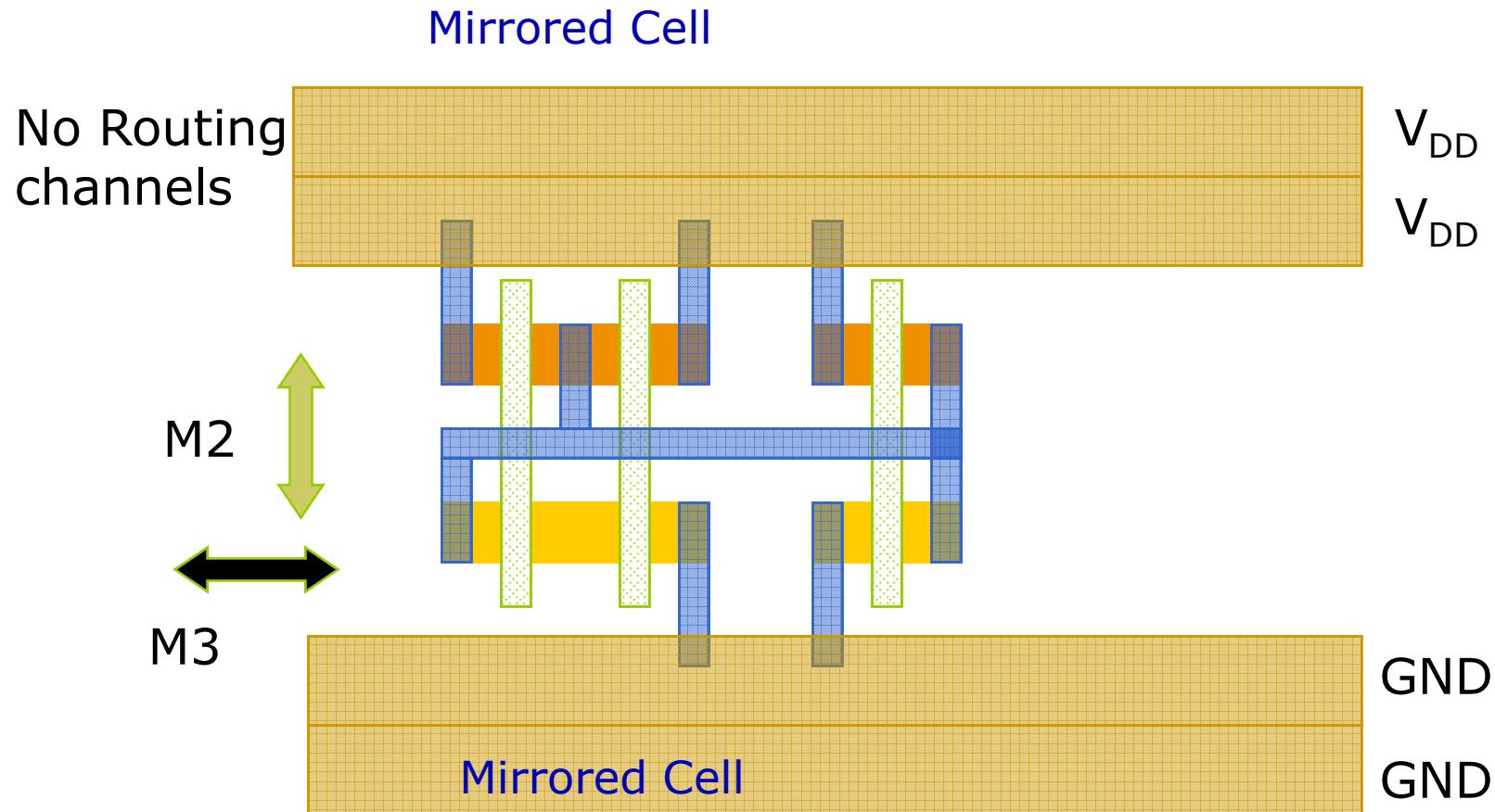
Standard Cell Layout Methodology – 1980s



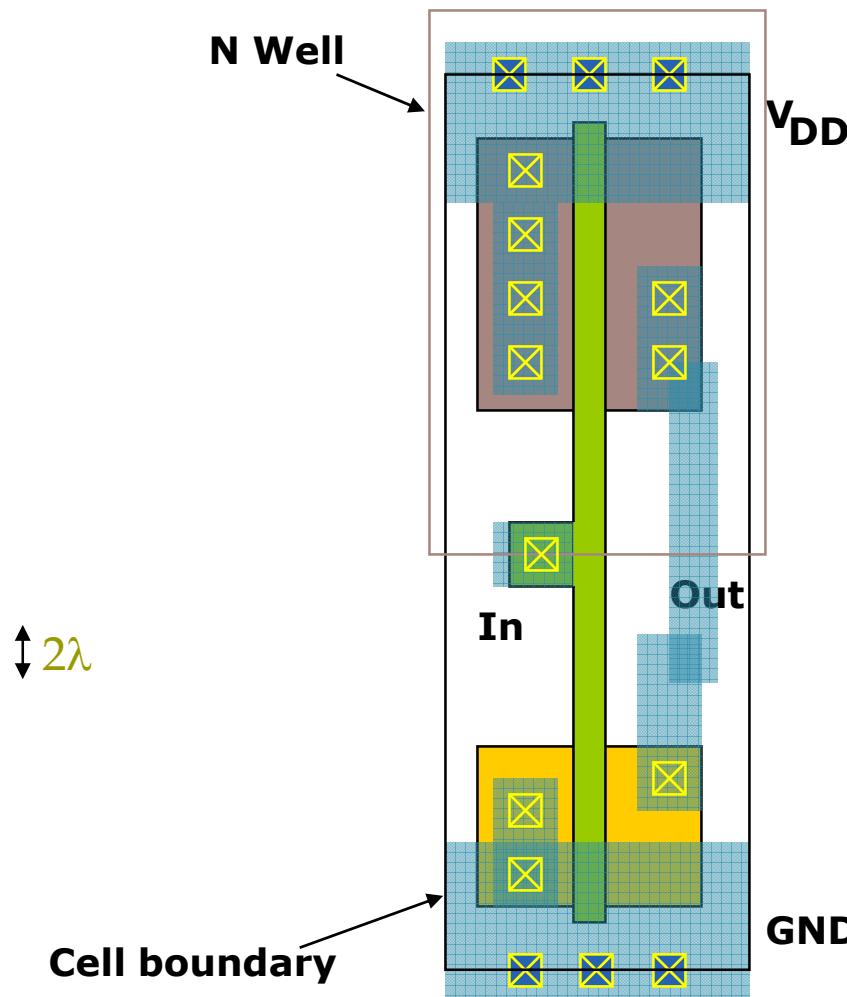
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Standard Cell Layout Methodology – 1990s



Standard Cells



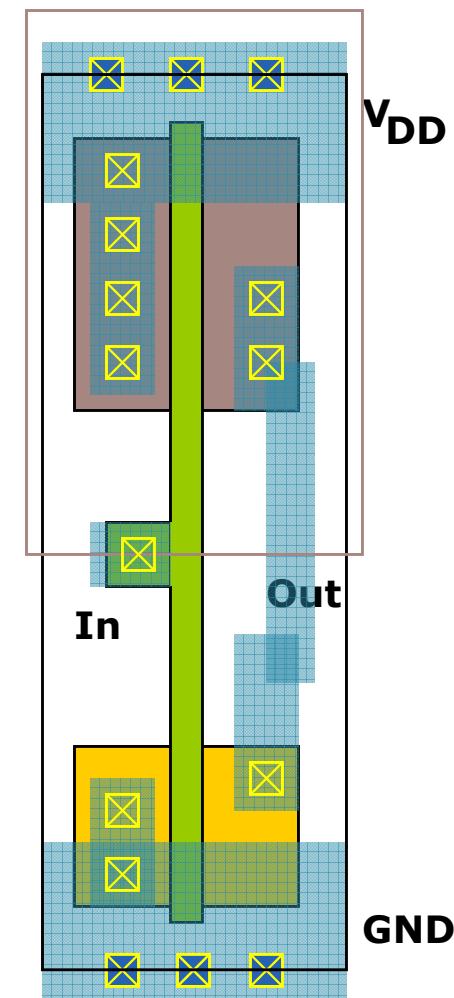
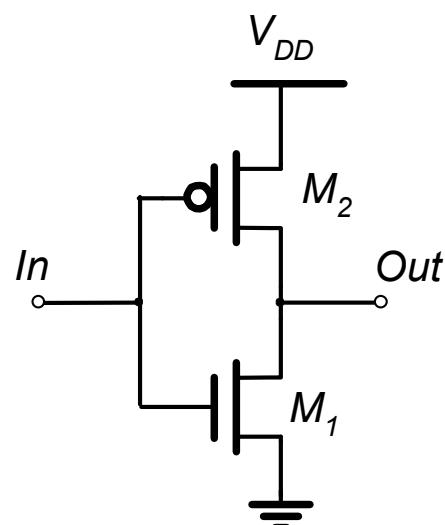
Cell height 12 metal tracks
Metal track is approx. $3\lambda + 3\lambda$
Pitch =
repetitive distance between objects

Cell height is “12 pitch”

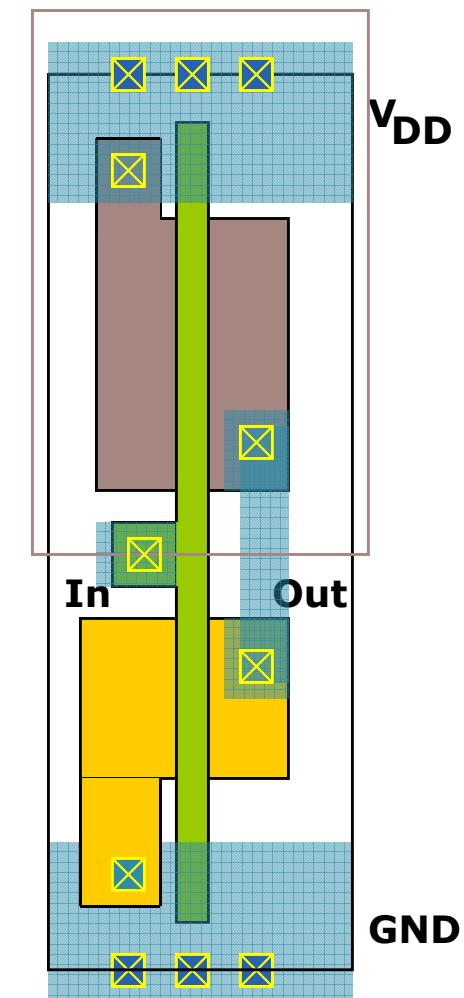


Standard Cells

With minimal diffusion routing

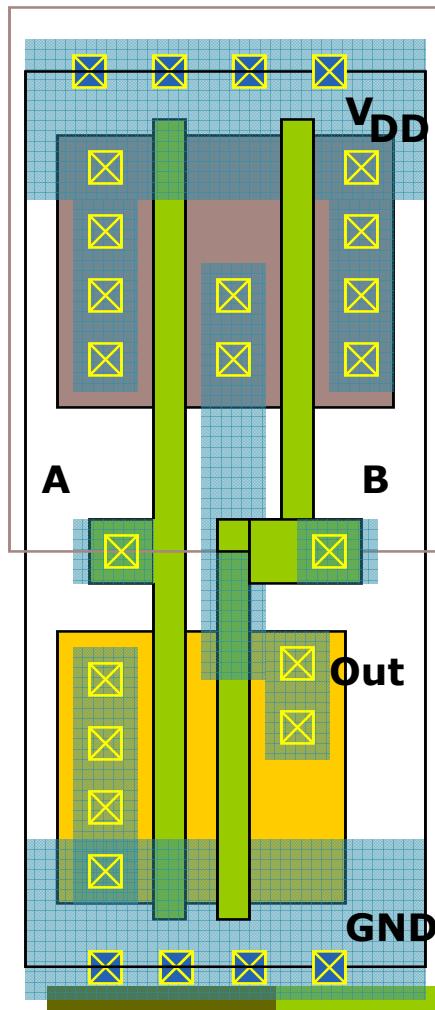


With silicided diffusion

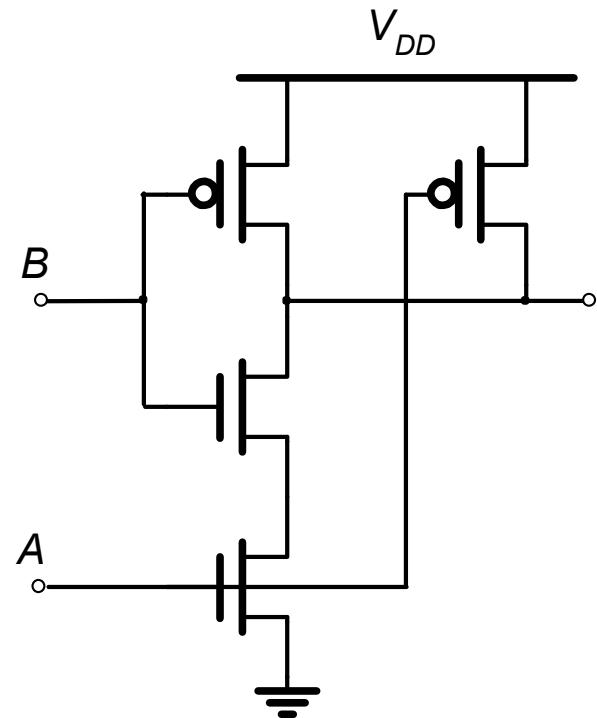


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Standard Cells



2-input NAND gate

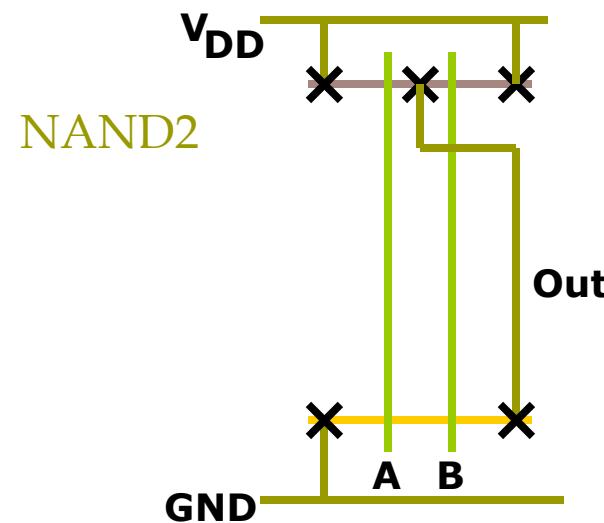
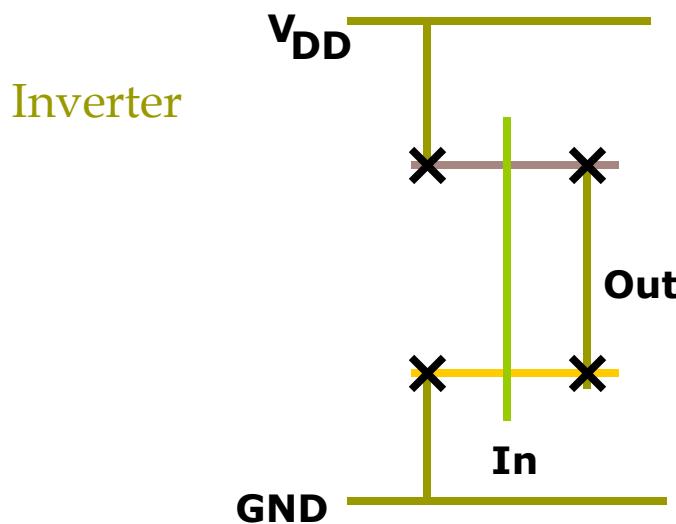


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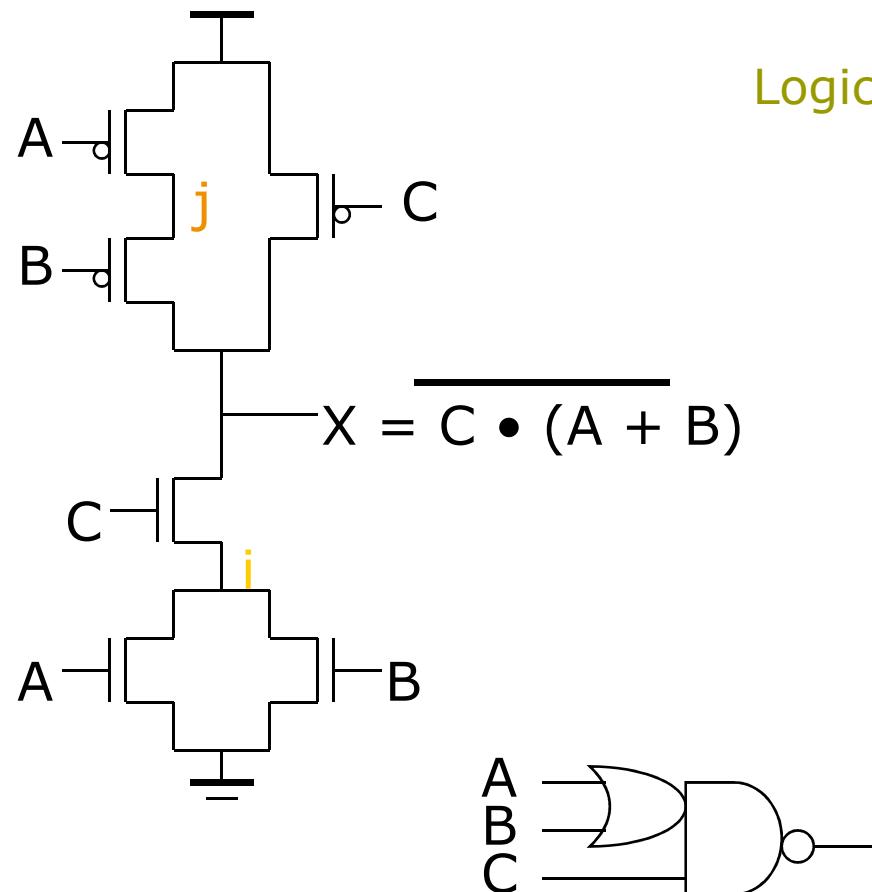
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Stick Diagrams

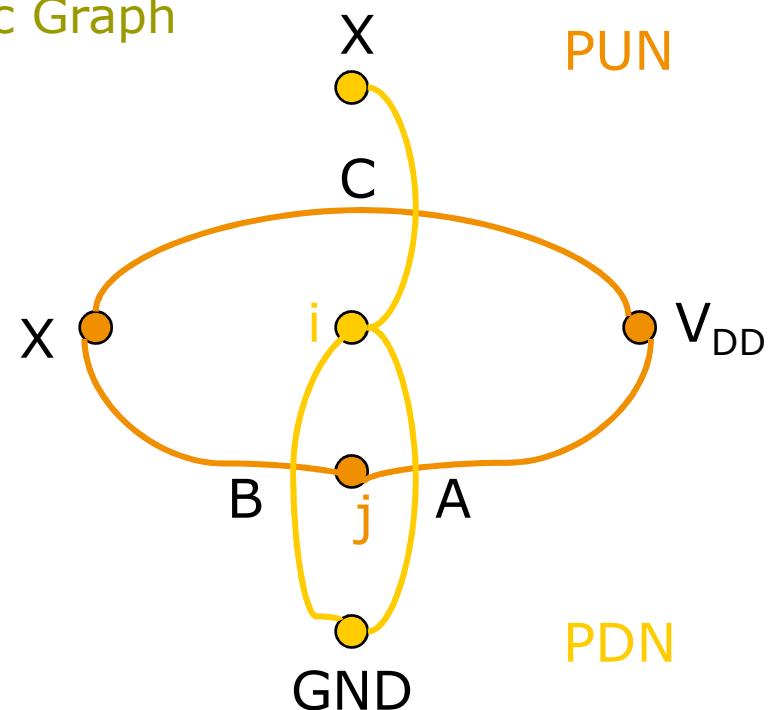
Contains no dimensions
Represents relative positions of transistors



Stick Diagrams



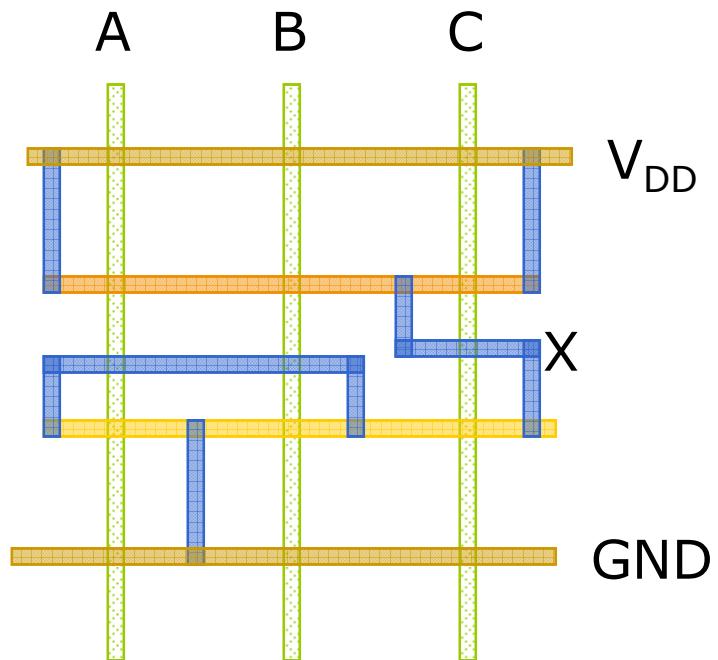
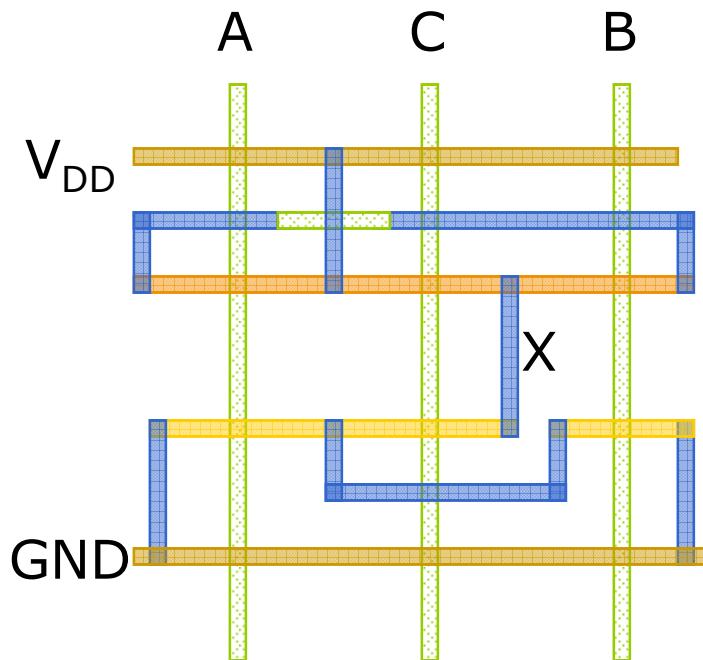
Logic Graph



PUN

PDN

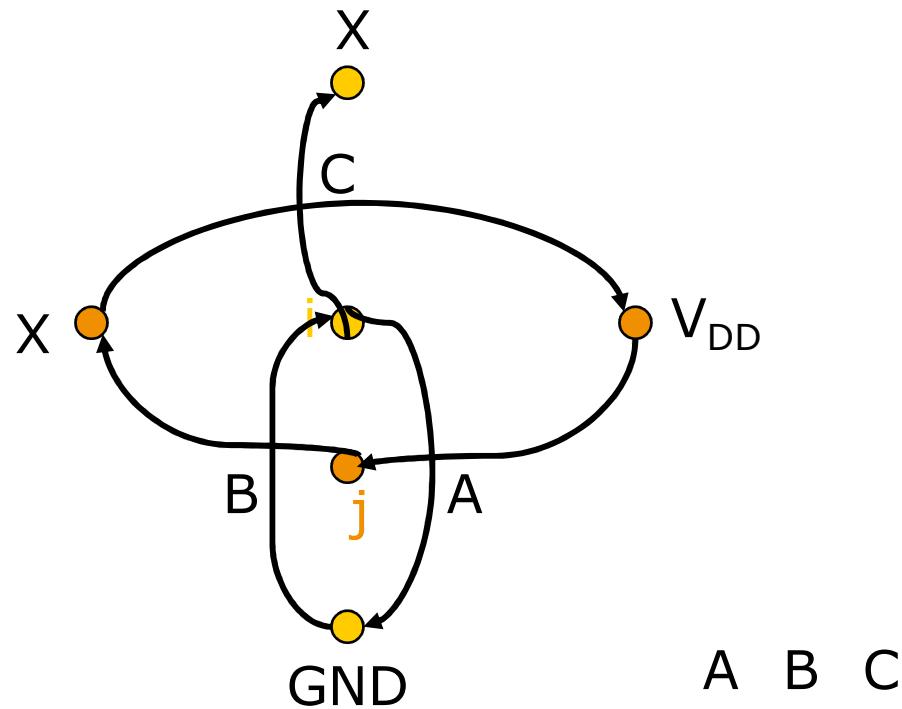
Two Versions of $\overline{C} \cdot (A + B)$



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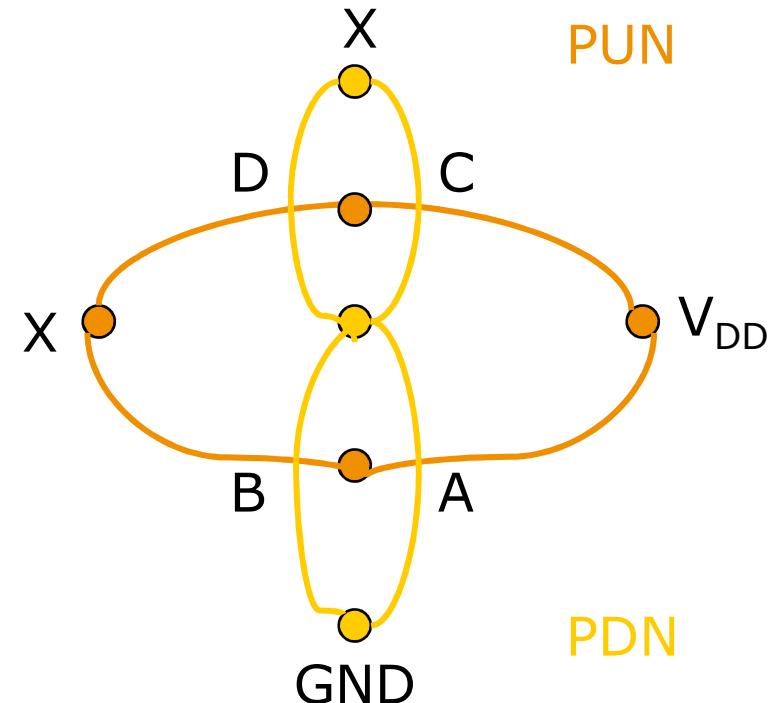
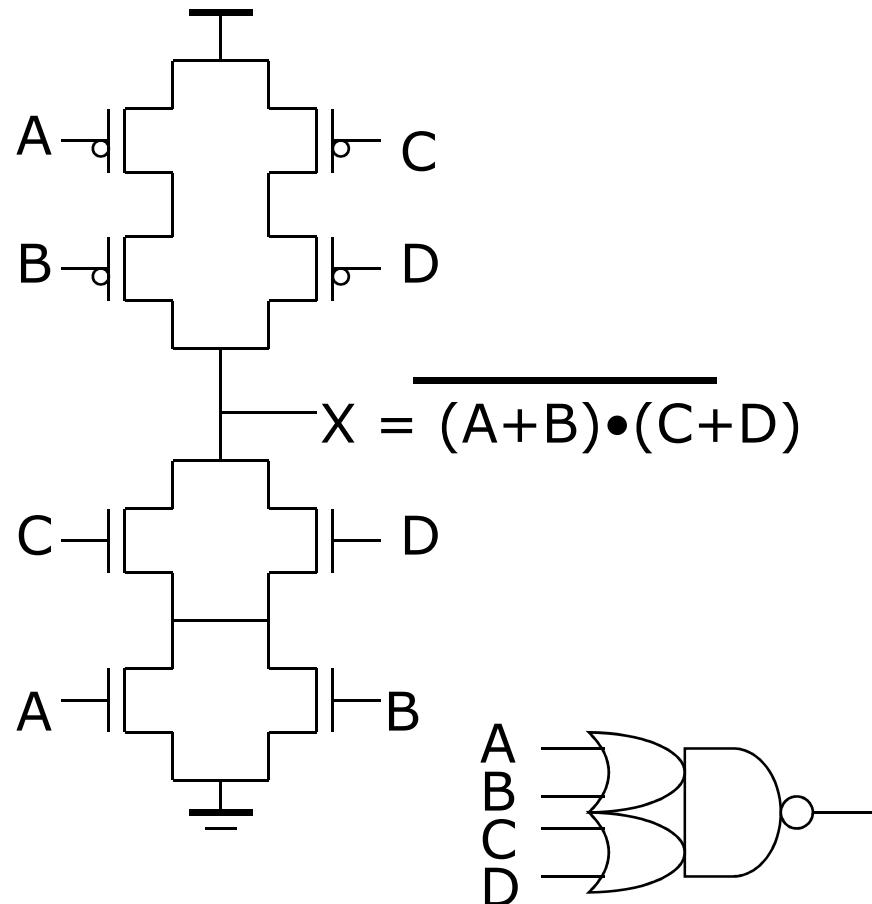
Consistent Euler Path



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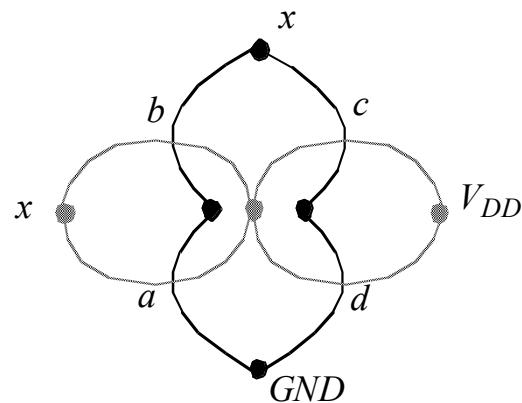
OAI22 Logic Graph



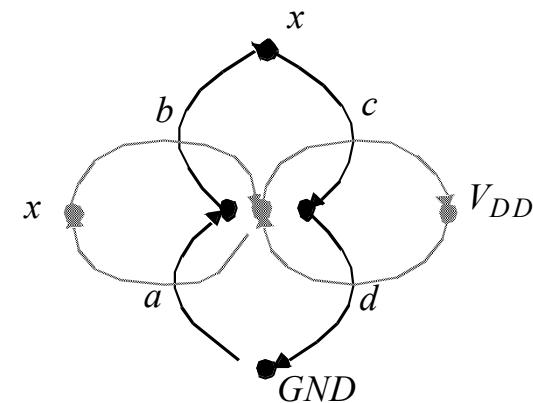
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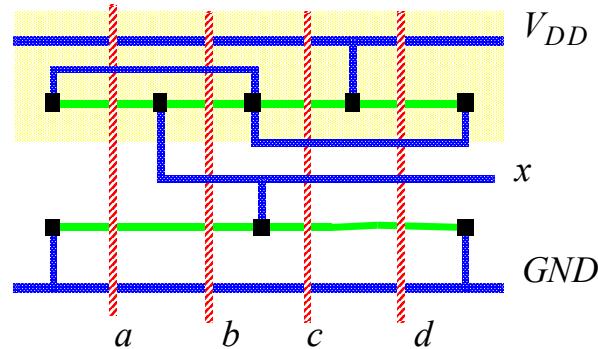
Example: $x = ab + cd$



(a) Logic graphs for $(ab+cd)$



(b) Euler Paths $\{a\ b\ c\ d\}$



(c) stick diagram for ordering $\{a\ b\ c\ d\}$

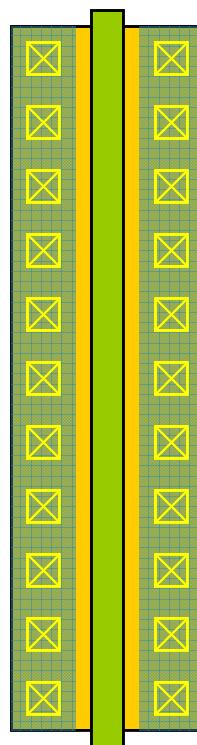


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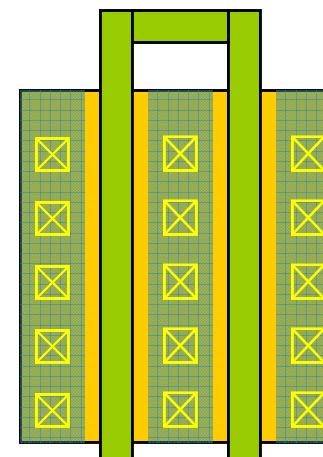
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Multi-Fingered Transistors

One finger



Two fingers (folded)



Less diffusion capacitance



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Properties of Complementary CMOS Gates Snapshot

High noise margins:

V_{OH} and V_{OL} are at V_{DD} and GND, respectively.

No static power consumption :

There never exists a direct path between V_{DD} and V_{SS} (GND) in steady-state mode

Comparable rise and fall times:

(under appropriate sizing conditions)



CMOS Properties

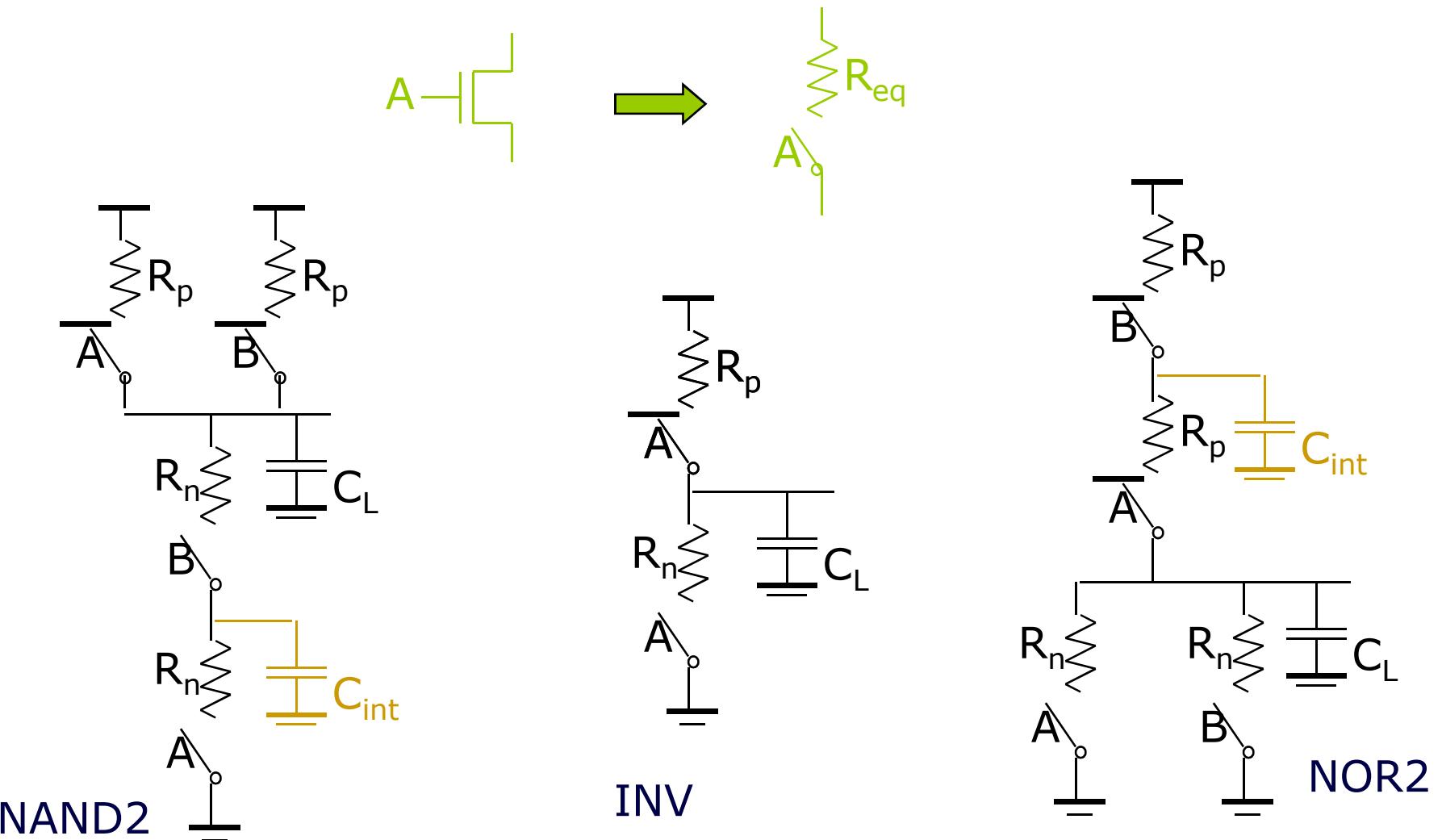
- Full rail-to-rail swing; **high noise margins**
- Logic levels not dependent upon the relative device sizes; **ratioless**
- Always a path to Vdd or Gnd in steady state; **low output impedance**
- Extremely **high input resistance**; nearly zero steady-state input current
- No direct path steady state between power and ground; **no static power dissipation**
- Propagation delay function of load capacitance and resistance of transistors



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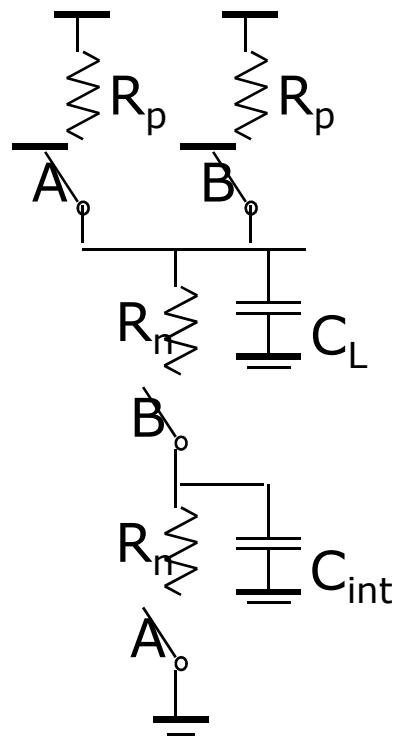
Switch Delay Model



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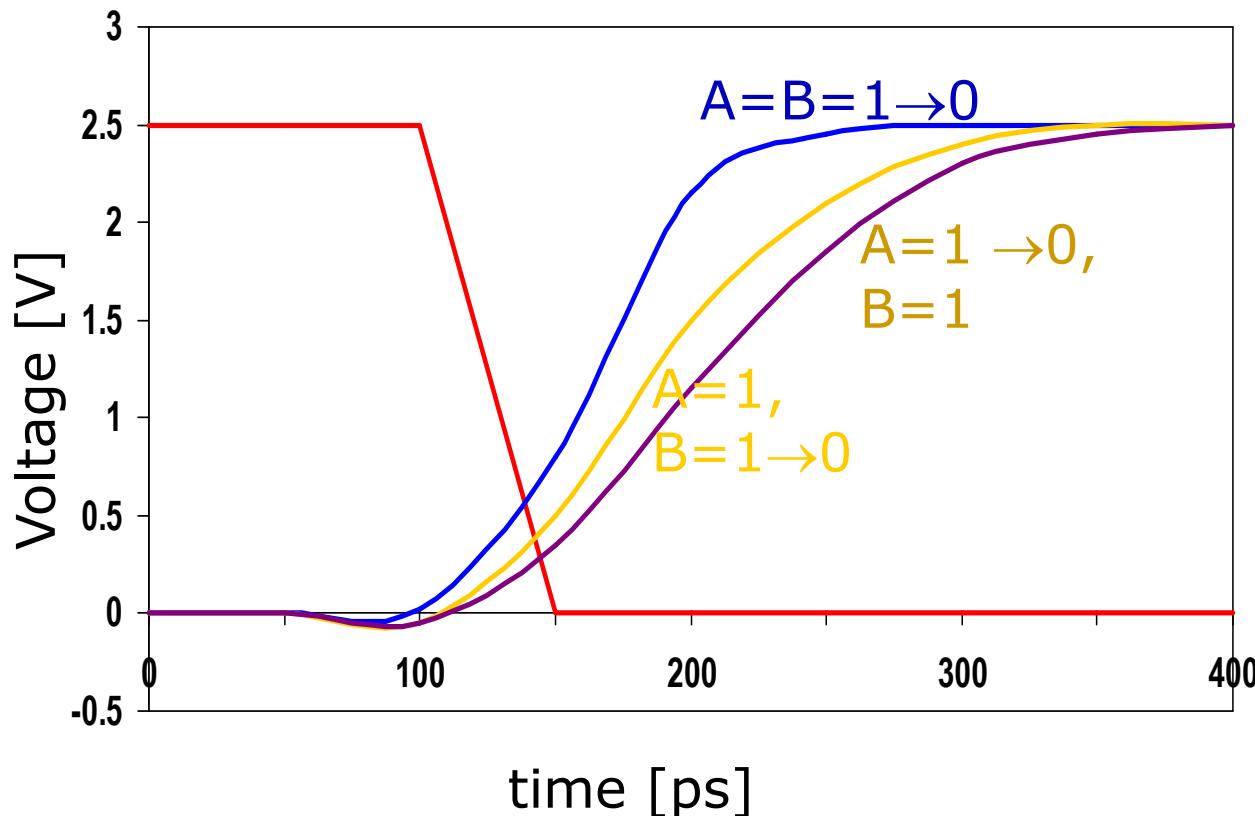
Input Pattern Effects on Delay



- Delay is dependent on the **pattern** of inputs
- Low to high transition
 - both inputs go low
 - delay is $0.69 R_p/2 C_L$
 - one input goes low
 - delay is $0.69 R_p C_L$
- High to low transition
 - both inputs go high
 - delay is $0.69 2R_n C_L$



Delay Dependence on Input Patterns



Input Data Pattern	Delay (psec)
A=B=0→1	67
A=1, B=0→1	64
A=0→1, B=1	61
A=B=1→0	45
A=1, B=1→0	80
A=1→0, B=1	81

NMOS = $0.5\mu\text{m}/0.25\mu\text{m}$

PMOS = $0.75\mu\text{m}/0.25\mu\text{m}$

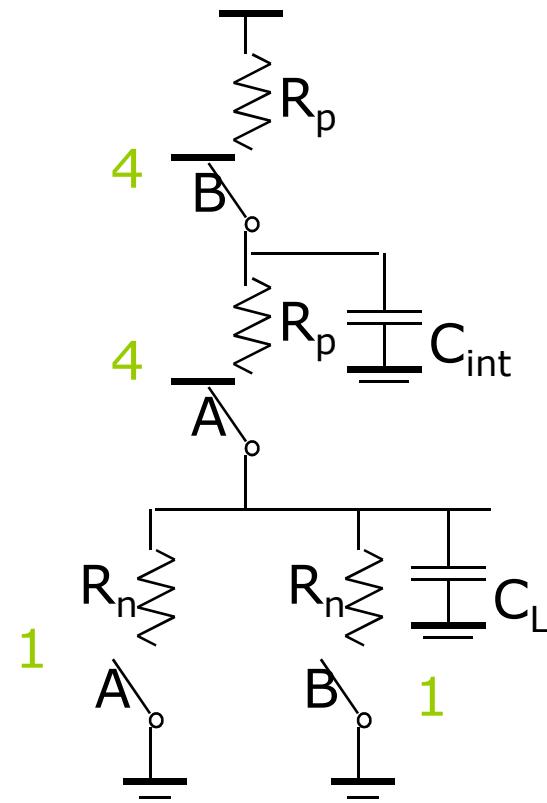
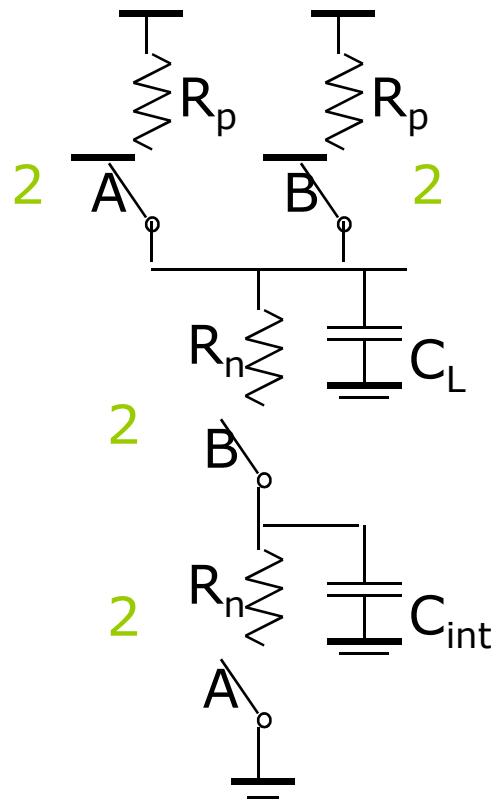
$C_L = 100 \text{ fF}$



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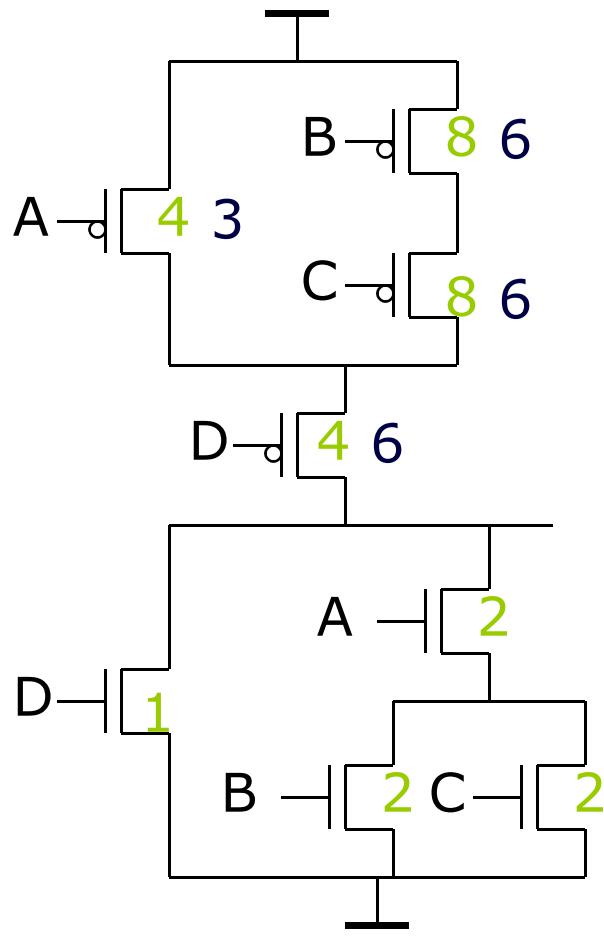
Transistor Sizing



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Transistor Sizing a Complex CMOS Gate



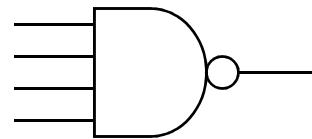
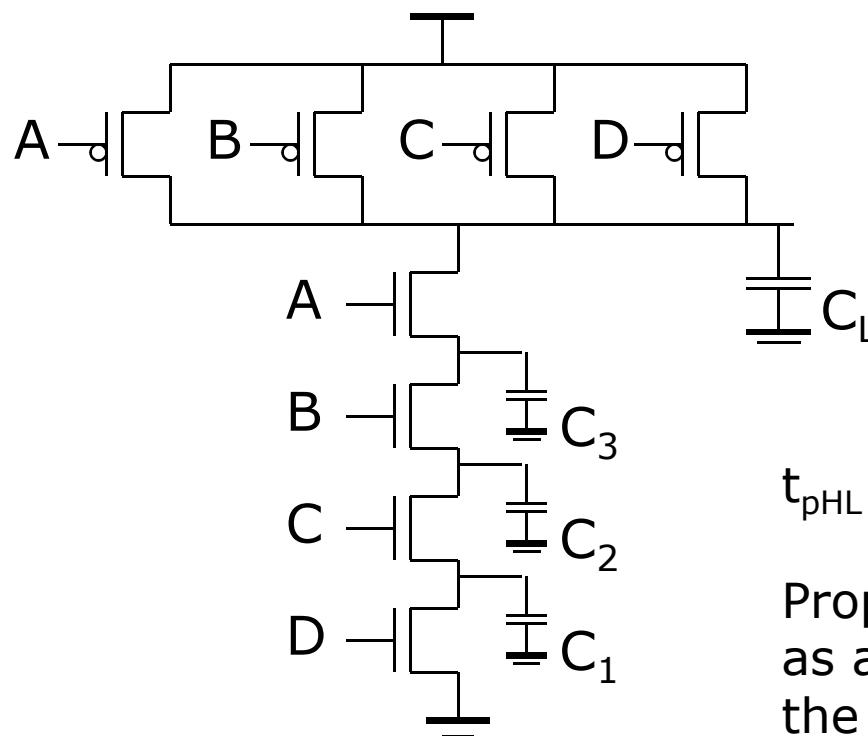
$$\text{OUT} = \overline{D + A \bullet (B + C)}$$



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Fan-In Considerations

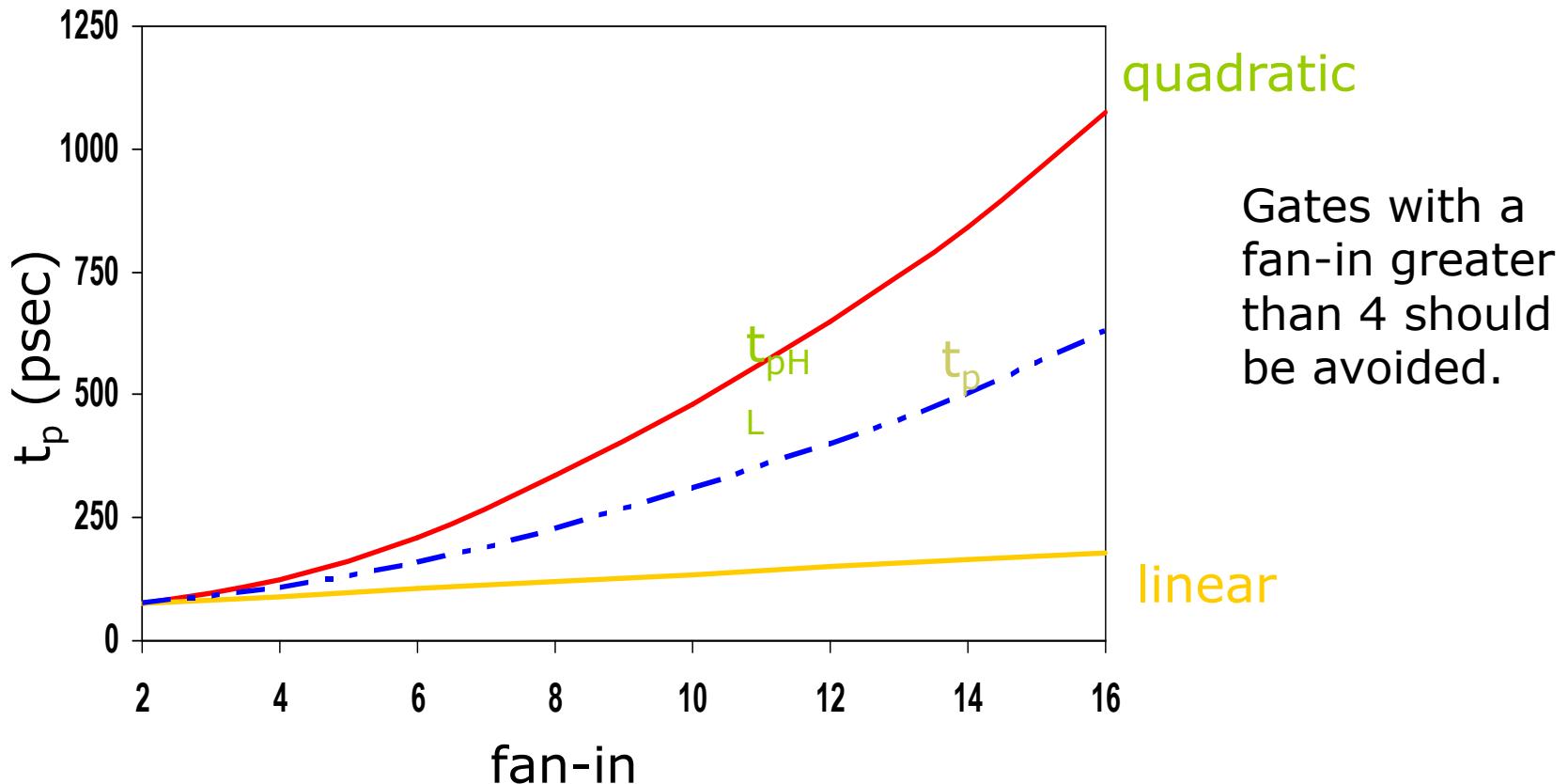


C_L Distributed RC model
(Elmore delay)

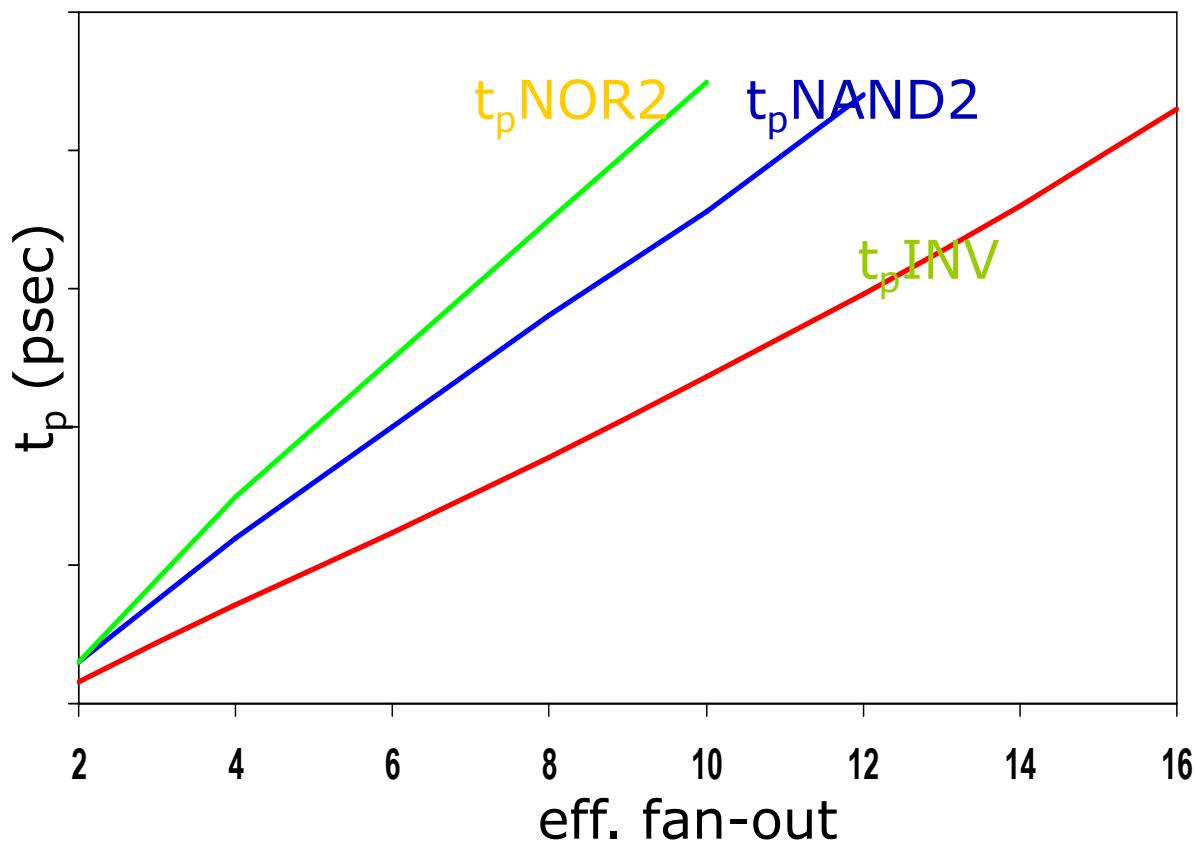
$$t_{pHL} = 0.69 R_{eqn}(C_1 + 2C_2 + 3C_3 + 4C_L)$$

Propagation delay deteriorates rapidly
as a function of fan-in – **quadratically** in
the worst case.

t_p as a Function of Fan-In



t_p as a Function of Fan-Out



All gates have the same drive current.

Slope is a function of “driving strength”



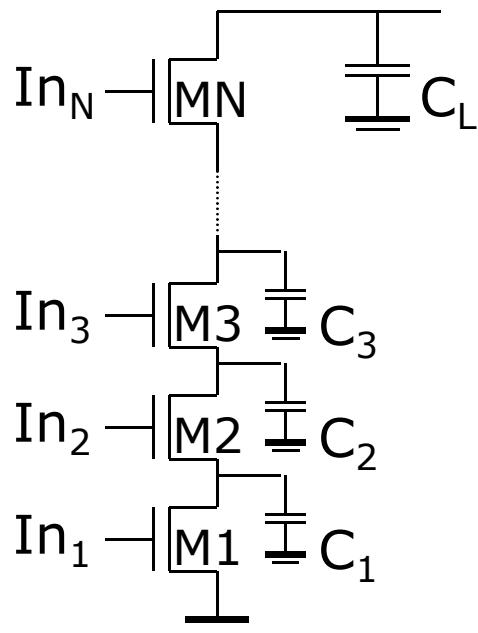
t_p as a Function of Fan-In and Fan-Out

- Fan-in: quadratic due to increasing resistance and capacitance
- Fan-out: each additional fan-out gate adds two gate capacitances to C_L

$$t_p = a_1 FI + a_2 FI^2 + a_3 FO$$

Fast Complex Gates: Design Technique 1

- Transistor sizing
 - as long as fan-out capacitance dominates
- Progressive sizing



Distributed RC line

$M_1 > M_2 > M_3 > \dots > M_N$
(the fet closest to the output is the smallest)

Can reduce delay by more than 20%; decreasing gains as technology shrinks

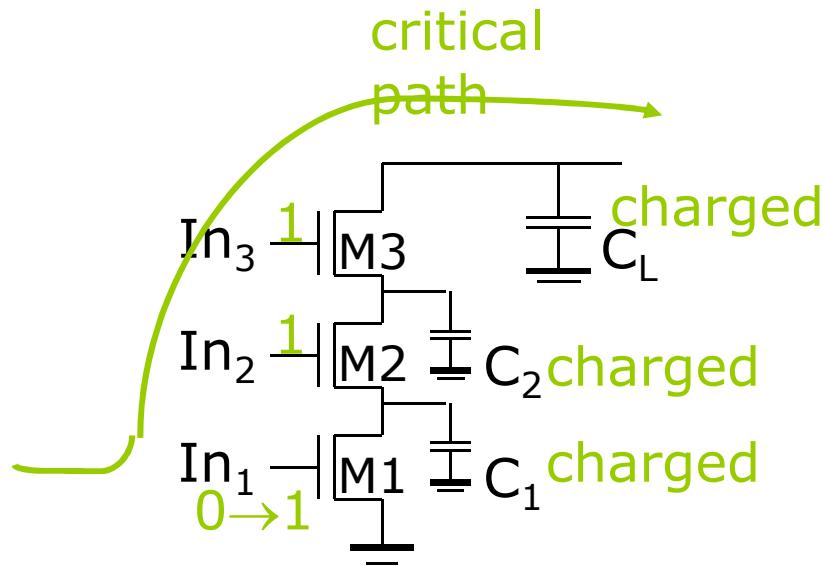


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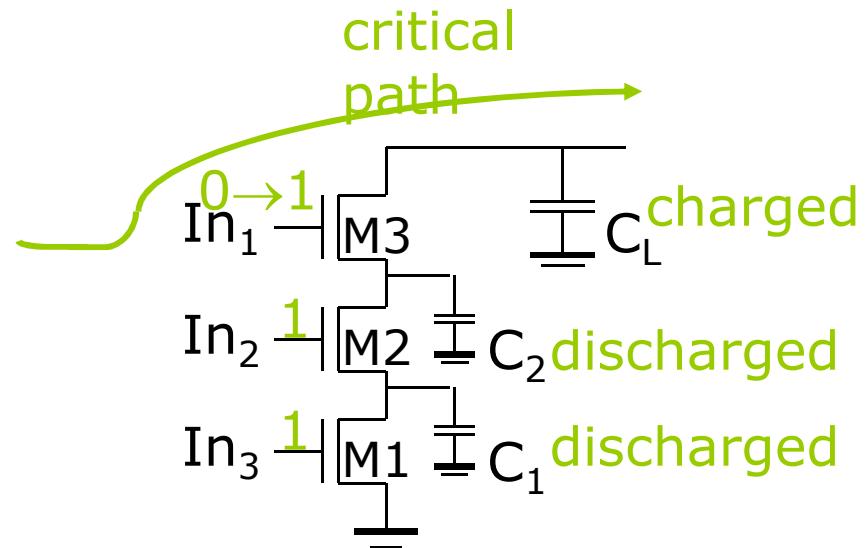
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Fast Complex Gates: Design Technique 2

□ Transistor ordering



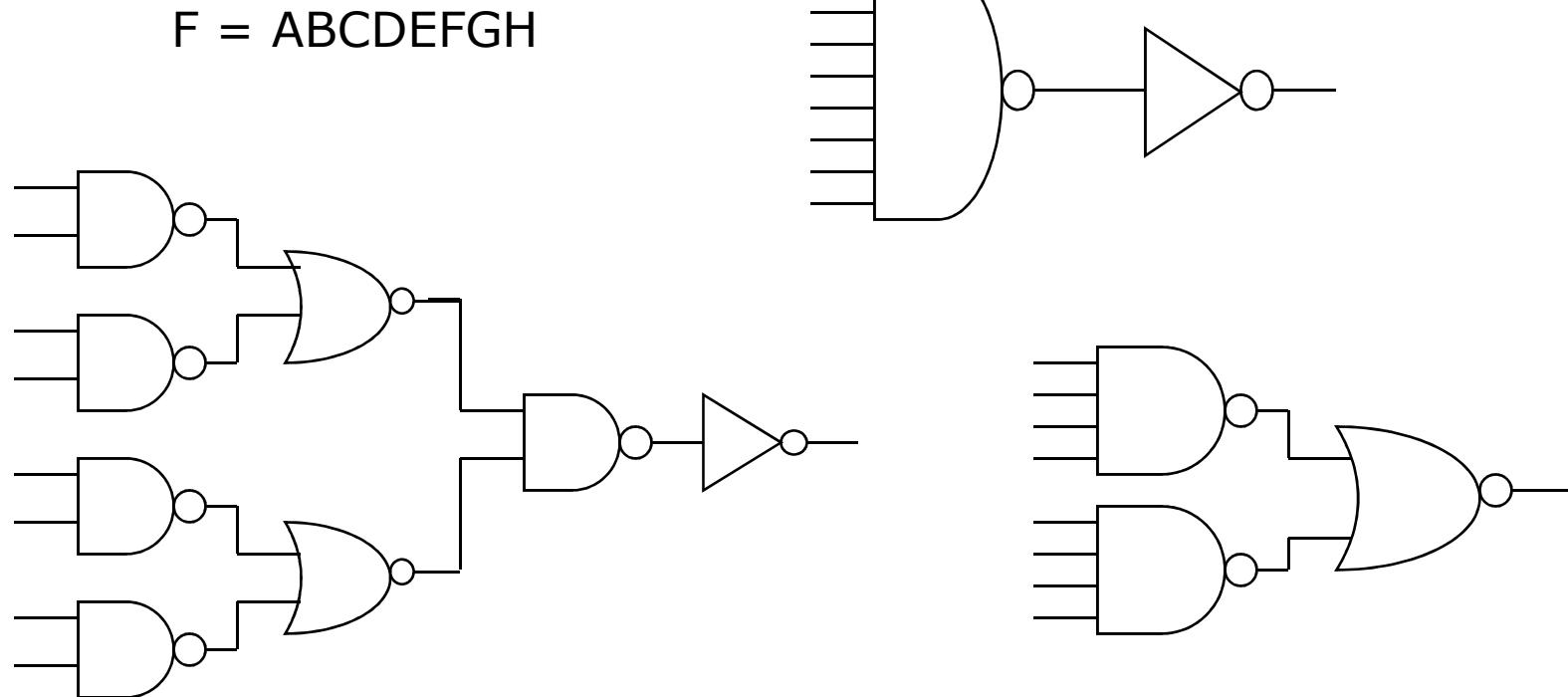
delay determined by
time to discharge C_L , C_1
and C_2



delay determined by
time to discharge C_L

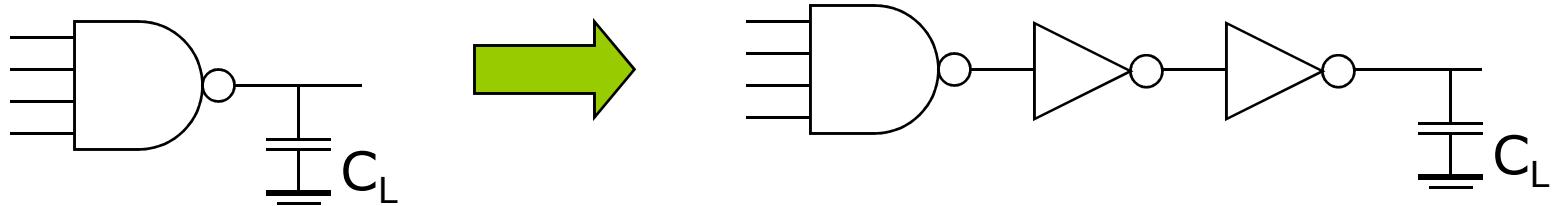
Fast Complex Gates:Design Technique 3

□ Alternative logic structures



Fast Complex Gates:Design Technique 4

- Isolating fan-in from fan-out using buffer insertion



Fast Complex Gates:Design Technique 5

- Reducing the voltage swing

$$t_{pHL} = 0.69 \left(\frac{3}{4} (C_L V_{DD}) / I_{DSATn} \right)$$

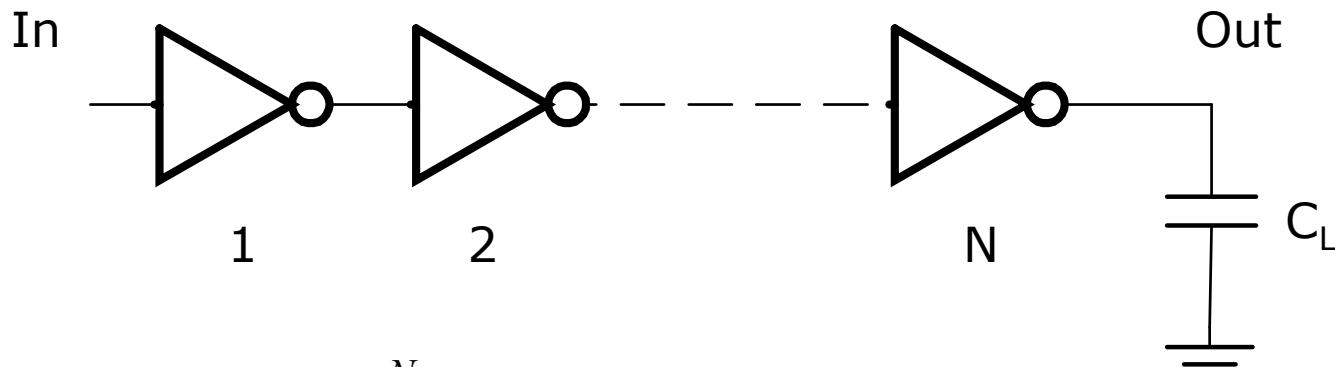
$$= 0.69 \left(\frac{3}{4} (C_L V_{swing}) / I_{DSATn} \right)$$

- linear reduction in delay
- also reduces power consumption
- But the following gate is much slower!
- Or requires use of “sense amplifiers” on the receiving end to restore the signal level (memory design)

Sizing Logic Paths for Speed

- ❑ Frequently, input capacitance of a logic path is constrained
- ❑ Logic also has to drive some capacitance
- ❑ Example: ALU load in an Intel's microprocessor is 0.5pF
- ❑ How do we size the ALU datapath to achieve maximum speed?
- ❑ We have already solved this for the inverter chain – can we generalize it for any type of logic?

Buffer Example



$$Delay = \sum_{i=1}^N (p_i + g_i \cdot f_i) \quad (\text{in units of } \tau_{\text{inv}})$$

For given N: $C_{i+1}/C_i = C_i/C_{i-1}$

To find N: $C_{i+1}/C_i \sim 4$

How to generalize this to any logic path?



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Logical Effort

$$\begin{aligned} \text{Delay} &= k \cdot R_{\text{unit}} C_{\text{unit}} \left(1 + \frac{C_L}{\gamma C_{in}} \right) \\ &= \tau(p + g \cdot f) \end{aligned}$$

p – intrinsic delay ($3kR_{\text{unit}}C_{\text{unit}}\gamma$) - gate parameter $\neq f(W)$

g – logical effort ($kR_{\text{unit}}C_{\text{unit}}$) – gate parameter $\neq f(W)$

f – effective fanout

Normalize everything to an inverter:

$g_{\text{inv}} = 1$, $p_{\text{inv}} = 1$

Divide everything by τ_{inv}

(everything is measured in unit delays τ_{inv})

Assume $\gamma = 1$.



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Delay in a Logic Gate

Gate delay:

$$d = h + p$$

effort delay **intrinsic delay**

Effort delay:

$$h = g f$$

logical effort **effective fanout =
 C_{out}/C_{in}**

Logical effort is a function of topology, independent of sizing

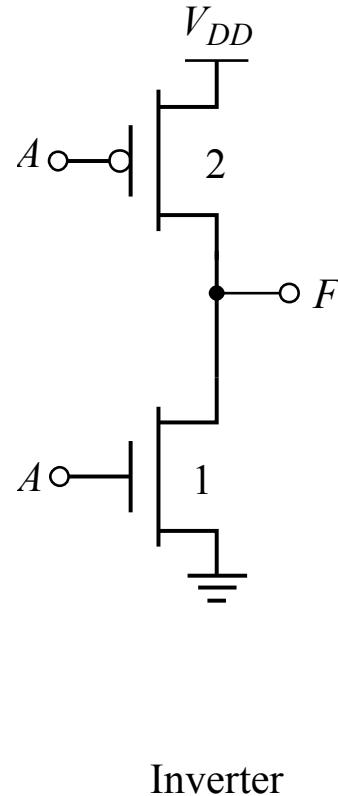
Effective fanout (electrical effort) is a function of load/gate size

Logical Effort

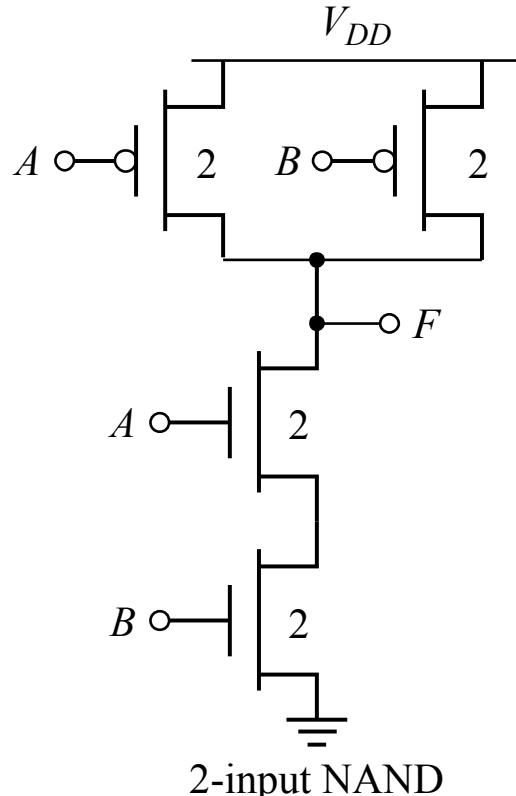
- ❑ Inverter has the smallest logical effort and intrinsic delay of all static CMOS gates
- ❑ Logical effort of a gate presents the ratio of its input capacitance to the inverter capacitance when sized to deliver the same current
- ❑ Logical effort increases with the gate complexity

Logical Effort

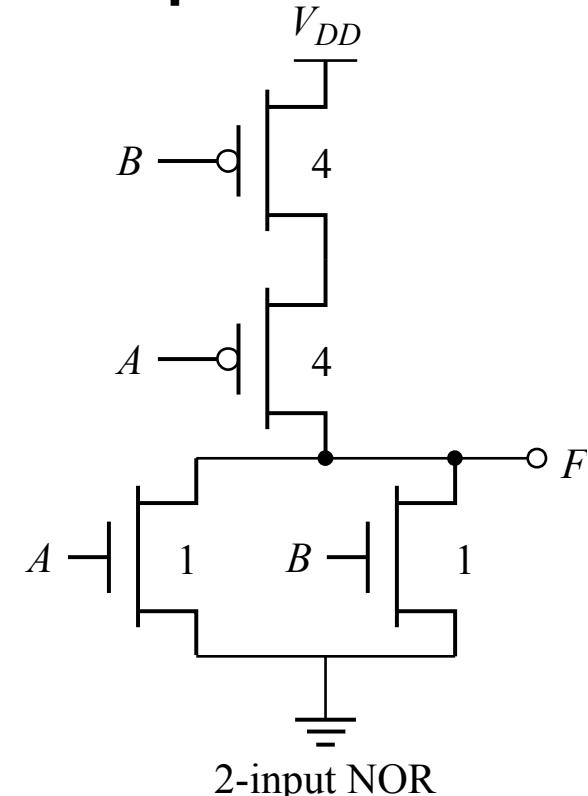
Logical effort is the ratio of input capacitance of a gate to the input capacitance of an inverter with the same output current



$$g = 1$$



$$g = 4/3$$

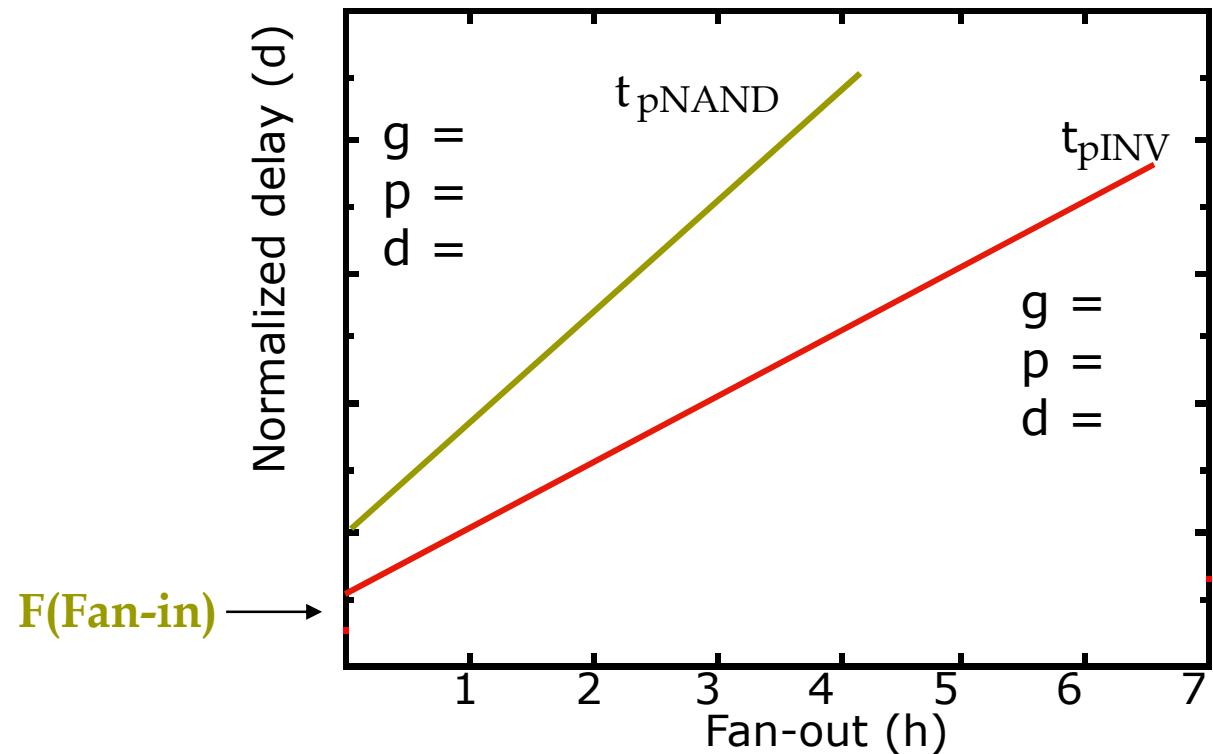


$$g = 5/3$$



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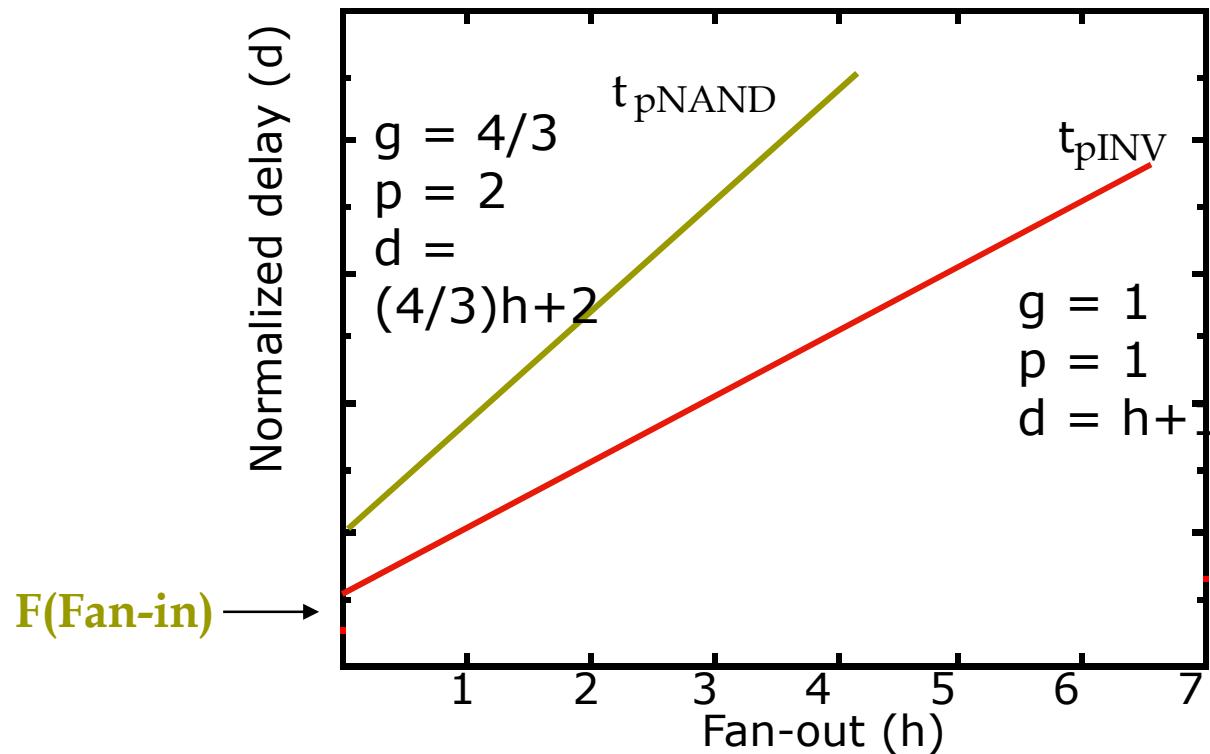
Logical Effort of Gates



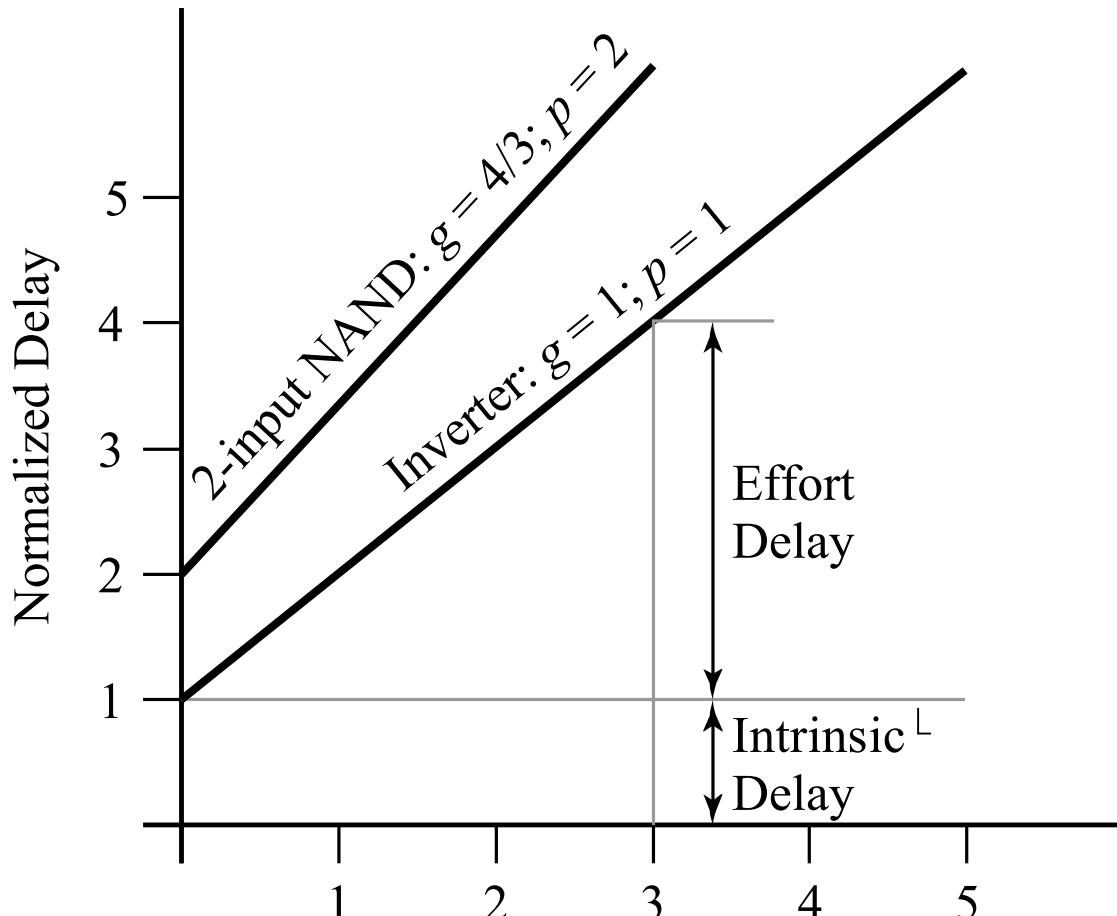
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Logical Effort of Gates



Logical Effort of Gates



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Fanout f

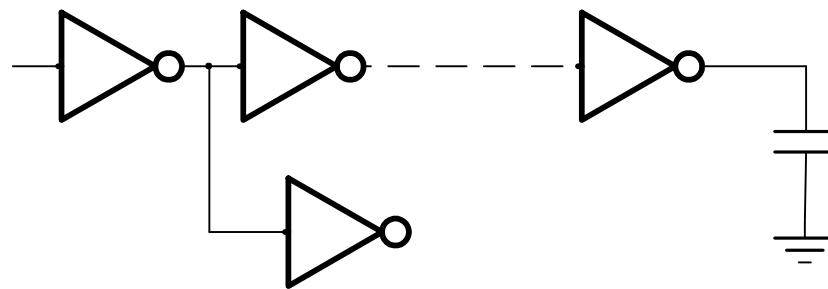
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Add Branching Effort

Branching effort:

$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$$



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Multistage Networks

$$Delay = \sum_{i=1}^N (p_i + g_i \cdot f_i)$$

Stage effort: $h_i = g_i f_i$

Path electrical effort: $F = C_{\text{out}}/C_{\text{in}}$

Path logical effort: $G = g_1 g_2 \dots g_N$

Branching effort: $B = b_1 b_2 \dots b_N$

Path effort: $H = GFB$

Path delay $D = \sum d_i = \sum p_i + \sum h_i$

Optimum Effort per Stage

When each stage bears the same effort:

$$h^N = H$$

$$h = \sqrt[N]{H}$$

Stage efforts: $g_1 f_1 = g_2 f_2 = \dots = g_N f_N$

Effective fanout of each stage: $f_i = h/g_i$

Minimum path delay

$$\hat{D} = \sum (g_i f_i + p_i) = NH^{1/N} + P$$



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Optimal Number of Stages

For a given load,
and given input capacitance of the first gate
Find optimal number of stages and optimal sizing

$$D = NH^{1/N} + Np_{inv}$$

$$\frac{\partial D}{\partial N} = -H^{1/N} \ln(H^{1/N}) + H^{1/N} + p_{inv} = 0$$

Substitute 'best stage effort'

$$h = H^{1/\hat{N}}$$



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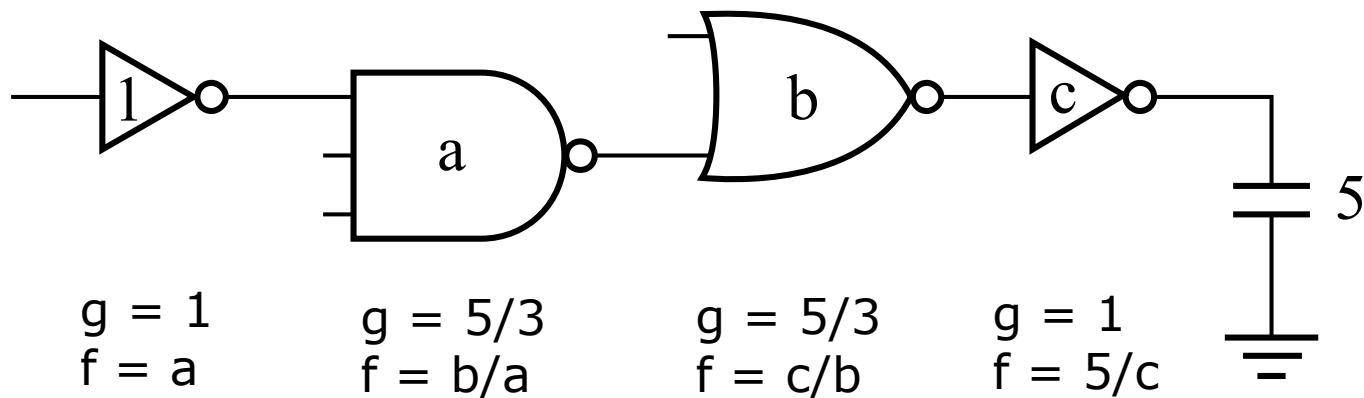
Logical Effort

Gate Type	Number of Inputs			
	1	2	3	n
Inverter	1			
NAND		4/3	5/3	(n + 2)/3
NOR		5/3	7/3	(2n + 1)/3
Multiplexer		2	2	2
XOR		4	12	

From Sutherland, Sproull



Example: Optimize Path



Effective fanout, F =

G =

H =

h =

a =

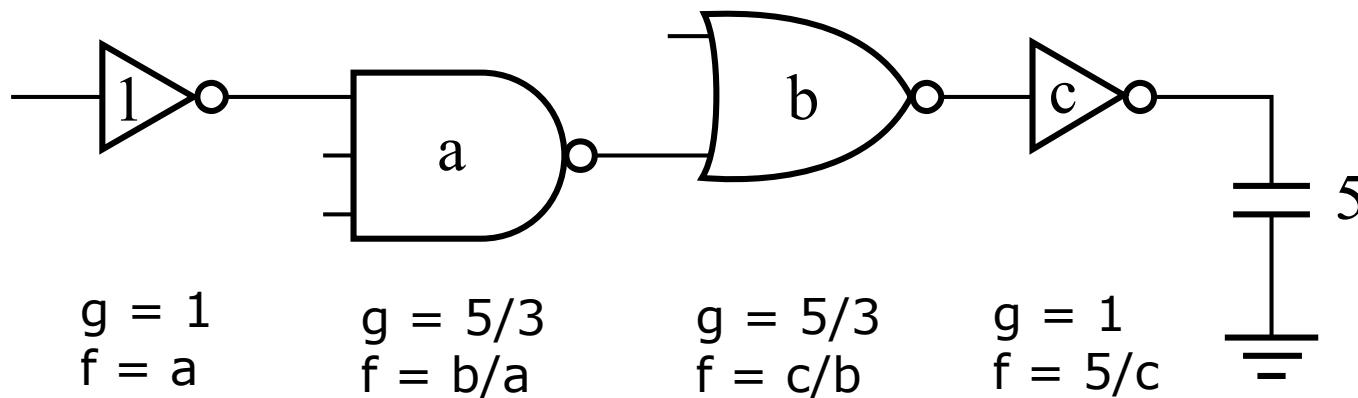
b =



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Example: Optimize Path



Effective fanout, $F = 5$

$$G = 25/9$$

$$H = 125/9 = 13.9$$

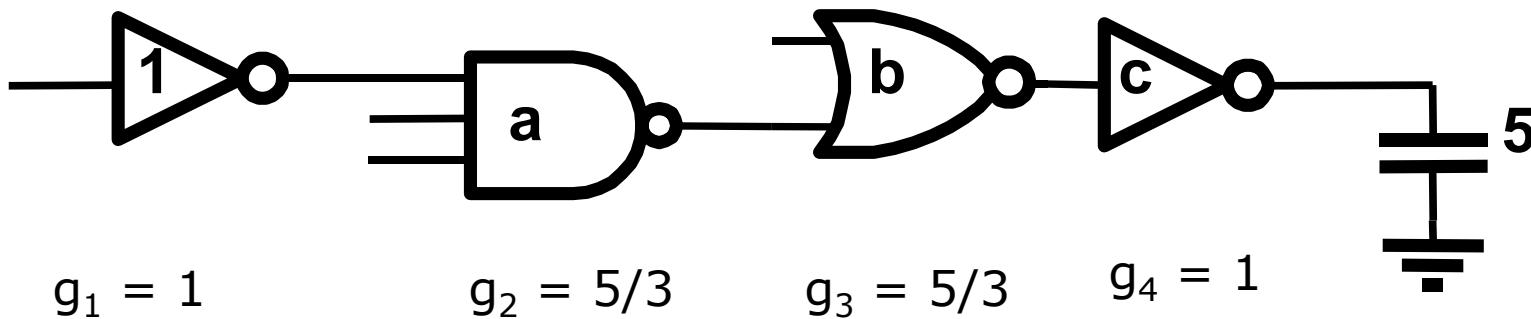
$$h = 1.93$$

$$a = 1.93$$

$$b = ha/g_2 = 2.23$$

$$c = hb/g_3 = 5g_4/f = 2.59$$

Example: Optimize Path



Effective fanout, $H = 5$

$$G = 25/9$$

$$F = 125/9 = 13.9$$

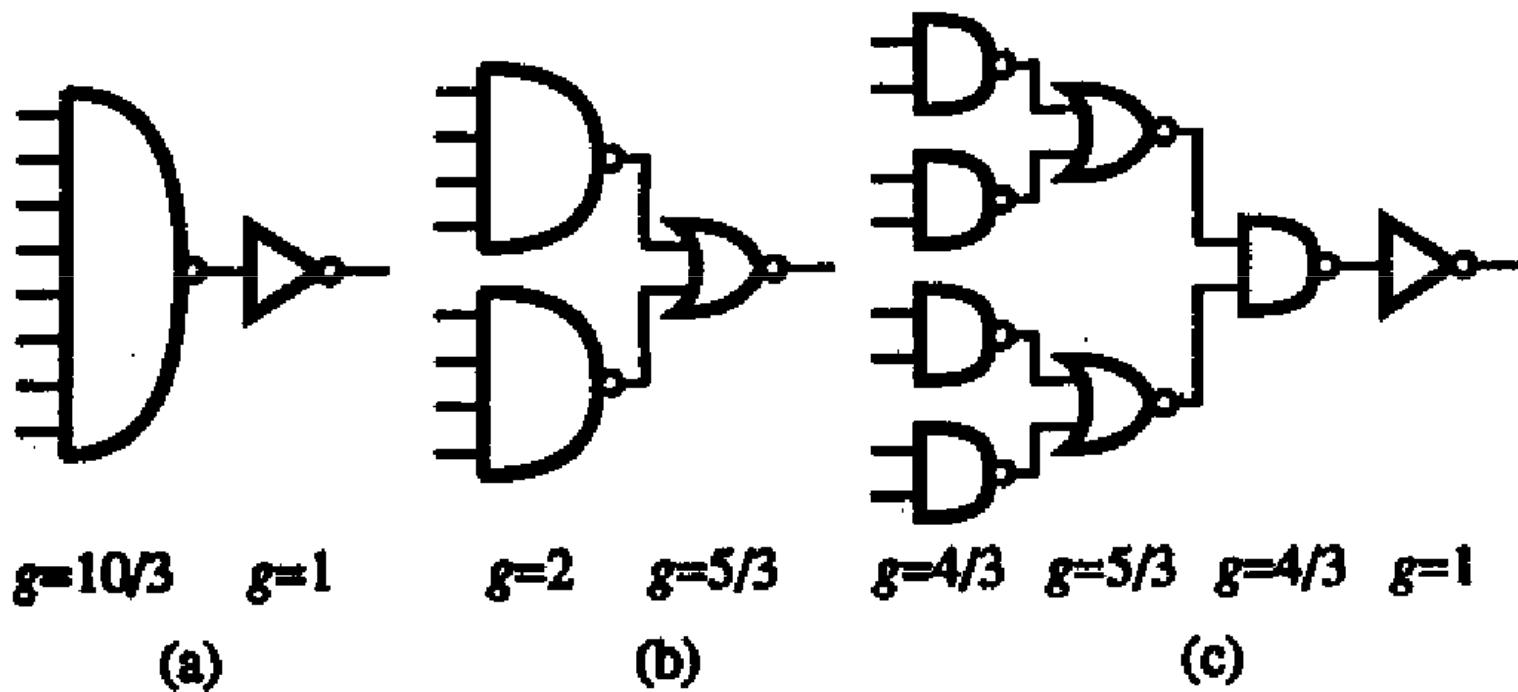
$$f = 1.93$$

$$a = 1.93$$

$$b = fa/g_2 = 2.23$$

$$c = fb/g_3 = 5g_4/f = 2.59$$

Example – 8-input AND



Method of Logical Effort

- Compute the path effort: $F = GBH$
- Find the best number of stages $N \sim \log_4 F$
- Compute the stage effort $f = F^{1/N}$
- Sketch the path with this number of stages
- Work either from either end, find sizes:
 $C_{in} = C_{out} * g/f$

Reference: Sutherland, Sproull, Harris, "Logical Effort, Morgan-Kaufmann 1999.



Summary

Table 4: Key Definitions of Logical Effort

Term	Stage expression	Path expression
Logical effort	g (seeTable 1)	$G = \prod g_i$
Electrical effort	$h = \frac{C_{out}}{C_{in}}$	$H = \frac{C_{out} (path)}{C_{in} (path)}$
Branching effort	n/a	$B = \prod b_i$
Effort	$f = gh$	$F = GBH$
Effort delay	f	$D_F = \sum f_i$
Number of stages	1	N
Parasitic delay	p (seeTable 2)	$P = \sum p_i$
Delay	$d = f + p$	$D = D_F + P$

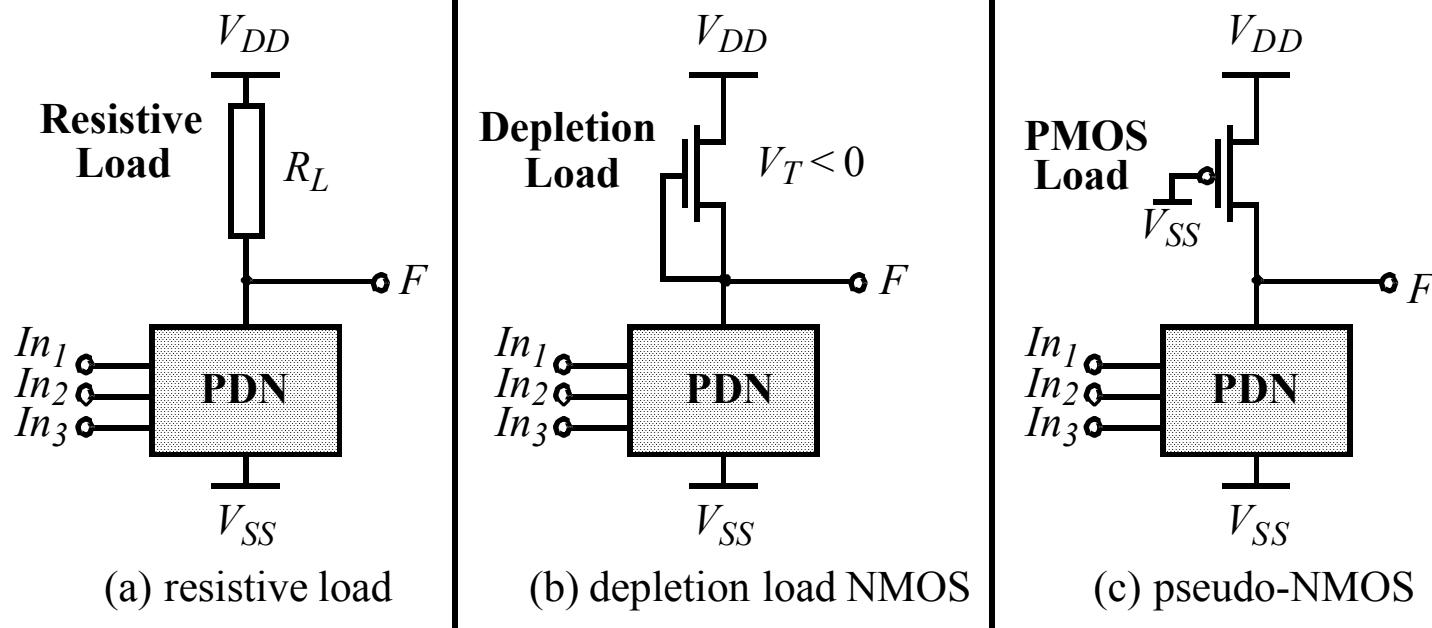
Sutherland,
Sproull
Harris



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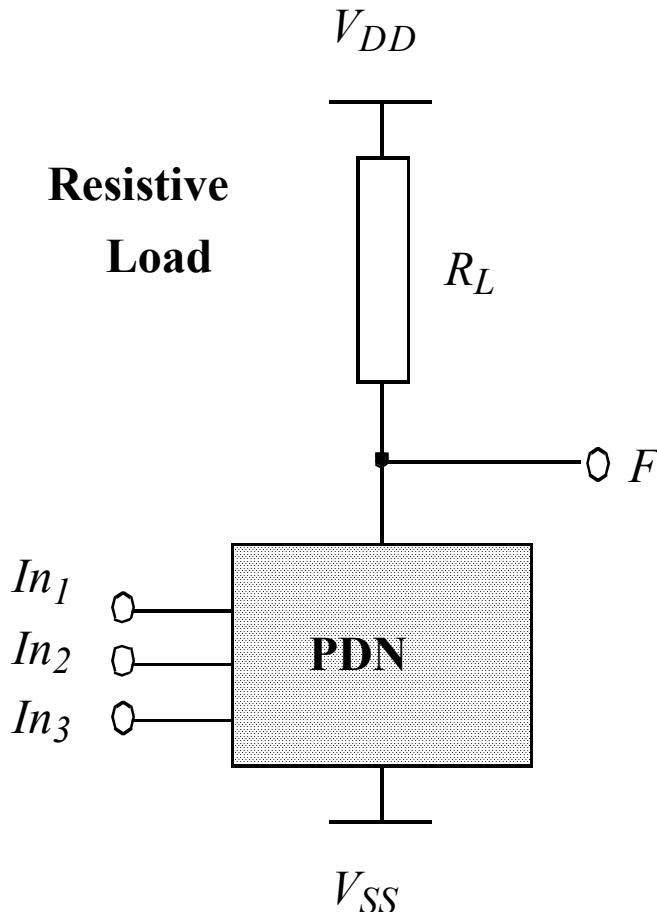
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Ratioed Logic



Goal: to reduce the number of devices over complementary CMOS

Ratioed Logic



- N transistors + Load

- $V_{OH} = V_{DD}$

- $V_{OL} = \frac{R_{PN}}{R_{PN} + R_L}$

- Assymetrical response

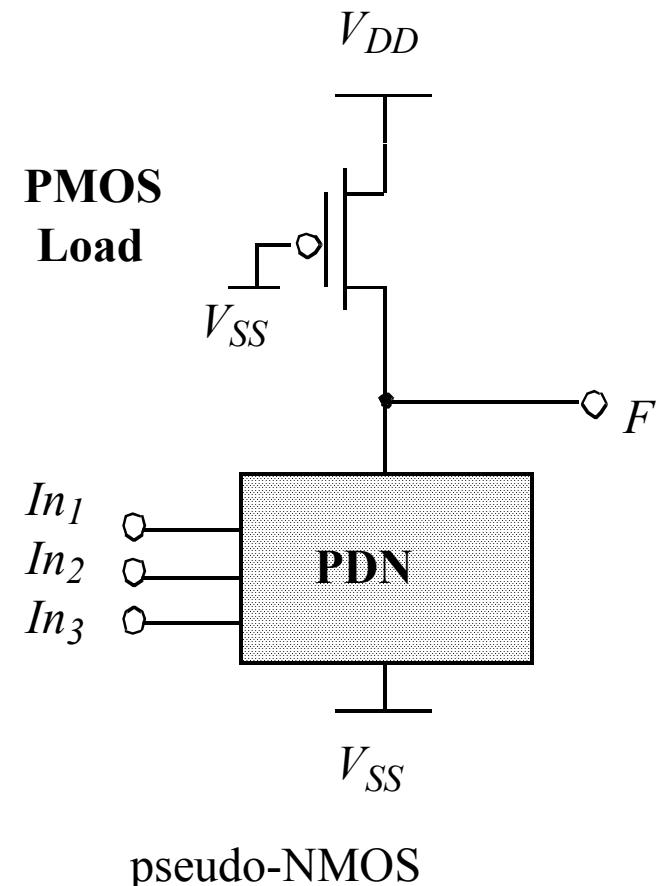
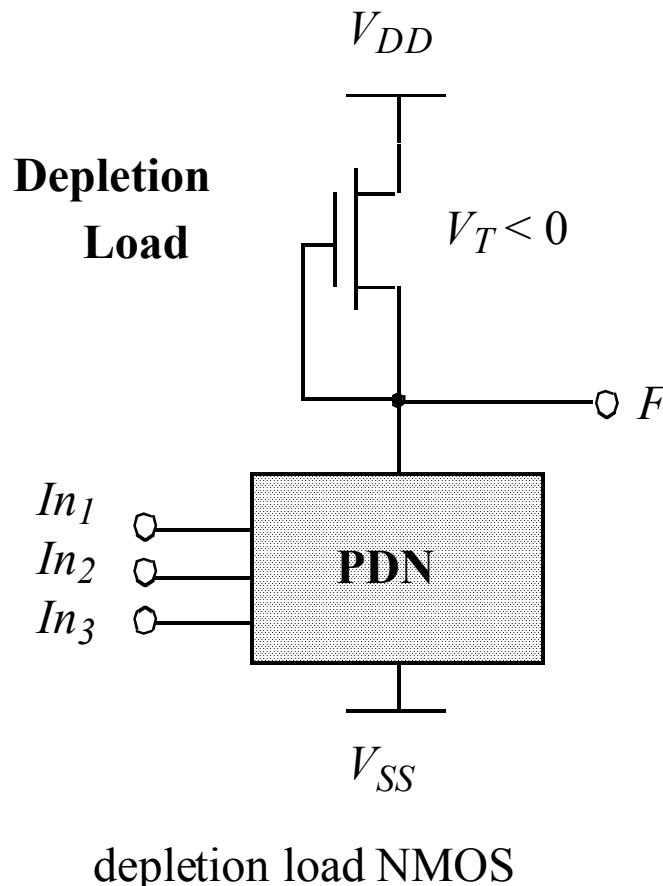
- Static power consumption

- $t_{pL} = 0.69 R_L C_L$

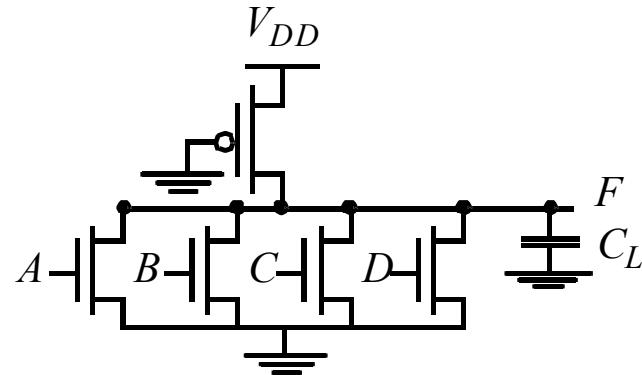


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Active Loads



Pseudo-NMOS



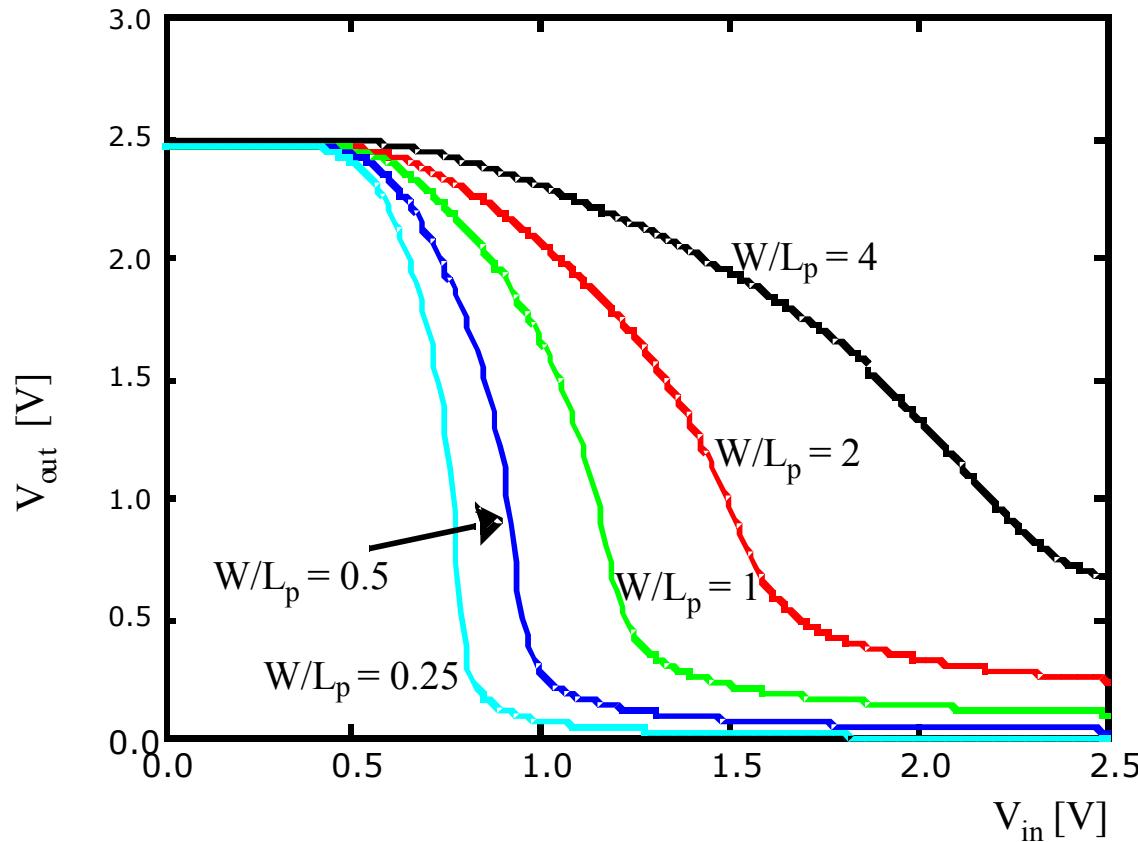
$V_{OH} = V_{DD}$ (similar to complementary CMOS)

$$k_n \left((V_{DD} - V_{Tn}) V_{OL} - \frac{V_{OL}^2}{2} \right) = \frac{k_p}{2} (V_{DD} - |V_{Tp}|)^2$$

$$V_{OL} = (V_{DD} - V_T) \left[1 - \sqrt{1 - \frac{k_p}{k_n}} \right] \text{ (assuming that } V_T = V_{Tn} = |V_{Tp}|)$$

SMALLER AREA & LOAD BUT STATIC POWER DISSIPATION!!!

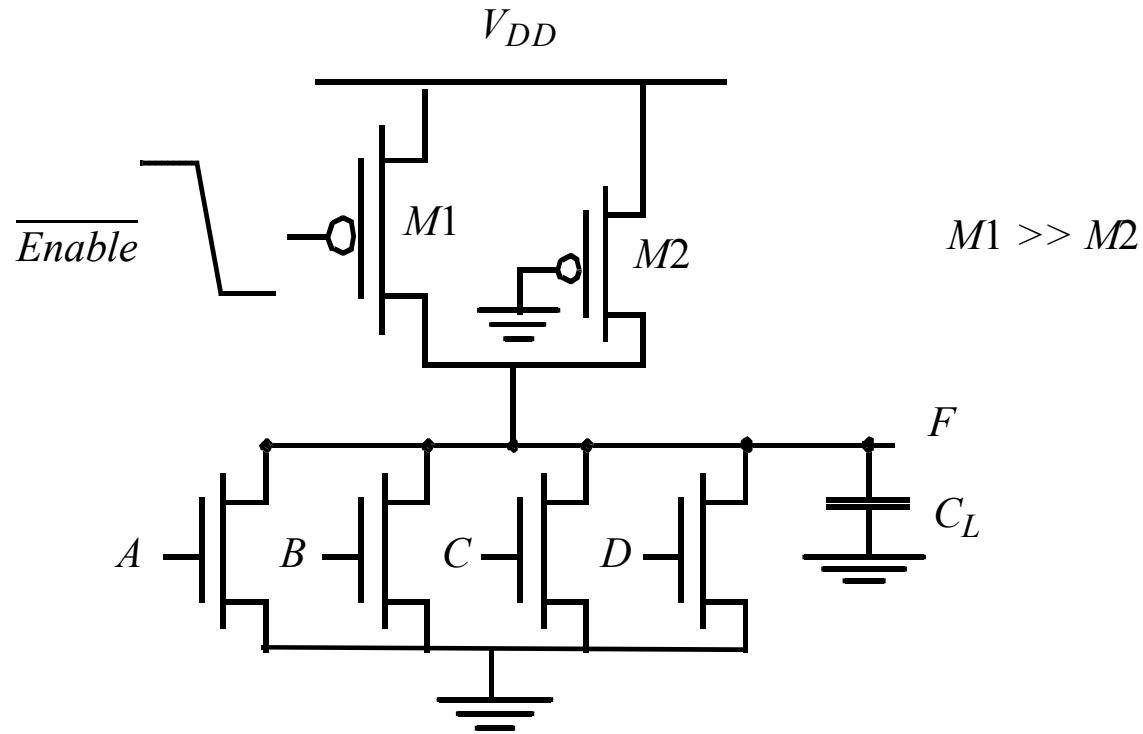
Pseudo-NMOS VTC



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Improved Loads



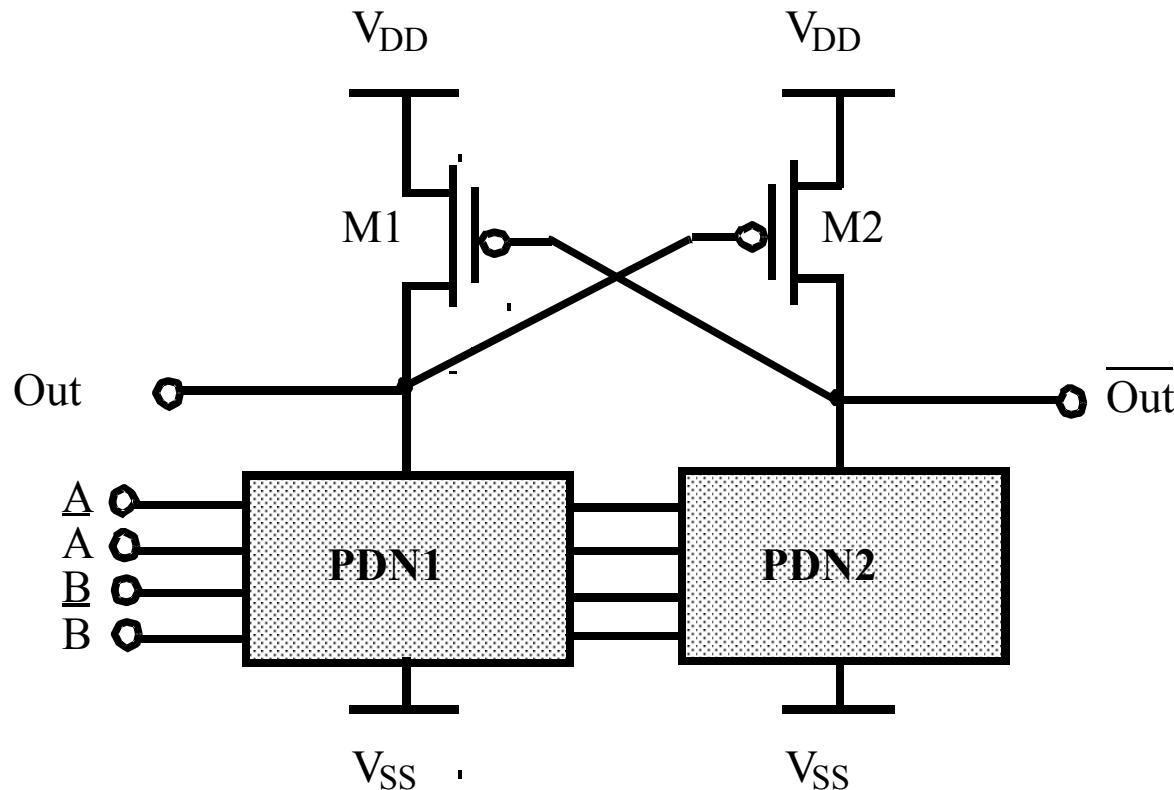
Adaptive Load



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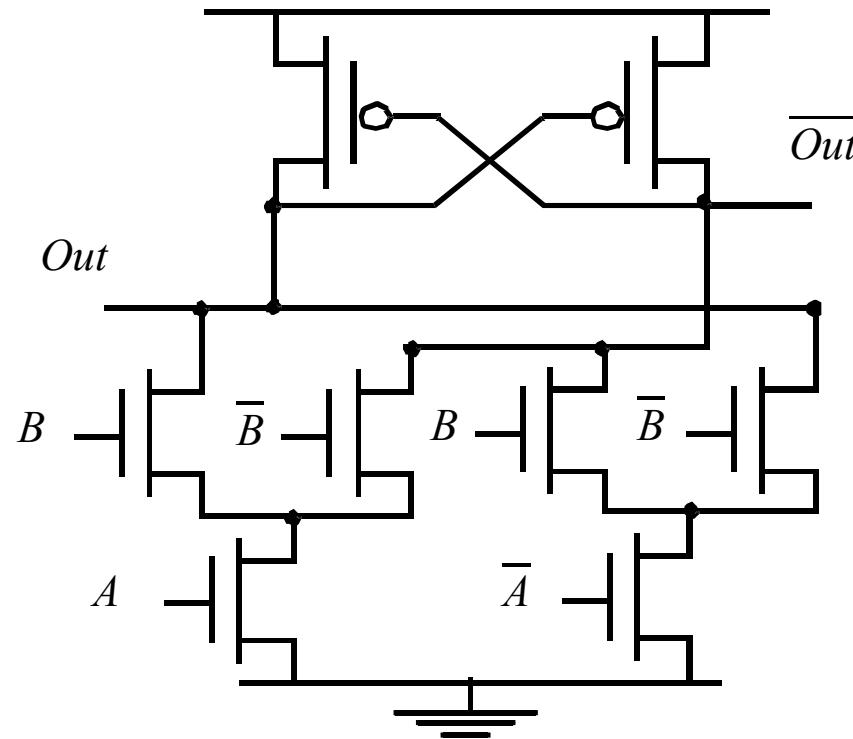
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Improved Loads (2)



Differential Cascode Voltage Switch Logic (DCVSL)

DCVSL Example



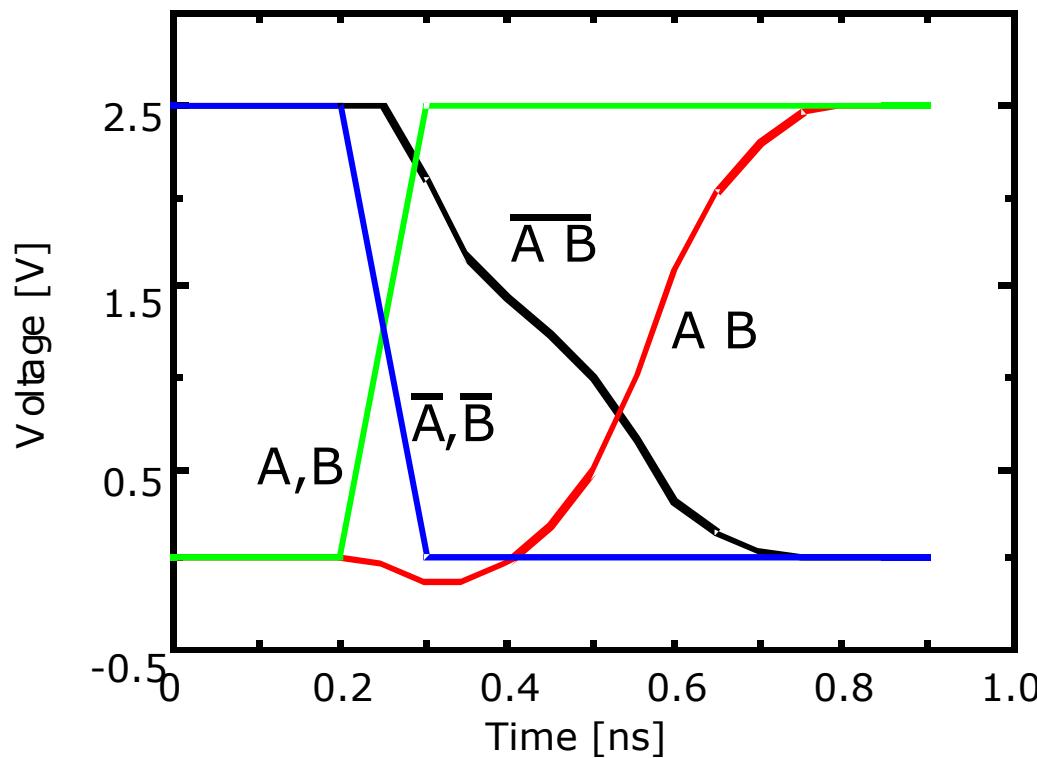
XOR-NXOR gate



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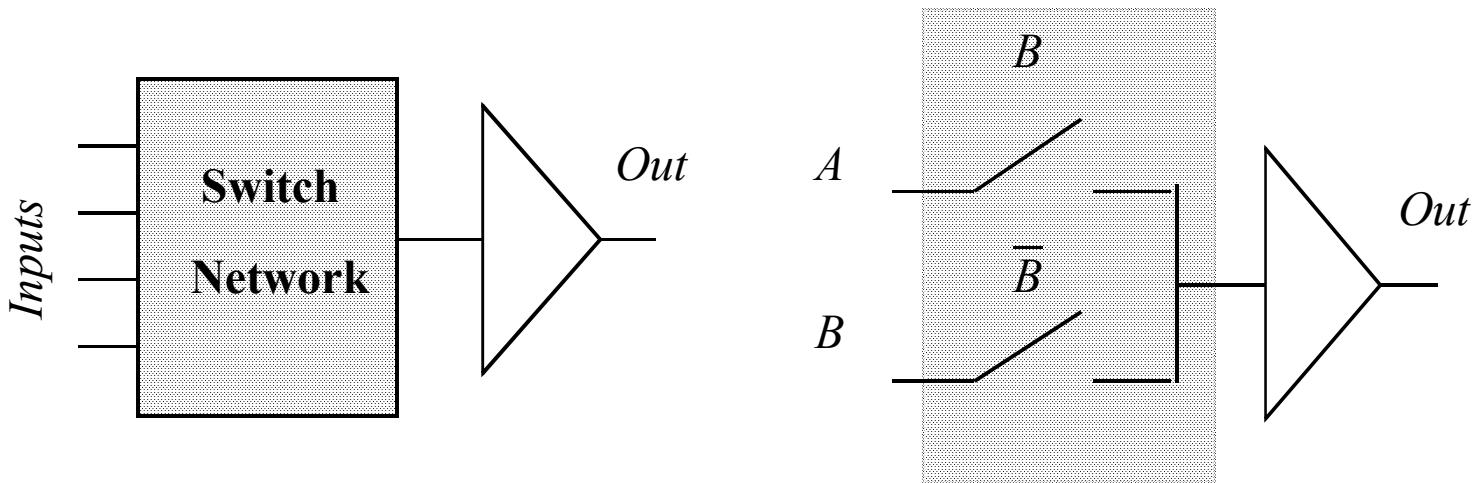
DCVSL Transient Response



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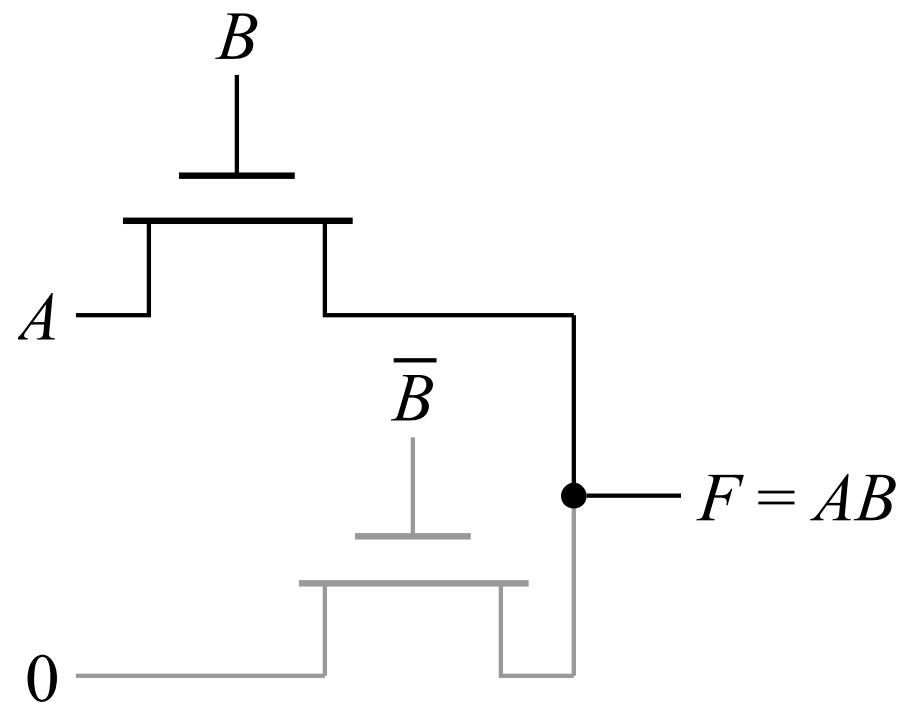
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Pass-Transistor Logic



- N transistors
- No static consumption

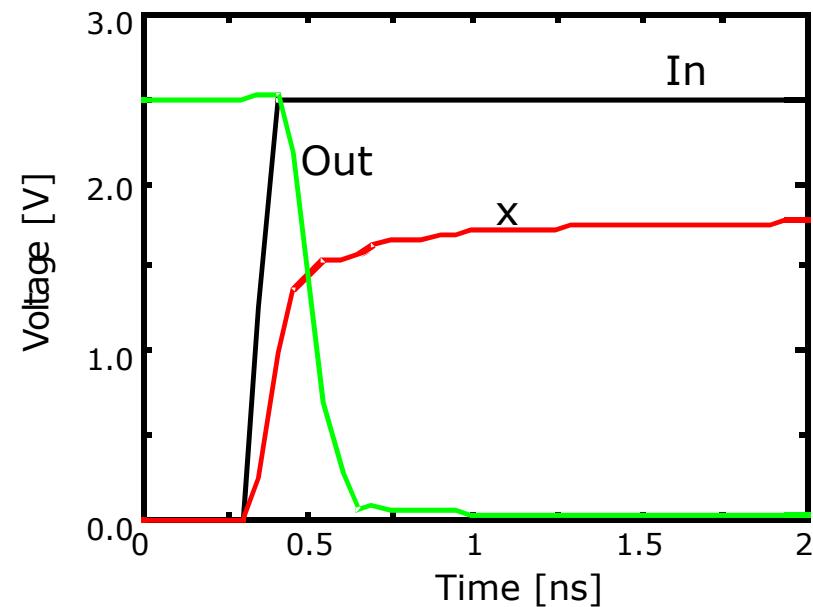
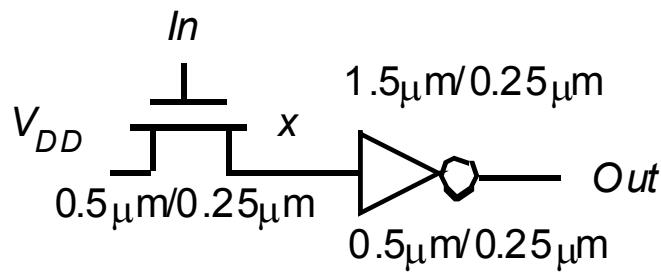
Example: AND Gate



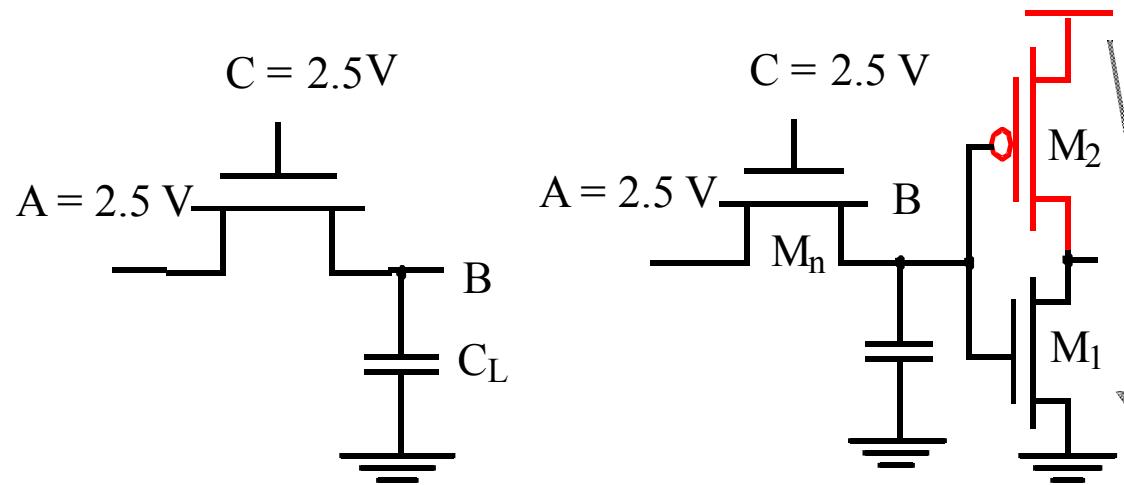
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NMOS-Only Logic



NMOS-only Switch



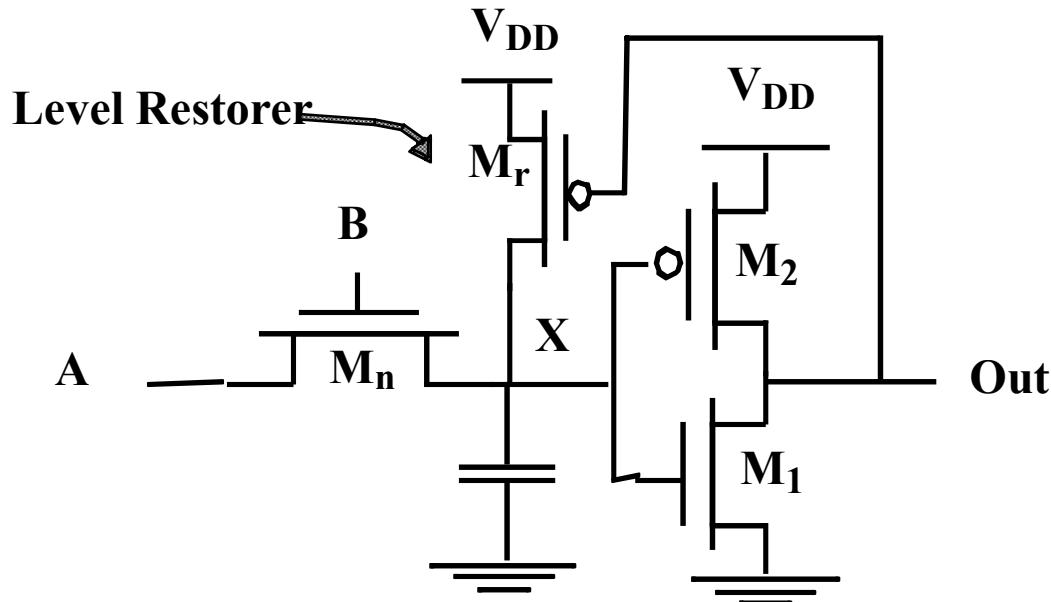
V_B does not pull up to 2.5V, but $2.5\text{V} - V_{TN}$

Threshold voltage loss causes static power consumption

NMOS has higher threshold than PMOS (body effect)

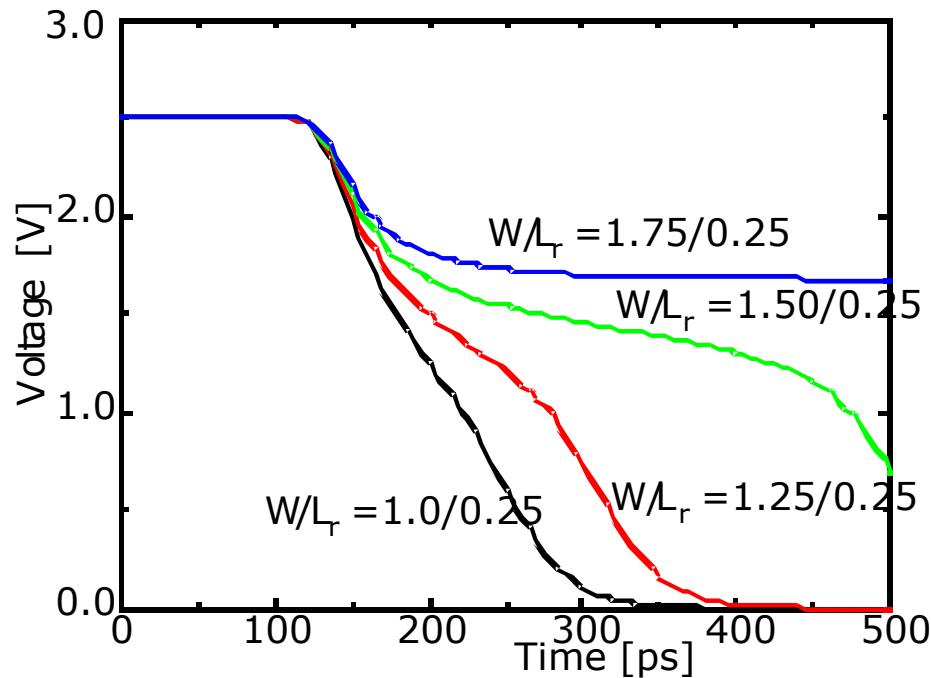
NMOS Only Logic:

Level Restoring Transistor



- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem

Restorer Sizing



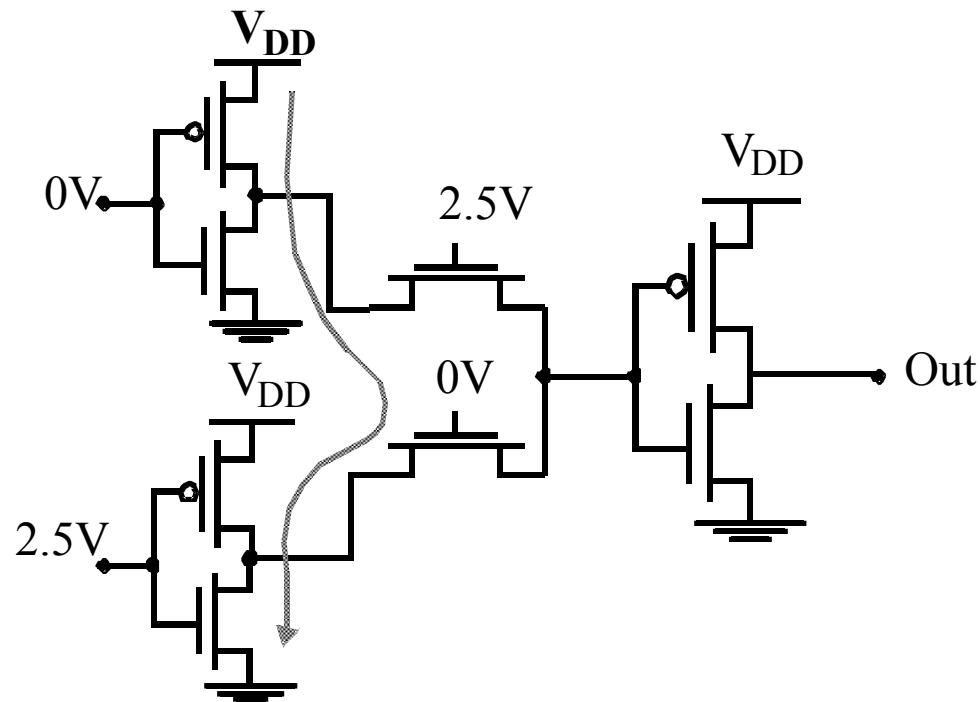
- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack



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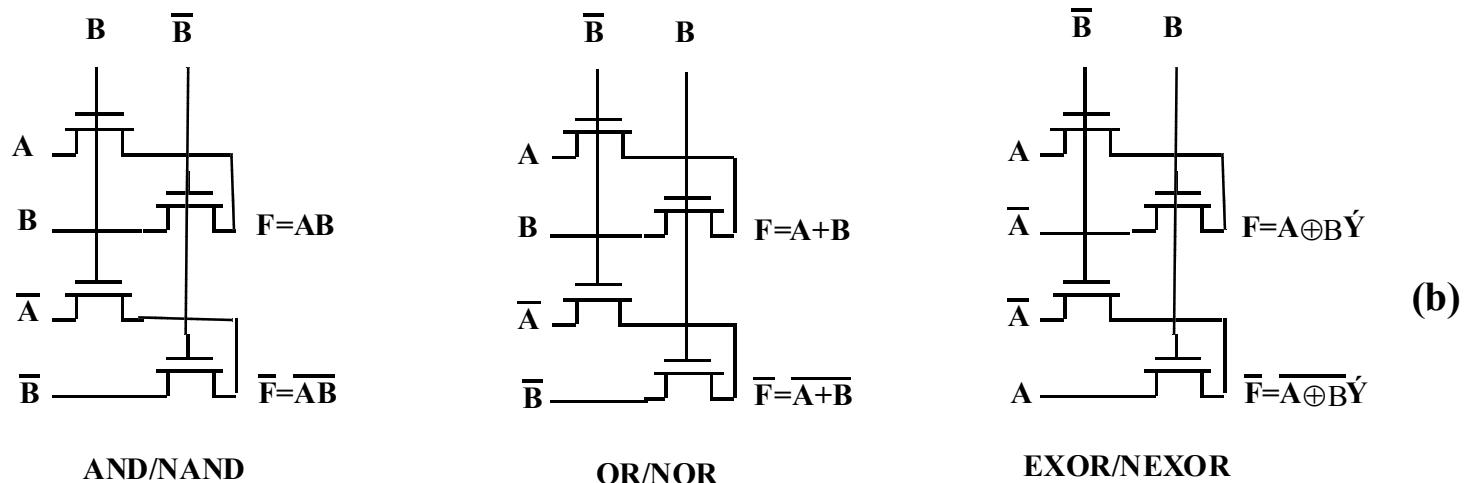
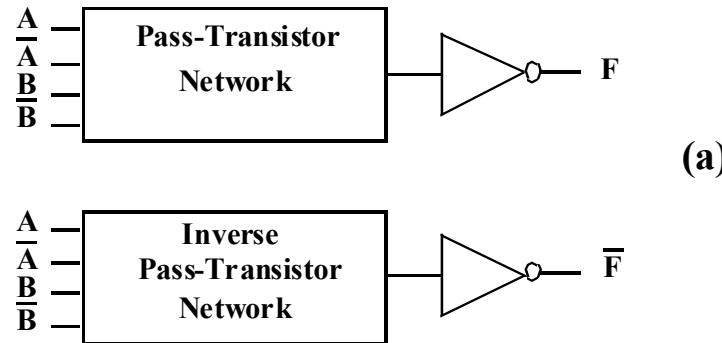
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Solution 2: Single Transistor Pass Gate with $V_T=0$

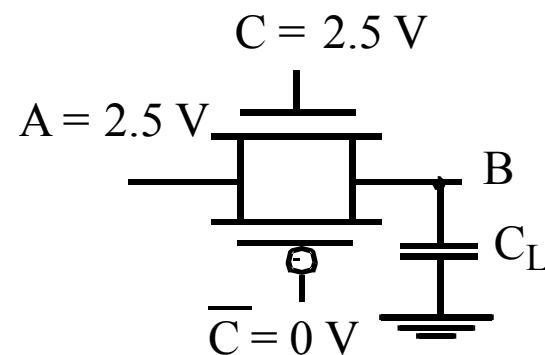
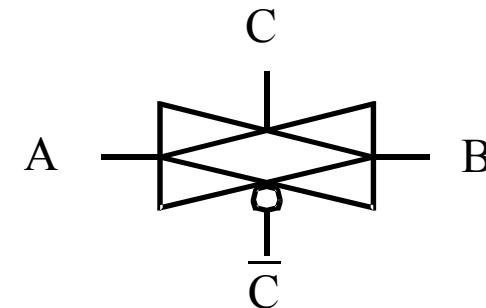
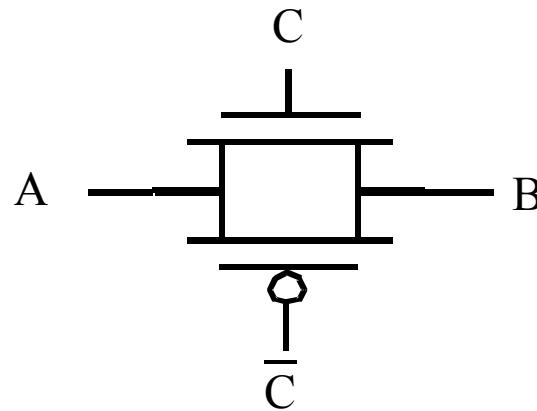


WATCH OUT FOR LEAKAGE CURRENTS

Complementary Pass Transistor Logic



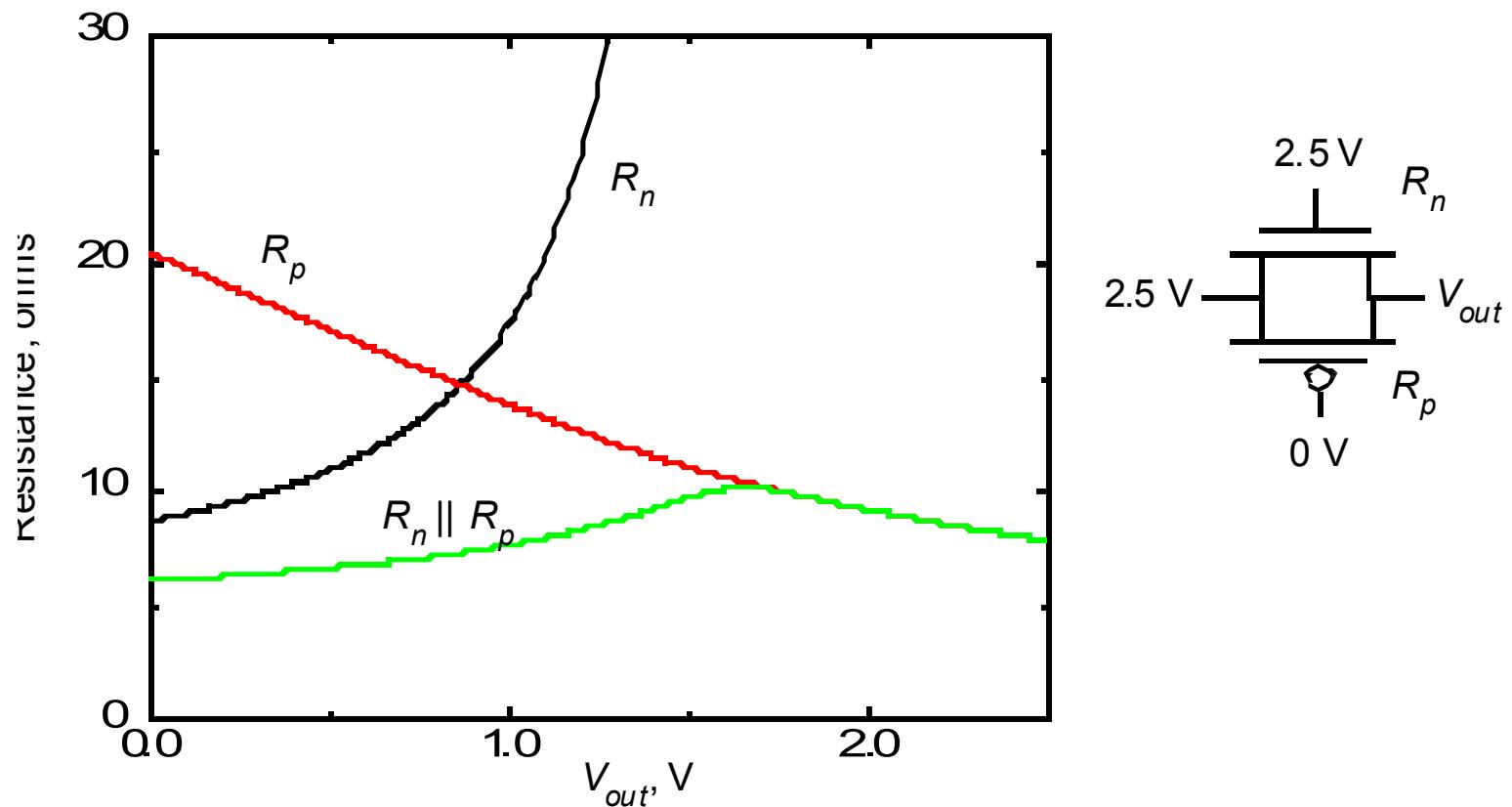
Solution 3: Transmission Gate



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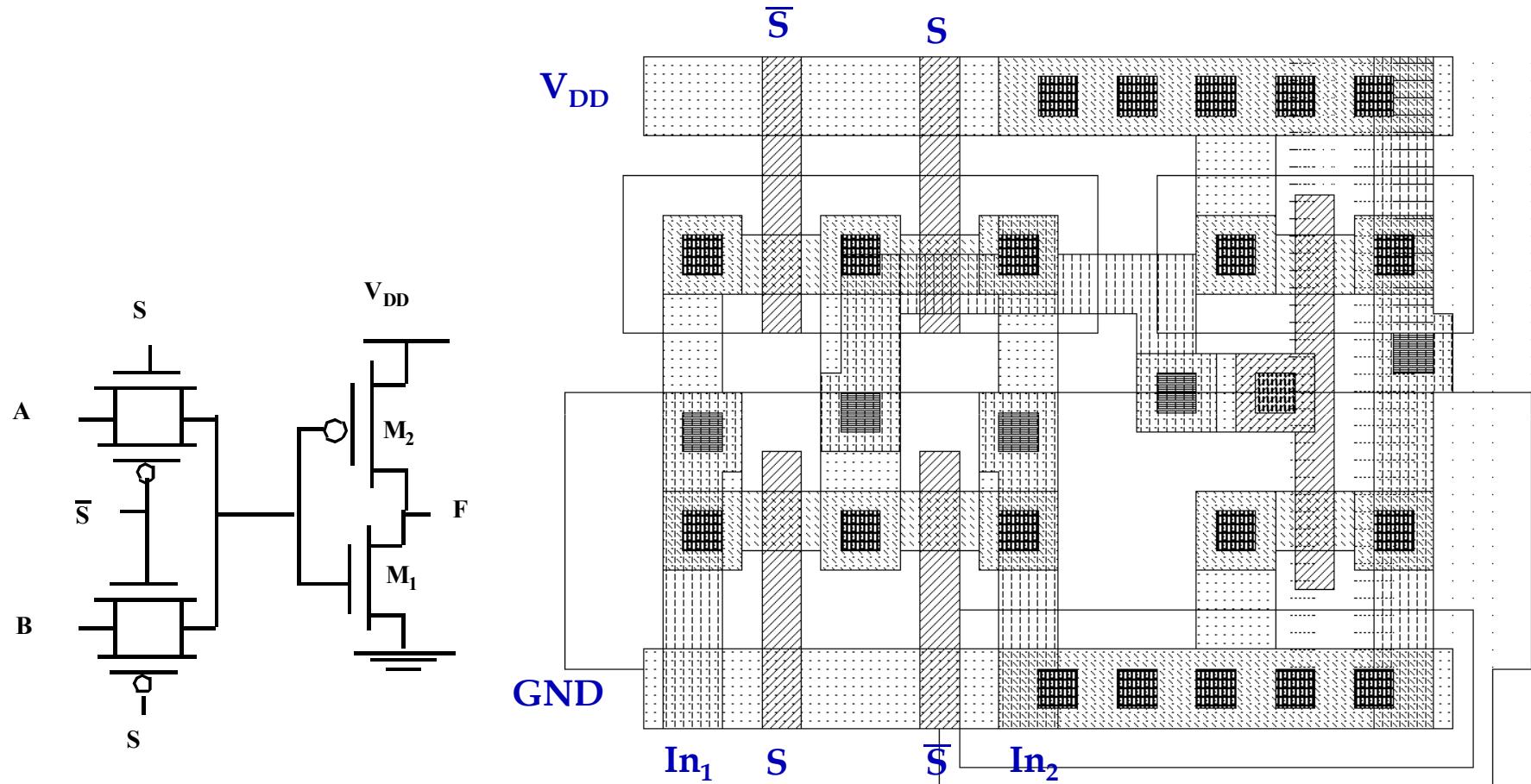
Resistance of Transmission Gate



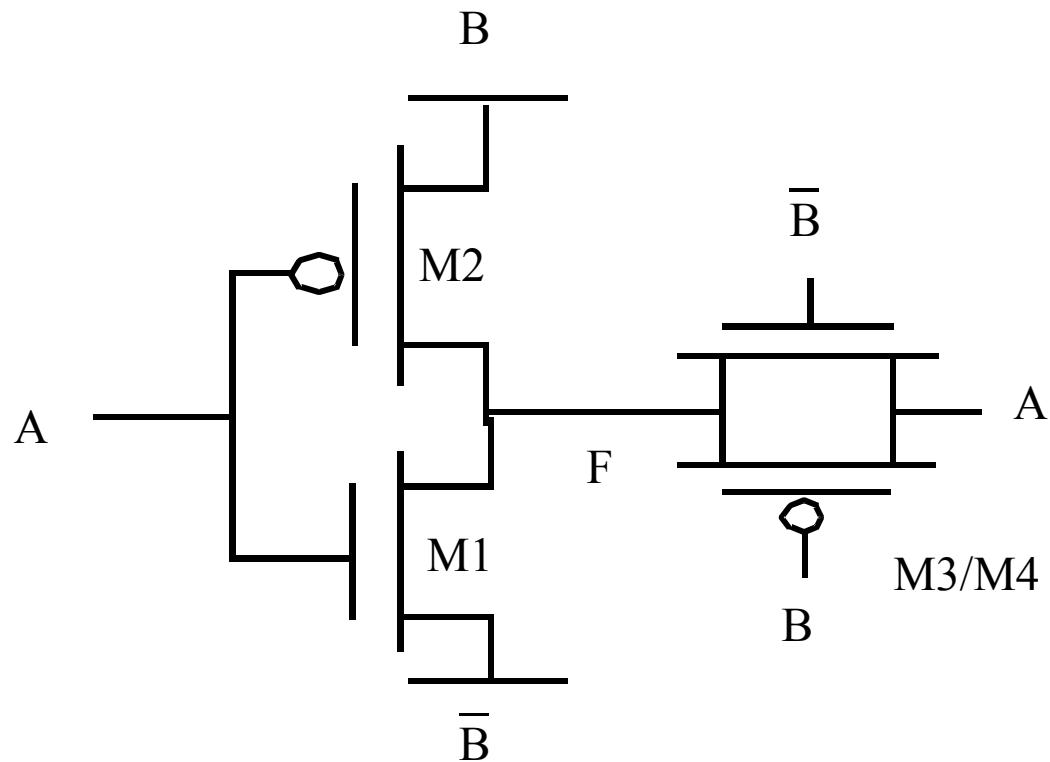
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Pass-Transistor Based Multiplexer



Transmission Gate XOR



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