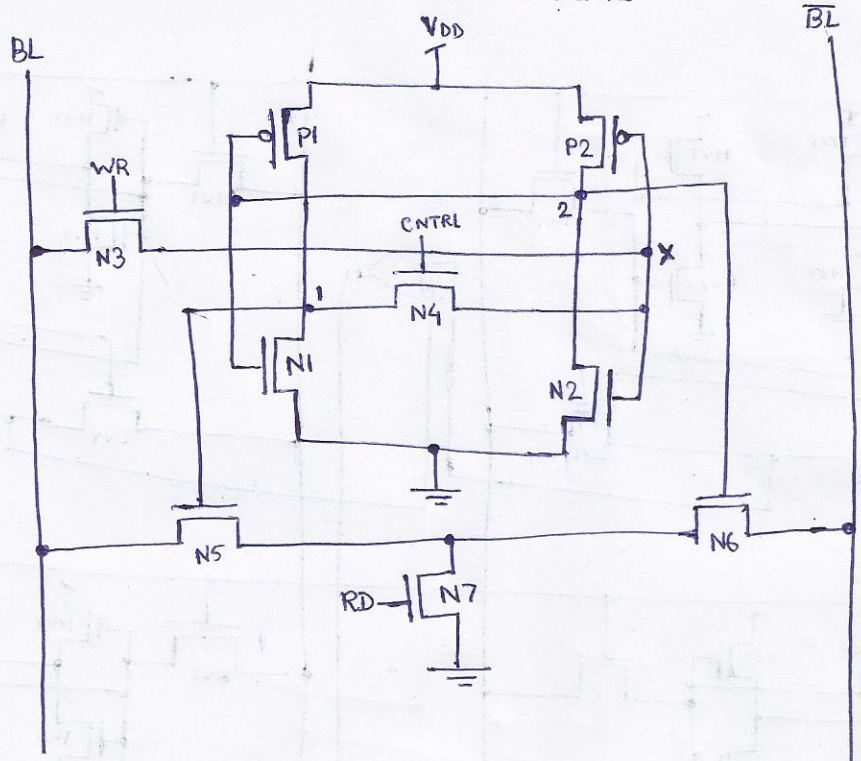
Temp 207

Hints and Solutions to
Mid Semester Examination 2 2012
VLSI Architectures

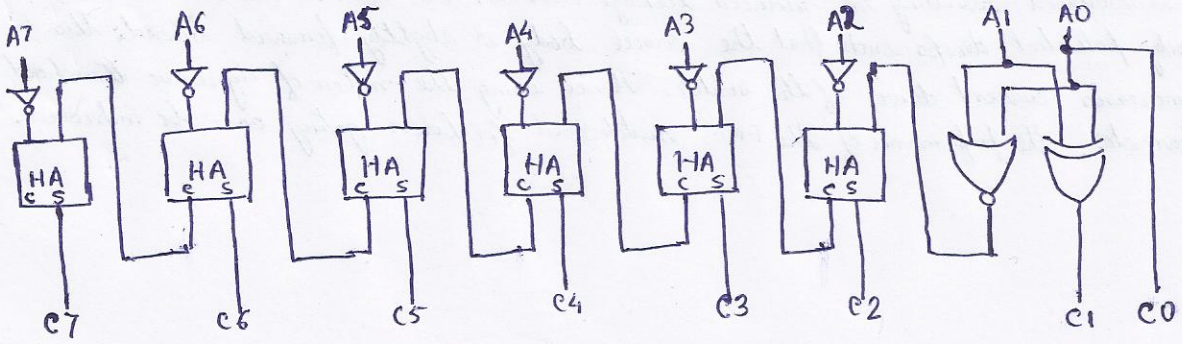
3.



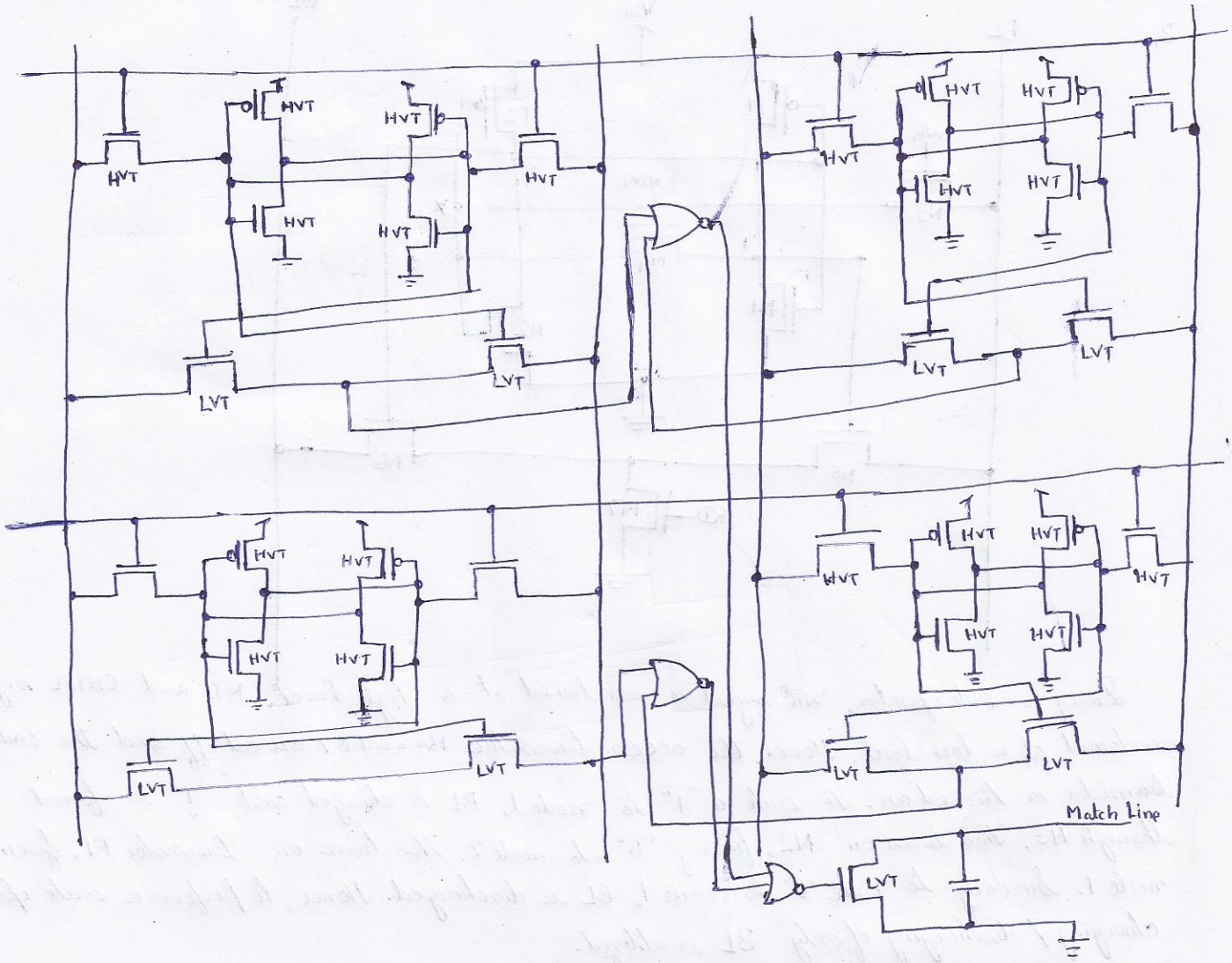
During a write operation, WR signal is maintained at a high level. RD and CNTRL signals are maintained at a low level. Hence the access transistors N4 and N7 are cut off and the write access transistor is turned on. To write a "1" to node 1, BL is charged and "1" is forced to node "X" through N3. This turns on N2, forcing "0" into node 2. This turns on transistor P1, forcing "1" into node 1. Similarly to write "0" to node 1, BL is discharged. Hence, to perform a write operation charging / discharging of only BL is utilized.

During a read operation, RD and CNTRL signals are maintained at a high level while WR is maintained at a low level. Hence N3 is cut off, while N4 and N7 are activated. To perform read operation, BL and $\overline{BL}$ are initially precharged to a high voltage. Suppose that node 1 stores "1", BL is discharged through N5 and N7. Alternatively, if node 2 stores "1", $\overline{BL}$ is discharged through N6 and N7. Since N3 is cut off, storage nodes 1 and 2 are completely isolated from the bit lines during read operation. This improves the static noise margin.

4.

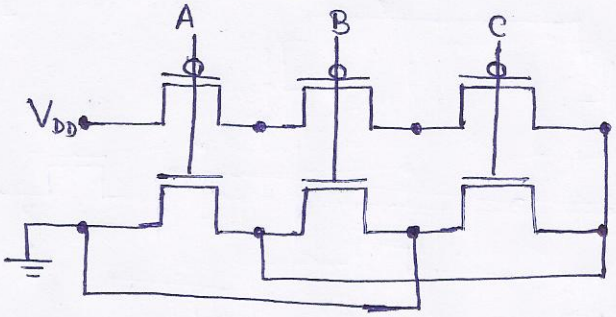


1.

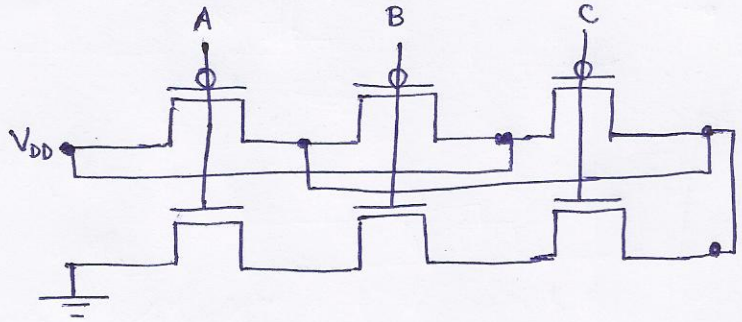


2. In figure 1(a), a conventional PMOS switch is used for power gating. The body of the transistor is either connected to V_{DD} or a higher potential to reverse bias the body source junction. In figure 1(b), the body of the PMOS transistor is connected to the source of a low V_T NMOS transistor. The drain terminal of the NMOS is connected to a reference voltage ($V_R > V_{DD} + V_{Tn}$). In this way, the body potential of the switch is dynamically changed with the sleep input. When the PMOS switch is put into OFF state by applying the sleep signal its body potential is raised through NMOS towards V_R, reverse biasing body source junction, and consequently V_{Tp} is increased resulting in reduced leakage current. On the other hand, when the switch is ON, the body potential drops such that the source body is slightly forward biased; this reduces V_{Tp} and increases current drive of the switch. Hence using the notion of dynamic threshold voltage for PMOS transistor, the performance of the PMOS switch used for power gating can be improved.

5. (i) 3 i/p CMOS NOR gate



(ii) 3 i/p CMOS NAND gate



6. The designer can obtain the carry output directly from the 8 bit parallel inputs using the look ahead approach and this does not require probing into the original circuit.