Overview of Fault Models

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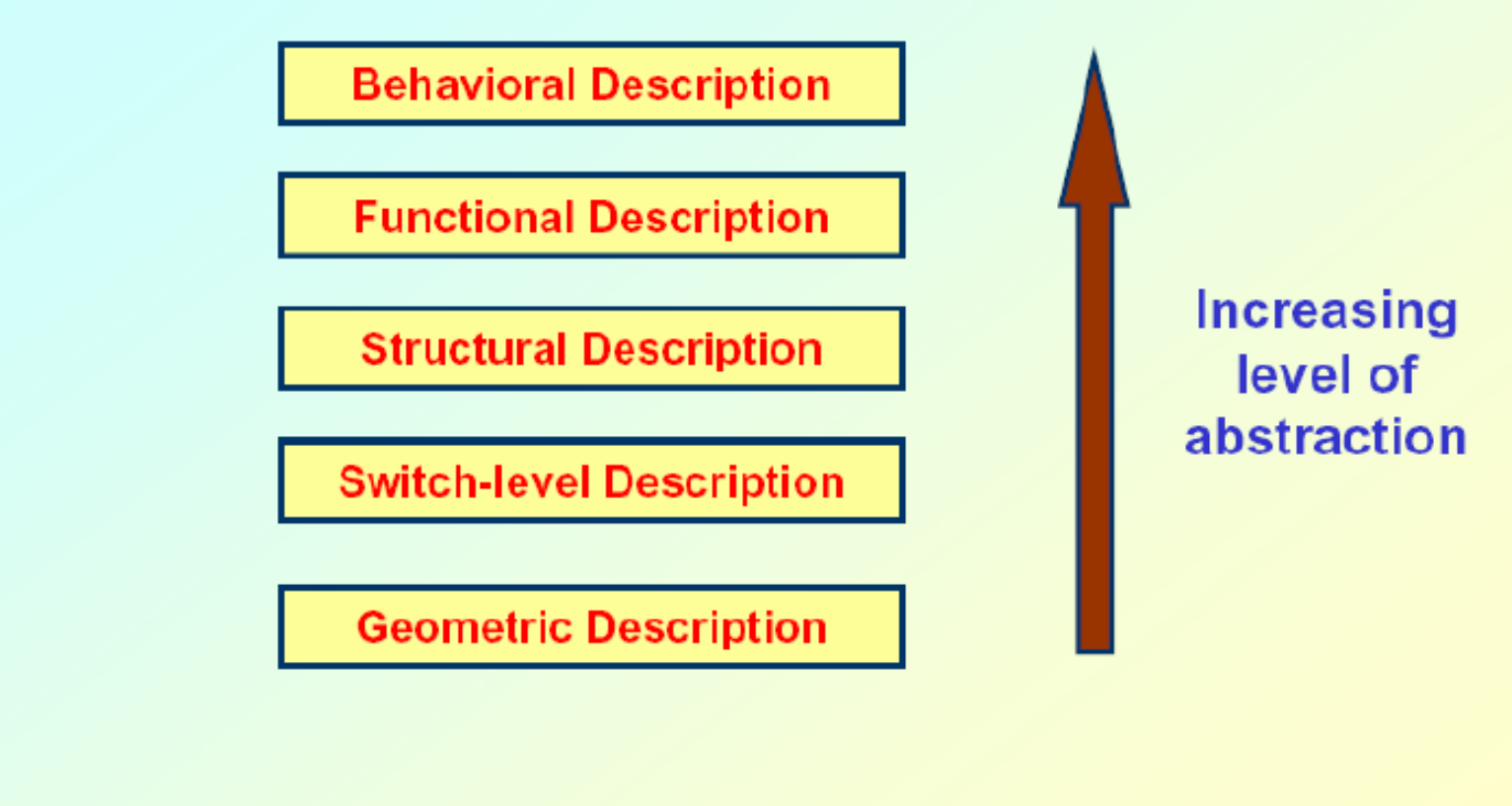
Why Fault Models?

- Too many actual number of physical defects in circuits.
  - Not possible to consider individually.
  - Difficult to analyze.
- Some logical fault models are considered.
  - A fault model identifies targets for testing.
  - Drastically reduces number of faults to be handled.
  - Makes analysis possible.
  - Effectiveness measurable by experiments.

Levels of abstraction in circuits



Observations

- Faults modeled at the lowest level of abstraction will be more accurate.
  - Will resemble closely with actual physical defects.
- Typically higher-level abstractions are used.
  - To reduce complexity.
  - An example:
    - 50 million transistors
    - 500 million possible defects
    - 5 million gates

Fault Models at Different Levels

- **Behavioral Fault Model**
  - Related to failure modes of the constructs in HDL.
  - Ex: assignment, condition failures etc.
- **Functional Fault Model**
  - Try to ensure that the given functional block executes the function it was designed for.
  - Ex: Adder, Multiplexer etc.
- **Structural Fault Model**
  - The circuit is given as a netlist of blocks.
  - Here we try to make sure that the interconnections in the given structure are fault-free, and are able to carry both '0'and '1'signals.
    - The blocks (e.g. gates) assumed to be fault-free.
    - Leads to the *stuck-at-fault* model.

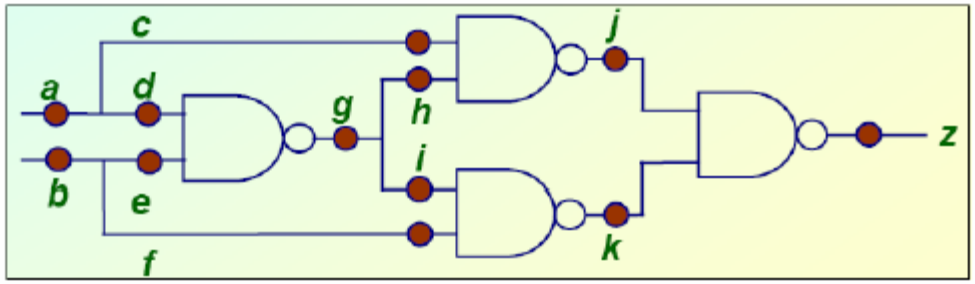
Stuck at fault model

- **Stuck-at-Fault Model:**
  - Some line(s) in the circuit are permanently stuck at logic 0 or logic 1
  - Denoted as s-a-0 & s-a-1, or as a/0 & a/1 for line 'a'.
  - A fan-out stem and fan-out branches are considered different lines.

- **Two Variants:**
  - **Single Stuck-at-Fault**
    - 'k' lines → '2k' number of faults
  - **Multiple Stuck-at-Fault**
    - 'k' lines → '3^k-1' number of faults

Stuck at fault

- **Why single stuck-at faults?**
  - Simpler to handle & reasonably good fault coverage.
  - A test set for detecting single stuck-at faults detects a large percentage of multiple stuck-at faults as well.
  - Technology independent. Can be applied to TTL, ECL, CMOS etc.
  - It is design style independent. Applicable to all design styles: Gate array, standard cell, full custom, etc.
- **Example:**



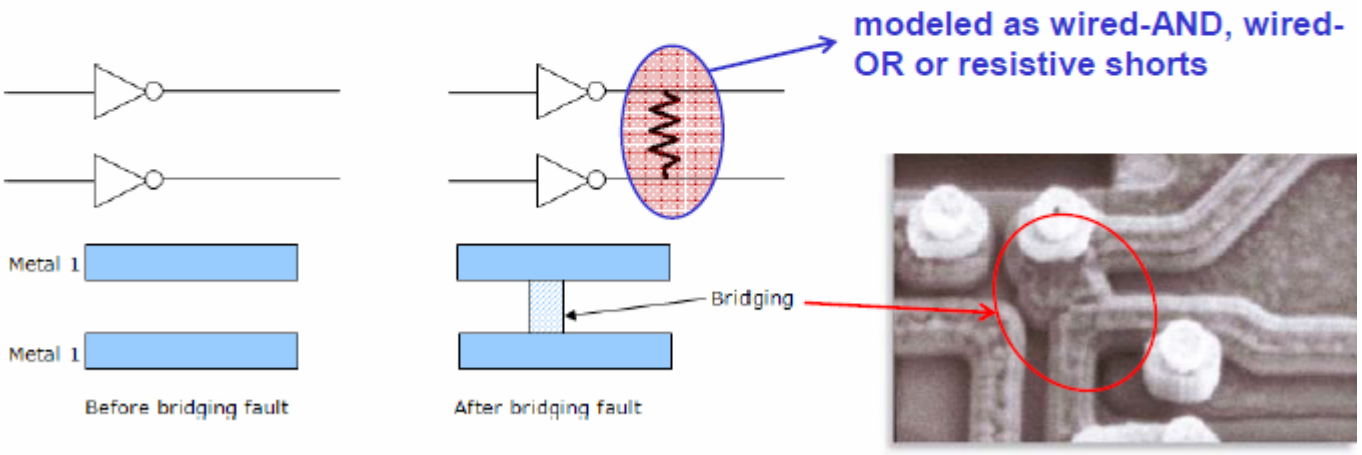
- 12 lines (a, b, c, d, e, f, g, h, I, j, k, z) of faults
- 2x12 = 24 single stuck-at-faults
- 3^{12}-1 = 5,31,441 multiple stuck-at-faults

Fault Models at different levels

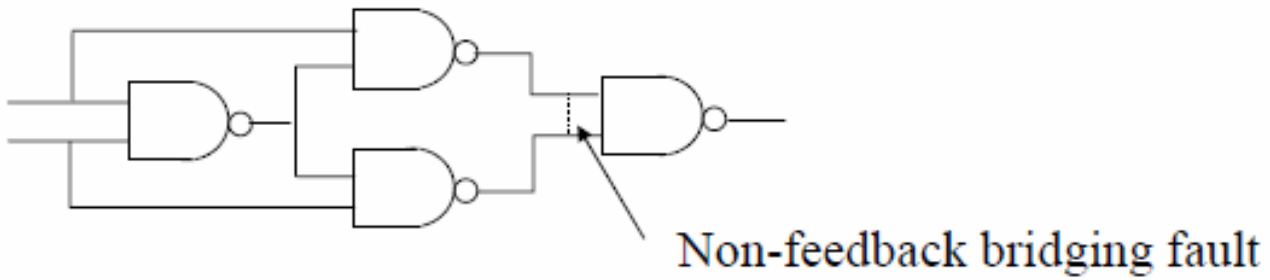
- **Switch-Level Fault Model**
  - Deals with faults in netlist of transistors in a switch-level description of a circuit.
    - MOS transistors considered as ideal switch.
  - Two kinds of faults:
    - *Stuck-open fault and Stuck-short fault*
- **Geometric Fault Model**
  - Derived directly from the layout of the circuit.
  - Some examples of geometric fault models:
    - Bridging fault model
    - PLA fault model
    - Memory fault model

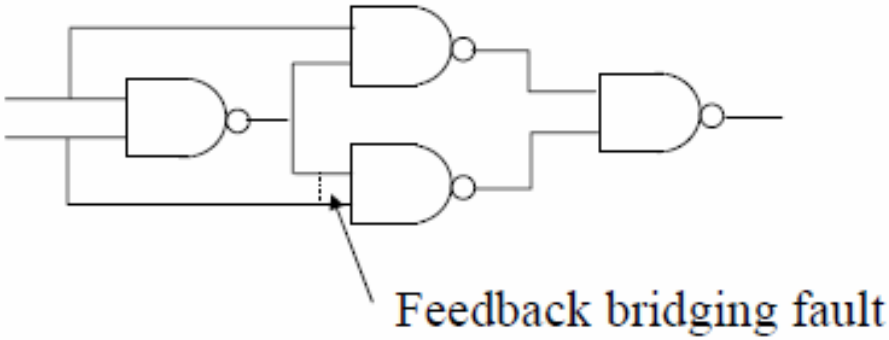
Bridging Fault Models

- Tests for resistive shorts between two normally unconnected nets
- Closest fault-model to real defects
- Bridging-faults are caused by manufacturing defects



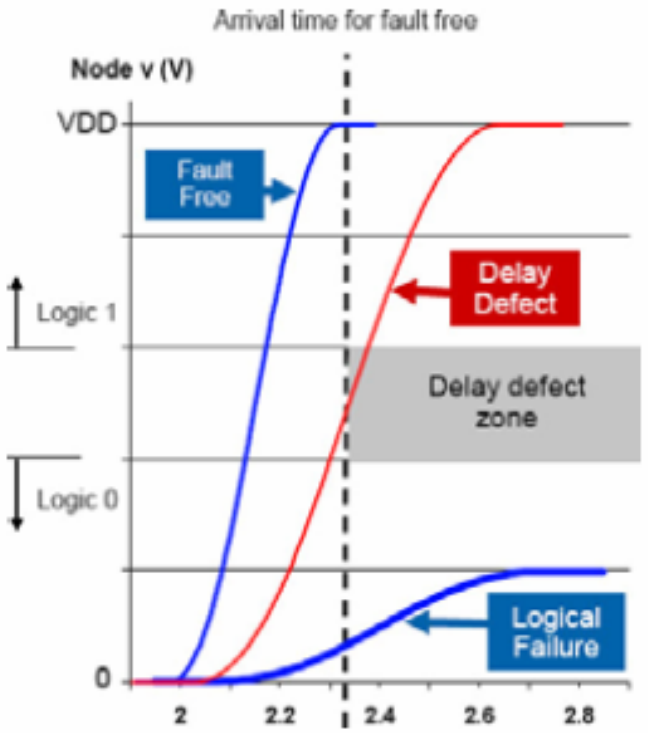
Feedback versus Non-feedback Bridging Fault





Delay Faults

- Affect propagation delay of the circuit, circuit fails at high speeds
- More important for high-speed circuits
- Gate delay fault (GDF): slow 1-to-0 or 0-to-1 transition at a gate output
- Path delay fault (PDF): exists a path from a primary input to primary output that is slow to propagate a 0-to-1 or 1-to-0 transition



Questions?