Fault Simulation

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Fault Simulation

- Introduction
- Serial Fault Simulation
- Parallel Fault Simulation
- Deductive Fault Simulation
- Fault Detection
- Alternative to Fault Simulation
- Conclusion

Introduction

- What is fault simulation?
  - Given
    - A circuit
    - A set of test patterns
    - A fault model
  - Determine
    - Faulty outputs
    - Undetected faults
    - Fault coverage

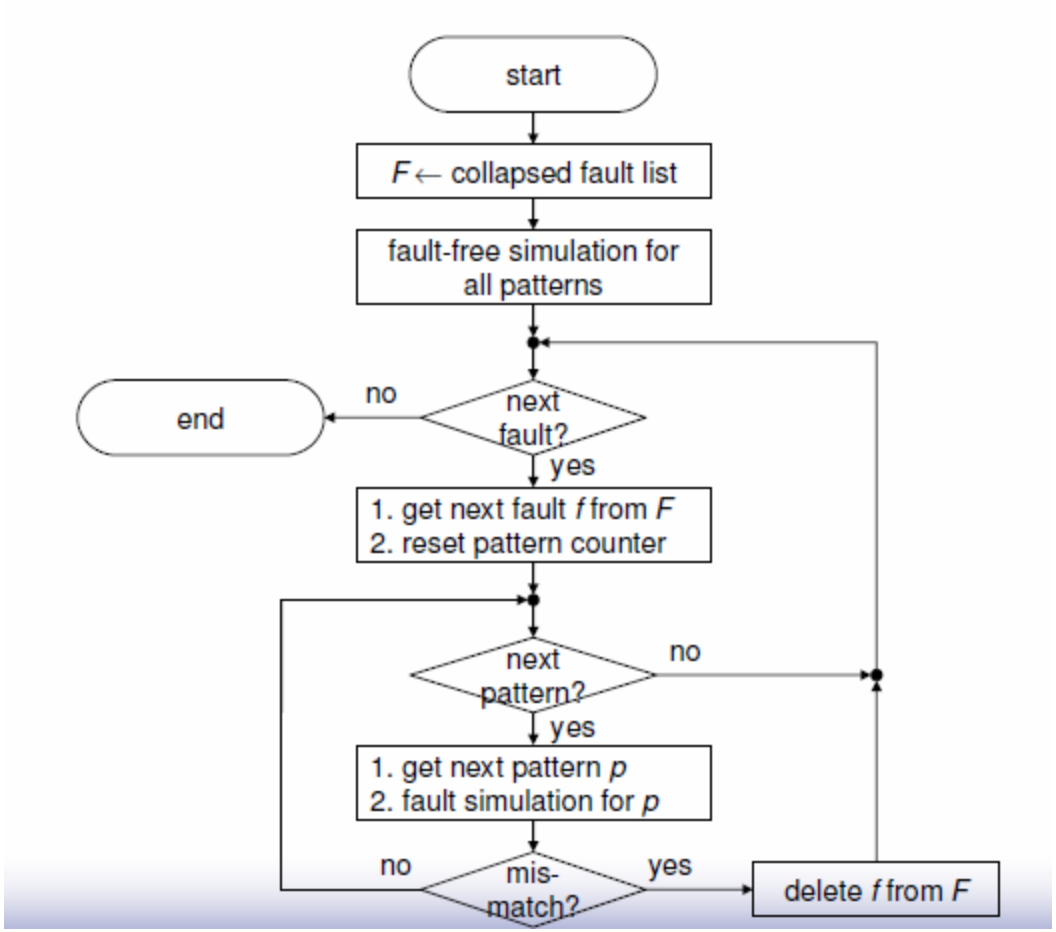
Time Complexity

- Proportional to
  - n: Circuit size, number of logic gates
  - p: Number of test patterns
  - f : Number of modeled faults
- Since f is roughly proportional to n, the overall time complexity is $O(pn^2)$

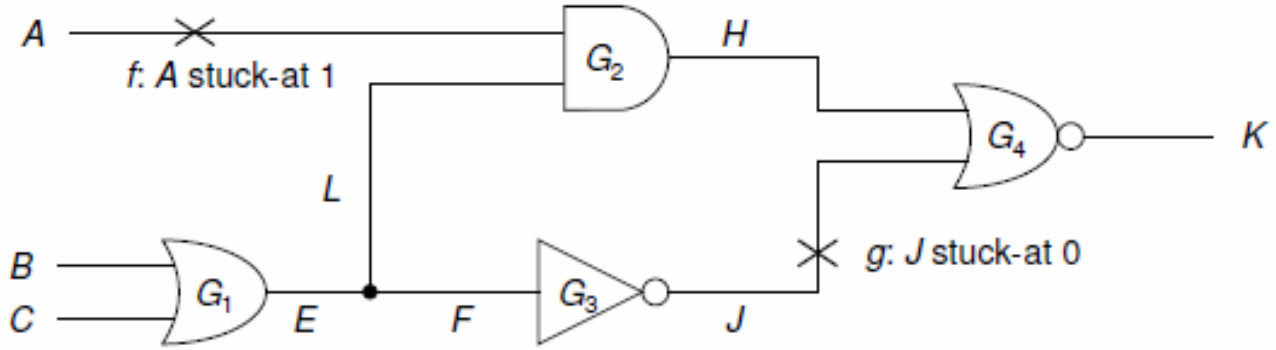
Serial Fault Simulation

- First, perform fault-free logic simulation on the original circuit
  - Good (fault-free) response
- For each fault, perform fault injection and logic simulation
  - *Faulty* circuit response

Algorithm for Serial Fault Simulation



Example of Serial Fault Simulation



Pat. #	Input			Internal					Output		
	A	B	C	E	F	L	J	H	K_{good}	K_f	K_g
P1	0	1	0	1	1	1	0	0	1	0	1
P2	0	0	1	1	1	1	0	0	1	0	1
P3	1	0	0	0	0	0	1	0	0	0	1

Fault Dropping

- Halting simulation of the detected fault
- Example
  - Suppose we are to simulate P_1, P_2, P_3 in order
  - Fault f is detected by P_1
  - Do not simulate f for P_2, P_3
- For fault grading
  - Most faults are detected after relatively few test patterns have been applied
- For fault diagnosis
  - Avoided to obtain the entire fault simulation results

Advantages and Disadvantages of Serial Fault Simulation

- Advantages
  - Easy to implement
  - Ability to handle a wide range of fault models (stuck-at, delay, Br, …)
- Disadvantages
  - Very slow

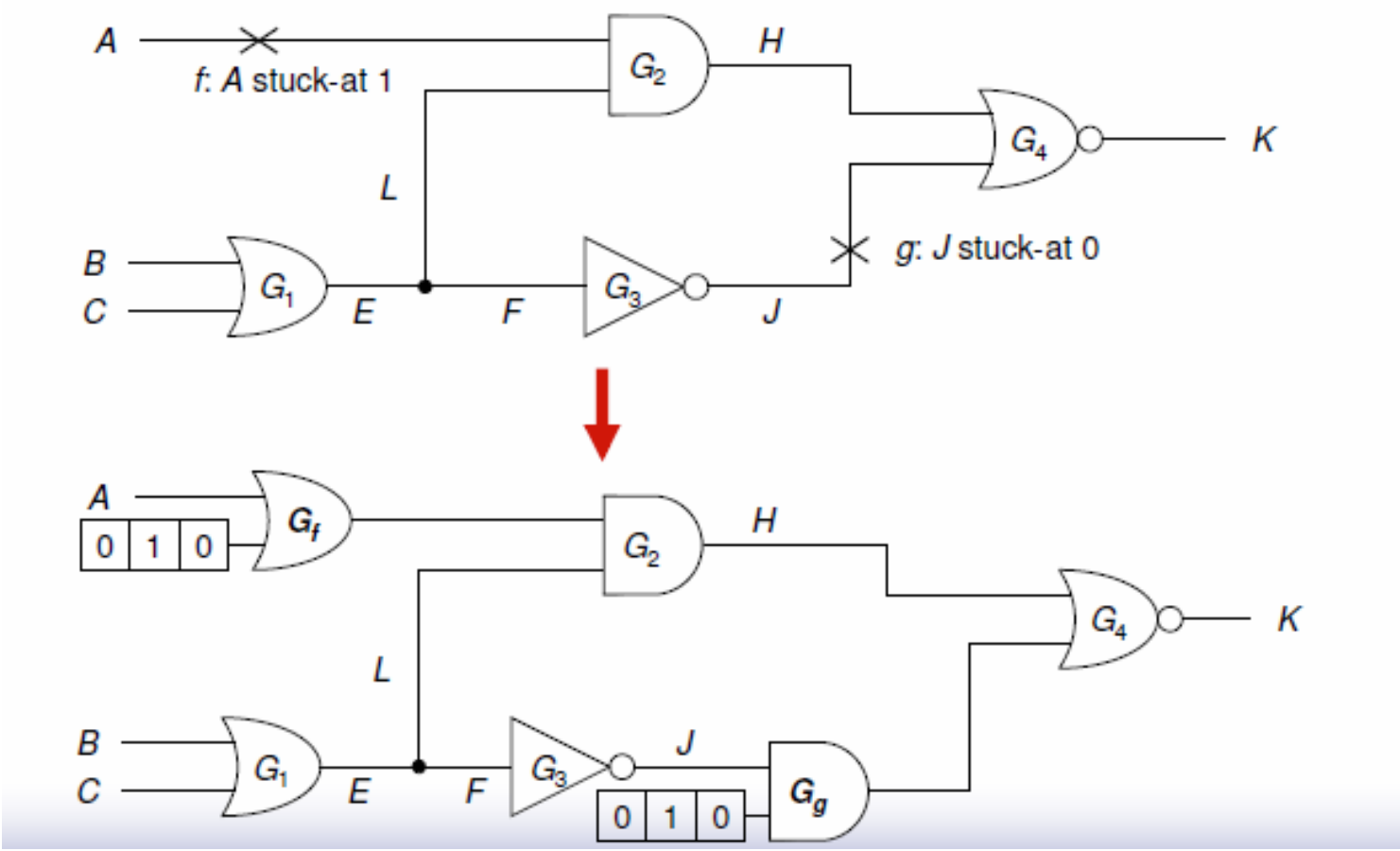
Parallel Fault Simulation

- Exploit the inherent parallelism of bitwise operations
- Parallel fault simulation [Seshu 1965]
  - Parallel in faults
- Parallel pattern fault simulation [Waicukauski 1986]
  - Parallel in patterns

Parallel Fault Simulation

- Assumption
  - Use binary logic: one bit is enough to store logic signal
  - Use *w*-bit wide data word
- Parallel simulation
  - *w*-1 bit for faulty circuits
  - 1 bit for fault-free circuit
- Process faulty and fault-free circuit in parallel using bitwise logic operations

Fault Injection



Example

Pat #		Input				Internal						Output
		A	A_f	B	C	E	F	L	J	J_g	H	K
P_1	FF	0	0	1	0	1	1	1	0	0	0	1
	f	0	1	1	0	1	1	1	0	0	1	0
	g	0	0	1	0	1	1	1	0	0	0	1
P_2	FF	0	0	0	1	1	1	1	0	0	0	1
	f	0	1	0	1	1	1	1	0	0	1	0
	g	0	0	0	1	1	1	1	0	0	0	1
P_3	FF	1	1	0	0	0	0	0	1	1	0	0
	f	1	1	0	0	0	0	0	1	1	0	0
	g	1	1	0	0	0	0	0	1	0	0	1

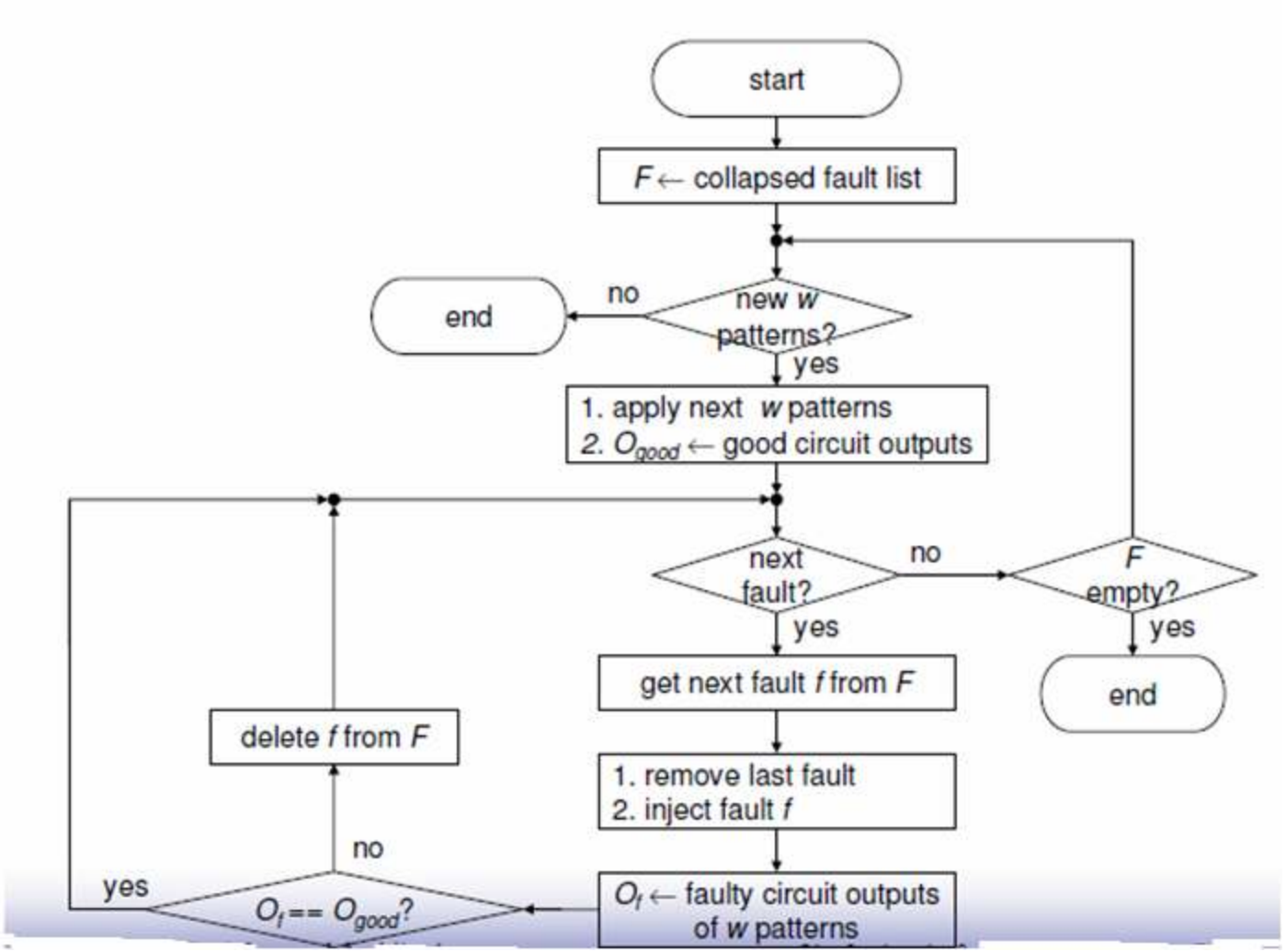
Advantages and Disadvantages of Parallel Fault Simulation

- Advantages
  - A large number of faults are detected by each pattern when simulating the beginning of test sequence
- Disadvantages
  - Only applicable to the unit or zero delay models
  - Faults cannot be dropped unless all (w-1) faults are detected

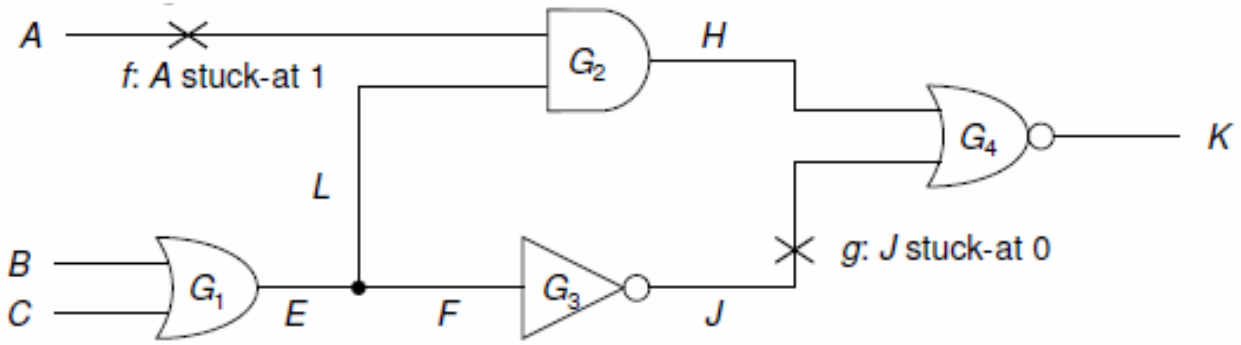
Parallel Pattern Fault Simulation

- Parallel pattern single fault propagation (PPSFP)
- Parallel pattern
  - With a *w*-bit data width, *w* test patterns are packed into a word and simulated for the fault-free or faulty circuit
- Single fault
  - First, fault-free simulation
  - Next, for each fault, fault injection and faulty circuit simulation

Algorithm for parallel pattern fault simulation



Example



		Input			Internal					Output
		A	B	C	E	F	L	J	H	K
Fault Free	P_1	0	1	0	1	1	1	0	0	1
	P_2	0	0	1	1	1	1	0	0	1
	P_3	1	0	0	0	0	0	1	0	0
f	P_1	1	1	0	1	1	1	0	1	0
	P_2	1	0	1	1	1	1	0	1	0
	P_3	1	0	0	0	0	0	1	0	0
g	P_1	0	1	0	1	1	1	0	0	1
	P_2	0	0	1	1	1	1	0	0	1
	P_3	1	0	0	0	0	0	0	0	1

Advantages and Disadvantages of Parallel Pattern Fault Simulation

- Advantages
  - Fault is dropped as soon as detected
  - Best for simulating test patterns that come later, where fault dropping rate per pattern is lower
- Disadvantages
  - Not suitable for sequential circuits

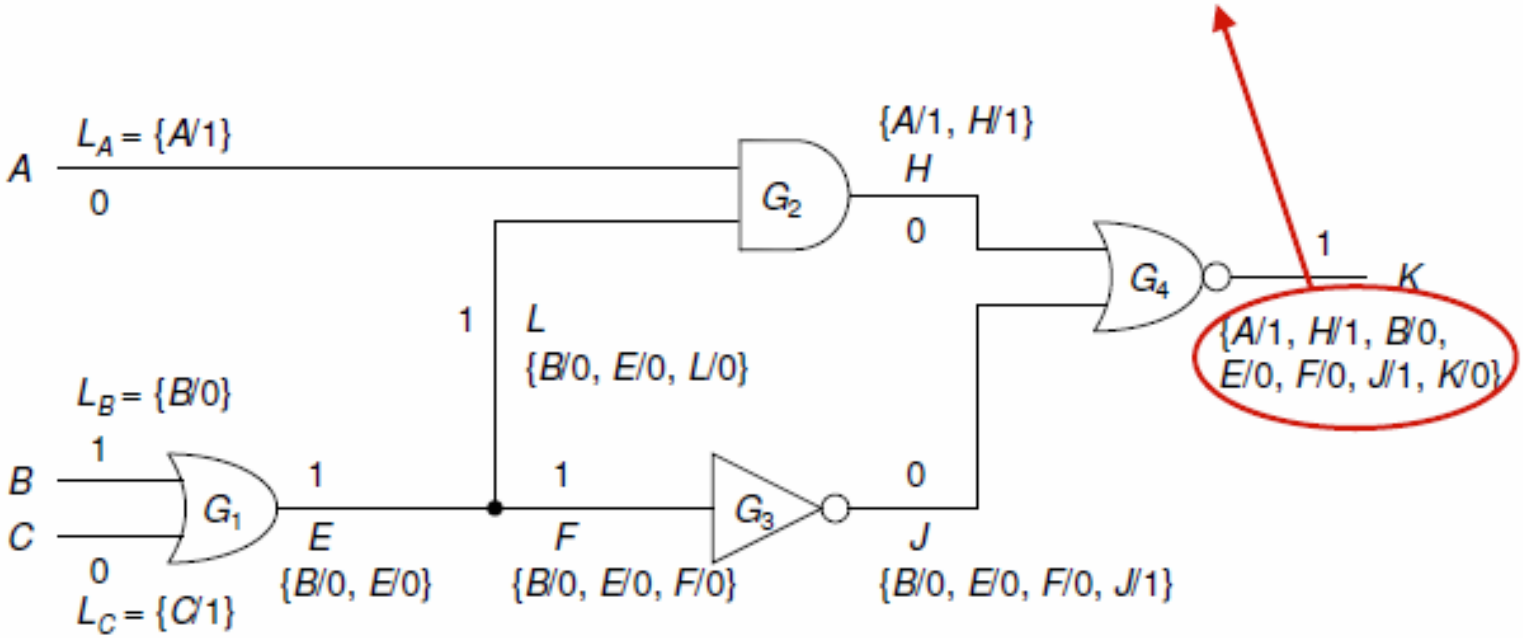
Deductive Fault Simulation

- [Armstrong 1972]
- Based on logic reasoning rather than simulation
- Fault list attached with signal x denoted as L_x
  - Set of faults causing x to differ from its fault-free value
- Fault list propagation
  - Derive the fault list of a gate output from those of the gate inputs based on logic reasoning

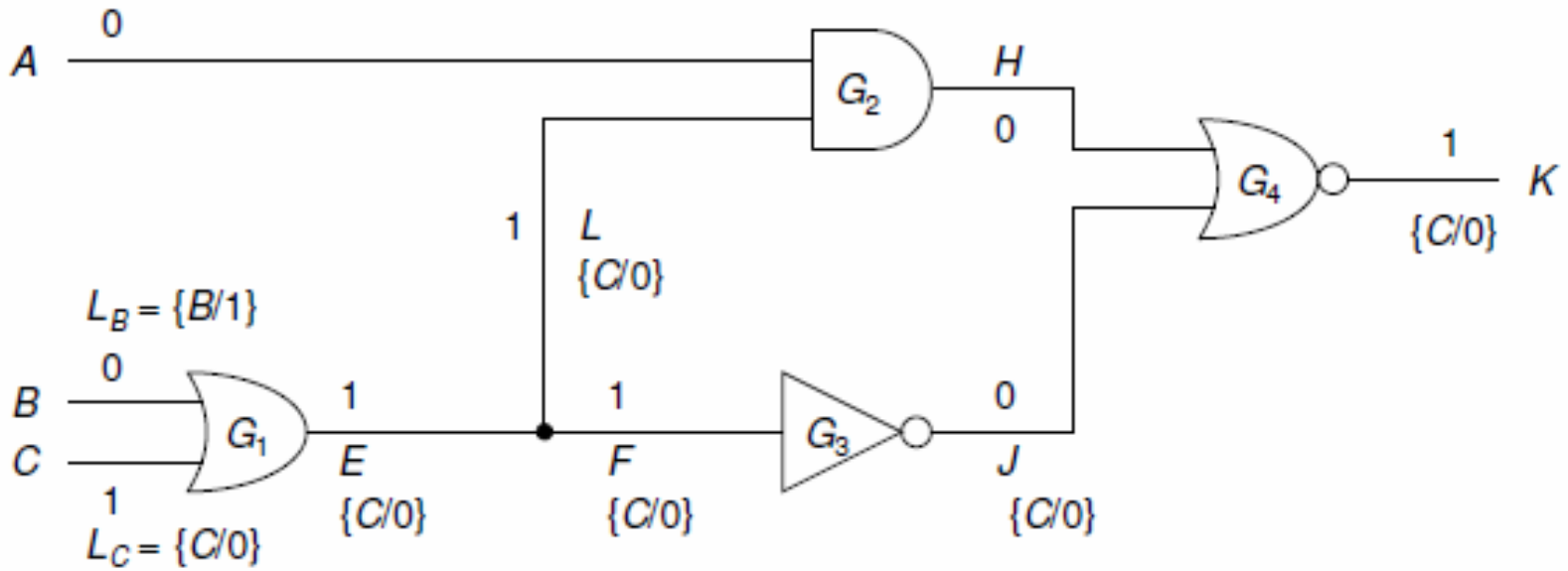
Example

- P_1

$$L_K = L_H \cup L_J \cup \{K/0\}$$ by Eq. (3.1)



Example



Advantages and Disadvantages of Deductive Fault Simulation

- Advantages
  - Very efficient
  - Simulate all faults in one pass
- Disadvantages
  - Not easy to handle unknowns
  - Only for zero-delay timing model
  - Potential memory management problem

Fault Detection

- Hard detected fault
  - Outputs of fault-free and faulty circuit are different
    - 1/0 or 0/1
    - No unknowns, no *Z*
- Potentially detected fault
  - Whether the fault is detected is unclear
  - Example: stuck-at-0 on enable signal of tri-state buffer

Fault Detection (Cont'd)

- Oscillation faults
  - Cause circuit to oscillate
  - Impossible to predict faulty circuit outputs
- Hyperactive faults
  - Catastrophic fault effect
    - Fault simulation is time and memory consuming
  - Example: stuck-at fault on clock
  - Usually counted as detected
    - Save fault simulation time

Alternatives to fault simulation

- Toggle Coverage
- Fault Sampling
- Critical Path Tracing
- Statistical Fault Analysis

Toggle Coverage

- Popular for estimating fault grading
- Only one single fault-free simulation
- A net is toggled if
  - Relaxed def: its value has been set to zero and one during fault-free simulation
  - Stringent def: it has both a zero-to-one transition and a one-to-zero transition during fault-free simulation
- Toggle coverage

$$\frac{\text{number of toggled nets}}{\text{number of total nets in the circuit}}$$

Fault Sampling

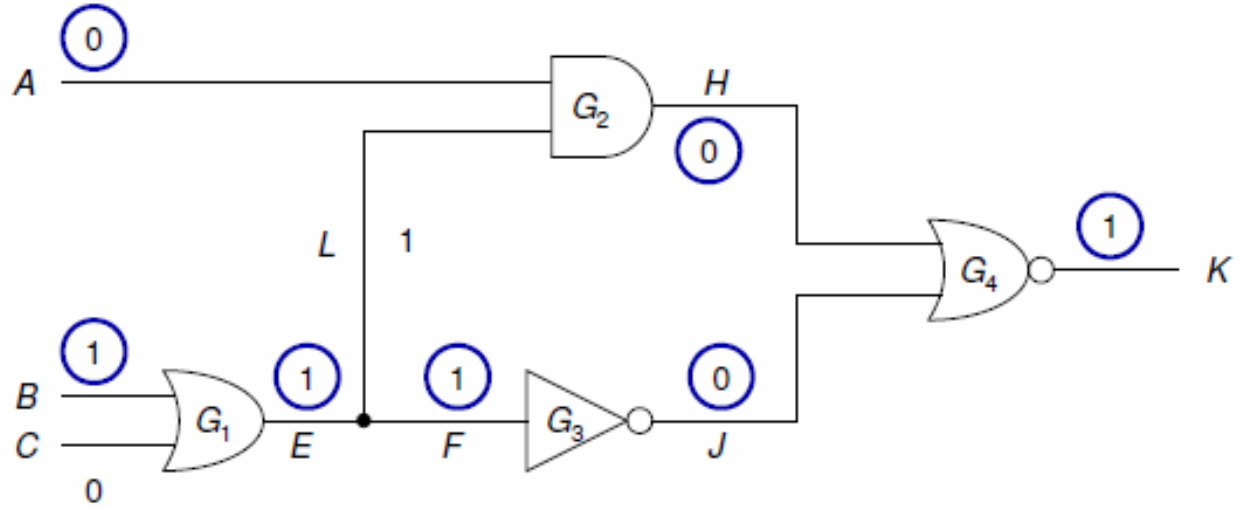
- [Butler 1974]
- Simulate only a sampled group of faults
- Error depends on two factors
  - Sample size
  - The sample is biased or not

Critical Path Tracing

- [Abramovici 1984]
- Critical value
  - For net *x*, stuck-at *v*' can be detected by test pattern *t* ↔ Net *x* has critical value *v*
- Critical path
  - Path consisting of nets with critical value
- Special attention required for fanout reconvergence

Example

- P_1



Statistical Fault Analysis

- [Jain 1985]
- Use probability theory to estimate expected value of fault coverage
- Detectability of fault f (d_f)
  - 1-controllability, $C1(x)$
  - 0-controllability, $C0(x)$
  - Observability, $O(x)$
  - Sensitization probability, $S(x)$

Summary

- Fault simulation is very important for
  - ATPG
  - Diagnosis
  - Fault grading
- Popular techniques
  - Serial, Parallel, Deductive
- Requirements for fault simulation
  - Fast speed, efficient memory usage, modeling functional blocks, sequential circuits

Thank You