Test Compression

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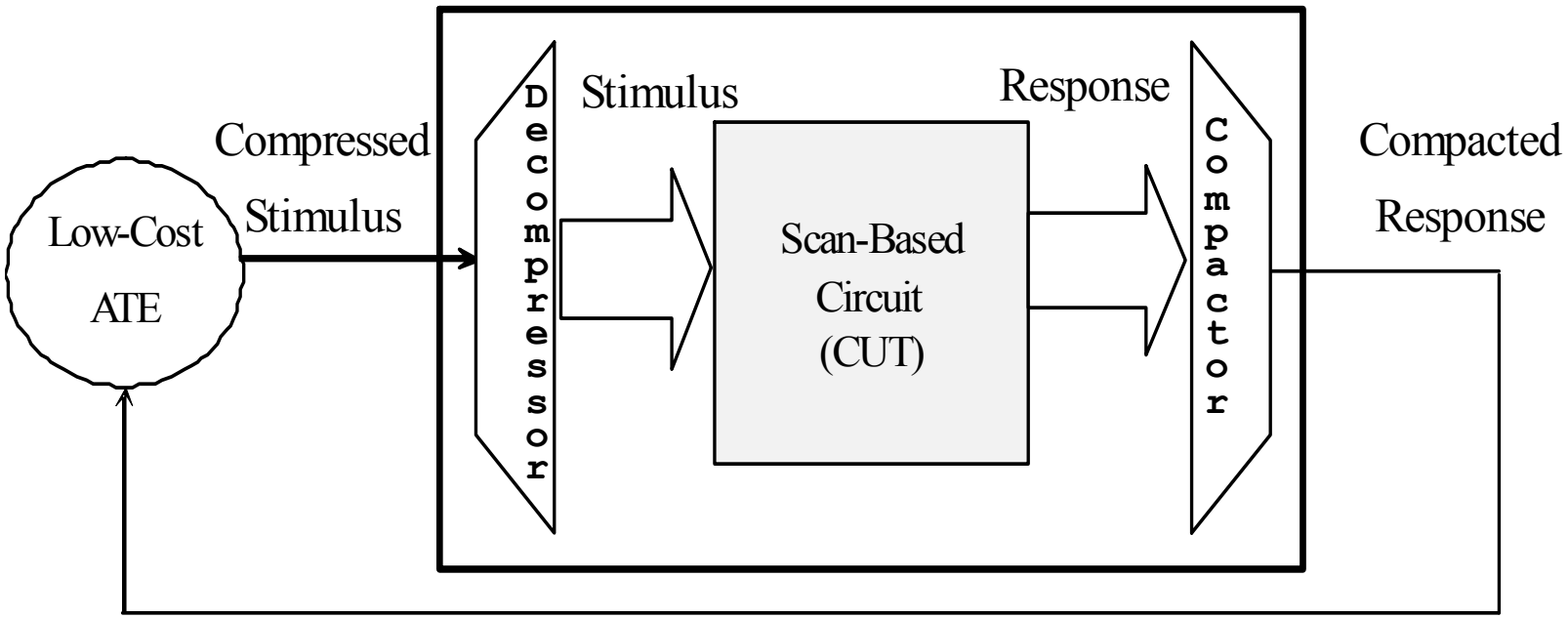
Test Compression

- Decompressor
  - Add some additional on-chip hardware before the scan chains to decompress the test stimulus
  - Use lossless compression
- Compactor
  - Add some additional on-chip hardware after scan chains to compact the response
  - The compaction is lossy
- Advantages:
  - Reduce ATE memory
  - Reduce test data volume and test application time

Test Compression Architecture



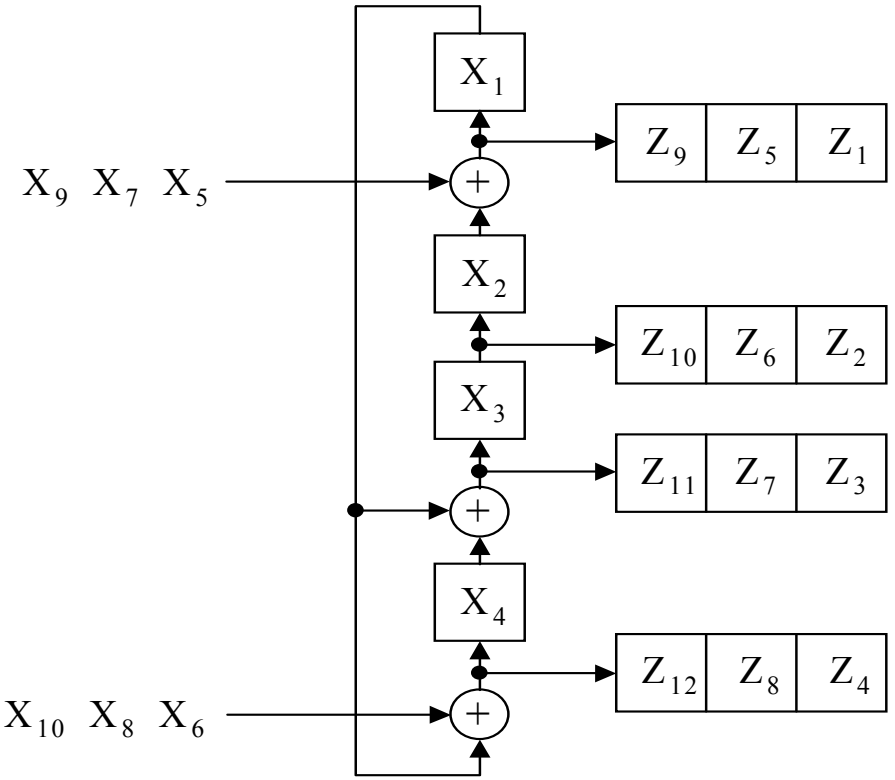
Circuits for Test Stimulus Compression

- Linear-Decompression-Based Schemes
  - Combinational linear decompressors
  - Sequential linear decompressors
- Broadcast-Scan-Based Schemes
  - Broadcast scan
  - Illinois scan
  - Multiple-input broadcast scan
  - Reconfigurable broadcast scan
  - Virtual scan
- Comparison

Linear-Decompression-Based Schemes

- Linear Decompressor Concept
  - Consists of only XOR gates and Flip-Flops
  - Its output space is a linear subspace that is spanned by a Boolean matrix.
- Combinational Linear Decompressor
  - Consists of only XOR gates
- Sequential Linear Decompressor
  - Consists of XOR gates and Flip-Flops
  - Flip-flops provides additional free variables for state encoding.

Example of symbolic simulation for linear decompressor



Z9 = X1 ⊕ X4 ⊕ X9	Z5 = X3 ⊕ X7	Z1 = X2 ⊕ X5
Z10 = X1 ⊕ X2 ⊕ X5 ⊕ X6	Z6 = X1 ⊕ X4	Z2 = X3
Z11 = X2 ⊕ X3 ⊕ X5 ⊕ X7 ⊕ X8	Z7 = X1 ⊕ X2 ⊕ X5 ⊕ X6	Z3 = X1 ⊕ X4
Z12 = X3 ⊕ X7 ⊕ X10	Z8 = X2 ⊕ X5 ⊕ X8	Z4 = X1 ⊕ X6

$$\begin{pmatrix} 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \\ X_7 \\ X_8 \\ X_9 \\ X_{10} \end{pmatrix} = \begin{pmatrix} Z_1 \\ Z_2 \\ Z_3 \\ Z_4 \\ Z_5 \\ Z_6 \\ Z_7 \\ Z_8 \\ Z_9 \\ Z_{10} \\ Z_{11} \\ Z_{12} \end{pmatrix}$$

System of linear equations for the decompressor

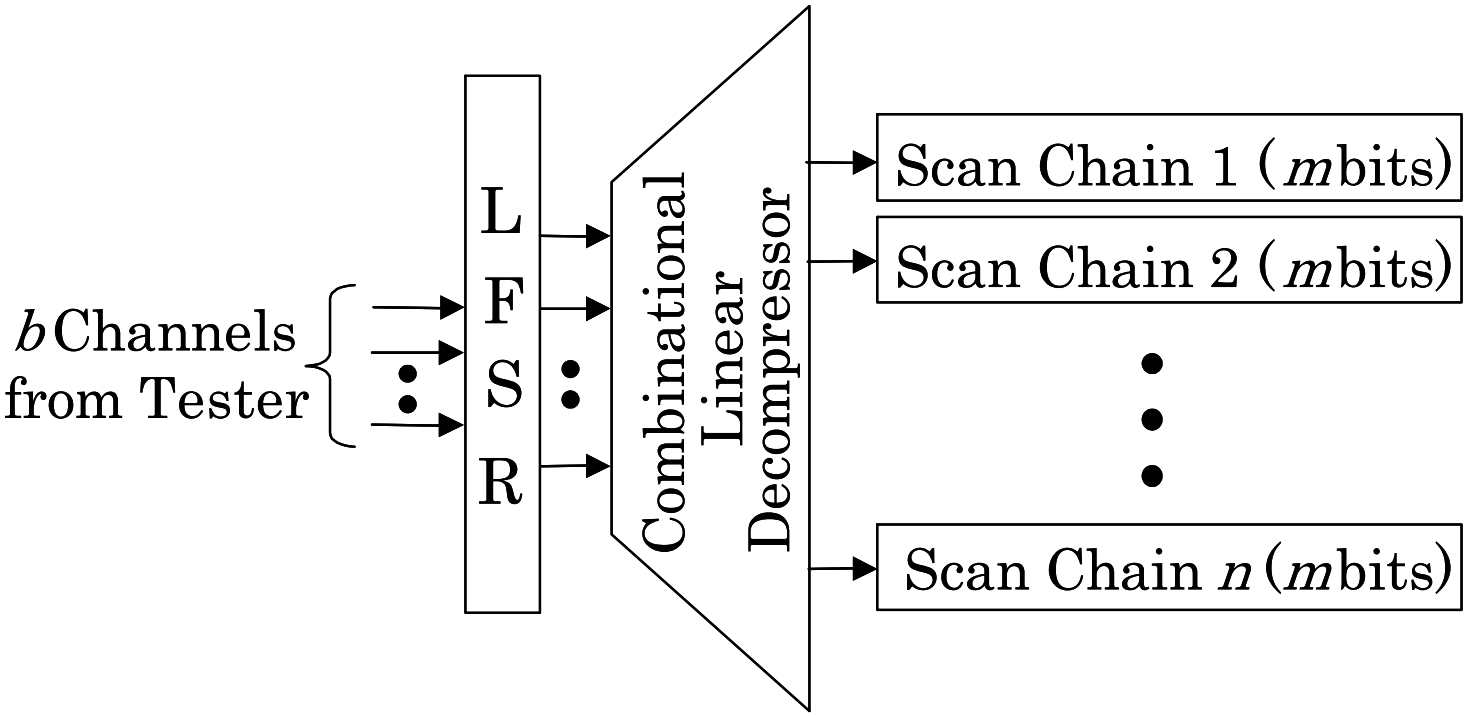
Combinational Linear Decompressor

- Advantage:
  - Simpler hardware and control because only XOR gates are used
- Disadvantages:
  - Low Encoding Efficiency
    - Because no free variables are used
    - Can be improved by dynamically adjusting the number of scan chains that are loaded in each clock cycle.

Sequential Linear Decompressor

- Based on linear finite-state machines
  - Examples: LFSRs, cellular automata, ring generators
- Advantages:
  - Allow free variables from earlier clock cycles
  - Much greater flexibility than combinational linear decompressor
- Two classes
  - Static reseeding
    - Drawbacks
      - The tester is idle while the LFSR is running in autonomous mode.
      - The LFSR must be at least as large as the number of specified bits in the test cube.
  - Dynamic reseeding

Typical Sequential Linear Decompressor

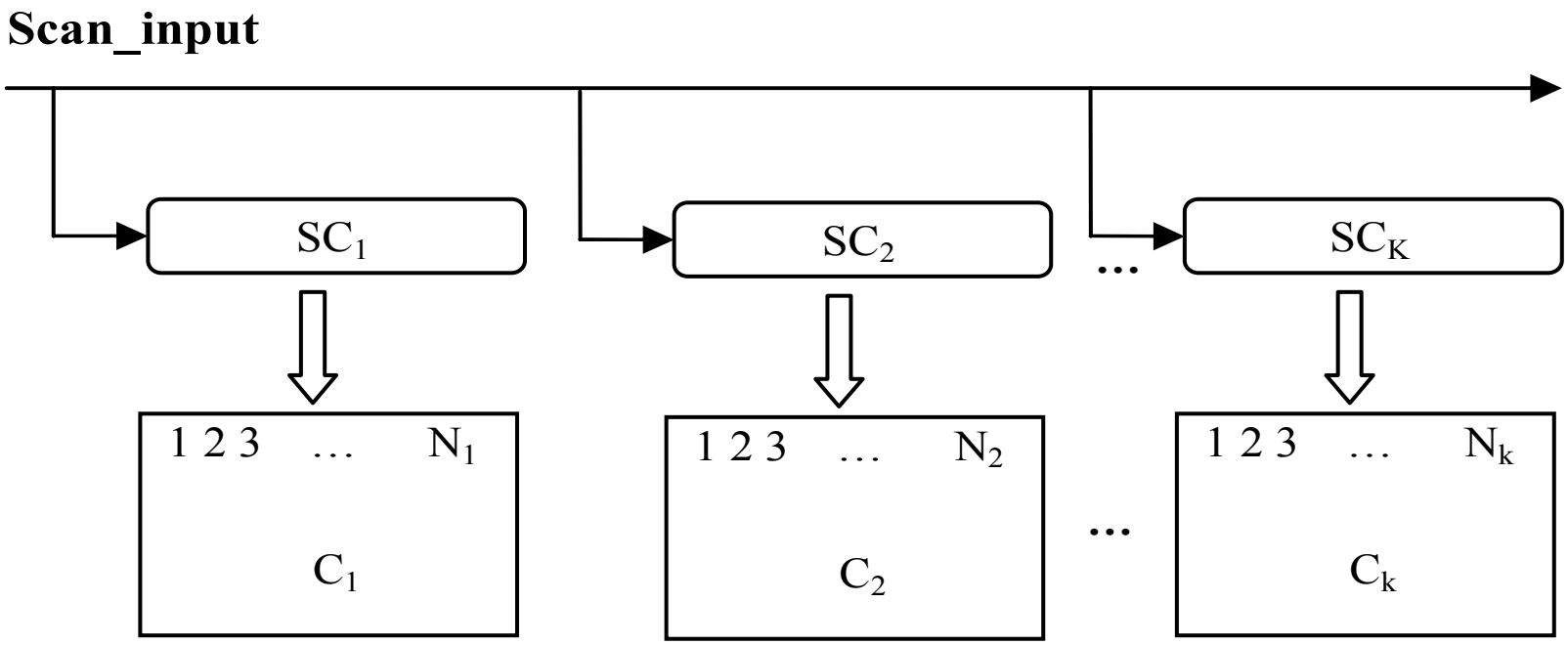


Dynamic reseeding calls for the injection of free variables coming from the tester into the LFSR as it loads the scan chains

Broadcast-Scan-Based Schemes

- Broadcast scan
- Illinois Scan
- Multiple input broadcast scan
- Reconfigurable broadcast scan
- Virtual scan

Broadcast Scan

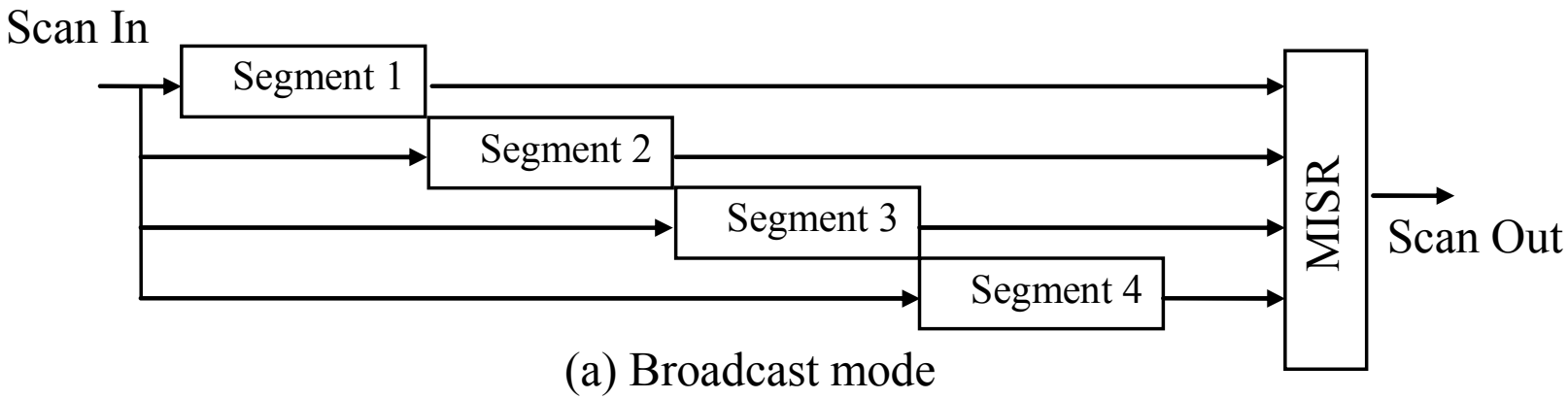


- Broadcasting to scan chains driving independent circuit
- Won't affect fault coverage if all circuits are independent

Illinois Scan

- Consists of two modes of operations
  - Broadcast mode
  - Serial scan mode
- Main Drawback
  - No test compression in serial scan mode
- Ways to reduce number of patterns
  - Multiple-Input broadcast scan
  - Reconfigurable broadcast scan

Illinois Scan Architecture



(a) Broadcast mode

(b) Serial chain mode

Two Mode of Illinois Scan Architecture

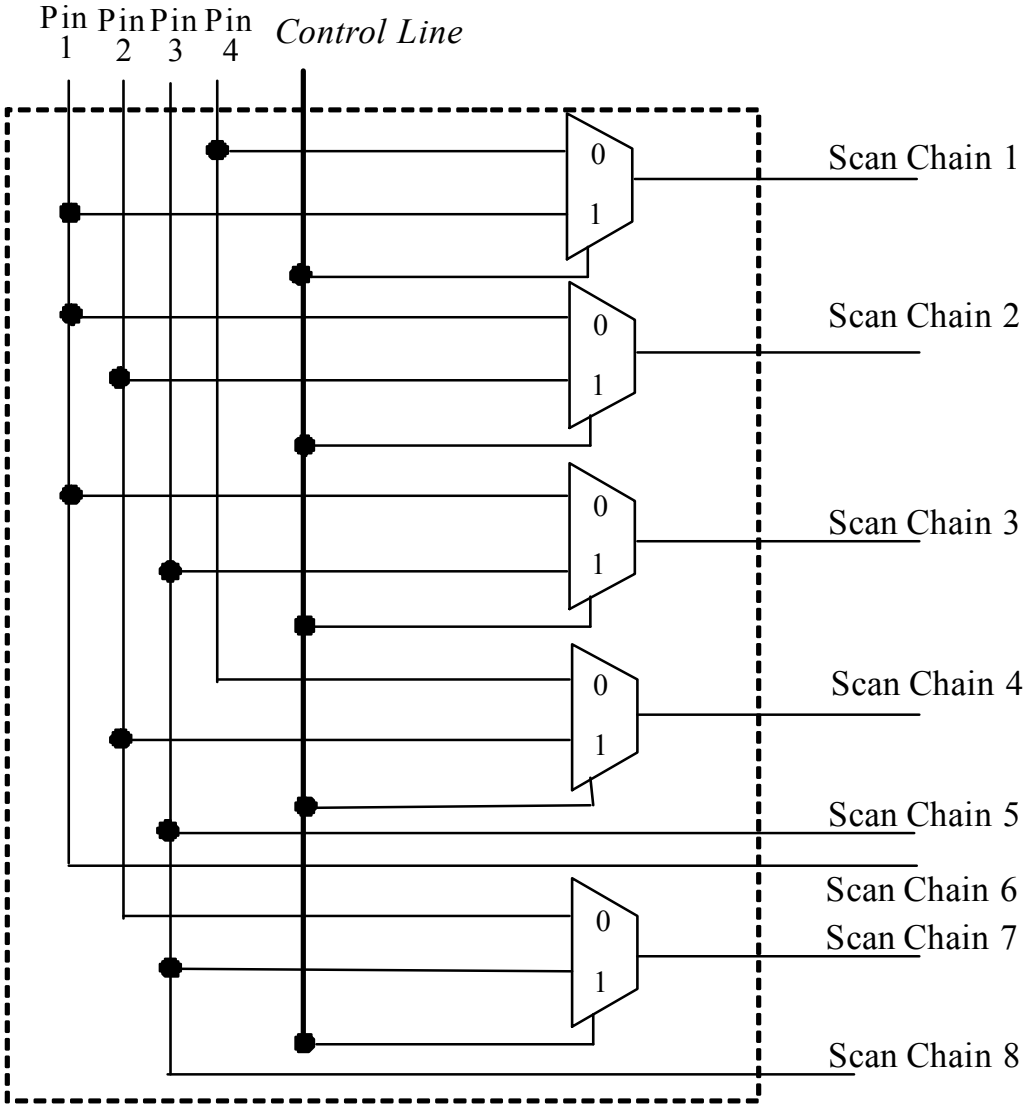
Multiple-input broadcast scan

- Use more than one channel to drive all scan chains
- The shorter each scan chain is, the easier to detect more faults because fewer constraints are placed on the ATPG

Reconfigurable Broadcast Scan

- Reduce the number of required channels compared to multiple-input broadcast scan
- Provide the capability to reconfigure the set of scan chains
- Two possible reconfiguration schemes
  - Static reconfiguration
  - Dynamic reconfiguration
    - Need more control information *versus* static reconfiguration

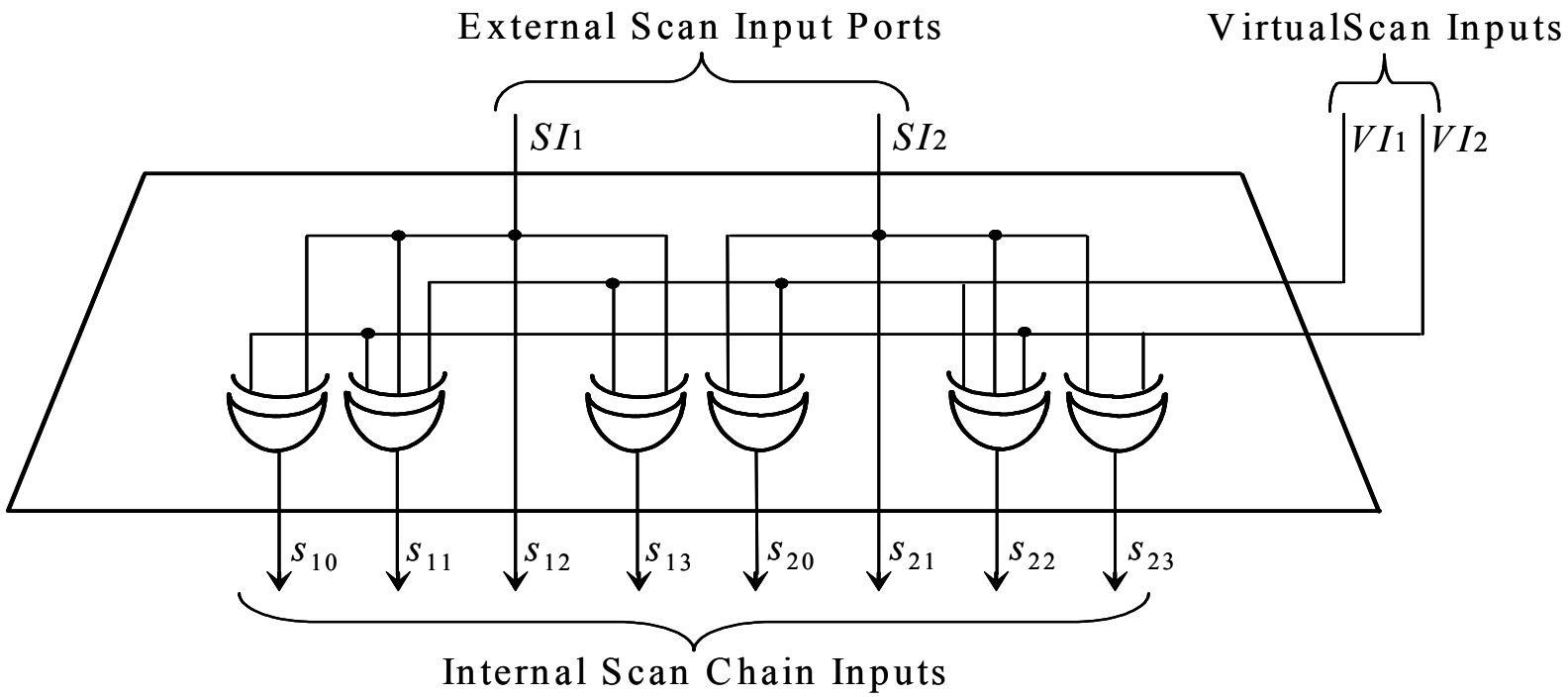
Example MUX Network with Control Line(s) connected only to select pins of the multiplexers



Virtual Scan

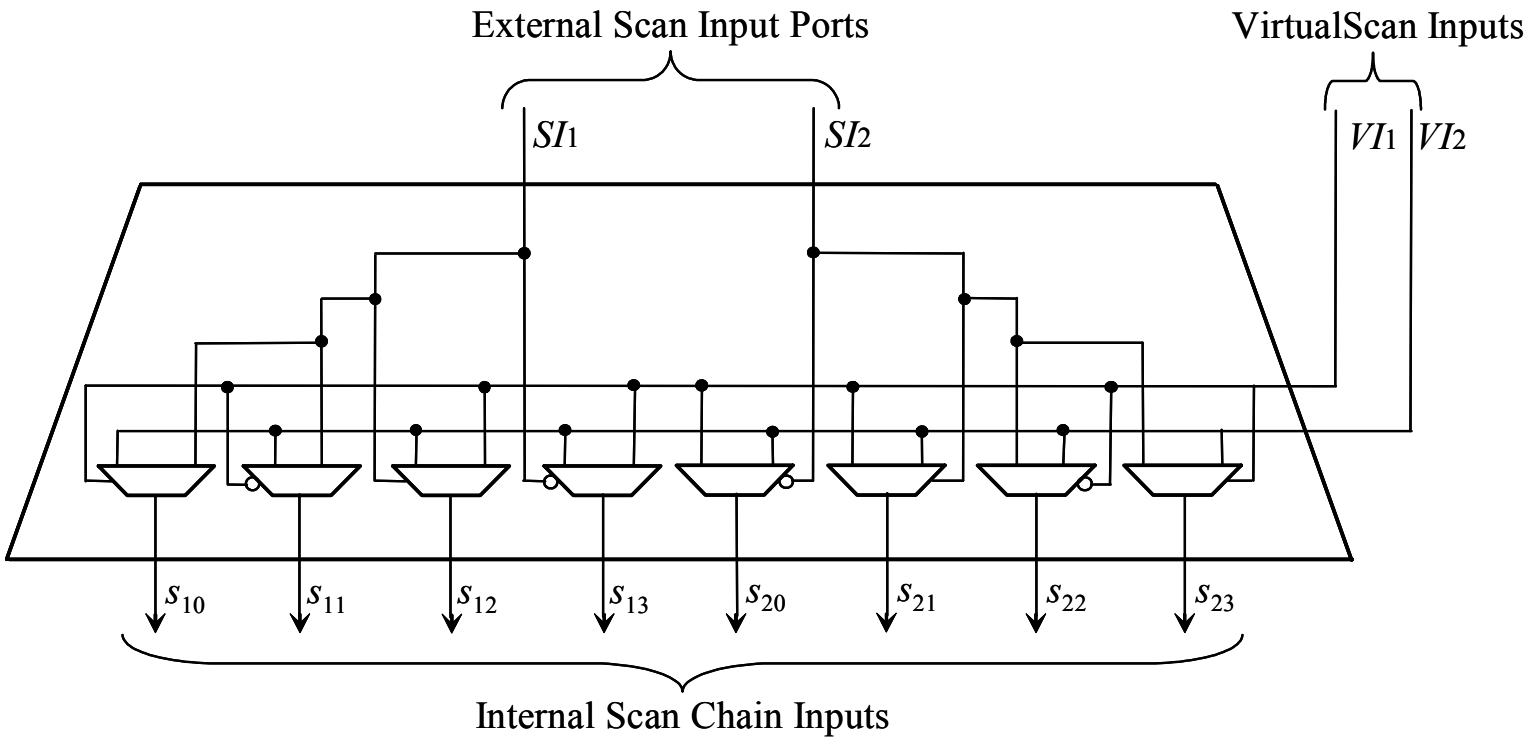
- Use Combinational logic network for stimulus decompression – called Broadcaster
  - Buffers, inverters, AND/OR gates, MUXs, XOR gates
- Advantages
  - One-Step ATPG – No need to solve linear equations as required in sequential linear decompressor.
  - Dynamic compaction can be effectively utilized during the ATPG process.

Example Virtual Scan Broadcaster Using an XOR Network



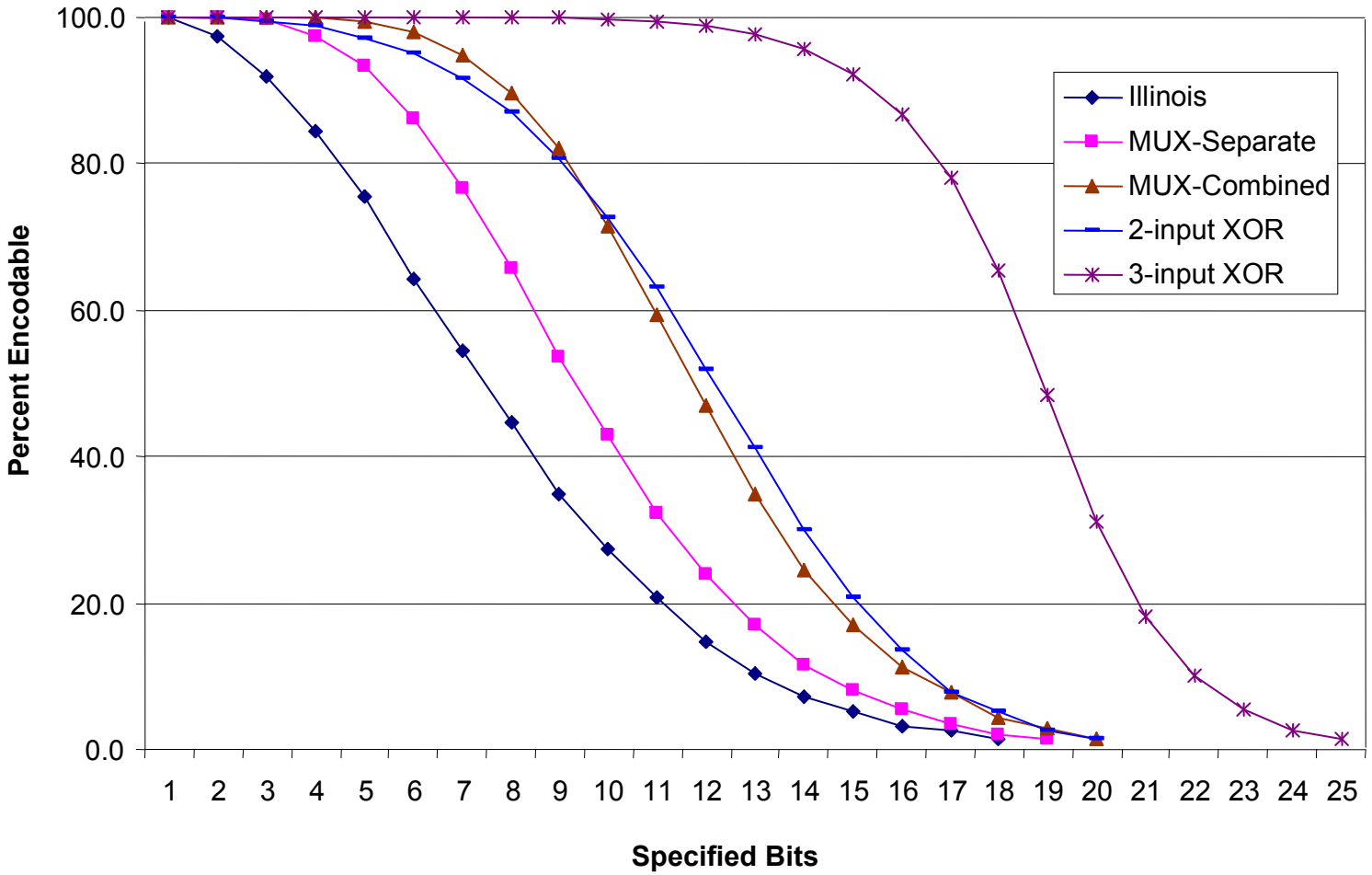
Broadcaster using an example XOR network with additional VirtualScan Inputs to reduce coverage loss

Example Virtual Scan Broadcaster Using a MUX Network



Broadcaster using an example MUX network with additional VirtualScan inputs that can also be connected to data pins of the multiplexers

Comparison



Encoding flexibility among combinational decompression schemes

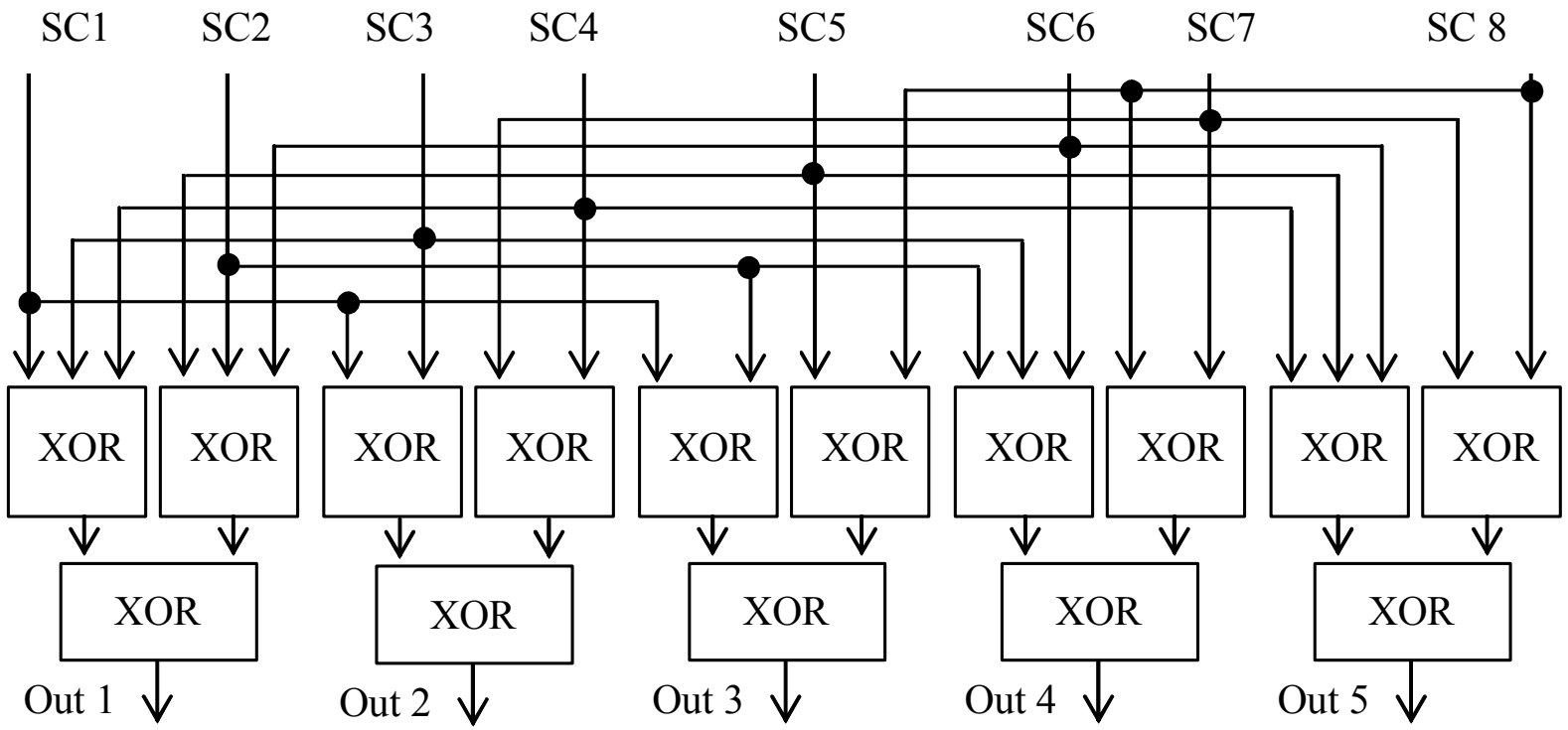
Circuits for Test Response Compaction

- Performed at the output of scan chains
- To reduce the amount of test response
- Grouped into three categories
  - Space compaction
  - Time compaction
  - Mixed space and time compaction

Space Compaction

- Space compactor is combinational
- Inverse procedure of linear expansion
- Compaction Techniques
  - X-Compact
  - X-Blocking
  - X-Masking
  - X-Impact

X-tolerant Response Compaction



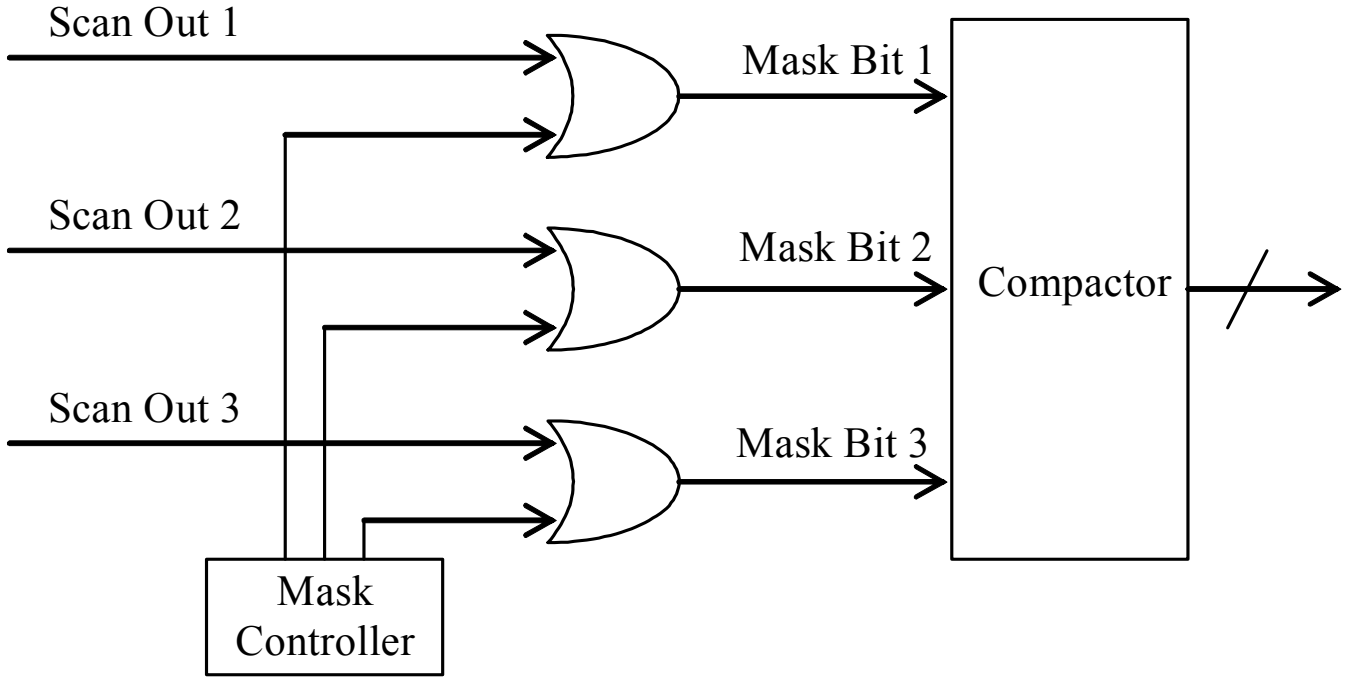
An X-compactor with 8 inputs and 5 outputs

X-Blocking (X-Bounding)

- Block X's before reaching the response compactor
- Scan design rule checker for identifying potential X-generators
- Impact
  - No X's will be observed
  - Fault coverage loss
  - Add area overhead
  - May impact delay due to the inserted logic

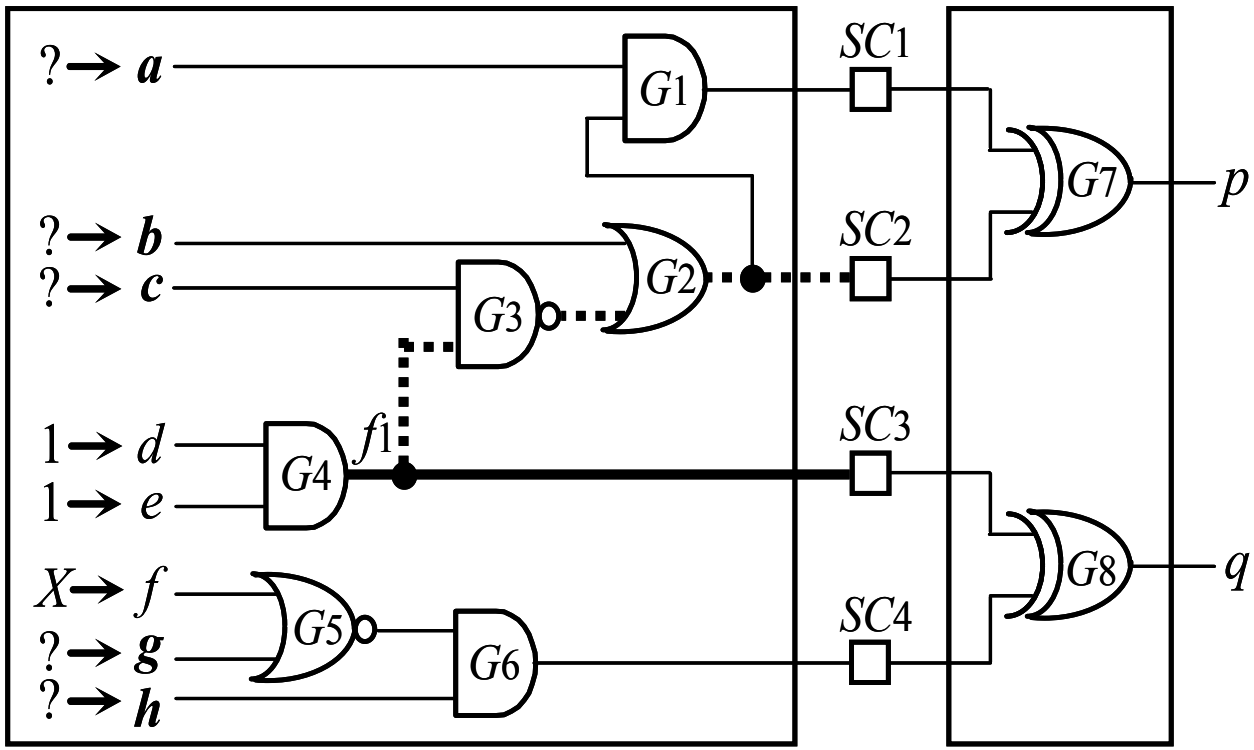
X-Masking

Mask off X's right before the response compactor



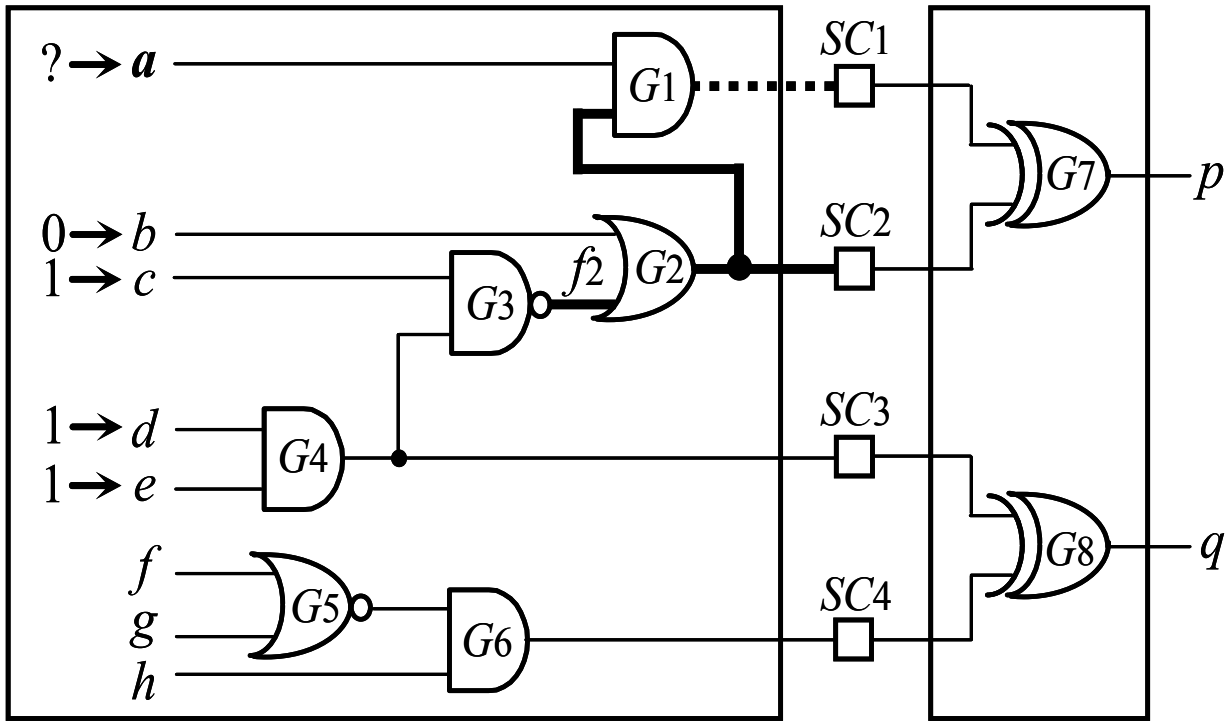
An example X-masking circuit

X-Impact



Handling of X-Impact

X-Impact

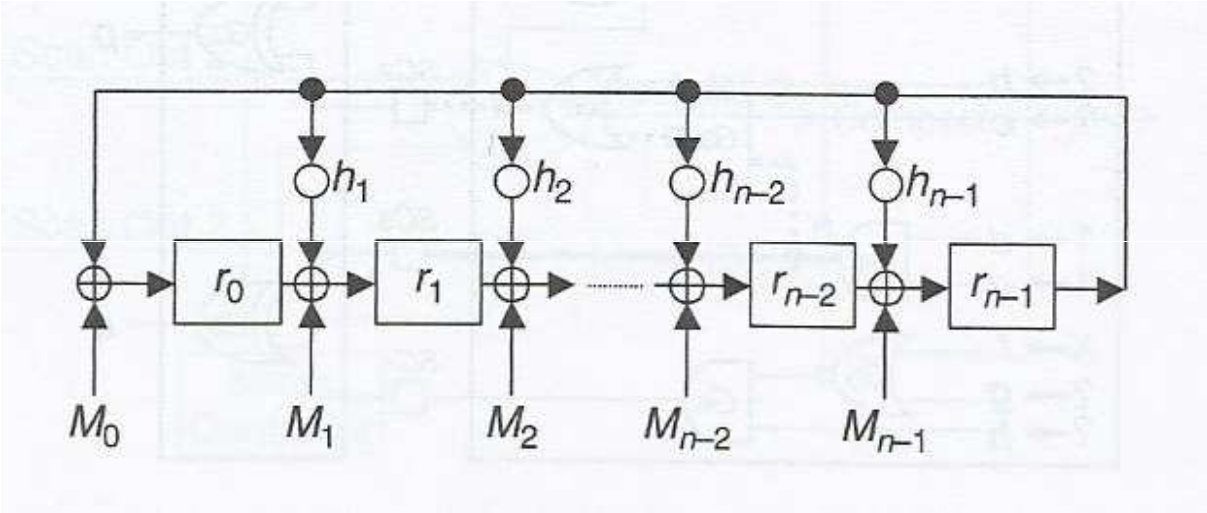


Handling of Aliasing

Time compaction

- Uses sequential logic to compact test response
- No unknown (X) values are allowed to reach the compactor; otherwise X-bounding, X-masking must be employed.
- MISR is most widely used

Multiple Input Signature Register (MISR)



Problem to solve

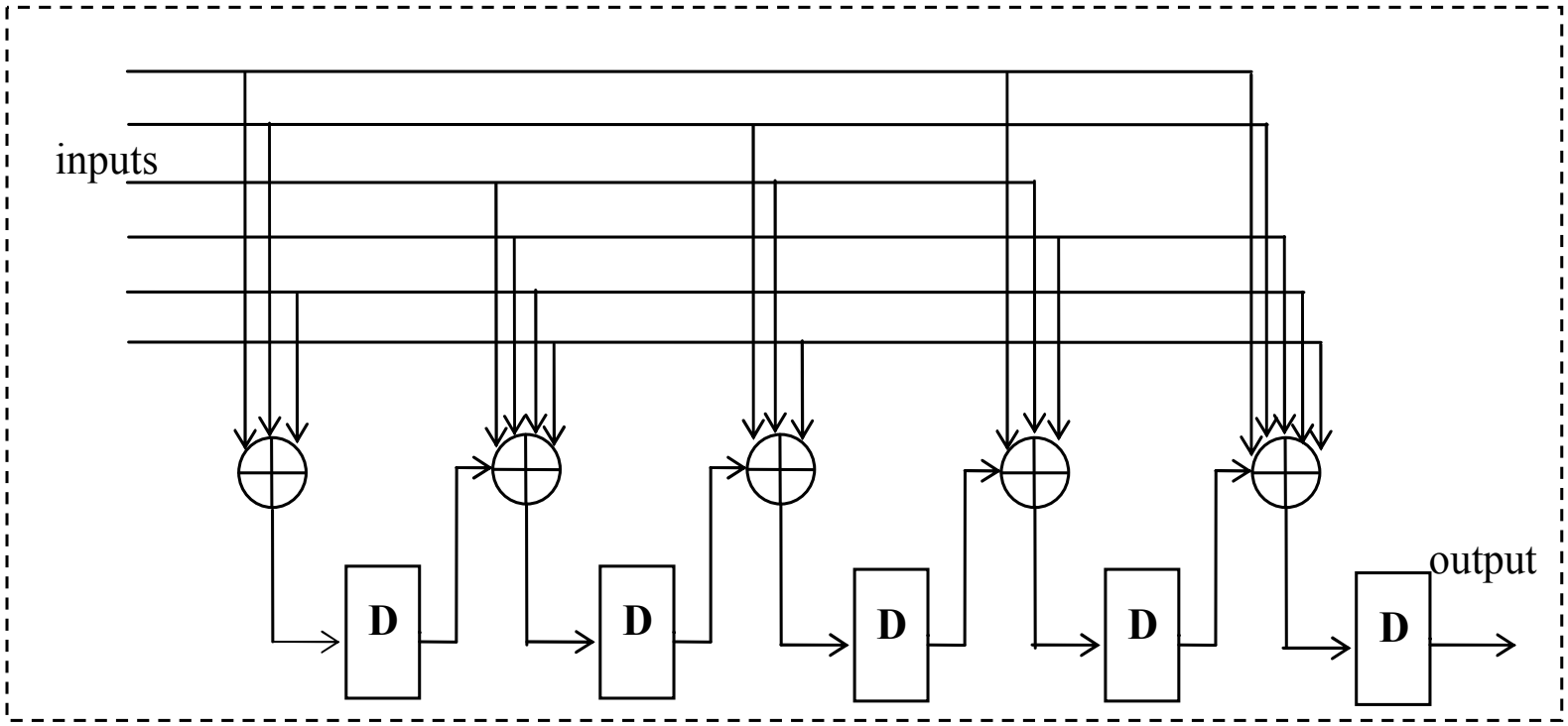
Consider a four stage MISR represented by function $f(x) = 1 + x + x^4$. Let M0={10010}, M1={11000}, M2={11000} and M3={10011}.

Evaluate the final signature stored in the MISR.

Mixed Time and Space Compaction

- Combine the advantages of a time compactor and a space compactor but with high area overhead
- Examples of mixed time and space compactors
  - OPMISR
  - Convolutional Compactor
  - q-compactor
    - No feedback path

q-compactor

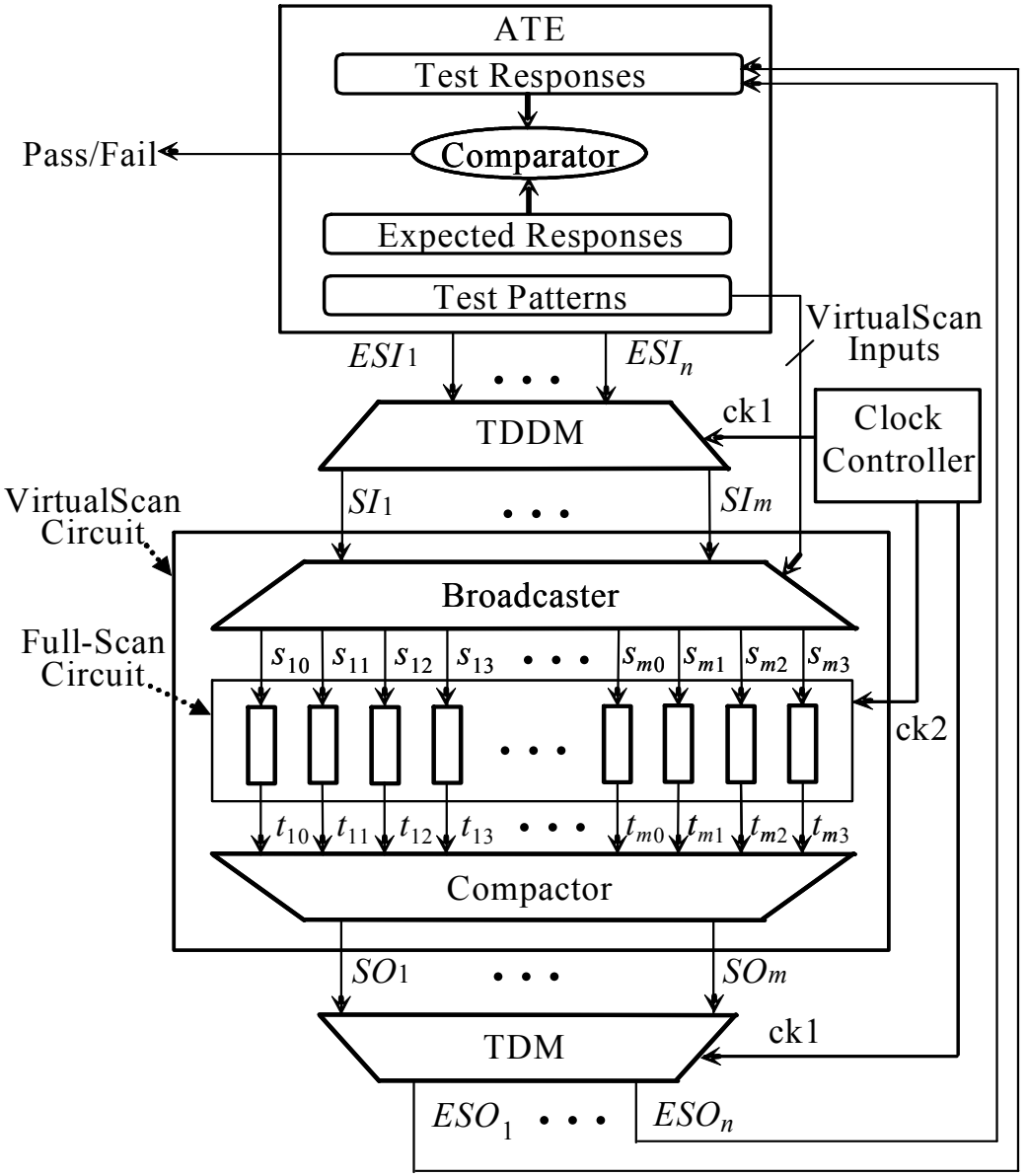


An example q-compactor with single output

Low-Power Test Compression Architectures

- Low-Power architectures
  - The Bandwidth-match low-power scan design can be used for test compression
- An Example – The UltraScan Architecture
  - Time-Division Demultiplexer (TDDM)
  - Time-Division Multiplexer (TDM)
  - Clock Controller
  - The TDDM/TDM circuit operates at 10 MHz and slow down the shift clock frequency to 1 MHz resulting in 10X reduction in shift power dissipation

UltraScan


ATE
Test Responses
Pass/Fail
Comparator
Expected Responses
Test Patterns
VirtualScan Inputs
ESI1
ESIn
ck1
TDDM
Clock Controller
VirtualScan Circuit
SI1
SIm
Broadcaster
Full-Scan Circuit
s10 s11 s12 s13 sm0 sm1 sm2 sm3
ck2
t10 t11 t12 t13 tm0 tm1 tm2 tm3
Compactor
SO1
SOm
ck1
TDM
ESO1
ESOn

Questions?