Digital Test Architectures:

Ad hoc testable design techniques and Scan design

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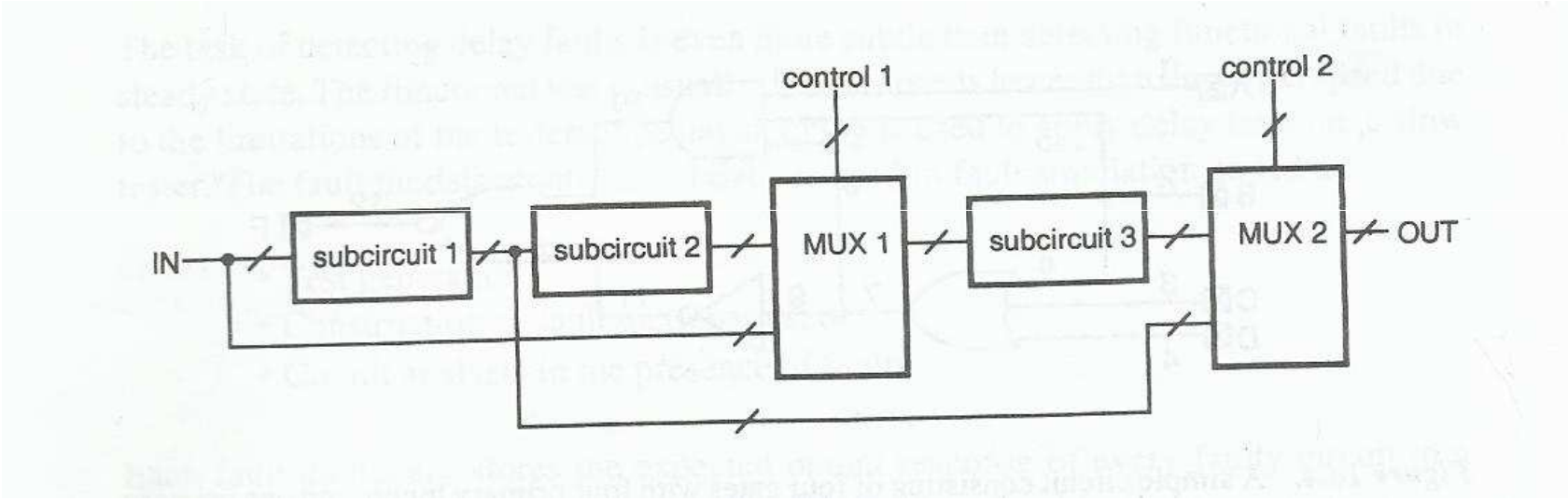
Digital Test Architectures

- Introduction
- Ad hoc Testable design techniques
- Scan Design
- Logic Built-In Self-Test
- Test Compression
- Random-Access Scan Design

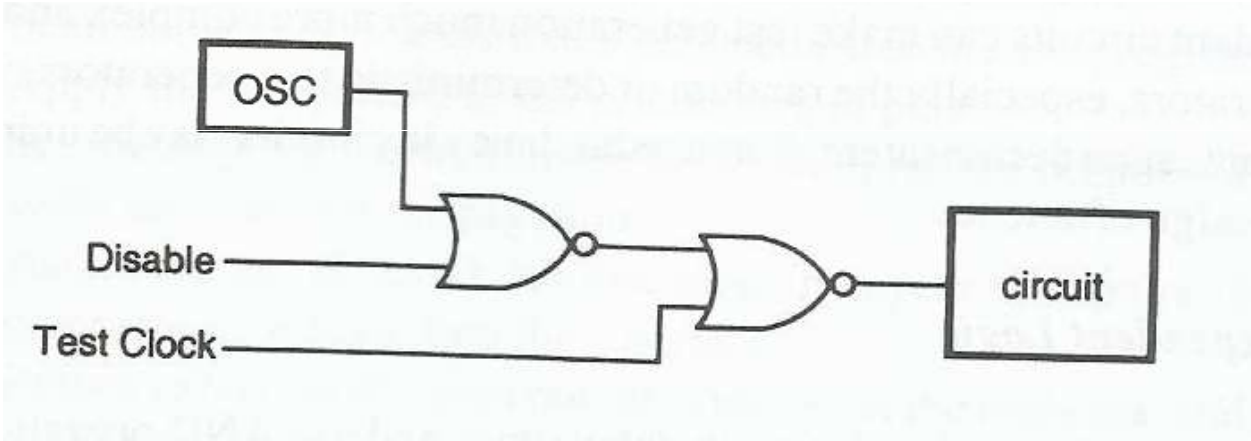
Ad hoc testable design approaches

- Good design practices learnt through experience are used as guidelines:
  - Avoid asynchronous (unclocked) feedback.
  - Make flip-flops initializable.
  - Avoid redundant gates. Avoid large fan-in gates.
  - Provide test control for difficult-to-control signals.
  - Avoid gated clocks.
  - Consider ATE requirements (tristates, etc.)
- Design reviews conducted by experts or design auditing tools.
- Disadvantages of ad-hoc DFT methods:
  - Experts and tools not always available.
  - Test generation is often manual with no guarantee of high fault coverage.
  - Design iterations may be necessary.

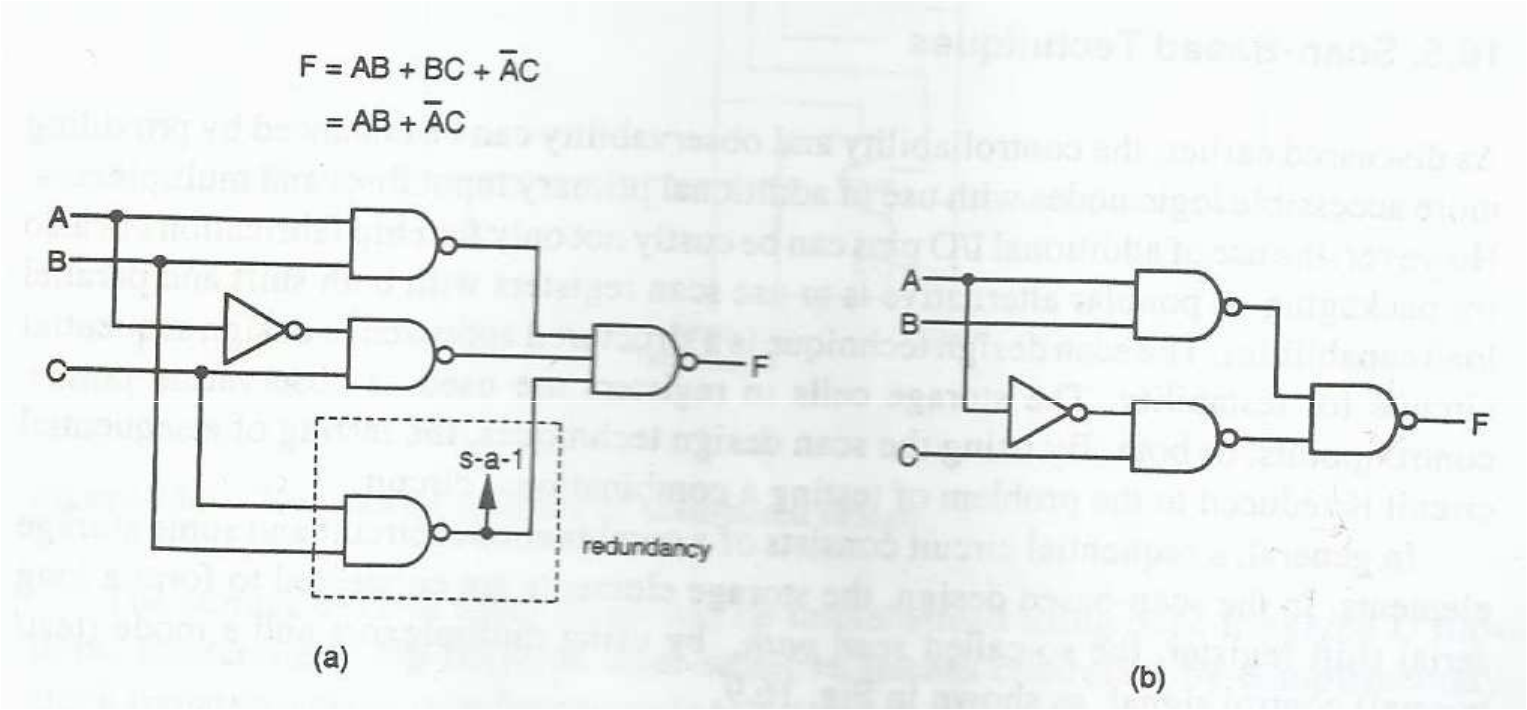
Partition and MUX method



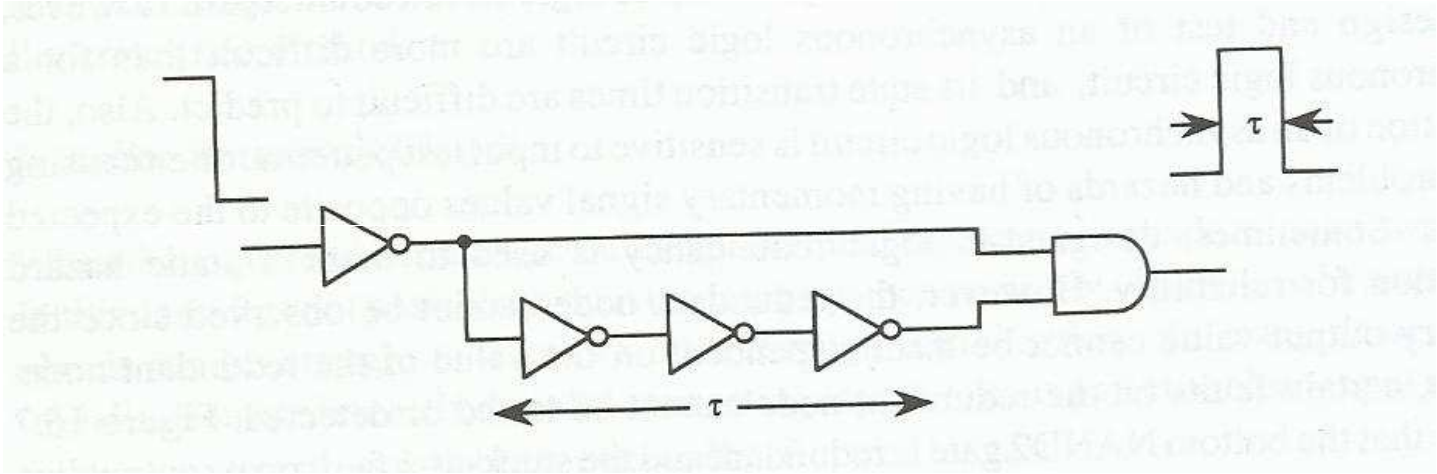
Disable Oscillator



Avoid Redundant Logic



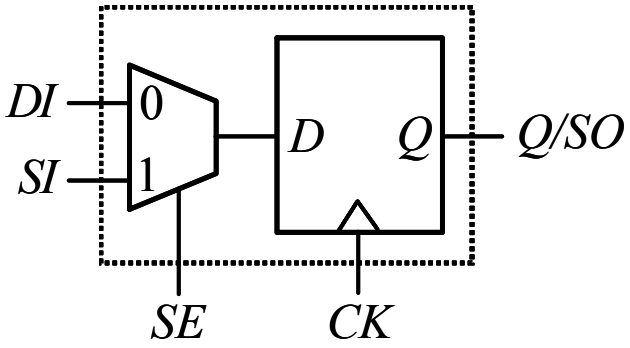
Avoid delay dependent logic



Scan Design

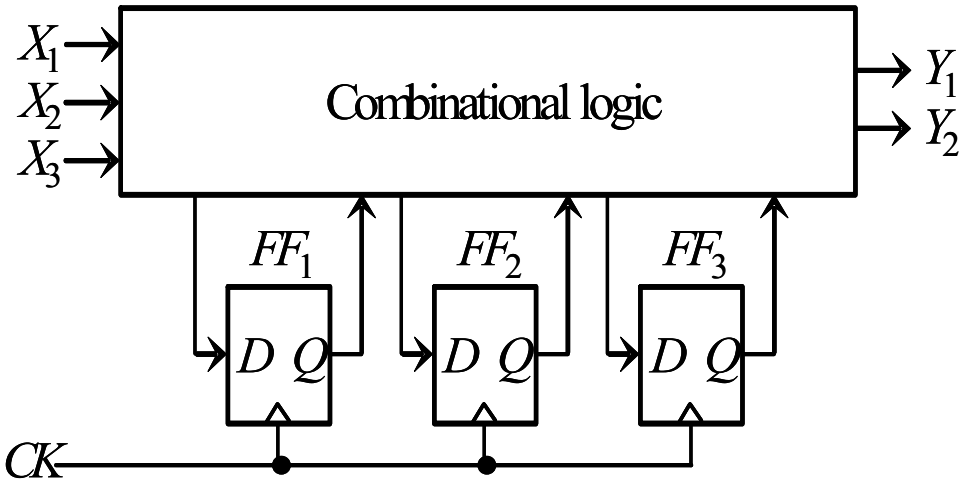
- Widely used structured DFT architecture
- Replace all selected storage elements with scan cells
- Connect scan cells into scan chains
- Operated in three modes:
  - Normal mode
    - All test signals are turned off.
    - The scan design operates in the circuit's original functional configuration.
  - Shift mode
    - to shift data into and out of the scan cells
  - Capture mode
    - to capture test response into scan cells

Scan Architectures



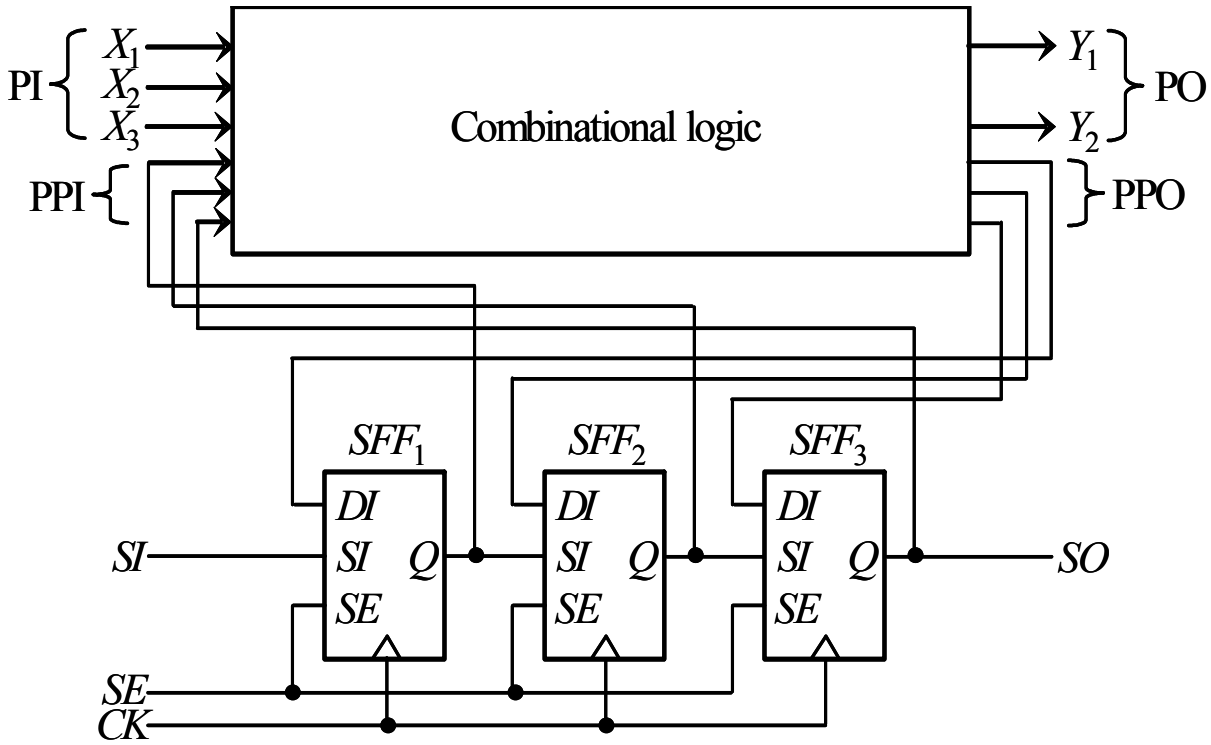
Muxed-D Scan Cell

The multiplexer uses a scan enable (SE) to select between the data input (DI) and the scan input (SI).



Sequential circuit example

Scan Architectures



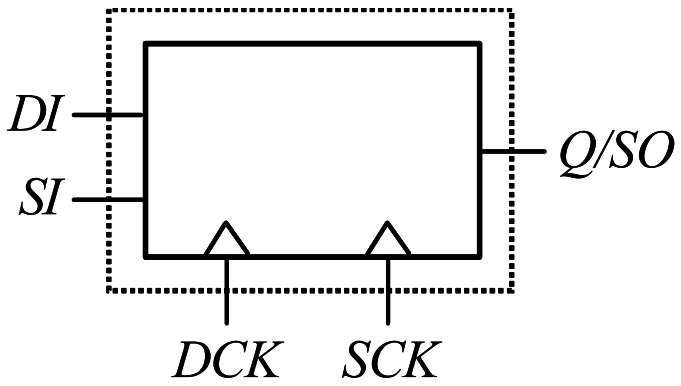
Muxed-D Scan Design

Replace FF1, FF2 and FF3 with SFF1, SFF2 and SFF3.

In shift mode, SE is set to 1, the scan cells operate as a single scan chain.

In capture mode, SE is set to 0, scan cells are used to capture the test response from the combinational logic.

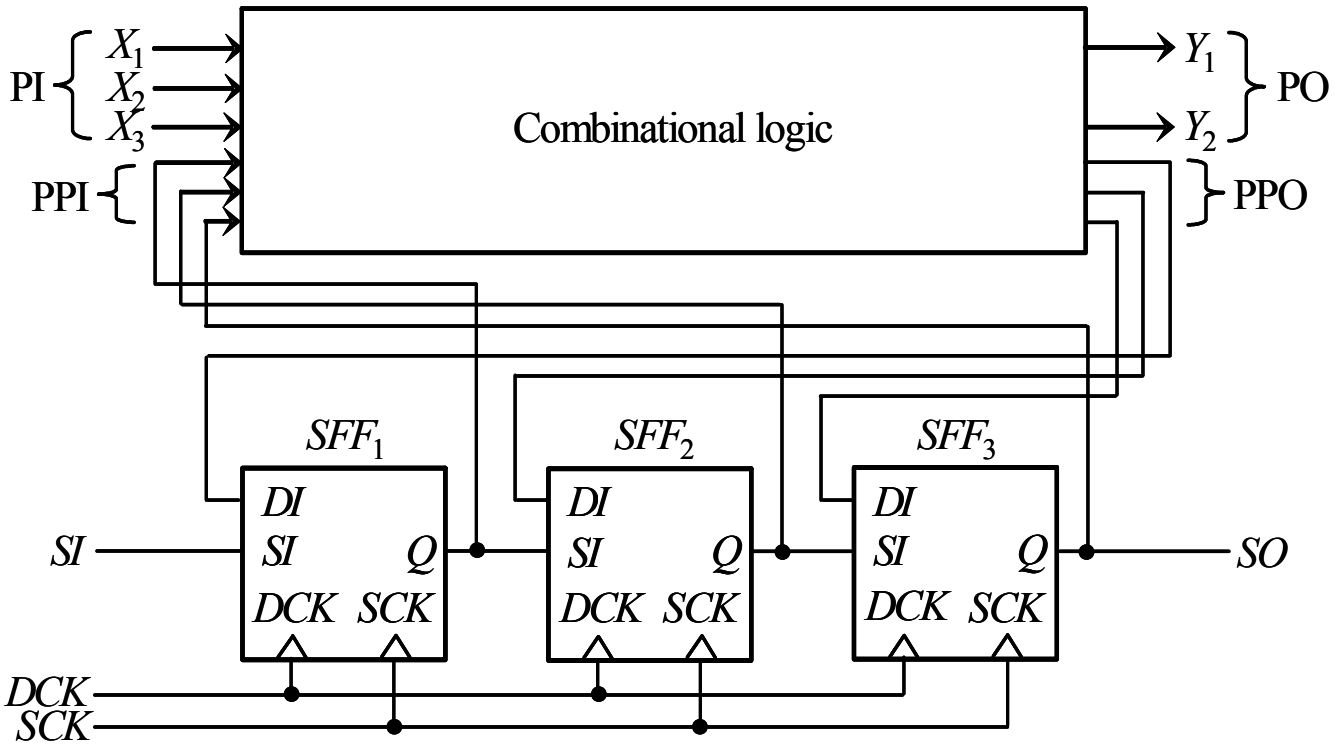
Scan Architectures



Input selection is conducted using two independent clocks, data clock DCK and shift clock SCK.

Clocked-Scan Cell

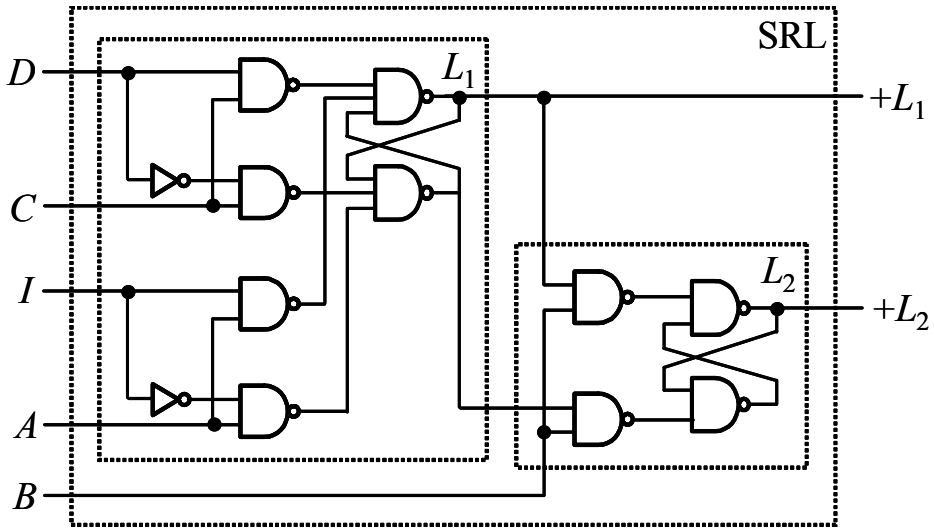
Scan Architectures



Clocked-Scan Design

DCK and SCK are used for distinguishing shift and capture operations; while SE is used to switch the shift and capture operations in muxed-D scan design.

Scan Architectures



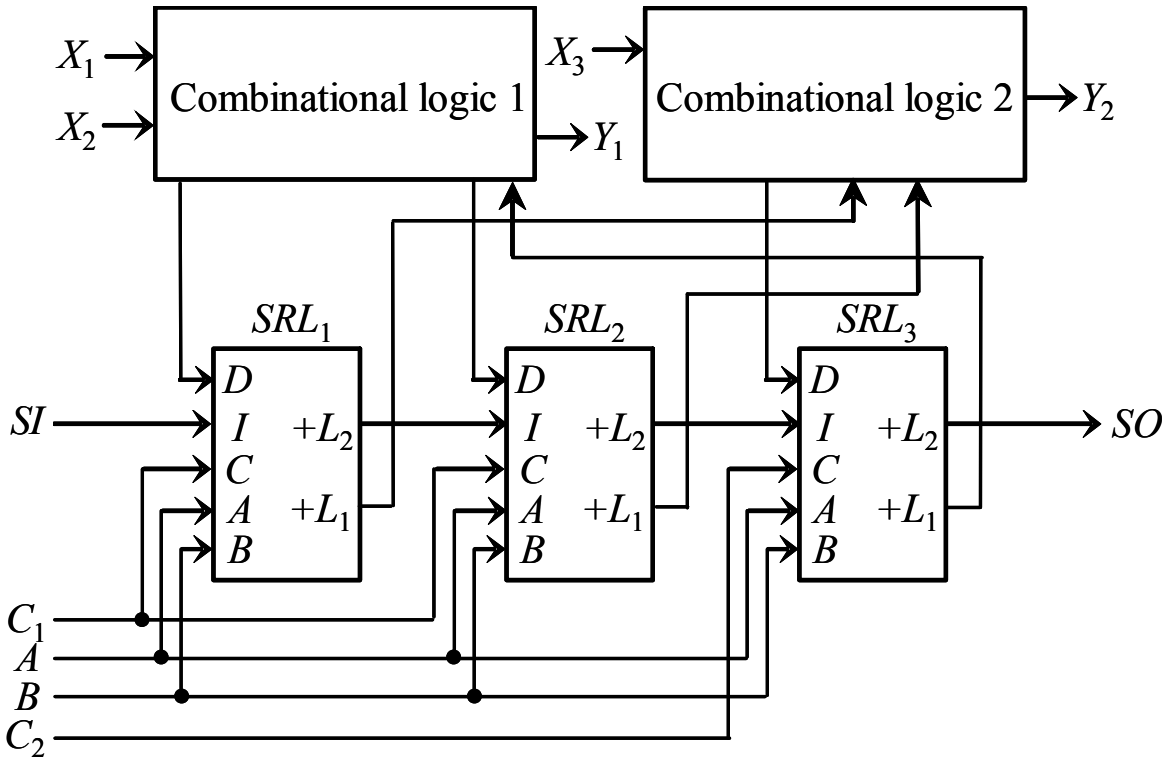
Polarity–hold shift register latch (SRL)

SRL can be used as an LSSD scan cell. This scan cell contains two latches, a master two-port D latch L_1 and a slave D latch L_2. Clocks C, A, and B are used to select between D and $+L_1$ and $+L_2$.

Level-Sensitive Scan Design (LSSD) can be implemented using a single-latch design or a double-latch design.

LSSD Scan Cell

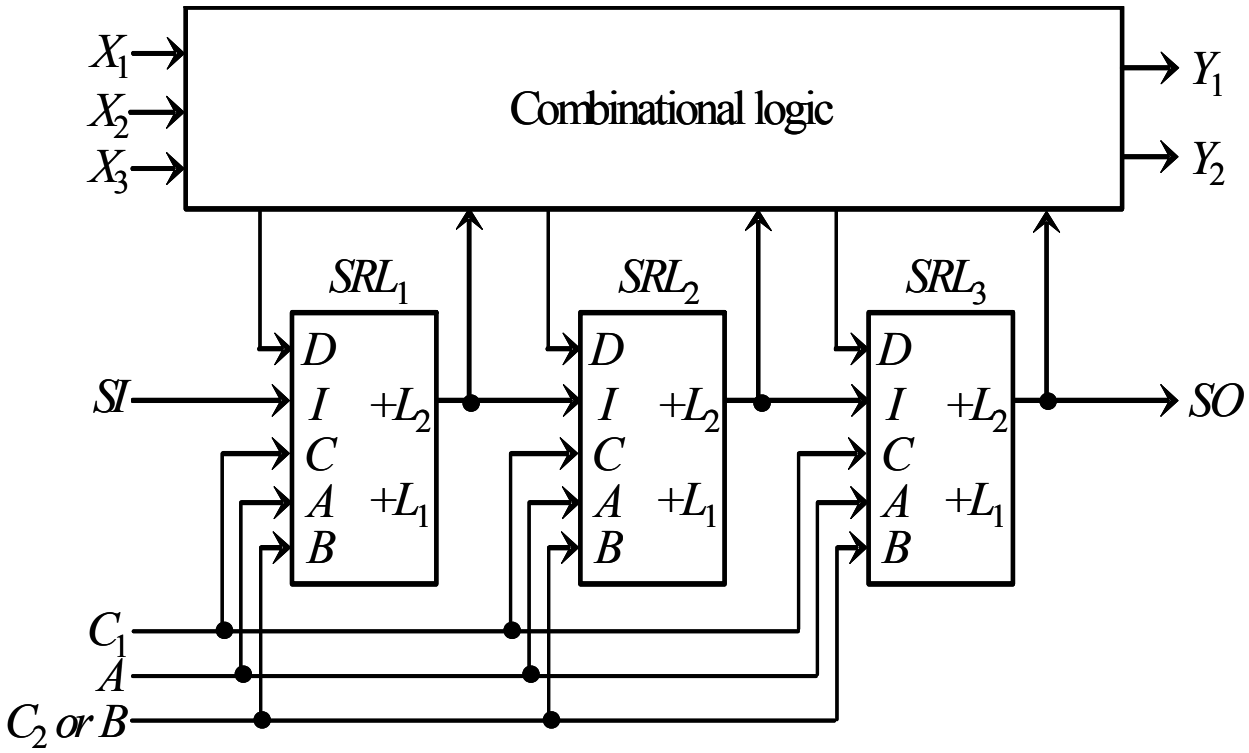
Scan Architectures



The system clocks C_1 and C_2 should be applied in a nonoverlapping fashion.

LSSD single-latch design

Scan Architectures



LSSD double-latch design

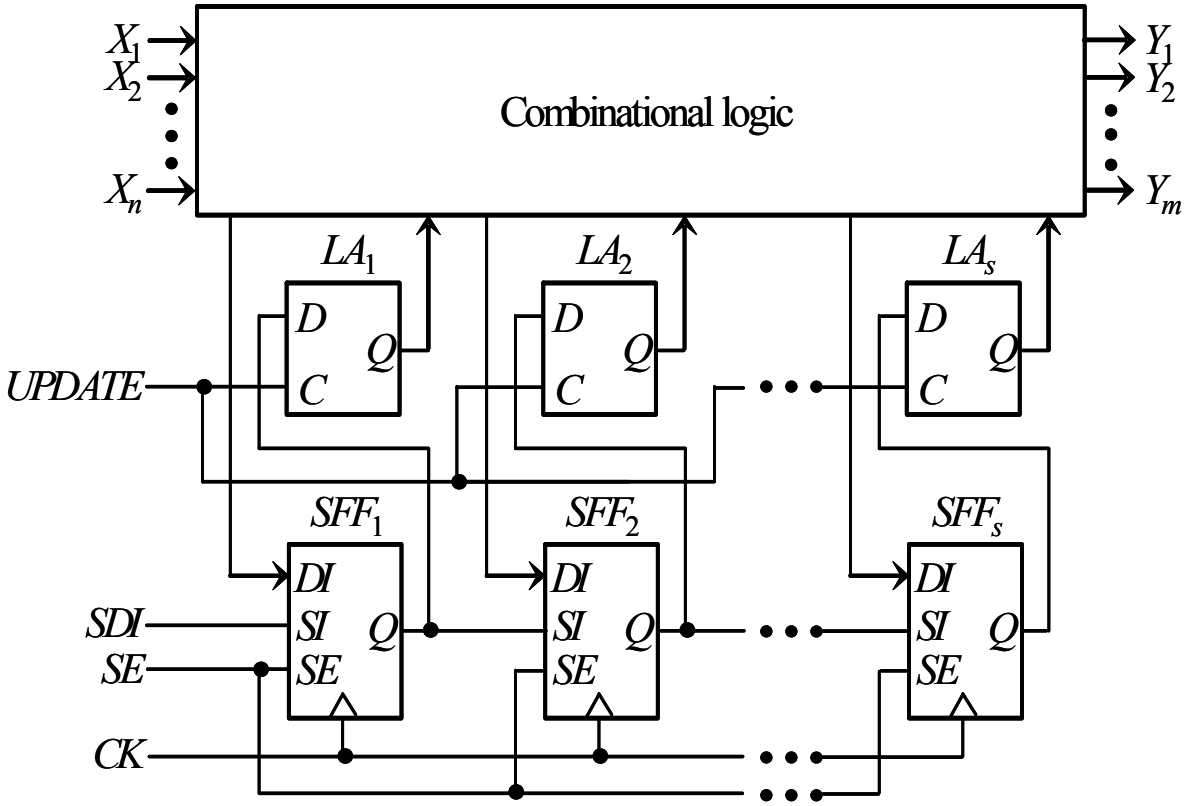
During the shift operation, clocks *A* and *B* are applied in a nonoverlapping manner, and the scan cells, SRL_1 ~ SRL_3, form a single scan chain from *SI* to *SO*.

During the capture operation, clocks C_1 and C_2 are applied in a non-overlapping manner to load the test response from the combinational logic into the scan cells.

Scan Architectures

- Enhanced-Scan Design
  - An alternative at-speed scan design for testing delay faults; testing of a delay fault requires a pair of test vectors in an at-speed fashion.
  - Enhanced-scan cell can store two bits of data; achieved by adding a D latch to a muxed-D scan cell or clocked-scan cell.
  - Disadvantages:
    - Higher hardware overhead
    - May activate many false paths causing an over-test problem

Scan Architectures



Enhanced-Scan Design

The first test vector *V*1 is shifted into *SFF*1 ~ *SFFs* and then stored into the additional latches (*LA*1 ~ *LAs*) when the *UPDATE* signal is set to 1.

Next, the second test vector *V*2 is shifted into the scan cells while the *UPDATE* signal is set to 0, in order to preserve the *V*1 value in the latches (*LA*1 ~ *LAs*).

Once the second vector *V*2 is shifted in, the *UPDATE* signal is applied, in order to change *V*1 to *V*2 while capturing the output response at-speed into the scan cells by applying *CK* after exactly one clock cycle.

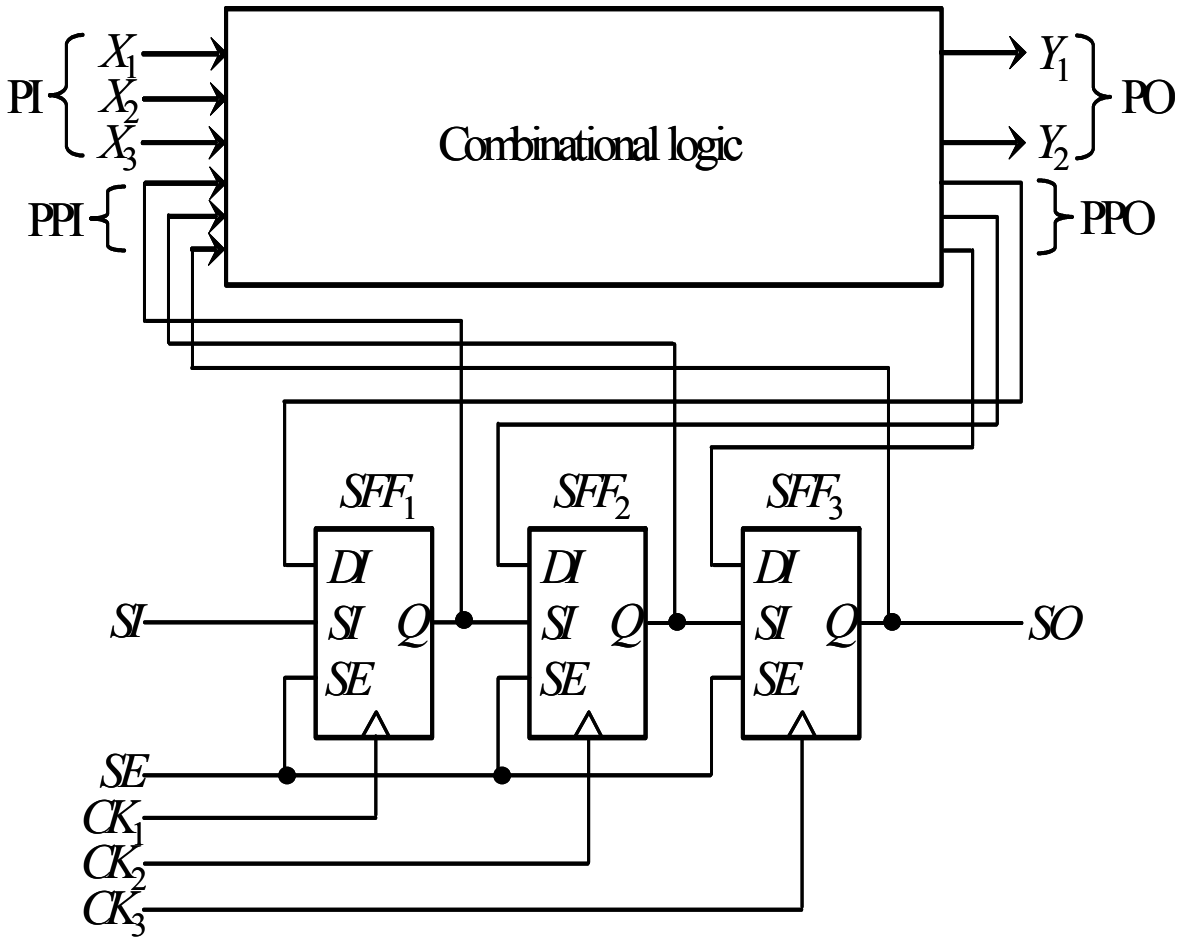
Low-Power Scan Architectures

- Serial Scan Design
  - Advantage:
    - Low routing overhead
  - Disadvantages:
    - Scan cells cannot be controlled or observed without affecting the values of other scan cells in the same scan chain
    - High switching activities during shift and capture can cause excessive shift (or test) power dissipation
- Low-Power Scan Design
  - Test power is related to dynamic power, and is proportional to $V_{DD}^2 f$
    - V_{DD} *is the supply voltage*
    - f is the switching frequency of the circuit node under test

Example Low-Power Scan Architectures

- Reduced-Voltage Low-Power Scan Design
  - Reduce the supply voltage
- Reduced-Frequency Low-Power Scan Design
  - Slow down the shift clock frequency but increase test application time
- Multi-Phase Low-Power Scan Design
  - Split the shift clock into a number of nonoverlapping clock phases but increase routing overhead and complexity during clock tree synthesis
- Bandwidth-Matching Low-Power Scan Design
  - Use pairs of serial-in/parallel-out shift register and parallel-in/serial-out shift register for bandwidth matching
- Hybrid Low-Power Scan Design
  - Combine any of the above-mentioned low-power scan designs

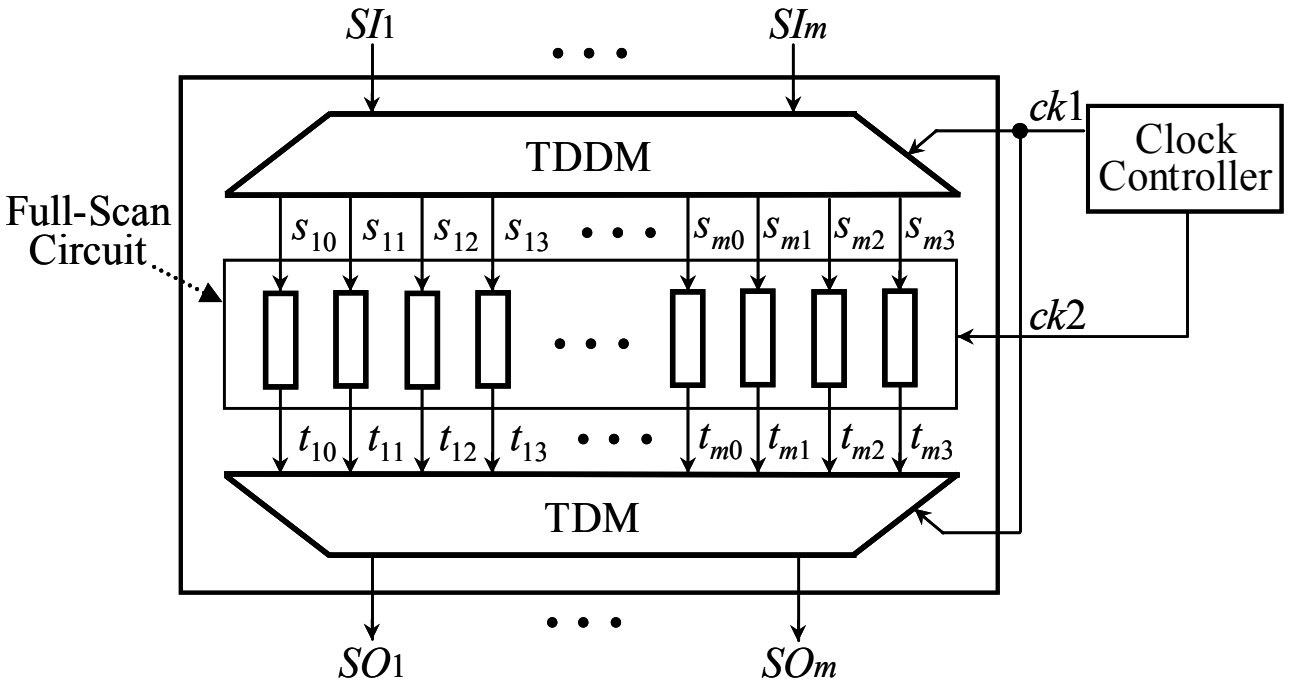
Multi-Phase Low-Power Scan Design



The clock *CK* is split into three clock phases CK_1, CK_2, and CK_3.

Using this scheme, a 3X reduction in shift power can be achieved, assuming each clock drives an equal number of scan cells.

Bandwidth-Matching Low-Power Scan Design



Each scan chain is split into 4 sub-scan chains with the SI and SO ports of each 4 sub-scan chains connected to a serial-in/parallel-out shift register and a parallel-in/serial-out shift register, respectively.

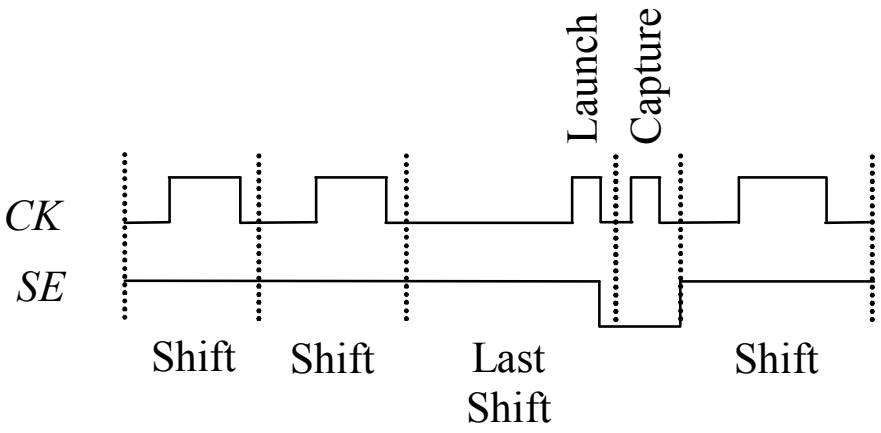
At-Speed Scan Architectures

- Synchronous Design
  - A scan design if the active edges of all capture clocks controlling the clock domains can be aligned precisely or triggered simultaneously
- Asynchronous Design
  - A scan design if not synchronous

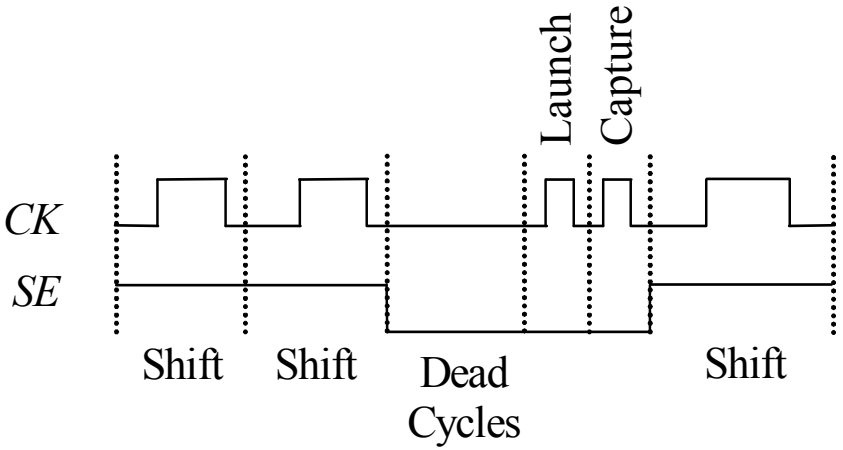
At-Speed Scan Architectures

- Two basic schemes for test multiple clock domain at-speed
  - Skewed-load (Launch-on-shift)
    - Use the last shift clock pulse followed immediately by a capture clock pulse to launch the transition and capture the output response
  - Double-capture (Launch-on-capture or Broad-side)
    - Use two consecutive capture clock pulses to launch the transition and capture the output test response

Basic At-Speed Test Schemes



Skewed-load

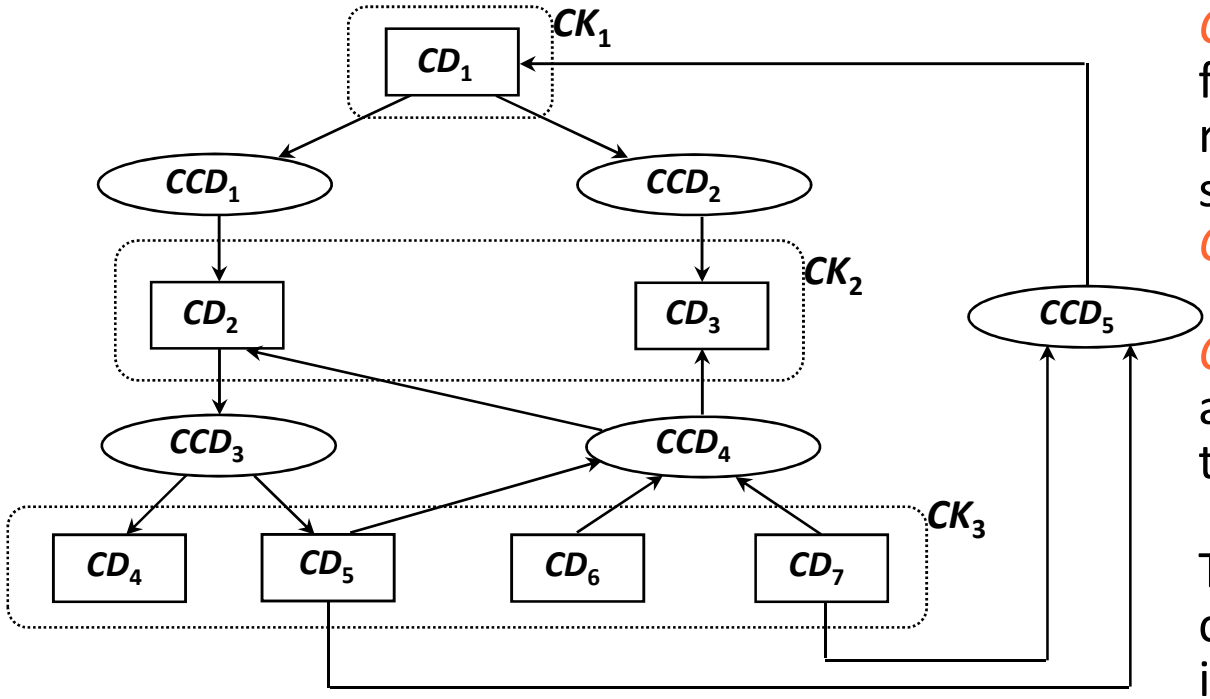


Double-capture

Clock grouping

- Can reduce test application time and test data volume during automatic test pattern generation (ATPG)
- Is a process used to analyse all data paths in the scan design in order to determine all independent or noninteracting clocks that can be grouped and applied simultaneously

Clock grouping example



CD_2 and CD_3 are independent from each other; hence their related clocks can be applied simultaneously during test as CK_2.

CD_4 through CD_7 can also be applied simultaneously during test as CK_3.

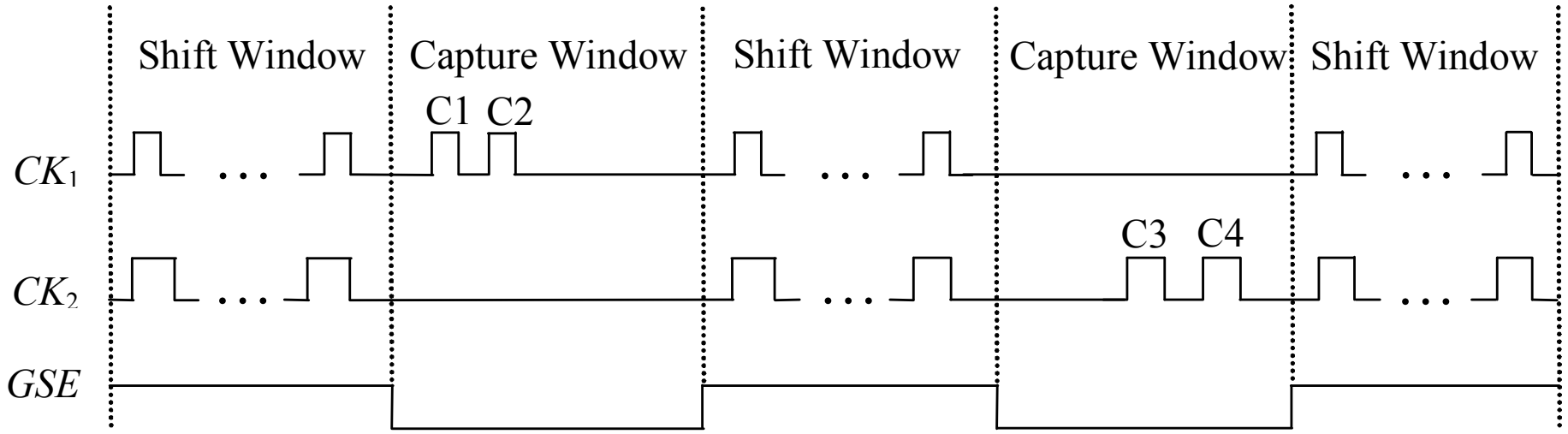
Therefore three grouped clocks instead of seven individual clocks can be used to test the circuit during the capture operation.

Clock schemes

- One-hot clocking
  - Apply only one grouped clock during each capture operation
  - Produce the highest fault coverage but generate most test patterns
- Simultaneous clocking
  - Mask off unknown values at the originating scan cells or receiving scan cells across clock domains
  - Generate the least number of patterns but may result in high fault coverage loss
- Staggered clocking
  - Grouped clocks are applied sequentially
  - Generate pattern count close to simultaneous clocking and fault coverage close to one-hot clocking

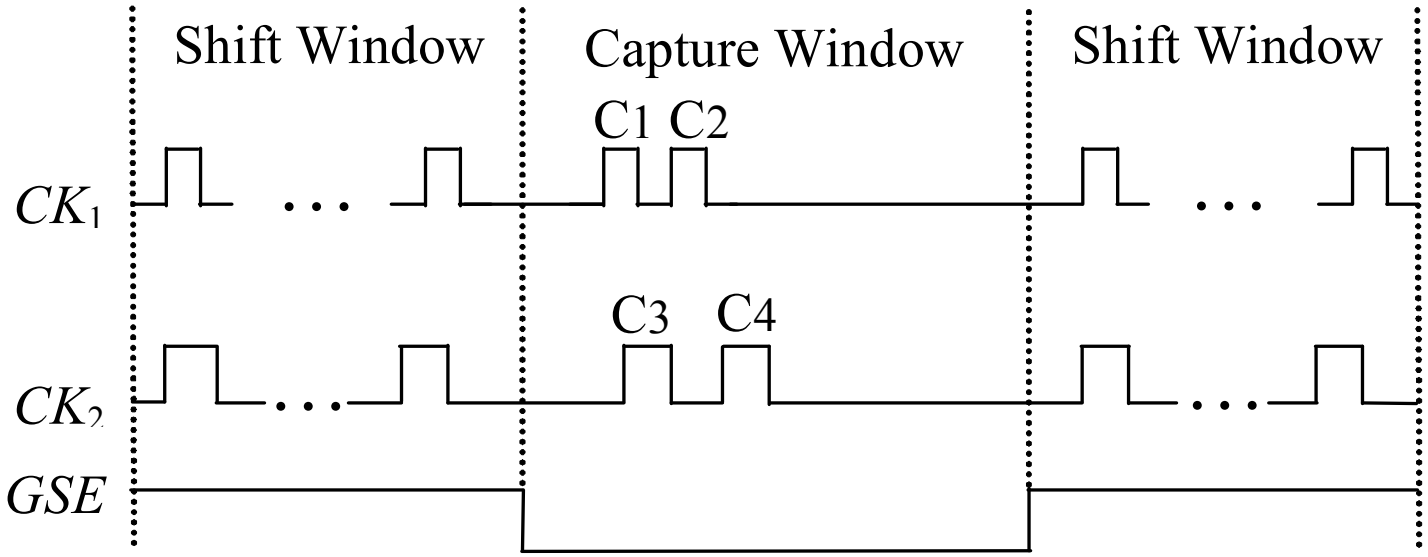
At-speed Clocking Scheme for Testing Two Interacting Clock Domains

(One-hot clocking)



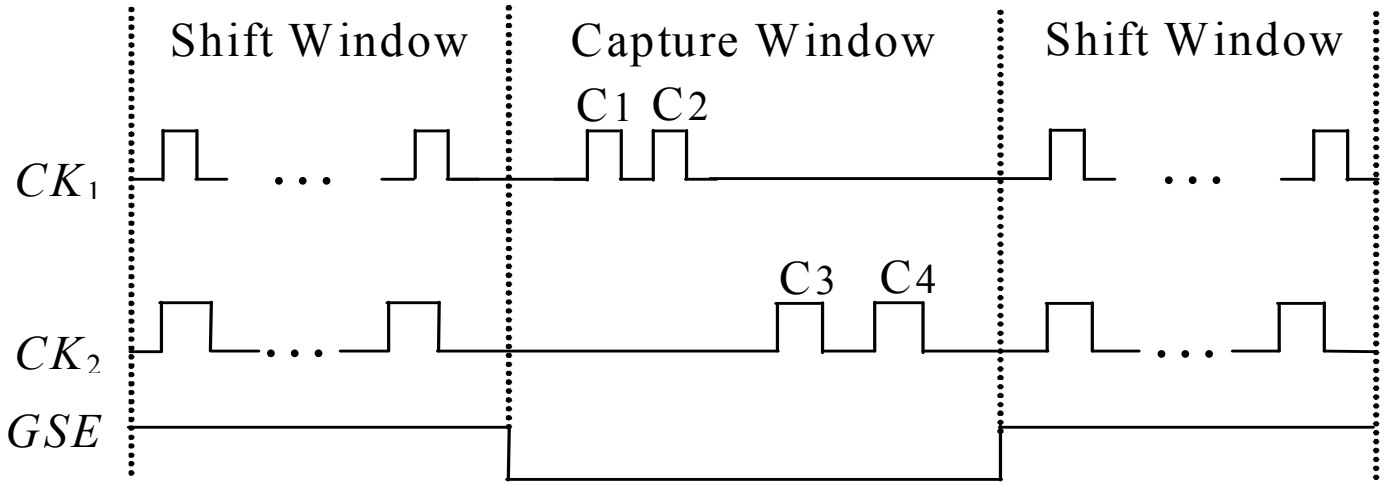
At-speed Clocking Scheme for Testing Two Interacting Clock Domains

(Simultaneous clocking)



At-speed Clocking Scheme for Testing Two Interacting Clock Domains

(Staggered clocking)



Questions?