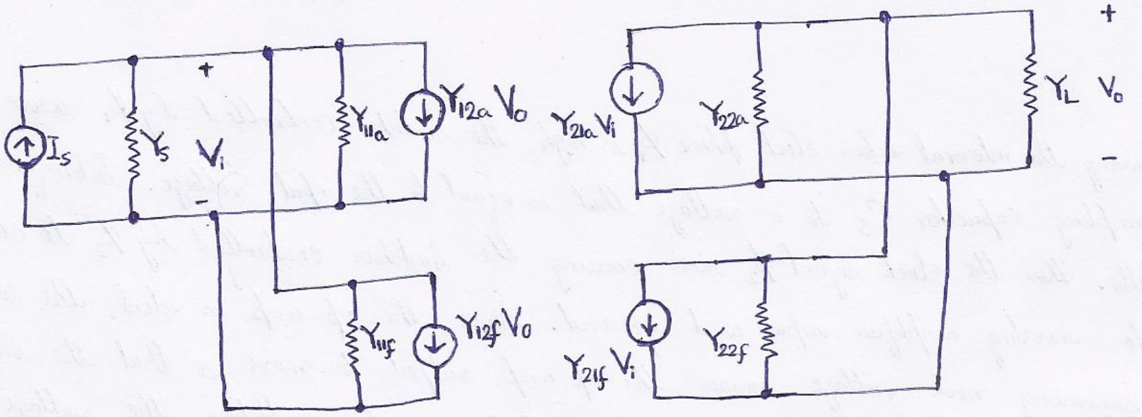
IEC 103

Hints and Solutions to Mid Semester Examination 2
Basic Electronic Circuits

1. The equivalent circuit for the given amplifier configuration is as follows:—



From the Y parameter representation, we get,

$$I_s = (Y_s + Y_{11a} + Y_{11f})V_i + (Y_{12a} + Y_{12f})V_o \quad \text{(At the input side)} \quad \ldots (1)$$

$$0 = (Y_{21a} + Y_{21f})V_i + (Y_L + Y_{22a} + Y_{22f})V_o \quad \text{(At the output side)} \quad \ldots (2)$$

Let $Y_i = Y_s + Y_{11a} + Y_{11f}$.

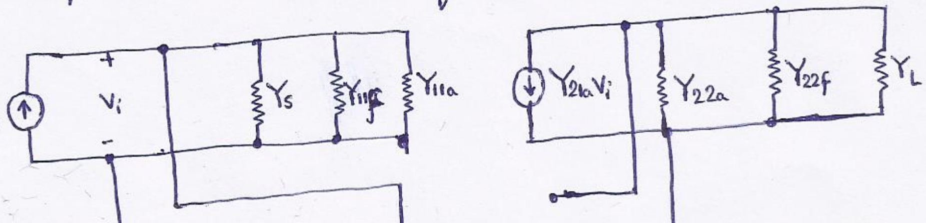
$Y_o = Y_L + Y_{22a} + Y_{22f}$.

Solving (1) and (2) we get,
$$\frac{V_o}{I_s} = \frac{-(Y_{21a} + Y_{21f})}{Y_iY_o - (Y_{21a}+Y_{21f})(Y_{12a}+Y_{12f})}$$

$$\Rightarrow \frac{V_o}{I_s} = \frac{-\dfrac{(Y_{21a}+Y_{21f})}{Y_iY_o}}{1 + \dfrac{-(Y_{21a}+Y_{21f})(Y_{12a}+Y_{12f})}{Y_iY_o}}$$

$$\Rightarrow \frac{V_o}{I_s} = \frac{-\dfrac{(Y_{21a}+Y_{21f})}{(Y_s+Y_{11a}+Y_{11f})(Y_L+Y_{22a}+Y_{22f})}}{1 - \dfrac{(Y_{21a}+Y_{21f})}{(Y_s+Y_{11a}+Y_{11f})(Y_L+Y_{22a}+Y_{22f})}(Y_{12a}+Y_{12f})} \quad \text{(Proved)}. \quad \ldots (A)$$

With the given approximation the circuit may be redrawn as:



For the given practical approximations, we have, $|Y_{21a}| >> |Y_{21f}|$ and $|Y_{12a}| << |Y_{12f}|$.

Hence from (A), we get, $$\frac{V_o}{I_s} \approx - \frac{\dfrac{Y_{21a}}{(Y_s + Y_{11a} + Y_{11f})(Y_L + Y_{22a} + Y_{22f})}}{1 - \dfrac{Y_{21a} Y_{12f}}{(Y_s + Y_{11a} + Y_{11f})(Y_L + Y_{22a} + Y_{22f})}}$$ (Proved).

2. During the interval when clock phase ϕ_1 is high, the switches controlled by ϕ_1 serve to close and charge the sampling capacitor C_s to a voltage that is equal to the input voltage. Subsequently the clock signal ϕ_1 falls. Then the clock signal ϕ_2 rises causing the switches controlled by ϕ_2 to close and C_s is connected to inverting amplifier input and ground. Since, the op-amp is ideal, the resulting change in the summing node voltage causes the op-amp output to move so that the summing node voltage is driven back to ground. After the transient has gone to completion, the voltage across C_s is driven to zero.

Applying the principle of charge conservation, the charge stored at time index $[n]$ is

$$Q[n] = (0 - V_s[n])C_s + (0 - V_o[n])C_I \quad \ldots\ldots (1)$$

Charge stored at time $[n+\frac{1}{2}]$ is:

$$Q[n+\tfrac{1}{2}] = (0)C_s + (0 - V_o[n+\tfrac{1}{2}])C_I \quad \ldots\ldots (2).$$

Since charge is conserved,

$$Q[n] = Q[n+\tfrac{1}{2}]. \quad \ldots (3)$$

Also, the charge stored in C_I is constant during ϕ_1.

Hence, $$V_o[n+1] = V_o[n+\tfrac{1}{2}] \quad (4)$$

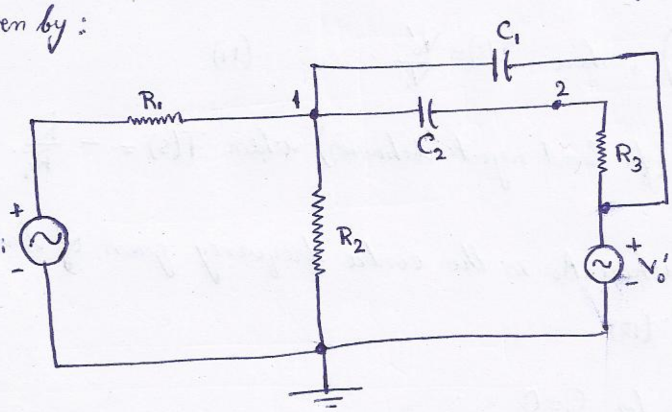
Combining (1), (2), (3), (4), we get, $$V_o[n+1] = V_o[n] + \left(\frac{C_s}{C_I}\right)V_s[n] \quad \ldots\ldots (5)$$

From (5), we have, $$V_o(j\omega) = V_o(j\omega)e^{-j\omega T} + \left(\frac{C_s}{C_I}\right)V_s(j\omega)e^{-j\omega T}$$

Hence, $$\frac{V_o(j\omega)}{V_s(j\omega)} = -\frac{C_s}{C_I}\frac{1}{(1-e^{j\omega T})} = \frac{C_s}{C_I}\cdot\frac{2j}{(e^{j\omega T/2} - e^{-j\omega T/2})}\cdot\frac{e^{-j\omega T/2}}{2j}$$

$$= \frac{C_s}{C_I}\cdot\left(\frac{1}{\sin\frac{\omega T}{2}}\right)\cdot\left(\frac{e^{-j\omega T/2}}{2j}\right).$$ (Proved).

3. Let V_o' be the voltage at the input of resistance R_5. The equivalent circuit for the subcircuit driving resistance R_5 is given by:



Applying KCL at nodes 1 and 2 we get,

$$\frac{V_1-V_i}{R_1}+\frac{V_1-V_o'}{(1/sC_1)}+\frac{V_1-V_2}{(1/sC_2)}+\frac{V_1}{R_2}=0 \quad \ldots\ldots (1)$$

$$\frac{V_2-V_1}{(1/sC_2)}+\frac{V_2-V_o'}{R_3}=0 \quad \ldots\ldots (2)$$

Rearranging (1) and (2) we get, $V_1\left(\frac{1}{R_1}+\frac{1}{R_2}+sC_1+sC_2\right)-sC_2V_2=\frac{V_i}{R_1}+sC_1V_o' \quad \ldots\ldots (3)$

and $V_1(-sC_2)+V_2\left(sC_2+\frac{1}{R_3}\right)=\frac{V_o'}{R_3} \quad \ldots\ldots (4)$

Solving (3) and (4) for V_2 and putting $V_2=0$ we get,

$$\begin{vmatrix} \frac{1}{R_1}+\frac{1}{R_2}+sC_1+sC_2 & \frac{V_i}{R_1}+sC_1V_o' \\ -sC_2 & \frac{V_o'}{R_3} \end{vmatrix}=0.$$

$$\Rightarrow V_o'\left(\frac{1}{R_1R_3}+\frac{1}{R_2R_3}+\frac{sC_1}{R_3}+\frac{sC_2}{R_3}+s^2C_1C_2\right)=-\frac{V_i}{R_1}sC_2.$$

$$\Rightarrow \frac{V_o'}{V_i}=-\frac{\frac{sC_2}{R_1}}{\frac{1}{R_1R_3}+\frac{1}{R_2R_3}+\frac{sC_1}{R_3}+\frac{sC_2}{R_3}+s^2C_1C_2}$$

$$\Rightarrow \frac{V_o'}{V_i}=-\frac{\frac{s}{R_1C_1}}{s^2+\left(\frac{C_1+C_2}{R_3C_1C_2}\right)s+\frac{(R_1+R_2)}{R_3C_1C_2R_1R_2}} \quad \ldots\ldots (5)$$

Equation (5) represents the standard form of a series resonant RLC circuit given by,

$$\left|\frac{V_o'}{V_i}\right|=\frac{A_0 s\frac{R}{L}}{s^2+\frac{R}{L}s+\frac{1}{LC}} \quad \ldots\ldots (6)$$

Comparing (5) and (6), we get, $R_1C_1=\frac{L}{A_0R}$ ...... (7) (where A_0 is the centre frequency gain).

$$\frac{R_3C_1C_2}{C_1+C_2}=\frac{L}{R} \quad \ldots\ldots (8)$$

$$\frac{R_1R_2R_3C_1C_2}{R_1+R_2}=LC \quad \ldots\ldots (9)$$

$$\frac{V_o}{R_6} + \frac{V_i}{R_4} + \frac{V_o'}{R_5} = 0 \quad \ldots\ldots (10).$$

$$\Rightarrow V_o = -V_i R_6 \left(\frac{1}{R_4} + \frac{T(s)}{R_5}\right), \text{ where } T(s) = \frac{V_o'}{V_i} \quad \ldots (11).$$

The minimum output V_o occurs (for band reject behavior) when $T(s) = -\frac{R_5}{R_4}$. Let this frequency at which V_o is minimum be ω_o.

But at ω_o, $T(s)$ must be $-A_o$, where A_o is the centre frequency gain of band pass section.

Hence, $A_o = \frac{R_5}{R_4}$. ...... (12)

From (7) and (8), we have for $C_1 = C_2$,

$$A_o R_1 C_1 = \frac{R_3 C_1}{2}.$$

$$\Rightarrow A_o = \frac{R_3}{2R_1} \quad \ldots (13)$$

Hence we have, (from (12) and (13)), $\frac{R_3}{2R_1} = \frac{R_5}{R_4}$. (Proved)

4. The amplitude of the input sinusoidal signal is $V_m = \sqrt{2} \times 7.5\,V = 10.61V$.

With no filter capacitor, $V_{DC} = \frac{2V_m}{\pi} - 2V_\gamma = 5.358V$

If filtering capacitor is used, ripple voltage $V_R = \frac{V_m - 2V_\gamma}{2fR_LC} = \frac{(V_m - 2V_\gamma) I_{LAV}}{2(V_m - 2V_\gamma - V_R/2)fC}$.

Solving for V_R, we have $V_R = 1.987V$.

Hence $V_{DC} = V_m - 2V_\gamma - \frac{V_R}{2} = 8.22V$.

$$\theta_o = \sin^{-1}(1 - V_R/V_m) = 0.9488 \text{ rad}.$$

$$\therefore I_{DP} = I_{LAV} + \omega C V_m \cos\theta_o = 0.12A.$$

Ans