Hints and Solutions to

Final Semester Examination 2012

VLSI Architectures

Temp 207

1. Output voltage of the phase detector, $V_{pd} = K_m K_{in} V_{osc} = K_m E_{in} E_{osc} \sin(\omega t)\cos(\omega t - \phi_d)$.

$$= \frac{K_m E_{in} E_{osc}}{2}\left[\sin\phi_d + \sin(2\omega t - \phi_d)\right]$$

Hence, $V_{cntl} = K_{lp} K_m \frac{E_{in} E_{osc}}{2} \sin(\phi_d)$.

For small ϕ_d, we have $\sin\phi_d \approx \phi_d$.

Hence, $V_{cntl} = K_{lp} K_m \frac{E_{in} E_{osc}}{2} \phi_d$ ..... (1)

Now, for the VCO, $\omega_{osc} = K_{osc} V_{cntl} + \omega_{fr}$

$\Rightarrow V_{cntl} = \frac{\omega - \omega_{fr}}{K_{osc}}$ [$\omega_{osc} \equiv \omega$ as given] ..... (2)

Hence, combining (1) and (2), we have, $\frac{\omega - \omega_{fr}}{K_{osc}} = K_{lp} K_m \frac{E_{in} E_{osc}}{2} \phi_d$.

$\Rightarrow \phi_d = \frac{2(\omega - \omega_{fr})}{K_{lp} K_m K_{osc} E_{in} E_{osc}}$ (Proved).

$$V_{cntl}(s) = K_{lp} K_m \frac{E_{in} E_{osc}}{2} H_{lp}(s)\left[\phi_{in}(s) - \phi_{osc}(s)\right] \quad \ldots\ldots (3)$$

$$\text{and } \phi_{osc}(s) = \frac{K_{osc} V_{cntl}(s)}{s} \quad \ldots\ldots (4)$$

Combining (3) and (4), we have, $\frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{s K_{pd} K_{lp} H_{lp}(s)}{s + K_{pd} K_{lp} K_{osc} H_{lp}(s)}$.

Putting the value of $H_{lp}(s)$, we get,

$$H(s) = \frac{\frac{1}{K_{osc}} s(1 + s\tau_2)}{1 + s\left(\frac{1}{K_{pd} K_{lp} K_{osc}} + \tau_2\right) + \frac{s^2 \tau_p}{K_{pd} K_{lp} K_{osc}}}, \text{ where } K_{pd} = \frac{E_{in} E_{osc}}{2} K_m$$

Now, $\omega_{in}(s) = s\phi_{in}(s)$

Hence, $\frac{V_{cntl}(s)}{\omega(s)} = \frac{\frac{1 + s\tau_2}{K_{osc}}}{1 + s\left(\frac{2}{K_{lp} K_m E_{in} E_{ose} K_{osc}} + \tau_2\right) + s^2 \tau_p \left(\frac{2}{K_{lp} K_m E_{in} E_{ose} K_{osc}}\right)}$.

(Proved)

2. (i) Procedure: Modified_Kernighan_Lin (G)

begin
loop: set p ← p;
partition G into p groups; $V_1, V_2, \ldots, V_p$ such that $|V_i| = |V_{i-1} \pm 1|$.
apply for $i = 1$ to $\frac{n}{2}$ (where n is the maximum number of vertices in a partition)

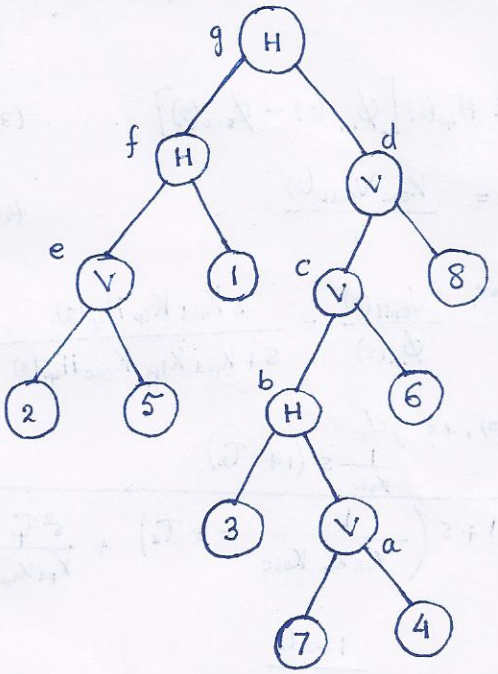
begin

find a pair of unlocked vertices into two partitions V_a and V_b such that their exchange make the largest decrease in cut cost;
lock the vertices;
compute the gain in partitioning;
next i;
set p ← p+1 if p < M;
goto loop until gain ≤ 0;

end procedure.

Now compute the space and time complexities.

(ii)



(The nodes that are internal are annotated as a to g).

To compute minimum area of sliceable floorplan,

(i) Visit node a: vertical merging of (1,2) and (3,5) results in $(1+3, \max\{2,5\}) = (4,5)$.
(ii) Visit node b: horizontal merging of (3,3) and (4,5) results in $(\max\{3,4\}, 3+5) = (4,8)$
(iii) Visit node c: vertical merging of (4,8) and (5,3) results in (9,8)
(iv) Visit node d: vertical merging of (9,8) and (2,4) results in (11,8)
(v) Visit node e: vertical merging of (1,3) and (3,2) results in (4,3).

3. (a) To equalize the delays, the PMOS devices would have to be approximately 2.4 times larger than the 4λ NMOS device. Therefore, the PMOS device size is approximately 10λ. The total capacitance at each output is 4.2fF.

The delay of the chain is simply four times the delay of each stage:

$$\tau_{total} = 4 t_{PHL} = 4 R_{eff} C_{load} = 4 (12.5\,k\Omega) \left(\frac{2}{4}\right) (4.2fF) \approx 105ps.$$

(b) We write the delay equation as:

$$D = \sum RC$$

$$= (R_P)(C_g + C_{eff})(W_P + W_N) + (R_N)(C_g + C_{eff})(W_P + W_N)$$

$$= \left(\frac{30 L_P}{W_P} + \frac{12.5 L_N}{W_N}\right)(C_g + C_{eff})(W_P + W_N)$$

$$= \left(\frac{30(2\lambda)}{W_P} + \frac{12.5(2\lambda)}{4\lambda}\right)(2+1)(W_P + 4\lambda)$$

$$= \left(\frac{60\lambda}{W_P} + \frac{25\lambda}{4\lambda}\right)(2+1)(W_P + 4\lambda)$$

$$= \left(180\lambda + \frac{720\lambda^2}{W_P}\right) + \frac{75}{4}(W_P + 4\lambda)$$

For minimum delay, $\frac{\partial D}{\partial W_P} = 0$

$$\Rightarrow -\frac{720\lambda^2}{W_P^2} + \frac{75}{4} = 0$$

$$\Rightarrow W_P = 2\lambda\sqrt{\frac{720}{75}} = 6.2\lambda.$$

$C_{load} = 2+1 = 3fF.$

Rise delay is given by $t_{PLH} = R_{eff} C_{load} = (30\,k\Omega)\left(\frac{2}{6}\right)(3fF) = 30ps.$

Similarly fall delay is given by, $t_{PHL} = R_{eff} C_{load} = (12.5\,k\Omega)\left(\frac{2}{4}\right)(3fF) \approx 18.8ps$

Hence total delay is, $\tau_{total} = 2(t_{PLH} + t_{PHL}) = 2(30 + 18.8)ps = 97.6ps.$

4. Average current consumption of the circuit's core $= f_{clk} V_{dd} (1+\sigma) \sum_{K=1}^{K} \frac{\alpha_K}{2} C_K = 100 \times 1.2 (1+0.2) 100000 \frac{1}{4} 18\,mA \approx 32\,mA.$

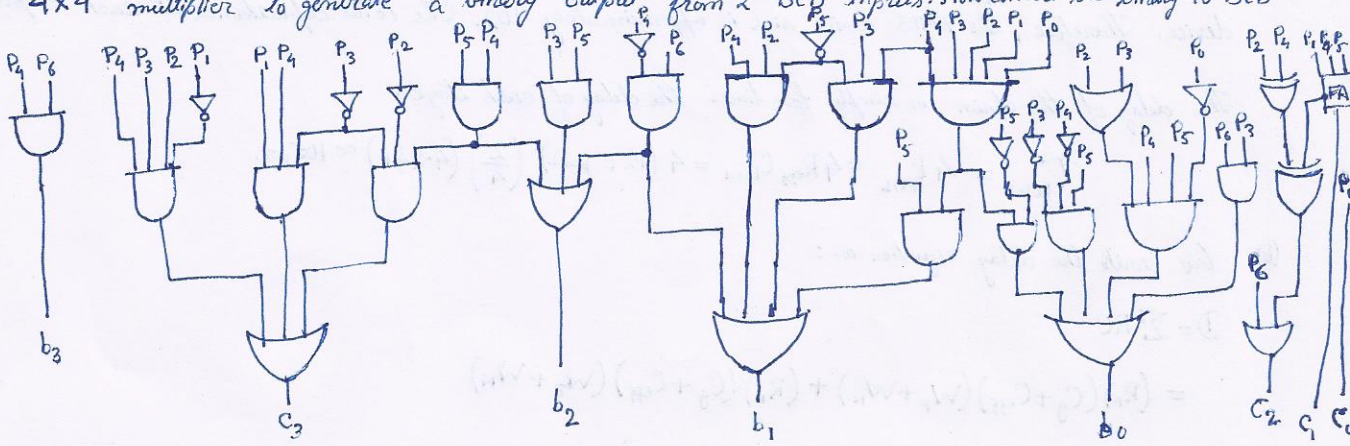
Total energy dissipated per computation cycle, $E_{cp} = V_{dd}^2 (1+\sigma) \sum_{K=1}^{K} \frac{\alpha_{K\,on\text{-}chip}}{2} C_{K\,on\text{-}chip} + V_{dd}^2 (1+\sigma) \sum_{K=1}^{K} \frac{\alpha_{K\,off\text{-}chip}}{2} C_{K\,off\text{-}chip}$

$$+ T_{cp}\left(V_{dd}^2 \sum_{K=1}^{K} \frac{\delta_{K\,off\,chip}}{R_{K\,off\,chip}} + V_{dd} \frac{\Delta I_{ds\,off}}{\Delta W} \sum_{g=1}^{G} W_g\right)$$

$$= (1.2)^2 (1+0.2) \sum_{K=1}^{100000} \frac{1}{2} \frac{1}{4} 18 + (2.5)^2 (1+0.2) \sum_{K=1}^{16} \frac{1}{2} \frac{1}{4} 25 + 10\left((2.5)^2 \sum_{K=1}^{16} \frac{1}{2} \frac{1}{3 \times 10^3} + 1.2 \cdot 80 \times \frac{10^{-9}}{10^{-6}} \sum_{g=1}^{50000} 1\right) \approx 0.96nJ.$$

Overall power consumption, $P = f_{cp} E_{cp} \approx 100\,MHz \cdot 0.96nJ = 96mW.$

5. Use a 4x4 multiplier to generate a binary output from 2 BCD inputs. Now convert the binary to BCD



The BCD output is $b_3 b_2 b_1 b_0\ C_3 C_2 C_1 C_0$.

6.

A. i, ii, iv

B. ii

C. ii, iii, iv

D. i, ii, iii, iv

E. ii, iii

F. i, iii

G. i, iii

H. i, ii, iii

I. ii, iv

J. ii, iv