Timing Models

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When we study the design of logic circuits and understand their behavior by looking at their timing diagrams, we take an idealized view of things. We treat each circuit component as a mathematical object with well-defined behavioral model as given by its truth table. We also have a well-defined model for interconnections between various circuit components. For example refer the Timing Diagram for the positive edge triggered D-FlipFlop in the Figure 1.

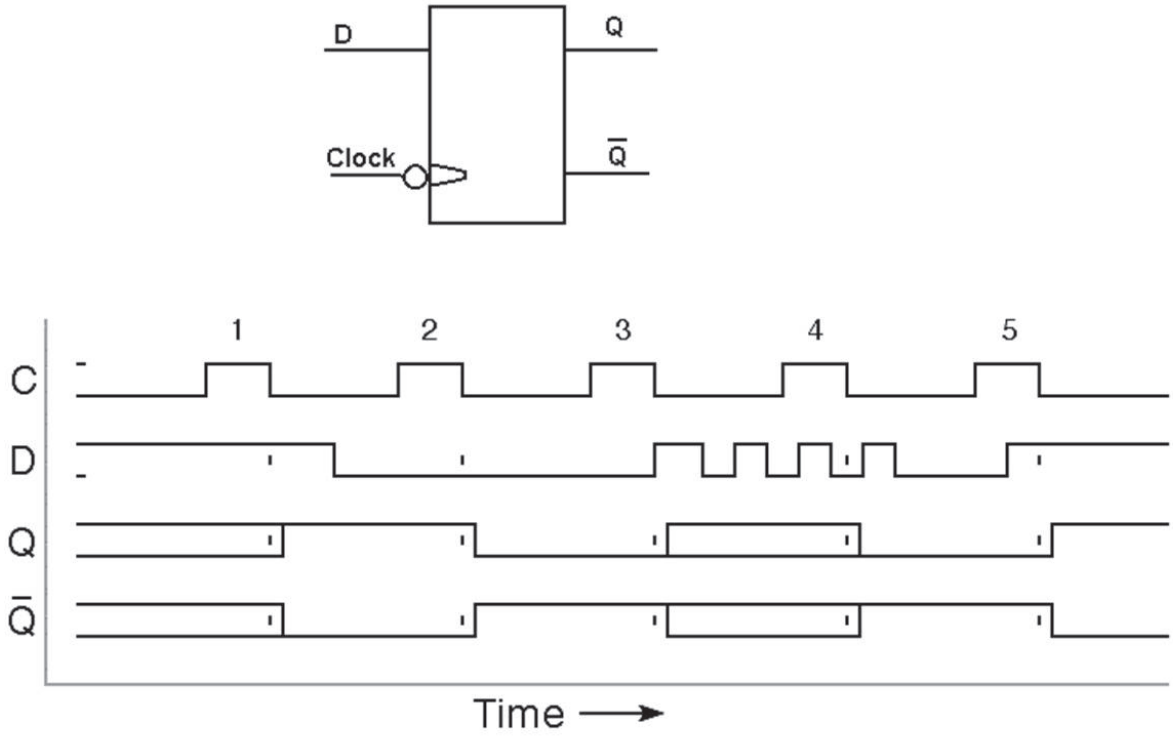

Figure 1: Timing Diagram for an Ideal Negative Edge Triggered D-Flip Flop

At the falling clock edge of the Clock Pulse 1, the D-Flip Flop input is equal to 1 and the D-Flip Flop reads the value and the output Q changes from 0 to 1 instantaneously. But that is not how it happens in any physical realization of the D-Flip Flop as against its mathematical model. In any physical realization of the D-flop the output Q will reflect the new value after certain delay. The following are three important characteristic parameters of the circuit components which are technology dependent (refer Figure 2).

1. **Set Up Time:** Setup time (denoted as t_{su}) is the minimum amount of time the data signal

should be held steady before the clock event so that the data are reliably sampled by the clock.

2. **Hold Time:** Hold time (denoted as t_h) is the minimum amount of time the data signal should be held steady after the clock event so that the data are reliably sampled.

3. **Clock-to-Q Time:** Clock-to-Q Time (denoted as t_{cq}) is the time it takes for the flip-flop to change its output after the clock edge.

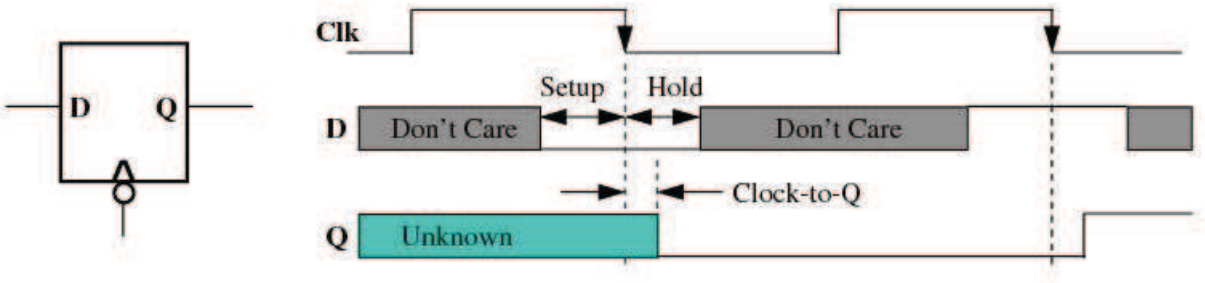

Figure 2: Diagram illustration Setup, Hold and Clock-to-Q Times.

You might wonder whether there is any relationship between the three parameters t_{su}, t_h and t_{cq}. Especially between the parameters t_h and t_{cq}, intuitively we feel there could be a relationship[1] For the sake of our discussion we can safely assume that all the three parameters are independent and their values are dictated by the underlying device physics. We shall now see how we have to factor in these parameters while designing logic circuits. Consider the Figure 3 where the output of the register R_1 is connected to the input of the register R_2 through some combinational logic circuit.

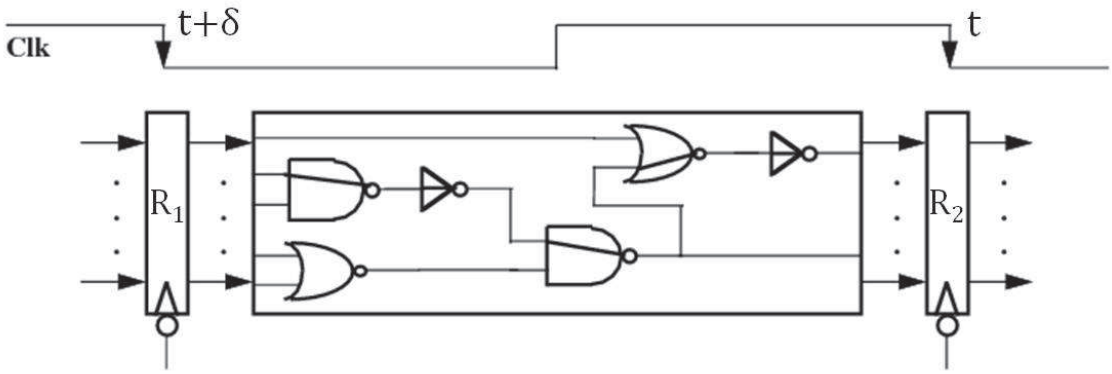

Figure 3: Two registers connected through intermediate combinational logic

At time instant t a falling clock edge arrives at both the registers R_1 and R_2 simultaneously (assuming no clock skew). The registers R_1 and R_2 sample their respective input signals at that falling clock edge and update their states accordingly and the updated state is available on the

[1]I am not aware of any such relation. However I have to double check before I give a definite answer to you all.

output after the Clock-2-Q time which would be at the time instant $t + t_{cq}$. Remember the input signals to the registers R_1 and R_2 should be stable during the interval $[t - t_{su}, t + t_h]$ for the proper update of the registers. Now let us focus on how the signals flow between the registers R_1 and R_2 alone. The updated output signals of the register R_1 which are available at the time instant $t + t_{cq}$ flow through the combination logic and reach the input of the register R_2. The combinational logic would induce some delay before the input signals to the register R_2 gets stabilized. This delay value is equal to the sum of the logic gate delays along the longest path through the combinational logic. This longest path is also called as the critical path. Let t_{cl} be the delay along this critical path. So the new input signals to the register R_2 will be available by the time instant $t + t_{cq} + t_{cl}$. It is important to note that during the time interval $[t + t_{cq}, t + t_{cq} + t_{cl}]$, the input signals to the register R_2 may oscillate (why?).

We expect that the newly available input signals to be latched onto the register R_2 at the next falling clock edge which arrives at the time instant $t + \delta$ where δ is the clock cycle length. If we factor in the setup time requirements for the proper update of the register R_2, we will get the following necessary condition on the clock cycle time.

$$\begin{aligned} t + t_{cq} + t_{cl} + t_{su} &\leq t + \delta \\ \delta &\geq t_{cq} + t_{cl} + t_{su} \end{aligned}$$

If the above condition is not satisfied, then we say there is a **setup time violation**. In general if t_{cl}^{ij} is the critical path length in the combinational logic connecting two registers R_i and R_j, then the following condition has to be satisfied.

$$\delta \geq t_{cq} + t_{cl}^{ij} + t_{su}$$

Assuming that the Clock-to-Q and setup times are same for all the registers, the clock cycle length is governed by the largest crictical path length. For example if the largest critical path correponds to the combinational logic between two registers R_m and R_n then we can choose the clock cycle length as $\delta = t_{cq} + t_{cl}^{mn} + t_{su}$.

There is another interesting problem that we can face during logic circuit design. Let us consider a path in the combinational logic circuit connecting the registers R_1 and R_2. Let t_p be the delay along this path. So after the falling clock edge occuring at time instant t, a signal can reach the input of the register R_2 by time $t + t_{cq} + t_p$. If it turns out that $t + t_{cq} + t_p \in [t - t_{su}, t + t_h]$ then the new signal value will over write the old input signals to register R_2 causing an instability of the input. We call this as **hold time violation**. To prevent hold time violation we need to make sure that for every path in the combinational logic circuit with delay t_p the following condition is true.

$$t + t_{cq} + t_p > t + t_h$$

If there is a path in the combinational circuit which does not satisfy the aforementioned condition, then the delay along the path has to be increased by adding buffer elements.

In the previous discussion we assumed that a following clock edge arrives at both the registers exactly at the same time instant. However in practice due to wire delays arising out of wire resistance and other physical characteristics of the wires, the same falling clock edge could reach different registers at different time instants (refer Figure 4). Let t_{cs} be the clock skew. Due to the clock skew the falling clock edge which is arriving at register R_2 at time instant t would now arrive at time instant $t + t_{cs}$. However it can so happen that during this time interval $[t, t + t_{cs}]$, along some path in the combination logic the new signal would flow and overwrite the old input signal to the register R_2. This can happen if

$$t + t_{cq} + t_p \leq t + t_{cs} + t_h$$

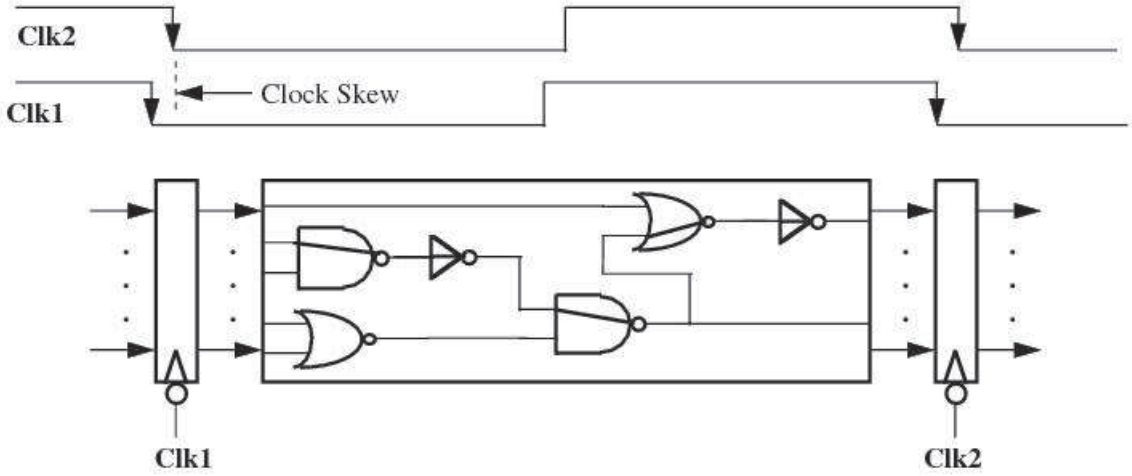

Figure 4: Clock skew due to clock signal propagation delays

where t_p is delay along the combination logic path under consideration. Refer to the Figures 5 and 6 which illustrate this problem.

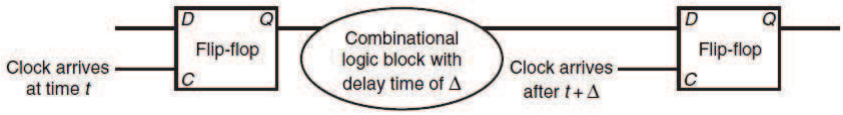

Figure 5: Potential problems due to clock skew

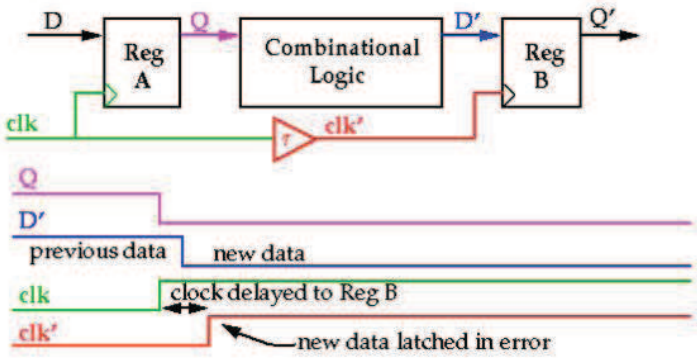

Figure 6: Potential problems due to clock skew