Temp 207

VLSI Architectures
Final Semester Examination
Spring 2012

Maximum Marks: 100 **Time Allowed: 180 minutes**

General Instructions:

a. There are six questions in this question paper. Attempt **ALL** questions
b. Figures in the right margin indicate marks for each question.
c. Answer in your own words as far as practicable.
d. Reasons are to be stated in support of your answers (except objective type questions). *No credit will be given to answers which are mere assertions*.
e. Use of laptops, mobile phones, pagers or any other electronic communication devices is strictly prohibited inside the examination hall.
f. Use of non programmable calculators is permitted.
g. Books may be opened at the time of the examination.
h. If any assumption is made at any step they have to be clearly stated.

::::::::BEST OF LUCK::::::::

1. Consider the usual design of a phase locked loop (PLL) used for generating precision sinusoidal oscillations. The loop consists of a phase detector, a loop filter, an amplifier and a voltage controlled oscillator (VCO). Let the input signal to the PLL be described by the sinusoid $V_{in} = E_{in} \sin \omega t$ and the output of the VCO is given by $V_{OSC} = E_{OSC} \cos(\omega t - \phi_d)$, where ϕ_d represents the difference between the input signal and the output of the oscillator. Let K_M be the multiplication constant of the phase detector. The loop filter is a first order low pass filter given by the transfer function $H_{lp}(s) = \dfrac{1 + s\tau_z}{1 + s\tau_p}$, where $\tau_z << \tau_p$. Let the gain of the amplifier be K_{lp}. Ignore any harmonic distortion of the amplifier. Let ω_{fr} be the free running frequency of the VCO and K_{OSC} be a constant relating the change in frequency to control voltage ratio. Prove that for small values of ϕ_d, we have $\phi_d = \dfrac{2(\omega - \omega_{fr})}{(K_{lp} K_M E_{in} E_{OSC} K_{OSC})}$. Hence prove that the control voltage V_{cntl} given as input to the VCO is related to the input frequency by $\dfrac{V_{cntl}(s)}{\omega(s)} = \dfrac{\dfrac{1 + s\tau_Z}{K_{OSC}}}{1 + s\left(\dfrac{2}{K_{lp} K_M E_{in} E_{OSC} K_{OSC}} + \tau_Z\right) + s^2 \tau_p \left(\dfrac{2}{K_{lp} K_M E_{in} E_{OSC} K_{OSC}}\right)}$. 7+8=15

2. (i) Consider the usual Kernighan Lin algorithm for circuit partitioning. Suppose the algorithm is modified to iteratively partition a graph representation of a circuit in the following way. The algorithm starts with 2-way partitioning at the initial stages of iteration and gradually increases linearly to a maximum value of m-way partitioning finally, where m is a finite number and m>2. Write the modified algorithm in pseudo-code. Suggest how the modification is going to affect the space complexity and time complexity of the algorithm.

   (ii) Consider the Polish expression $PE_1 = 25V1H374VH6V8VH$. The (*width, height*) of modules 1 through 8 are $\{(2,4),(1,3),(3,3),(3,5),(3,2),(5,3),(1,2),(2,4)\}$. Draw the slicing tree for the given Polish expression. Obtain the minimum area of the sliceable floor-plan. (4+4+4)+(4+4)=20

3. Consider a chain of four CMOS inverters connected as shown in figure 1. Inverter sizing can be performed to equalize rise/fall delays or to minimize the propagation delay. Assuming that the NMOS devices are all 4λ, size the PMOs devices with the following objectives one at a time:
   (a) equalize the rise and fall delays
   (b) minimize the delay through the chain.
   Compute the total delay of propagation of signal through the chain of inverters in both the cases.
   Assume that the effective resistance of an NMOS transistor is 12.5kΩ/□ and that of a PMOS transistor is 30kΩ/□. The average gate capacitance is 2fF/μm and the effective capacitance per unit width is 1fF/μm. 7+8=15

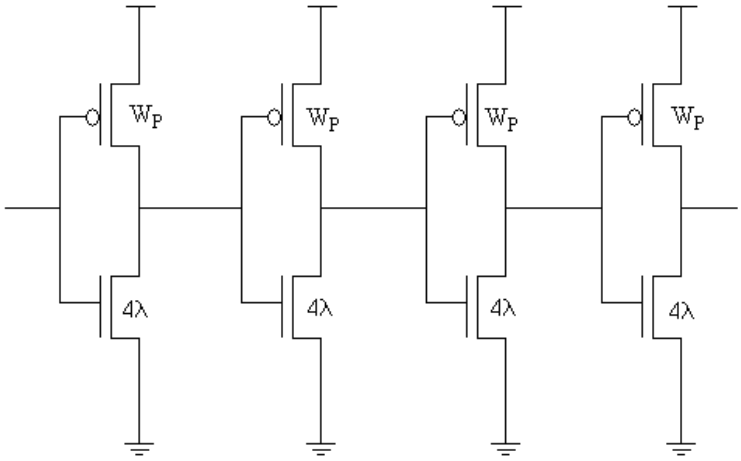

Figure 1

4. Consider a CMOS IC of modest size, say of 50000 gate equivalents to be manufactured in a 130nm technology, operated at 1.2V and driven from a 100MHz single edge triggered one phase clock. Overall node activity is $\alpha = \frac{1}{4}$, which means that the average node charges and discharges within eight clock cycles. Let each of the 100000 internal

nodes have a capacitance of 18fF. The circuit is to drive 16 off chip loads of 25pF and 3.3KΩ each that toggle at the same rate as the core nodes do. These 2.5V outputs equally share their time between the "on" and "off" conditions. Assume 20% of the energy being spent for charging and discharging the parasitic load capacitance is actually being spent towards short circuit power dissipation. Further assume that the MOSFET off-state current is on the order of 80nA/μm at 70^0C junction temperature.

(i) Compute the average current consumption of the circuit's core.
(ii) How much energy is being dissipated per computation cycle?
(iii) What is the overall power consumption? 5+7+3=15

5. Design a logic circuit to multiply two single digit BCD numbers and the result should also be in BCD. 15

6. In the following set of multiple choice type questions one or more than options is(are) correct. Choose the correct alternative(s). Marks will be awarded for each question if and only if all the correct alternatives are chosen. 10X2=20

A. Meta-stability becomes a threat to system reliability when
i. Synchronizers are operated close to their maximum clock frequency
ii. Synchronizers are operated close to their maximum data frequency
iii. Synchronizers are involved in large quantities
iv. Clock signal involves a considerable amount of phase noise

B. In a multi-driver bus it is preferable to use
i. Microprogrammed control and centralized bus control
ii. Hardwired control and centralized bus control
iii. Hardwired control and distributed bus control
iv. Microprogrammed control and distributed bus control

C. Downscaled fabrication processes
i. Reduce stringency of process corners
ii. Reduce parasitic capacitances
iii. Reduce supply voltages
iv. Reduce static leakage current

D. When layout design of a circuit is transferred on to a silicon wafer the possible problems can be:
i. Wave diffraction
ii. Proximity effects
iii. Reflections from underlying layers
iv. Misalignments of photomasks

E. Input pads in a chip are protected from electrostatic discharges by
i. T-section network at the input end

ii. ∏-section network at the input end
iii. Decoupling resistors
iv. Inductive coupling

F. Guard rings are provided in a chip to
i. Absorb stray currents
ii. Attract majority carriers
iii. Attract minority carriers
iv. Protect against electrostatic discharges

G. Redundant logic in a chip can create problems with
i. Controllability
ii. Observability
iii. Testability
iv. Manufacturability

H. Instability can develop in Mealy machine if
i. Surrounding logic provides immediate feedback from output to input of same machine
ii. One or more output bits of a through path feedback to one or more input bits of the same through path
iii. Redundancy is there in the state encoding
iv. Input capacitances of the logic gates are too high

I. Which of the following is (are) true about electro-migration?
i. It is a short term wear out process
ii. It is a long term wear out process
iii. It is analogous to fusing in household wiring
iv. It can be reduced when a wire is made narrower than the average grain size in the conduction material.

J. In synchronous RAMs
i. Both read and write operations are always timed on the active edge of the clock signal
ii. Write operations are timed but read operations may or may not be timed
iii. Read operations are timed but write operations may not be timed
iv. Operation resembles like that of a flip flop.