Assignment-3

Adder Architectures

1. Design a 4 bit ripple carry adder using CADENCE Virtuoso Schematic Editor and simulate it using Spectre simulator. Draw the layout using Virtuoso Layout Editor. Estimate the area, power dissipation and delay of the adder.

2. Design a 4 bit carry look ahead adder using CADENCE Virtuoso Schematic Editor and simulate it using Spectre simulator. Draw the layout using Virtuoso Layout Editor. Estimate the area, power dissipation and delay of the adder.

3. In problems 1 and 2, redesign the circuits increasing the width of the adders from 4 bits to 16 bits in steps of 1 bit. Draw the layouts of the circuits and estimate the power dissipation, delay and area of the adders. Prepare a table for your comparison. What conclusions can you draw from the table?

4. Design 16 bit Brent Kung and Kogge-Stone Adders. Draw the layouts of the three adders. Compare the area and performance parameters of these adders with the ripple carry and carry look ahead adders that you already designed. What conclusions can you draw from this?