Memory Devices used in Embedded Systems

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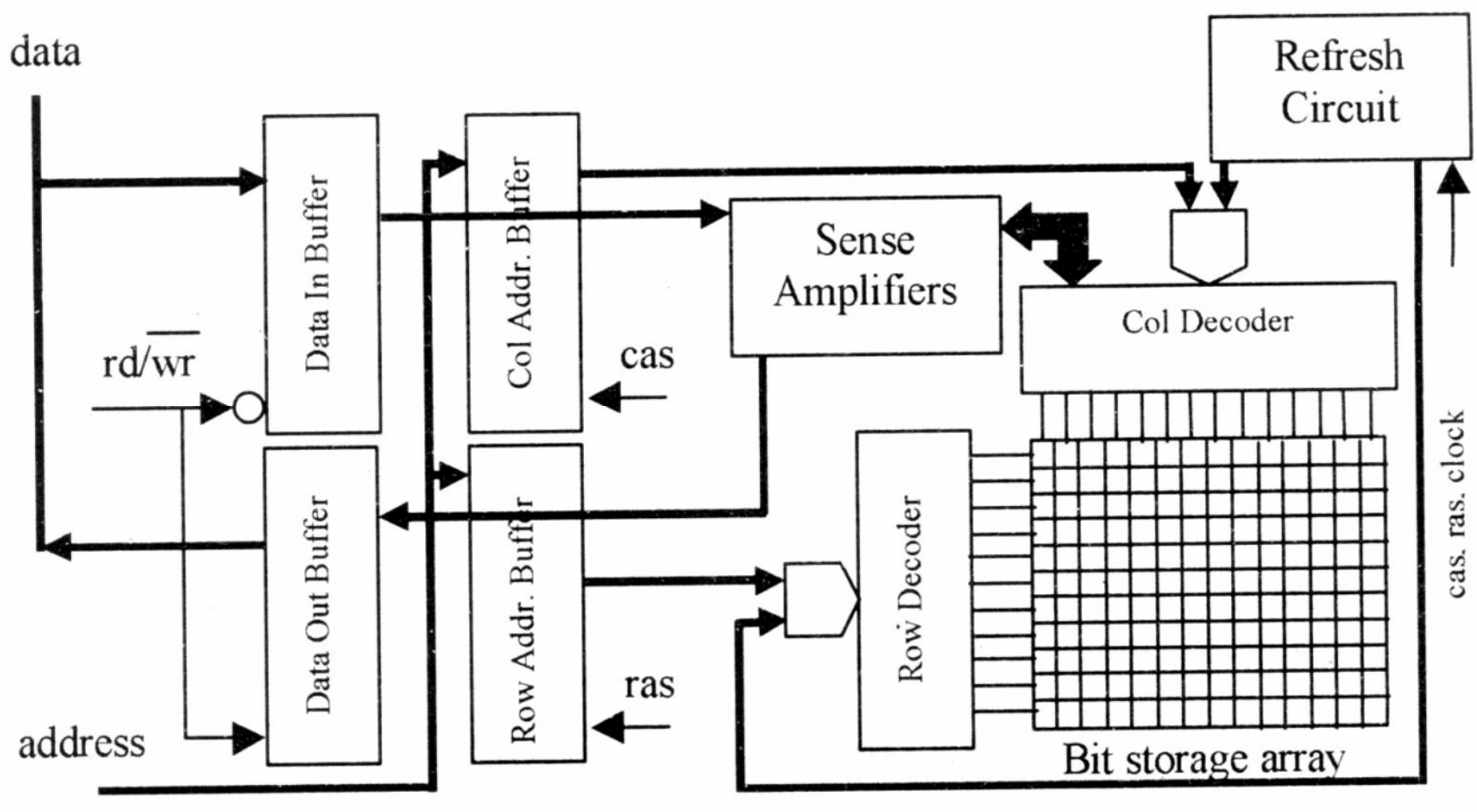
On Memory
- A Different View

- Instead of RAMs and ROMs

- Writability and Data Permanence

Basic DRAM Architecture

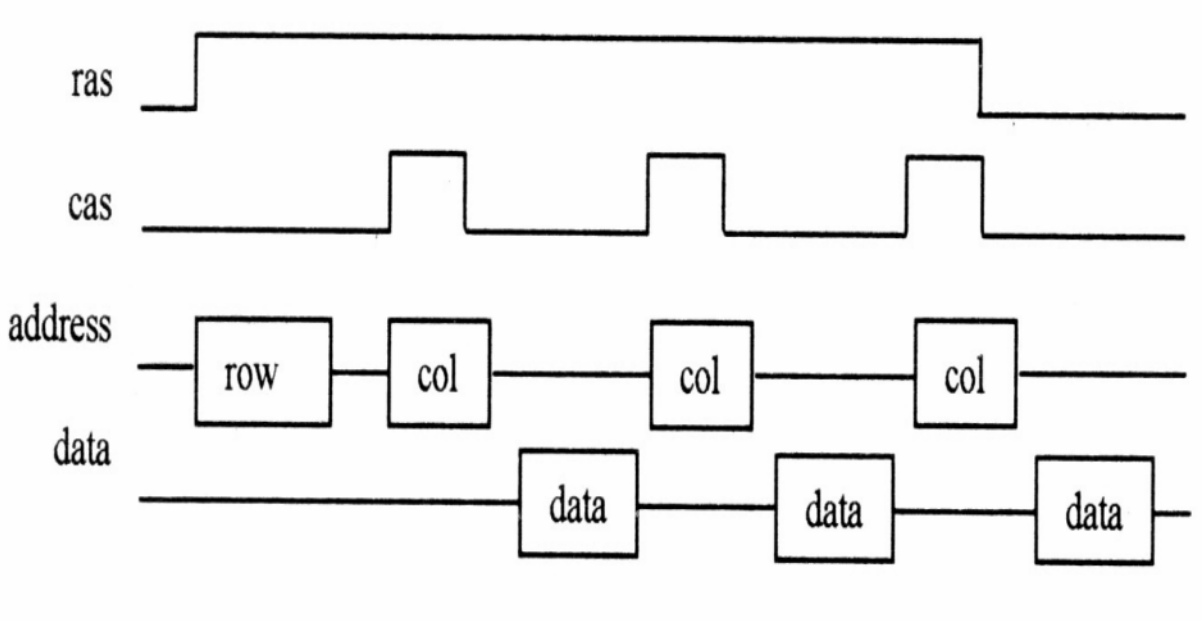


Fast Page Mode DRAM (FP DRAM)

A row is selected and the col. addresses are sequenced. A row is considered a page, consisting of multiple words.

Each word has a sep. col. address.

The sense amplifier buffers a page.

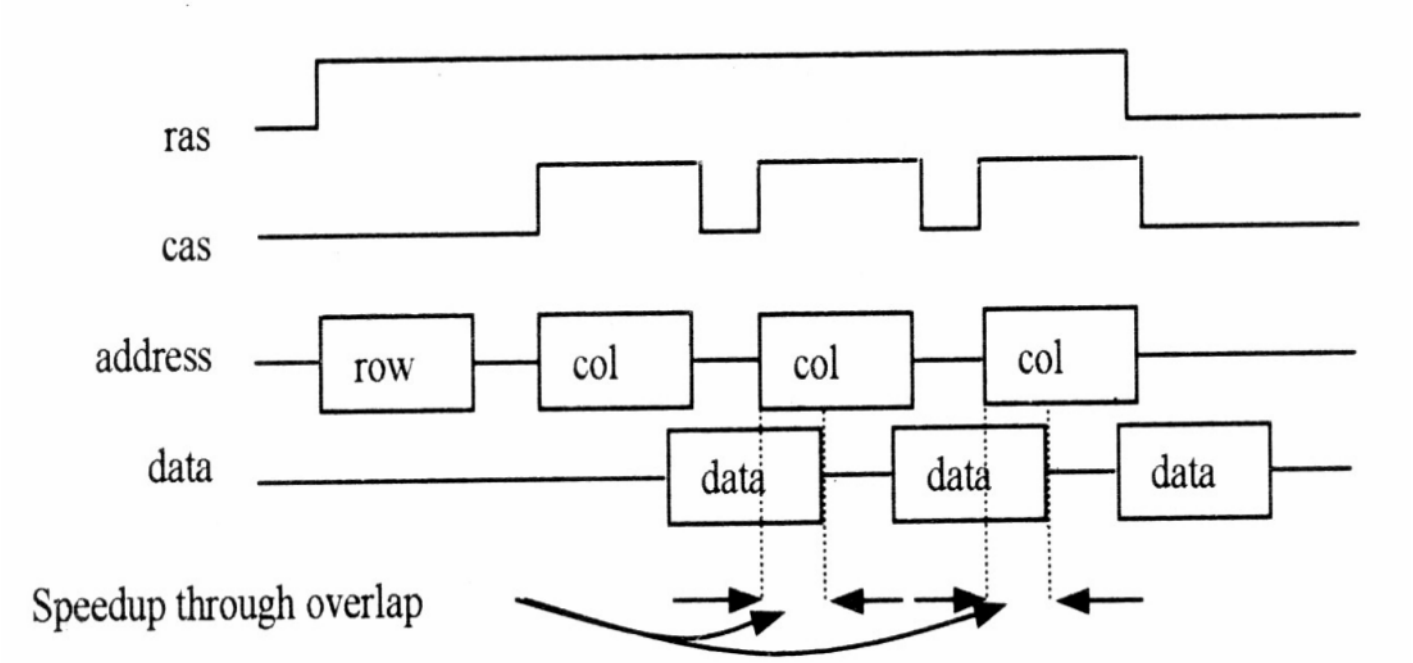


EDO DRAM (Extended Data Out DRAM)

-- Extra output latch between the sense ampl. and output buffer

-- allows overlap bet. Col. Select and previous data out

-- saves one cycle over FP DRAM



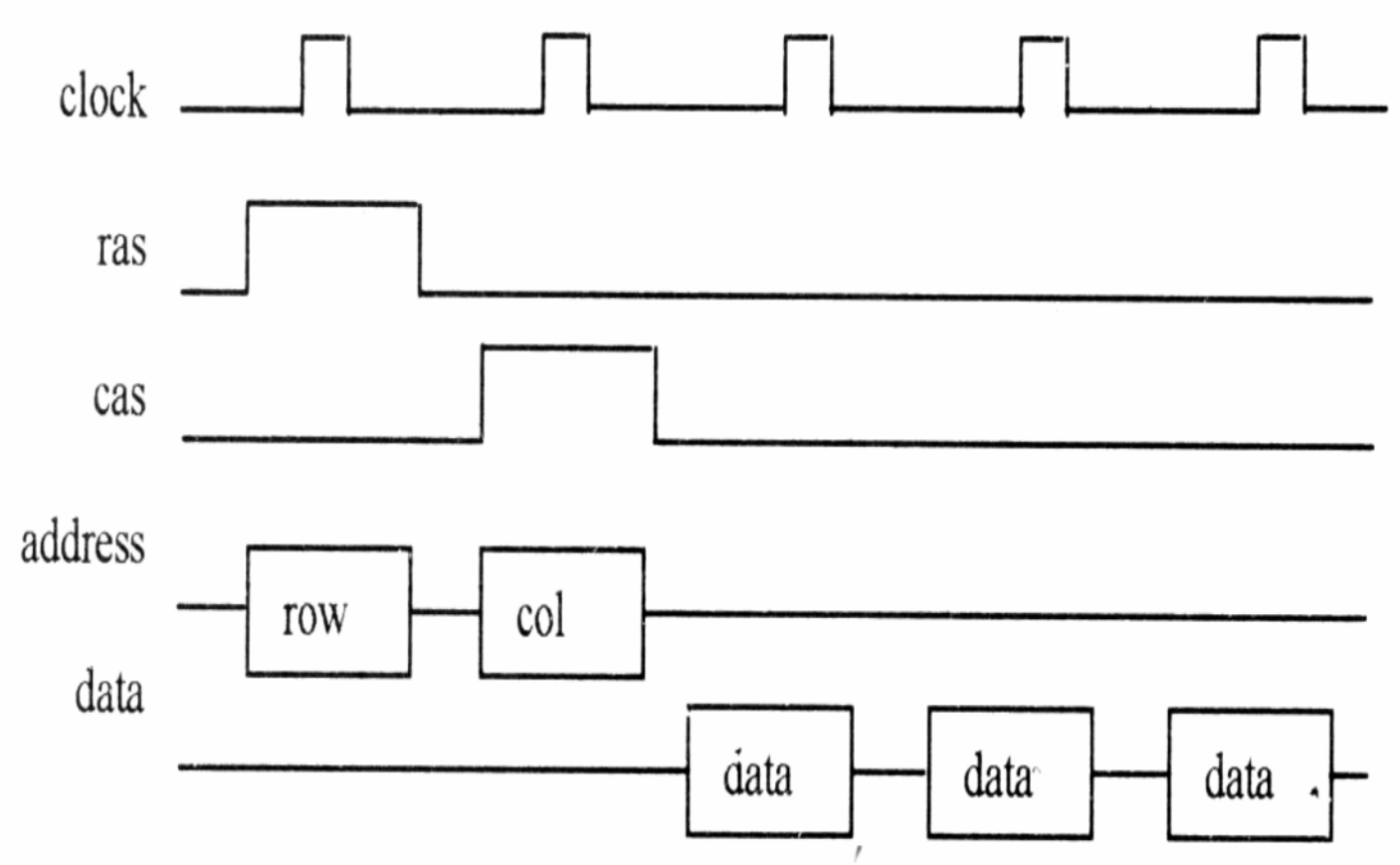
SDRAM

•FPM and EDO RAM controlled asynchronously by the processor or the memory controller.

•A synchronous DRAM interface will eliminate a small amount of time (thus latency) that is needed by the DRAM to detect the ***ras/cas*** and ***rd/wr*** signals. DRAM latches information to and from the controller on the active edge of the clock signal

•In addition to a lower latency I/O, after a proper page and column setup, an SDRAM may store the starting address internally and output new data on each active edge of the clock signal, as long as the requested data are consecutive memory locations. This is accomplished by adding a column address counter to the base DRAM architecture. This counter is seeded with a starting column address strobed in by the processor (or memory controller) and is thereafter incremented internally by the DRAM on each clock cycle.

SDRAM Timing



RDRAM

- RDRAM uses multiplexed address/data lines to connect memory controller to the RDRAM device.
- Data is latched on both rising and falling edge of the clock
- Packet driven data transfer. Address packets are followed by data packets.

DDRRAM

- Double-Data-Rate Synchronous Dynamic Random Access Memory, better known as **DDR SDRAM** or **DDR RAM** for short, is a type of very fast computer memory. DDR RAM is based on the same architecture as SDRAM, but utilizes the *clock signal* differently to transfer twice the data in the same amount of time.

- In a computer system, the clock signal is an oscillating frequency used to coordinate interaction between digital circuits. Simply put, it synchronizes communication. Digital circuits designed to operate on the clock signal may respond at the rising or falling edge of the signal. SDRAM memory chips utilized only the rising edge of the signal to transfer data, while DDR RAM transfers data on both the rising *and* falling edges of the clock signal. Hence, DDR RAM is essentially twice as fast as SDRAM.

DDR2RAM

- **DDR2 SDRAM** is a double data rate synchronous dynamic random access memory interface. It supersedes the original DDR SDRAM specification and the two are not compatible. In addition to double pumping the data bus as in DDR SDRAM (transferring data on the rising and falling edges of the bus clock signal), DDR2 allows higher bus speed and requires lower power by running the internal clock at half the speed of the data bus. The two factors combine to require a total of four data transfers per internal clock cycle.

THANK YOU