VLSI Design

Circuit Characterization

Resistance

- Formula
- Sheet resistance
- Difference between Metal and poly and diff
- Channel resistance
- Non rectangular regions
- Contacts and vias

Capacitance

- Total load on a gate
  - Gate capacitance
  - Diffusion cap.
  - Routing cap.
- MOS Cap.
- Capacitance model
- R and C of interconnects

Delay

- Can be there due to
  - Architectural level
  - Logic level
  - Circuit level
  - Layout level
- In one clock cycle
  - Gate delays, adder speed, multiplier, fetching, propagation etc

Delay

- Delay definitions
- Simulations can help but not help
- Delay can be improved by
  - Comparing blocks which does same fn
  - Fan-in fan-out
  - Poor architecture problem