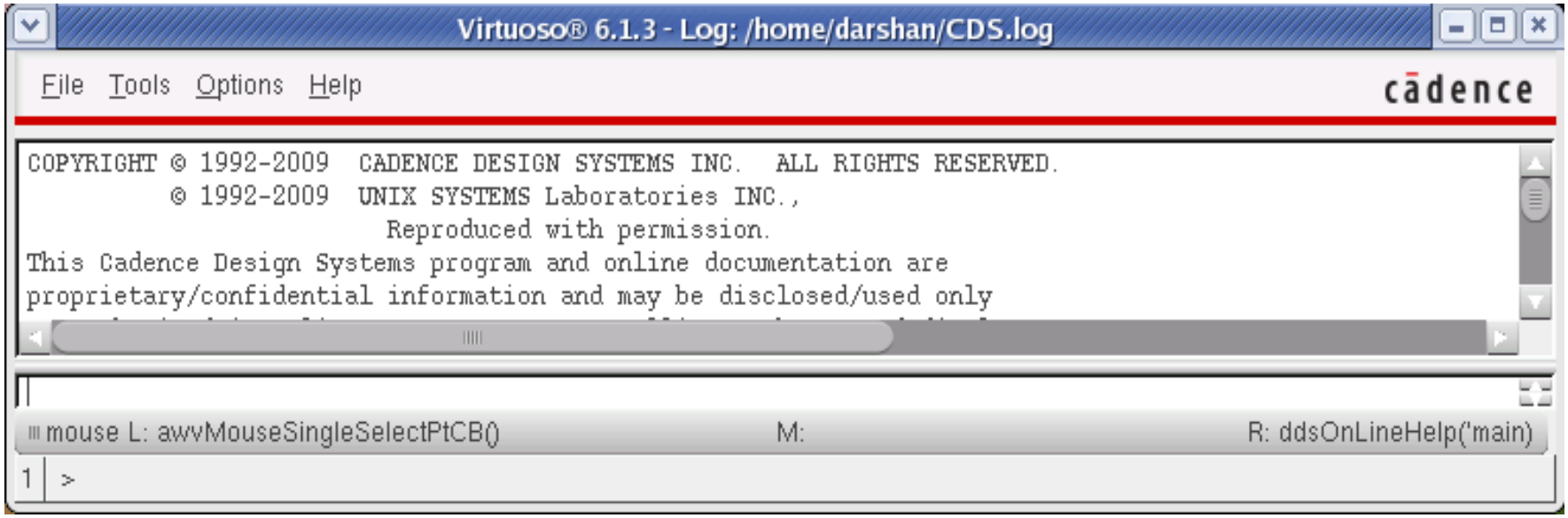
CADENCE TUTORIAL

GETTING STARTED→

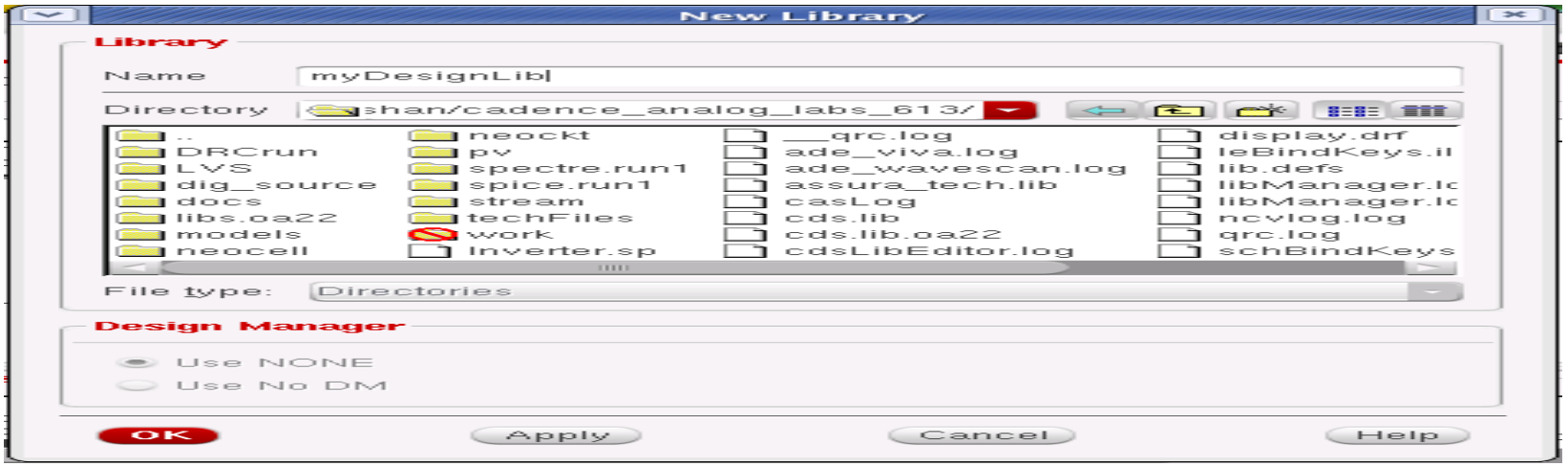
On the terminal after logging in write 3 commands to start cadence virtuoso-

- csh
- source cshrc
- virtuoso

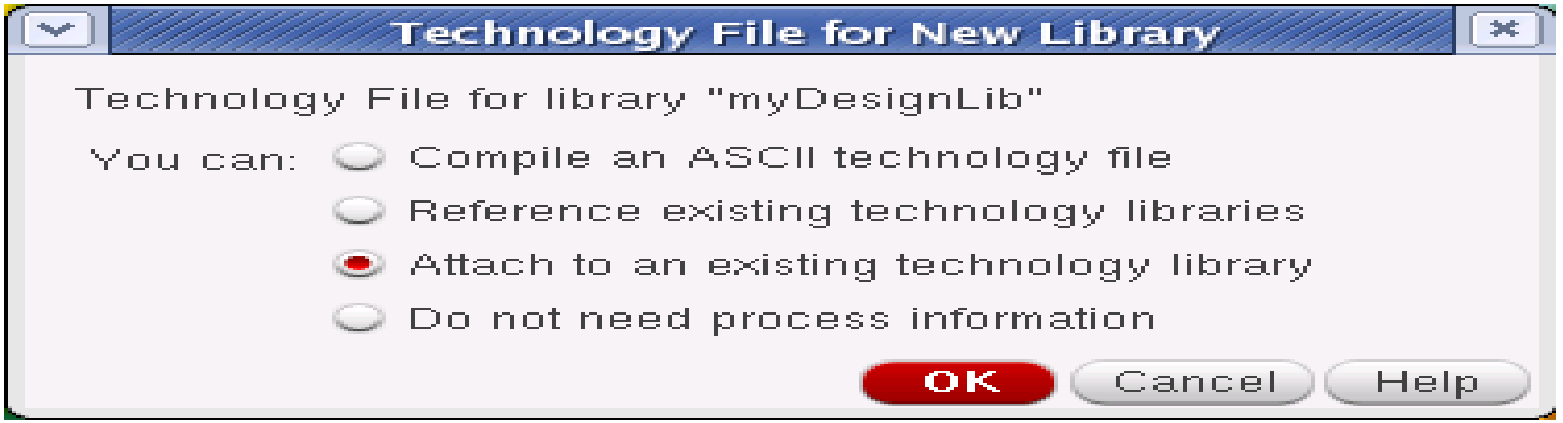


CREATING A NEW LIBRARY

• In the Library Manager, execute **File -> New – Library**. The new library form appears.



• In the “New Library” form, type “**mydesignlib**” in the Name section and click on “Attach to an existing technology library”. Then click OK.



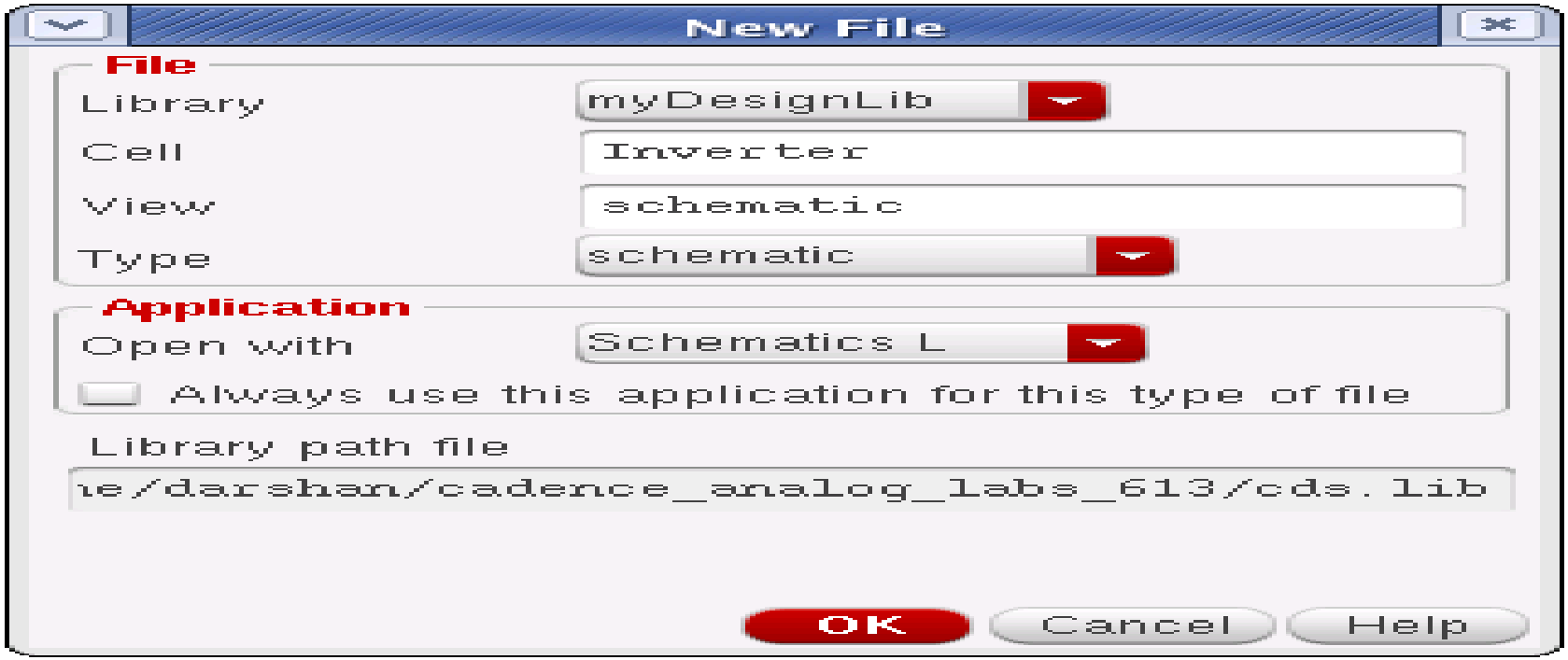
CREATING A NEW LIBRARY (contd..)

•In the the "**Attach Design Library to Technology File**" form, select **gpdk180** from the cyclic field and click **OK**

Creating a Schematic Cellview

•In the Library manager, execute **File – New – Cellview**.

• Set up the New file form as follows:



•. Click **OK** when done the above settings. A blank schematic window for the **Inverter** design appears.

Adding Components to schematic

• In the Inverter schematic window, click the **Instance** fixed menu icon to display the Add Instance form .

• Click on the **Browse** button. This opens up a Library browser from which you can select **components and the symbol view .**

• Now update the Library Name, Cell Name, and the property values as shown.

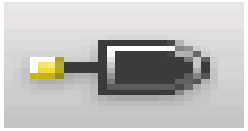
gpdk 180	pmos	For M0: Model name = pmos1, W= 2u, L=180n
gpdk 180	nmos	For M1: Model name = nmos1, W= 2u, L=180n

• After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

• If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters. Use the **Edit— Move** command if you place components in the wrong location.

• After entering components, click **Cancel** in the Add Instance form or press **Esc** with your cursor in the schematic window.

Adding pins to Schematic

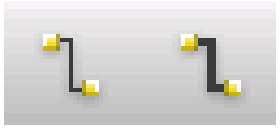
• Click the **Pin** fixed menu icon in the schematic window. 

• Type the following in the Add pin form in the exact order leaving space between the pin names.

PIN NAMES	DIRECTION
Vin	Input
Vout	Output

• Select **Cancel** from the Add – pin form after placing the pins.

Adding wires to Schematic

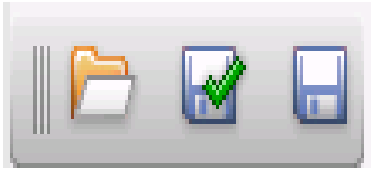
• Click the **Wire (narrow)** icon in the schematic window. 

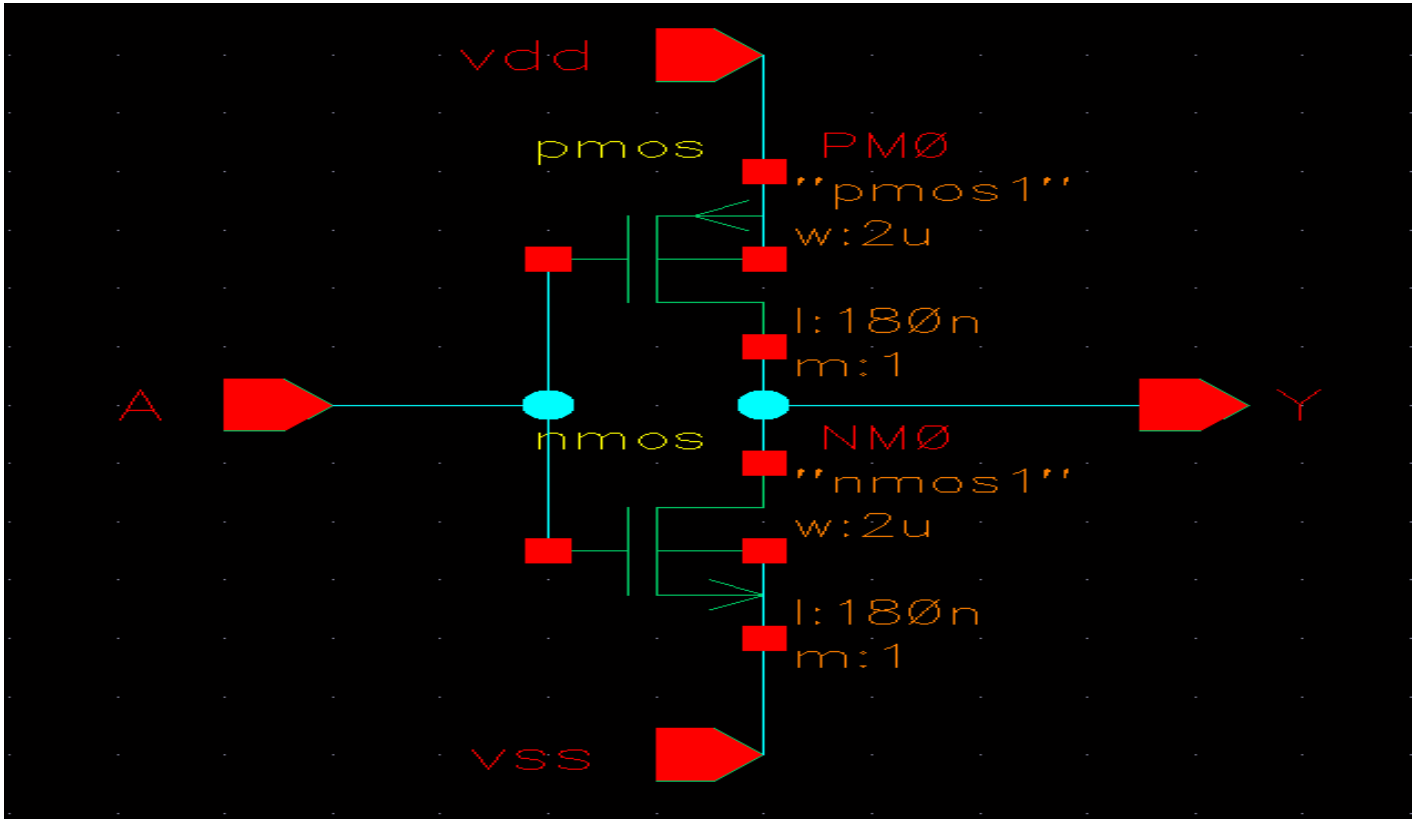
• In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.

• Follow the prompts at the bottom of the design window and click **left** on the destination point for your wire. A wire is routed between the source and destination points

SAVING THE DESIGN

- Click the ***Check and Save*** icon in the schematic editor window.

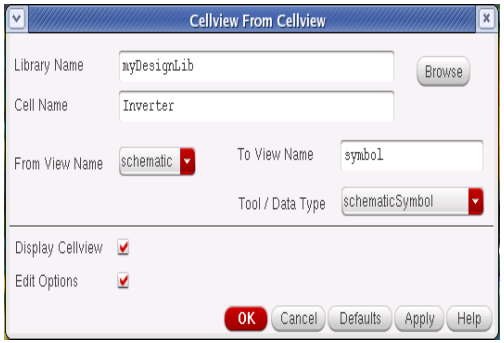




Symbol / Block Creation

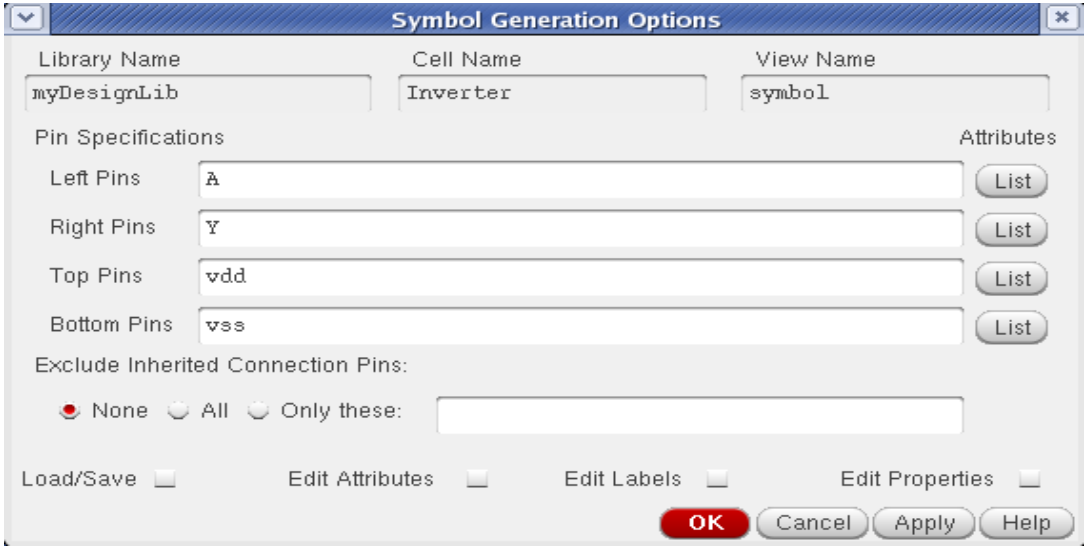
- In the Inverter schematic window, execute **Create — Cellview— From Cellview**

- Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **Schematic Symbol**.



- Click **OK** in the **Cellview From Cellview** form. The Symbol Generation Form appears.

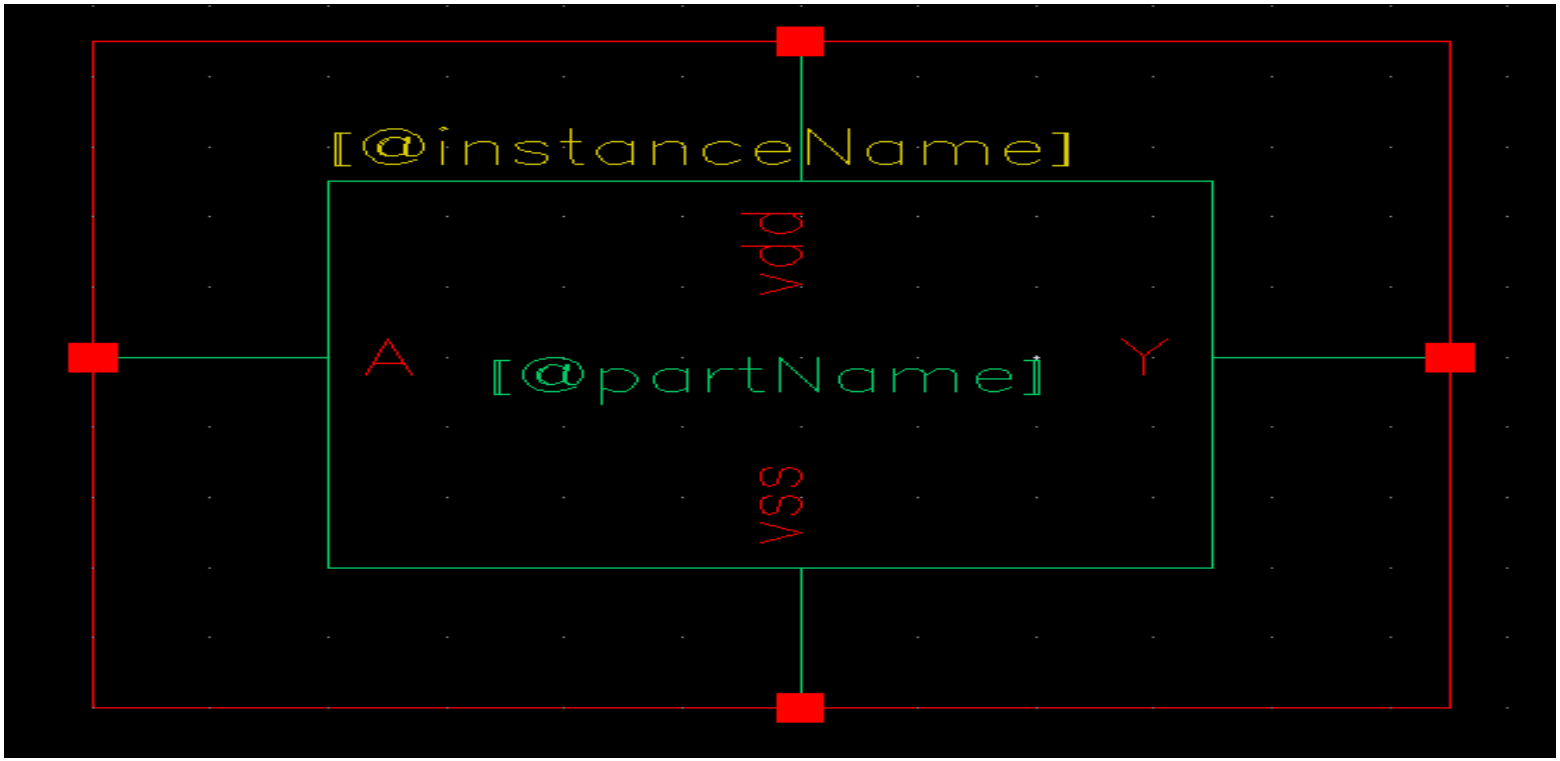
- Modify the **Pin Specifications** as



Symbol / Block Creation (contd..)

- Click **OK** in the Symbol Generation Options form.

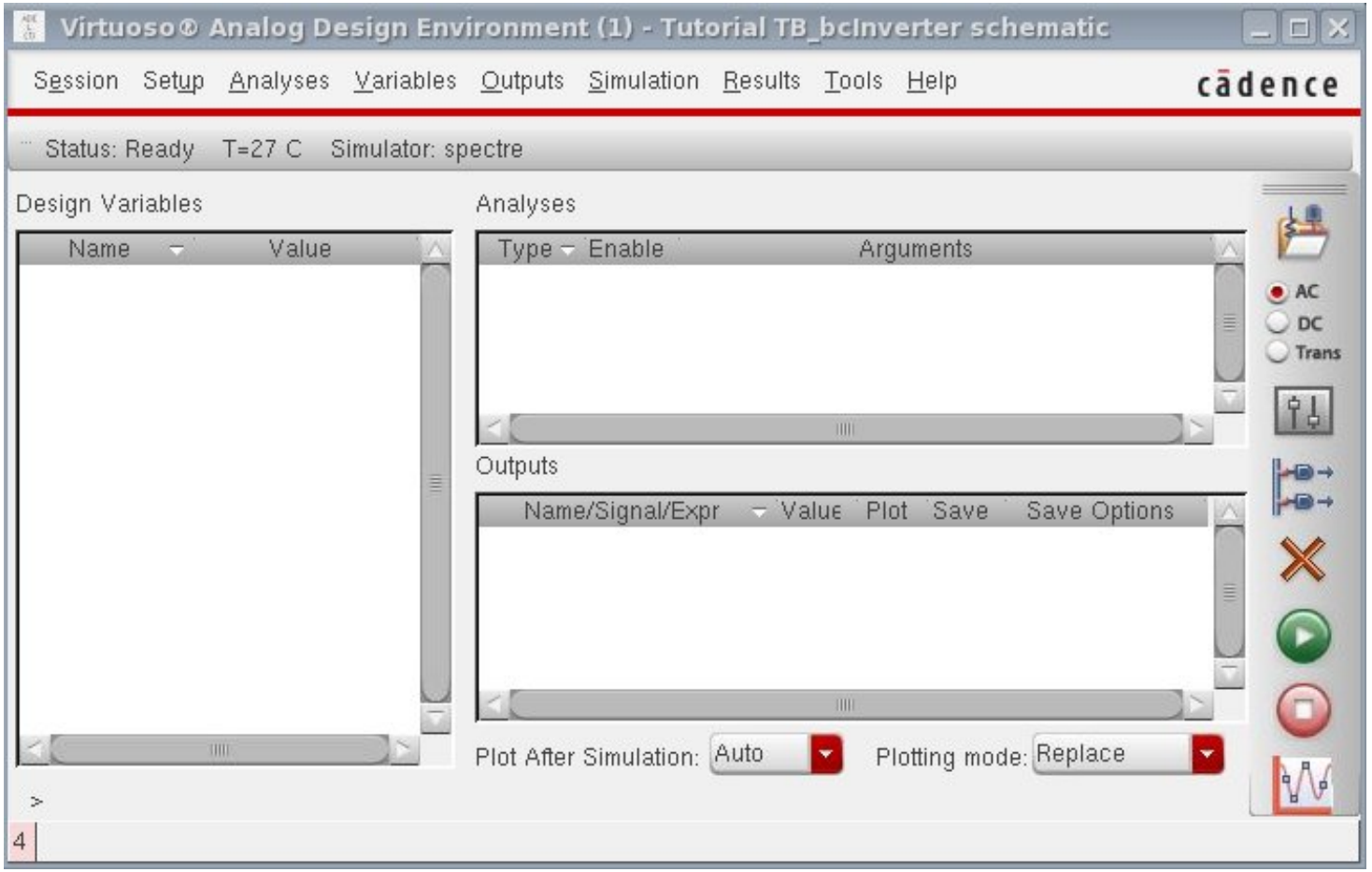
- A new window displays an automatically created Inverter symbol as shown here.



Simulation with SPECTRE

- In the **Inverter_Test** schematic window, execute **Launch – ADE L**

- The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

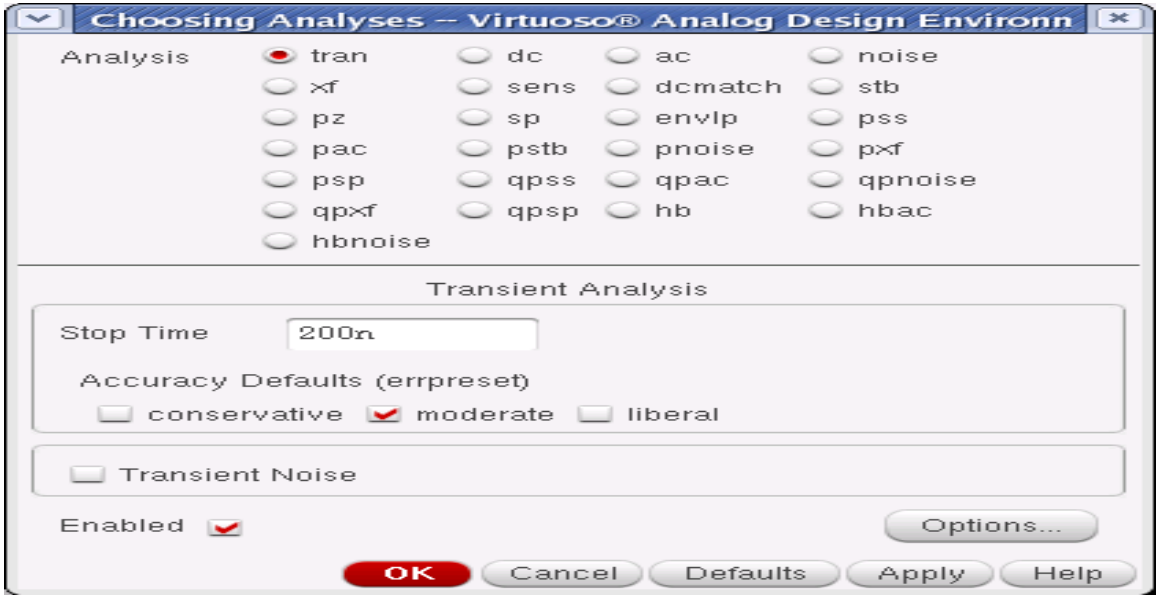


Simulation with SPECTRE (contd..)

Choosing Analyses:-

- In the Simulation window (ADE), click the **Choose - Analyses** icon.

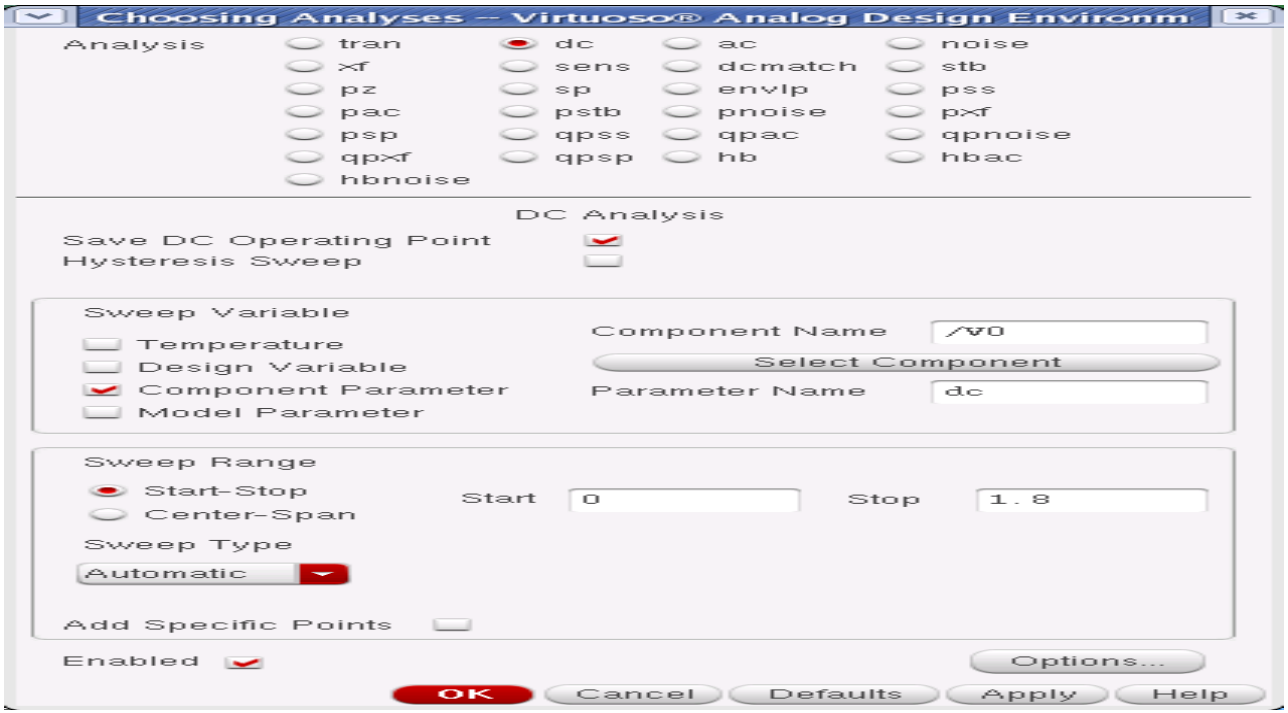
- To setup for transient analysis -
  a. In the Analysis section select **trans**
  b. Set the stop time as **200n**
  c. Click at the **moderate** or **Enabled** button at the bottom, and then click **Apply**.



Simulation with SPECTRE (contd..)

Choosing Analyses:-

- To setup for DC analysis –
  - a. In the Analyses section, select **dc**.
  - b. In the DC Analyses section, turn on **Save DC Operating Point.**
  - c. Turn on the **Component Parameter**.
  - d. Double click the **Select Component**, Which takes you to the schematic window.
  - e. Select input signal **vpulse source** in the test schematic window.
  - f. Select **"DC Voltage"** in the **Select Component Parameter** form and click OK.
  - f. In the analysis form type **start** and **stop** voltages as **0** to **1.8** respectively.
  - g. Check the enable button and then click **Apply.**



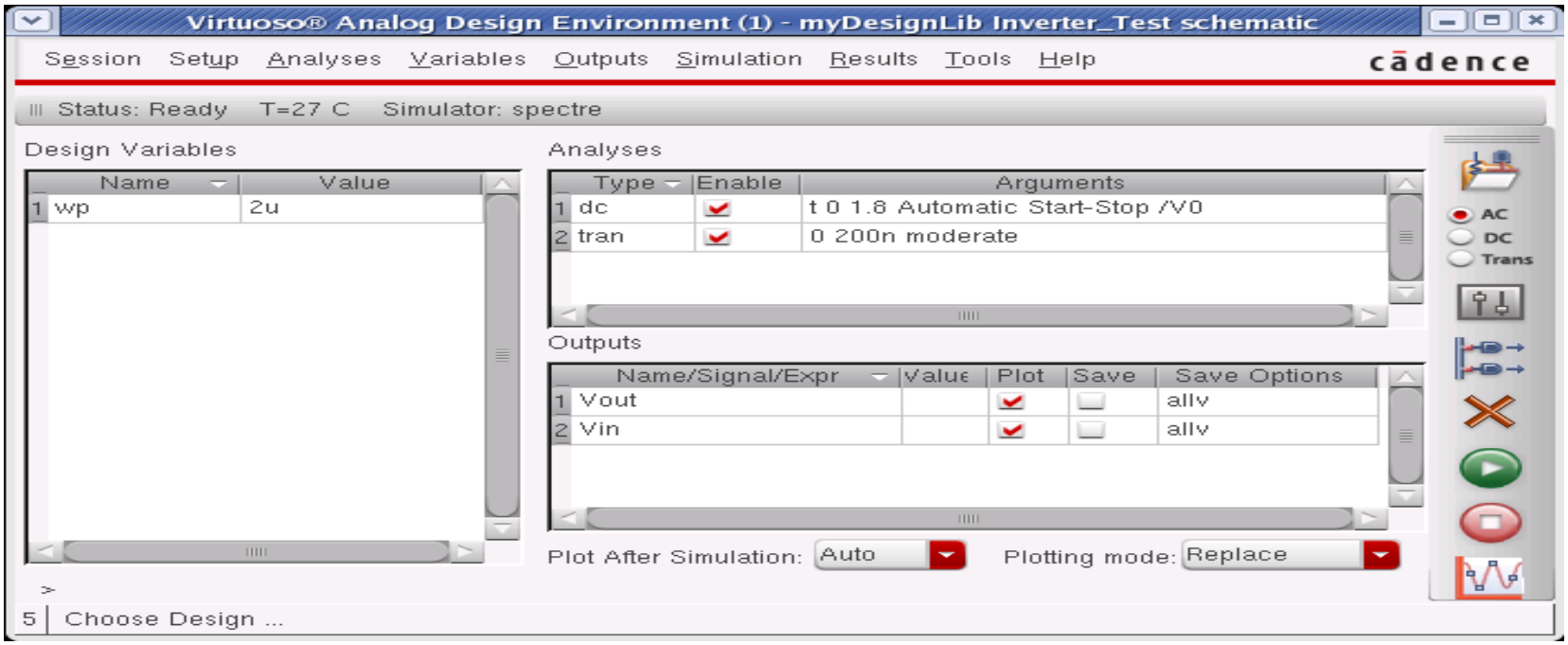
Simulation with SPECTRE (contd..)

Selecting outputs for plotting:-

• Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.

• Follow the prompt at the bottom of the schematic window, Click on output net **Vout**, input net **Vin** of the Inverter. Press **ESC** with the cursor in the schematic after selecting it

• Simulation window looks like this

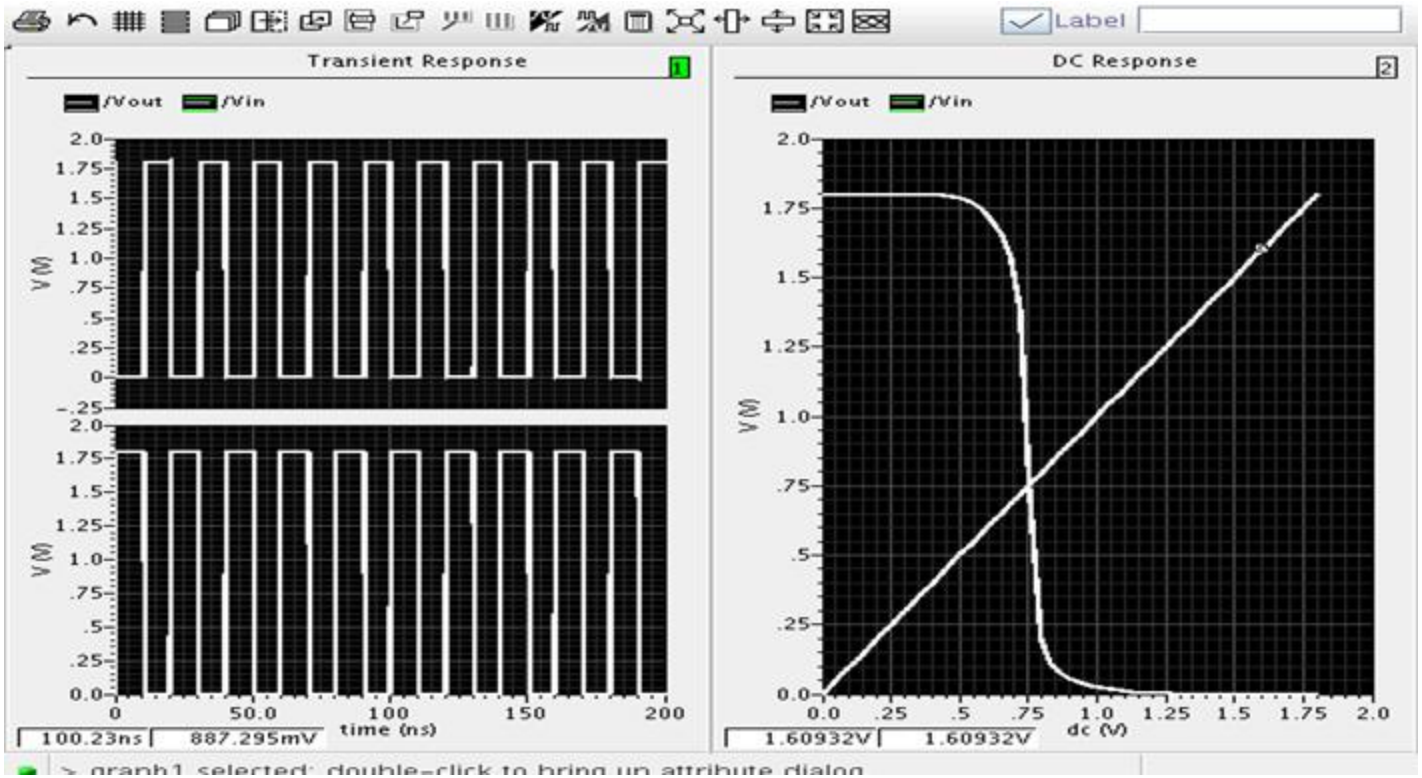


Simulation with SPECTRE (contd..)

Running the simulation

• Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation or the icon, this will create the netlist as well as run the simulation.

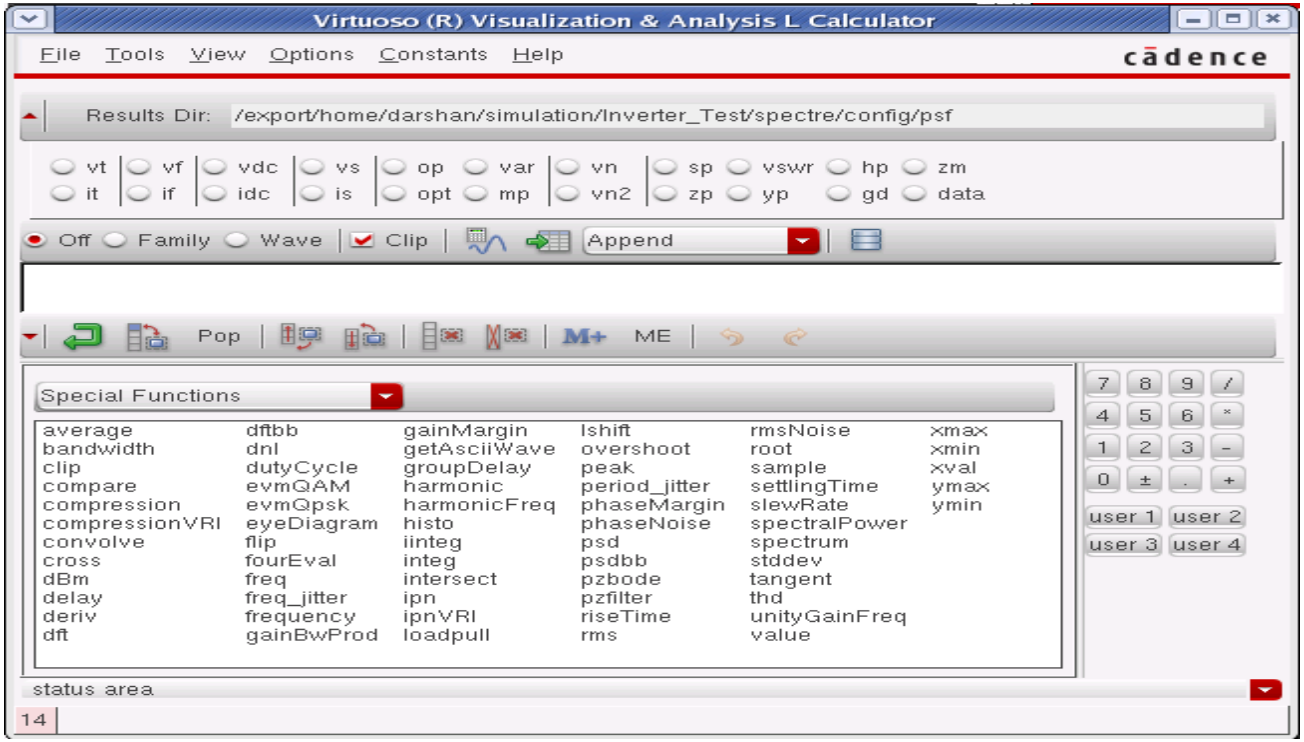
• When simulation finishes, the Transient, DC plots automatically will be popped up along with log file.



MEASURING THE PROPAGATION DELAY

• In the waveform window execute **Tools – Calculator…** 

• The calculator window appears.



• From the functions select **delay,** this will open the delay data panel.

• Place the cursor in the text box for Signal1, select the **wave** button and select the input waveform from the waveform window.

MEASURING THE PROPAGATION DELAY (contd..)

• Repeat the same for Signal2, and select the output waveform.

• Set the **Threshold value 1** and **Threshold value 2** to 0.9, this directs the calculator to calculate delay at 50% i.e. at 0.9 volts.

• Execute **OK** and observe the expression created in the calculator buffer.

• Click on **Evaluate the buffer icon**  to perform the calculation, note down the value returned after execution.

• Close the calculator window.

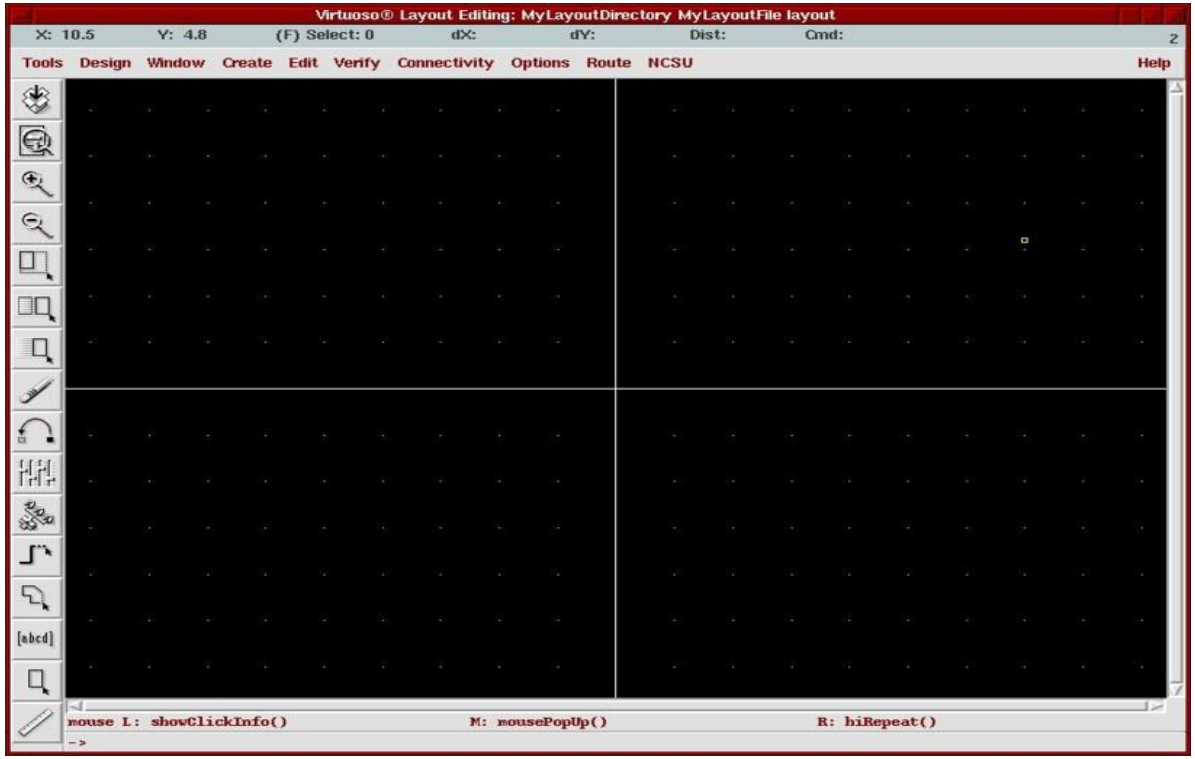
CREATING LAYOUT OF INVERTER

•From the **Inverter** schematic window menu execute **Launch – Layout XL**. A **Startup Option** form appears.

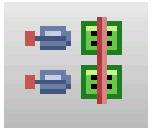
• Select ***Create New*** option. This gives a New Cell View Form

• Check the Cellname **(Inverter)**, Viewname **(layout).**

• Click **OK** from the New Cellview form

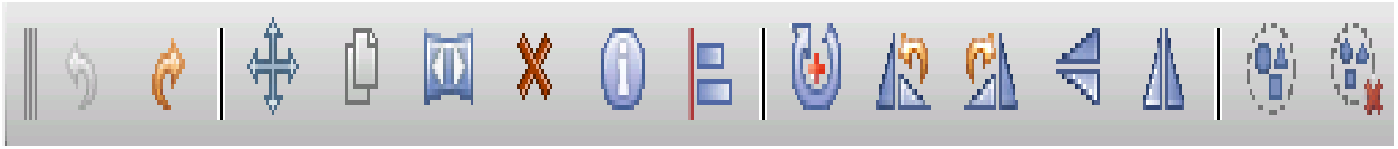


Adding components to Layout

• Execute **Connectivity – Generate – All from Source** or click the icon  in the layout editor window, **Generate Layout** form appears. Click **OK** which imports the schematic components in to the Layout window automatically.

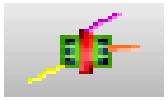
• Re arrange the components with in PR-Boundary.

•To rotate a component, Select the component and execute **Edit –Properties**. Now select the degree of rotation from the property edit form.



•To Move a component, Select the component and execute **Edit -Move** command.

Making interconnections

• **Execute Connectivity –Nets – Show/Hide selected Incomplete Nets or click** the icon in the Layout Menu. 

•From the layout window execute **Create – Shape – Path/ Create wire** or **Create – Shape – Rectangle (**for vdd and gnd bar**)** and select the appropriate Layers and Vias for making the inter connections

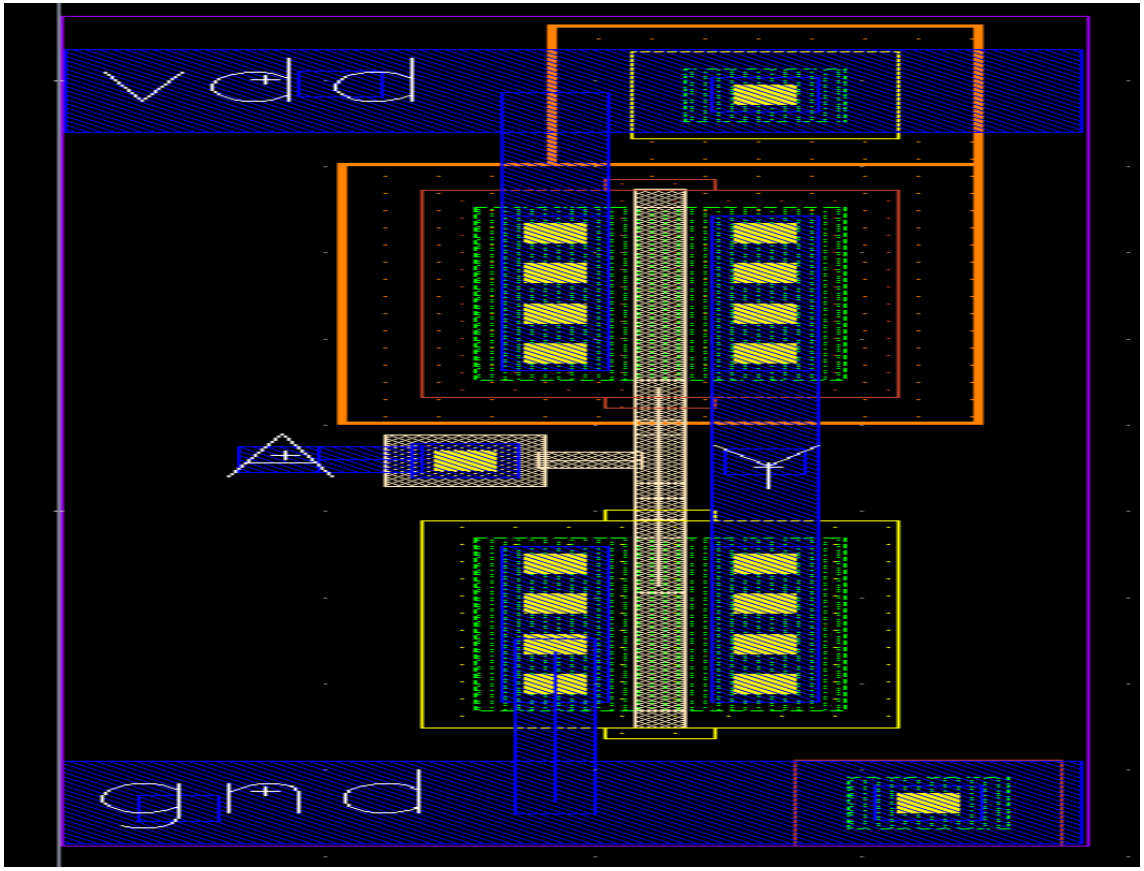
Creating Contacts / Vias

• You will use the contacts or vias to make connections between two different layers.
• Execute **Create — Via** or select command to place different Contacts, as given in below table:

Connection	Contact Type
For Metal1- Poly Connection	Metal 1 – Poly
For Metal1- P substrate Connection	Metal 1 – P sub
For Metal1- N well Connection	Metal 1 – N well

Saving the design

• Save your design by selecting **File — Save** or click  to save the layout, and layout should appear as below

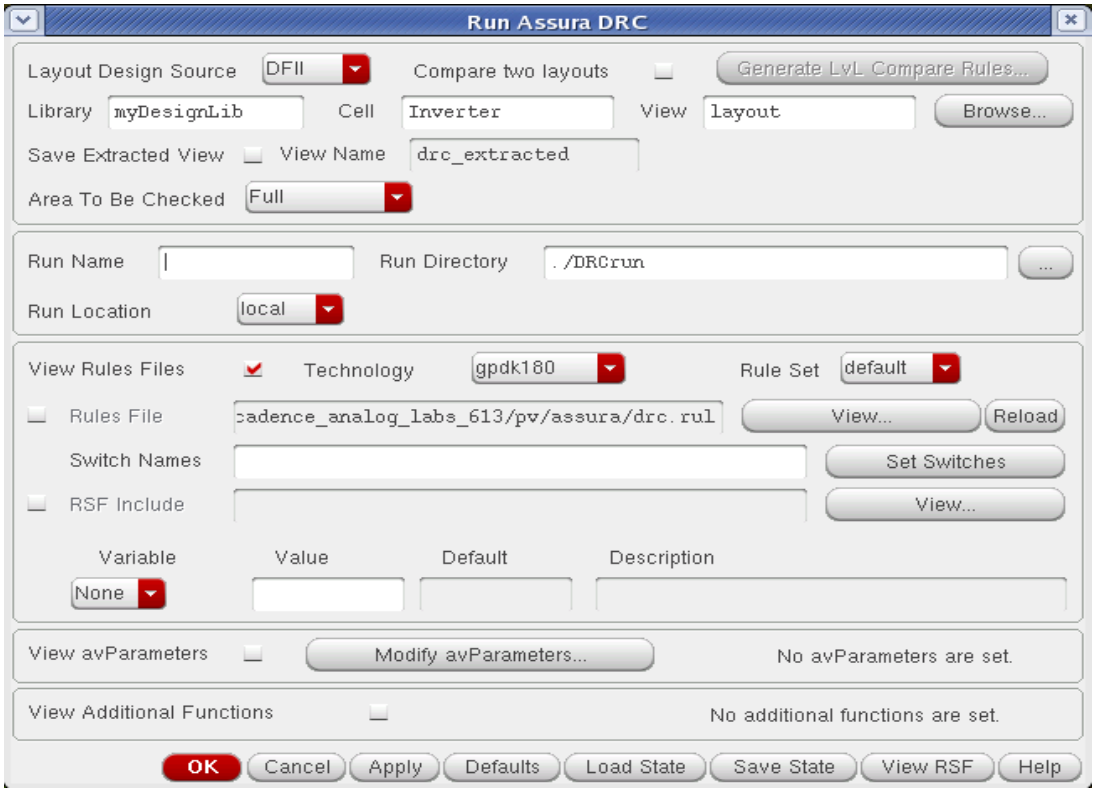


Physical Verification

ASSURA DRC:-

• Select **Assura - Run DRC** from layout window.

• The DRC form appears. The Library and Cell name are taken from the current design window, but rule file may be missing. Select the Technology as **gpdk180.** This automatically loads the rule file.



• Click OK to start DRC.

• A Progress form will appears. You can click on the watch log file to see the log file.

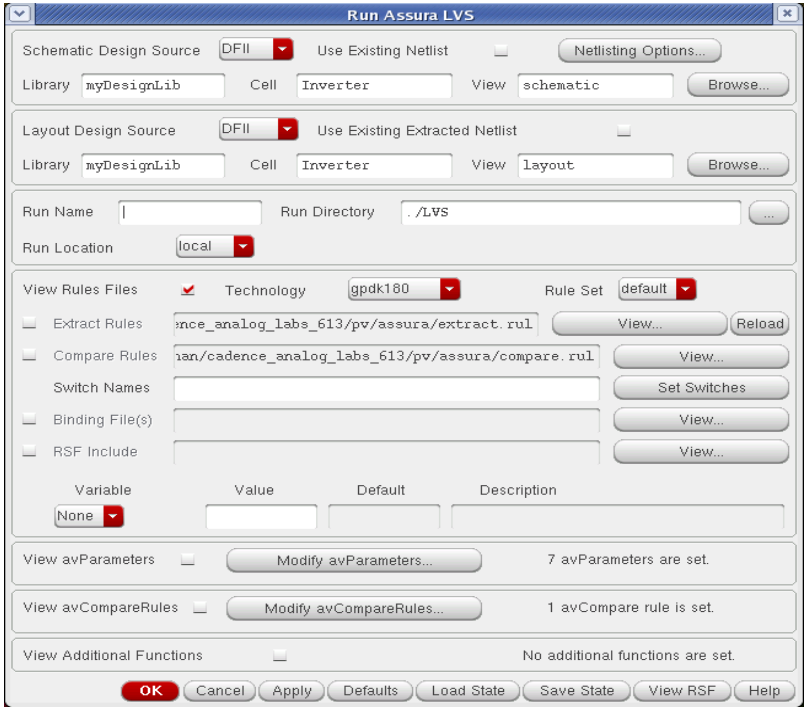
• When DRC finishes, a dialog box appears asking you if you want to view your DRC results, and then click **Yes** to view the results of this run.

• If there any DRC error exists in the design **View Layer Window** (VLW) and **Error Layer Window** (ELW) appears. Click **View – Summary** in the ELW to find details of errors.

Physical Verification

ASSURA LVS:-

• Select **Assura – Run LVS** from the layout window. The Assura Run LVS form appears. It will automatically load both the schematic and layout view of the cell.



• The LVS begins and a Progress form appears.

• If the schematic and layout matches completely, you will get the form displaying **Schematic and Layout Match.**

• If the schematic and layout do not matches, a form informs that the LVS completed successfully and asks if you want to see the results of this run.

• Click **Yes** in the form. LVS debug form appears, and you are directed into LVS debug environment.

• In the **LVS debug form** you can find the details of mismatches and you need to correct all those mismatches and **Re – run** the LVS till you will be able to match the schematic with layout.

Physical Verification

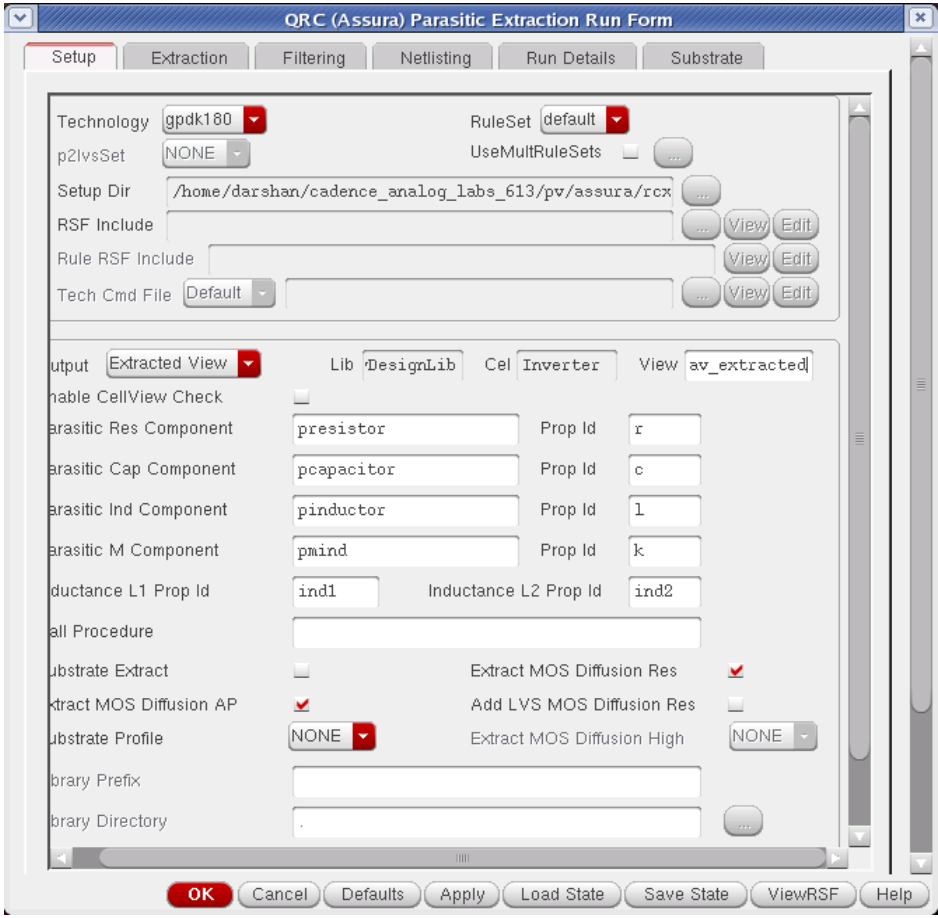
ASSURA RCX:-

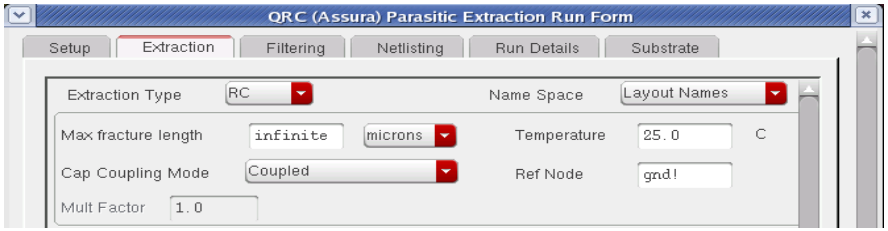
In this section we will extract the RC values from the layout and perform analog circuit simulation on the designs extracted with RCX.

- From the layout window execute **Assura – Run RCX**.

- Change the following in the Assura parasitic extraction form. Select **output** type under **Setup** tab of the form.

- In the **Extraction** tab of the form, choose Extraction type, Cap Coupling Mode and specify the Reference node for extraction.





Physical Verification

Assura RCX (contd..)

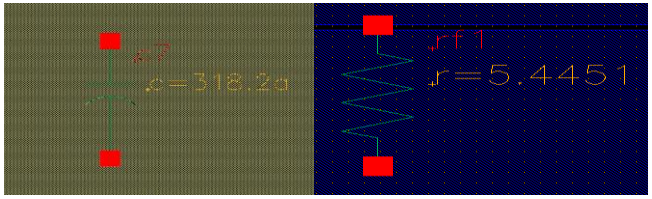
• In the **Filtering** tab of the form, **Enter Power Nets** as **vdd!, vss!** and **Enter Ground Nets** as **gnd!**

• Click **OK** in the Assura parasitic extraction form when done.

• The RCX progress form appears, in the progress form click **Watch log file** to see the output log file.

• When RCX completes, a dialog box appears, informs you that **Assura RCX run Completed successfully.**

• You can open the **av_extracted** view from the library manager and view the parasitic.



Questions ?