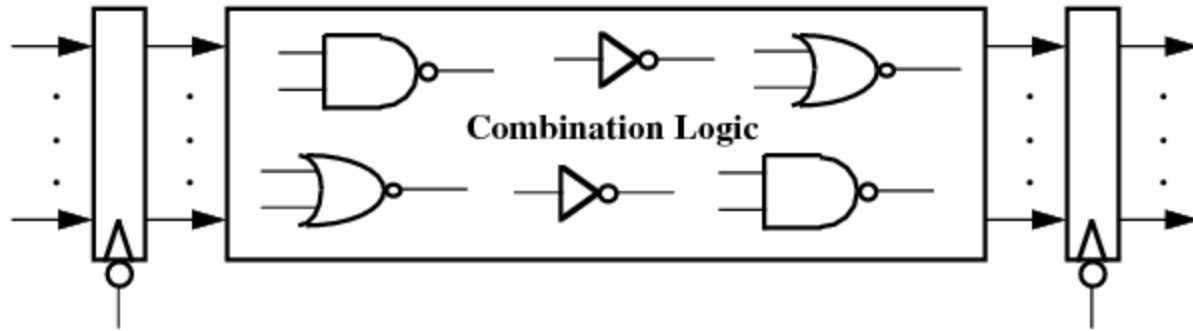


**Acknowledgment:** Almost all of these slides are based on Dave Patterson's CS152 Lecture Slides at UC, Berkeley.

## COMPUTER SYSTEMS ORGANIZATION

Timing Model and Register File Design -- Spring 2011 --  
IIT-H -- Suresh Purini

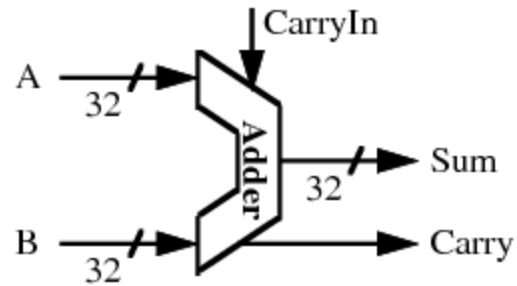
# Sequential and Combinational Circuits



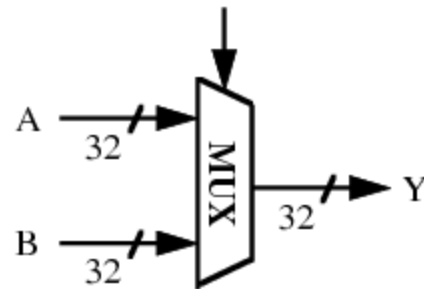
- ❑ What's the difference between sequential and combinational circuits?

# Combinational Logic Elements

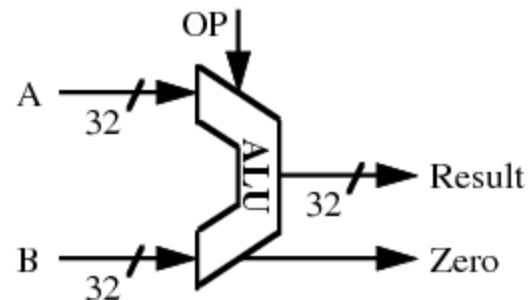
- **Adder**



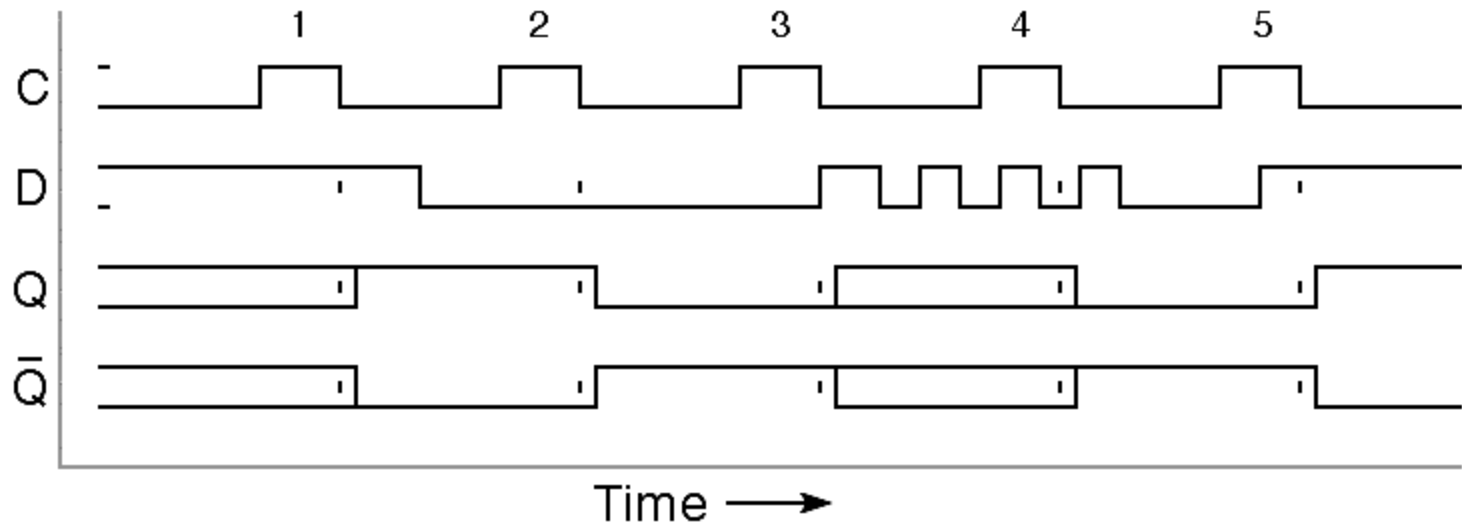
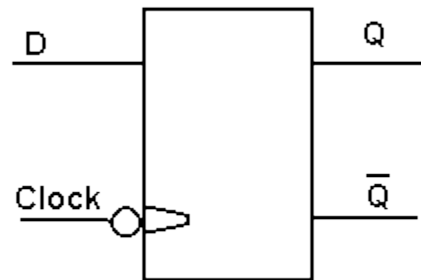
- **MUX**



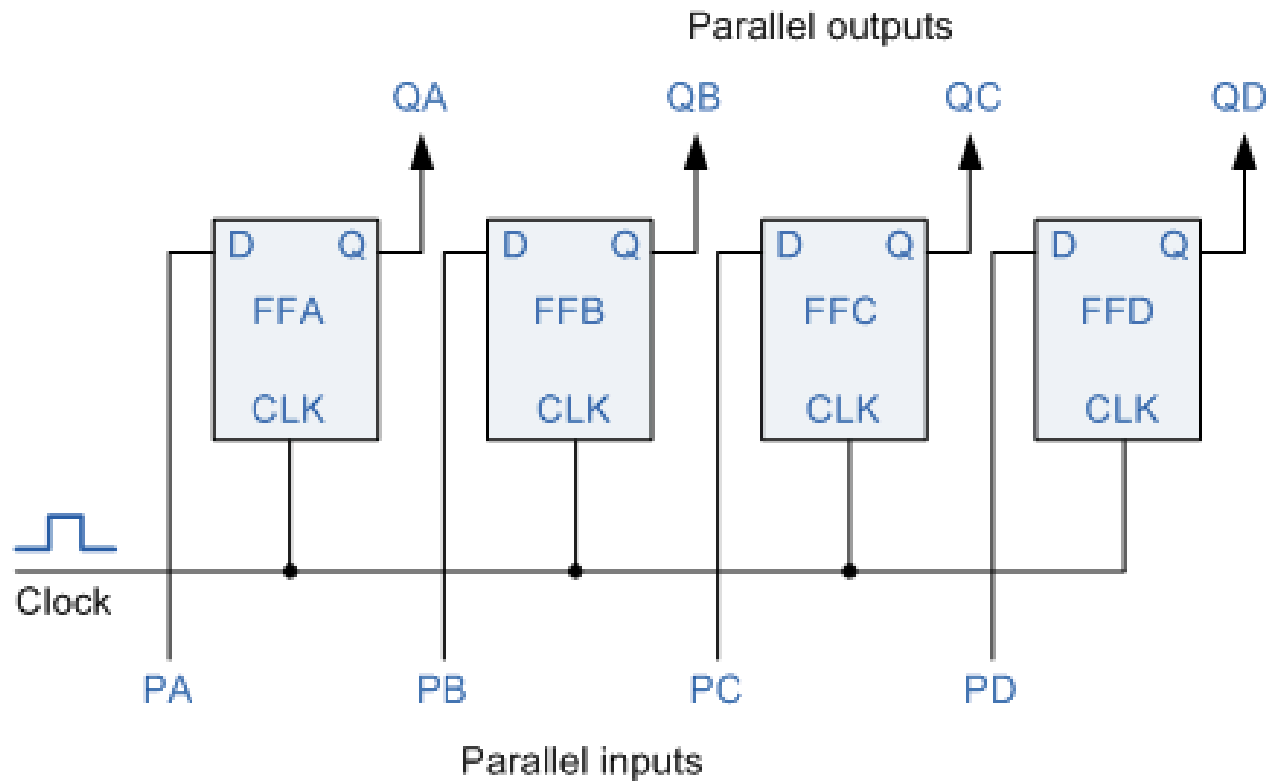
- **ALU**



# Sequential Element: Negative Edge Triggered D-Flip Flop



# 4-bit Register



# Sequential Element: Register

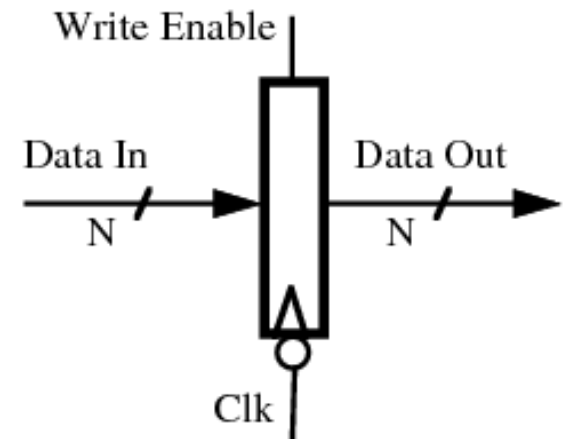
## □ Register

### ▣ Similar to D Flip Flop except

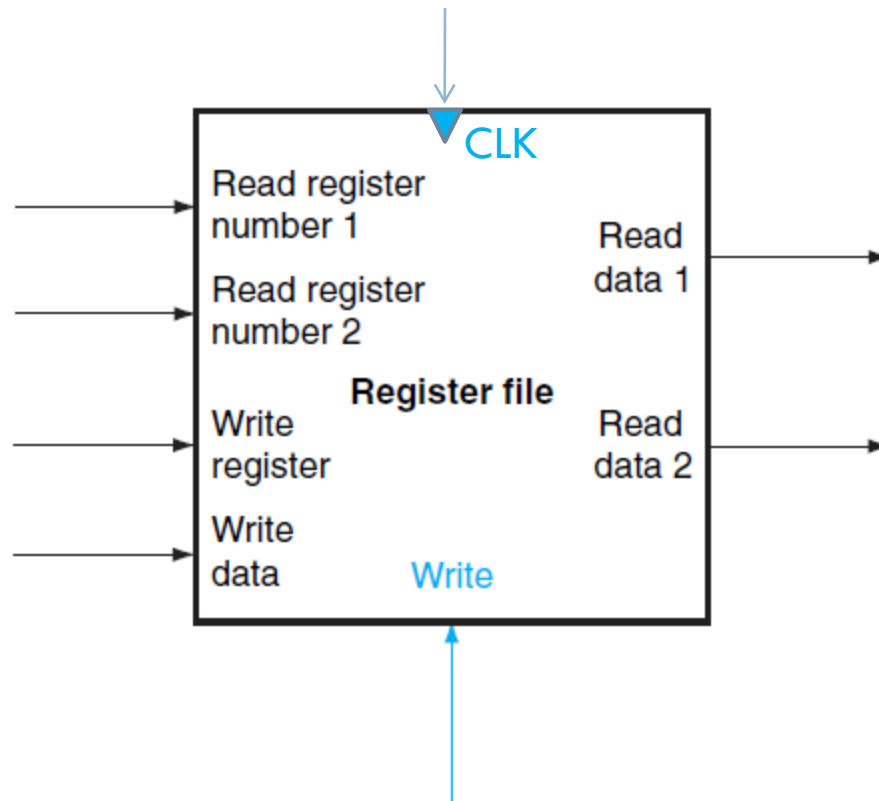
- N bit input and output
- Write Enable input

### ▣ Write Enable

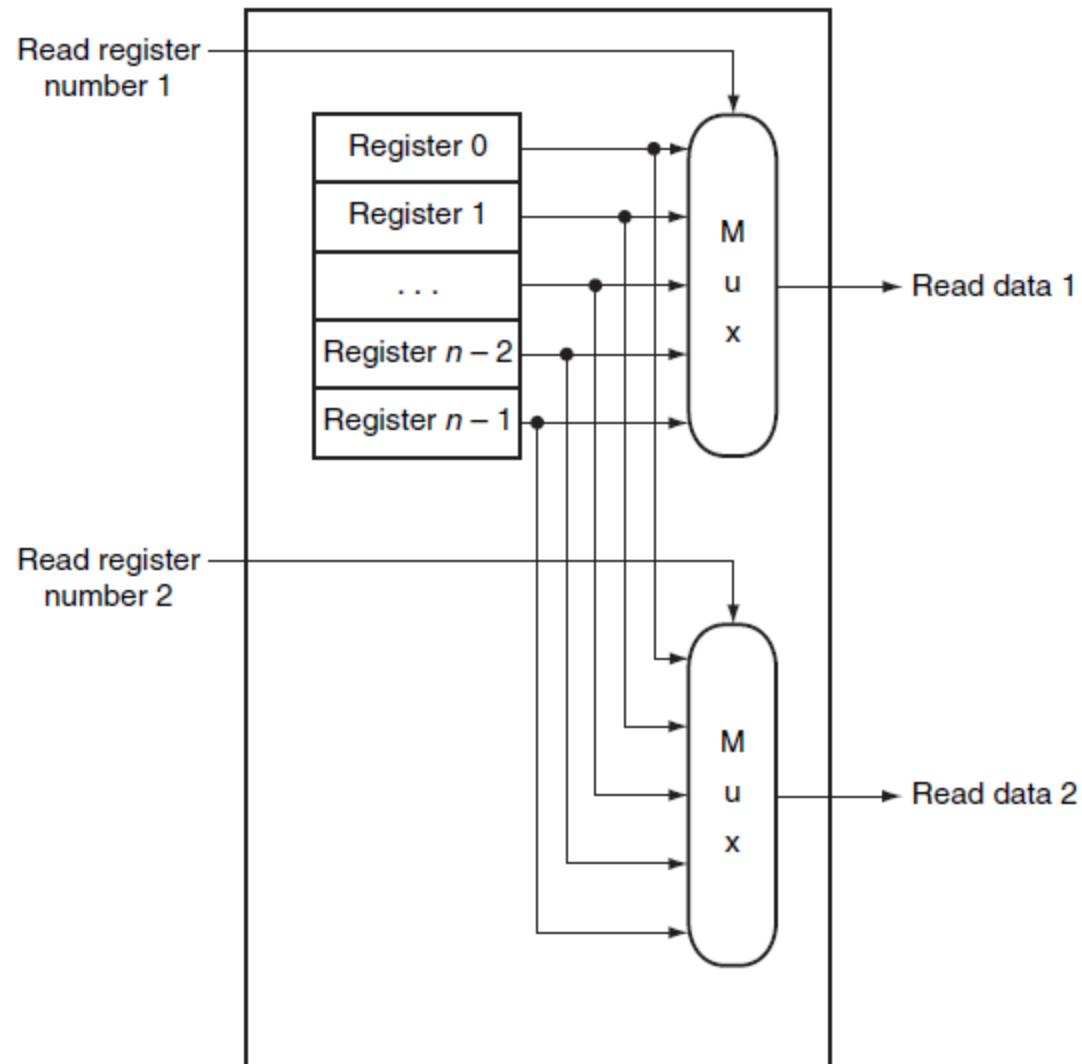
- 0: Data out will not change
- 1: Data out will become Data In



# Register File

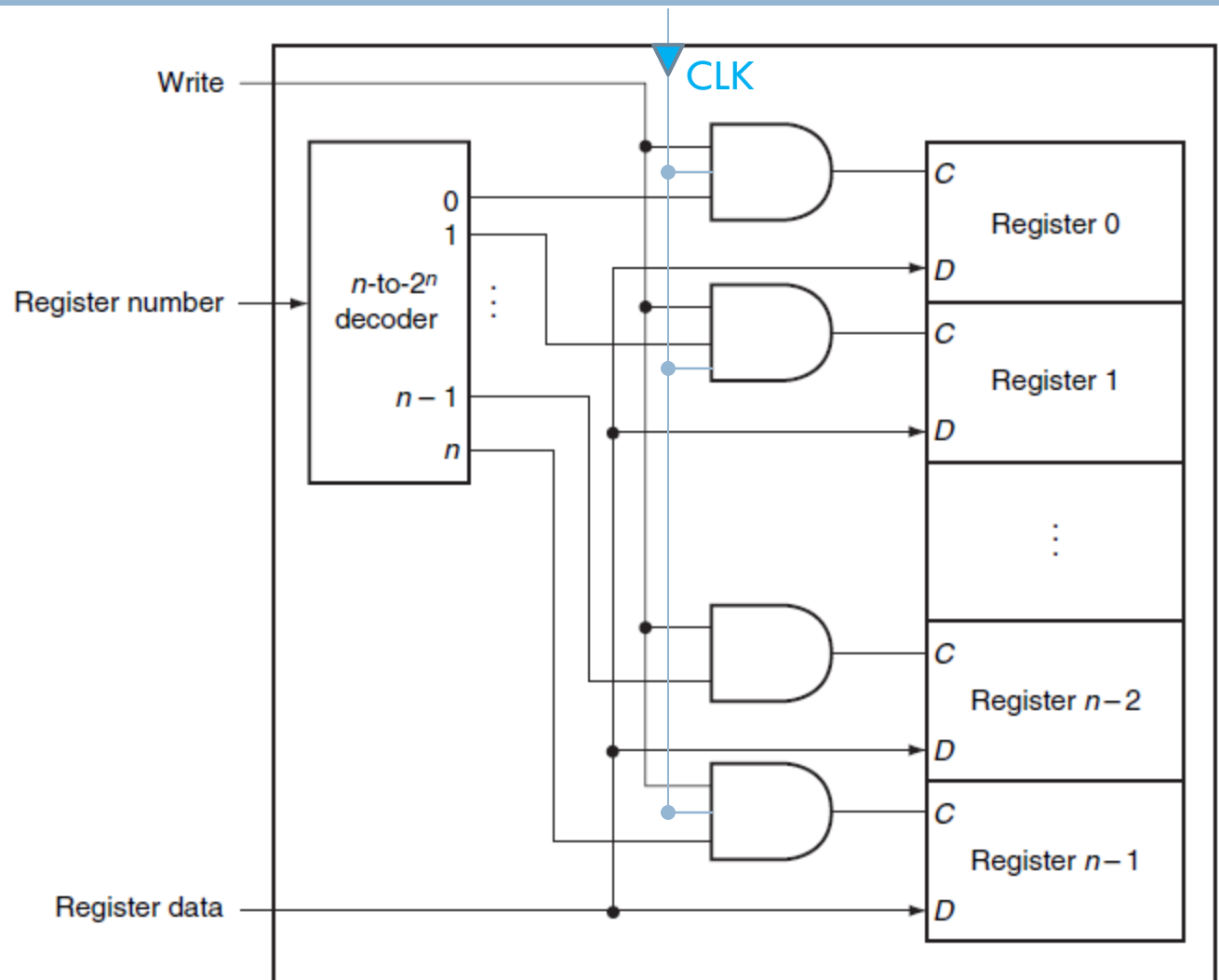


# Register File



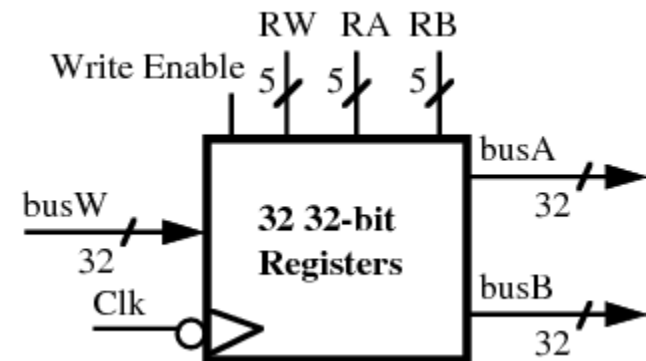


# Register File



# Storage Element: Register File

- Register File consists of 32 registers
  - ▣ Two 32-bit output busses: busA and busB
  - ▣ one 32-bit input bus: busW
- Register is selected by
  - ▣ RA selects the register to put on busA
  - ▣ RB selects the register to put on busB
  - ▣ RW selects the register to be written via busW when Write Enable is 1
- Clock input (CLK)
  - ▣ The CLK input is a factor ONLY during write operation
  - ▣ During read operation, behaves as a combinational logic block
    - RA or RB valid  $\Rightarrow$  busA or busB valid after access time



# Storage Element: Memory

## □ Memory

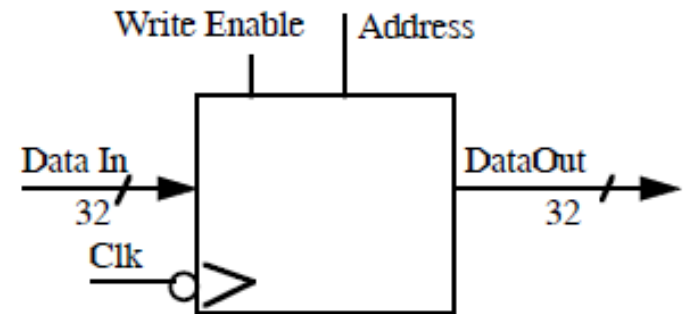
- ▣ One input bus: Data In
- ▣ One output bus: Data Out

## □ Memory word is selected by:

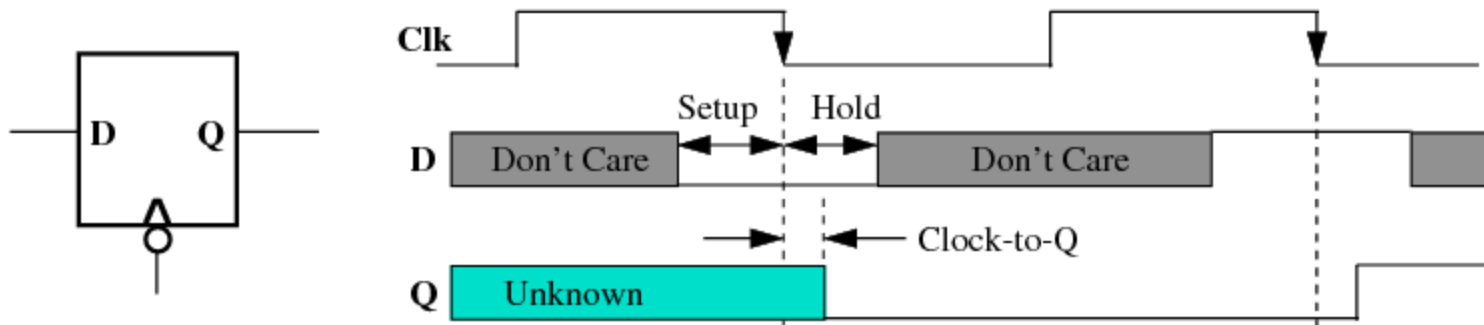
- ▣ Address selects the word to put on Data Out
- ▣ Write Enable = 1: address selects the memory word to be written via the Data In bus

## □ Clock input (CLK)

- ▣ The CLK input is a factor ONLY during write operation
- ▣ During read operation, behaves as a combinational logic block:
  - Address valid => Data Out valid after “access time.”

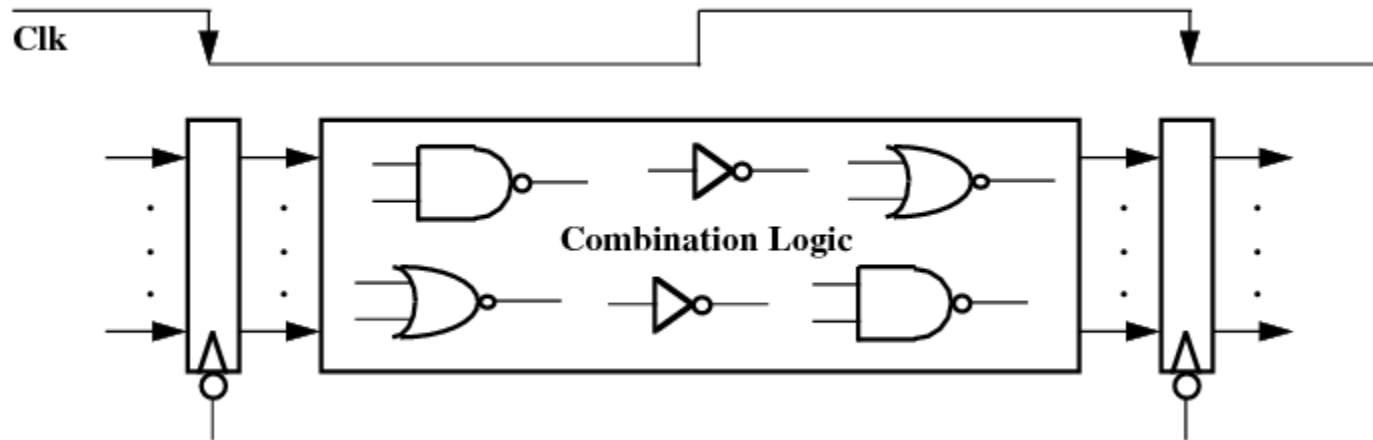


# Storage Element Timing Model – Negative Edge Triggered D-Flip Flop



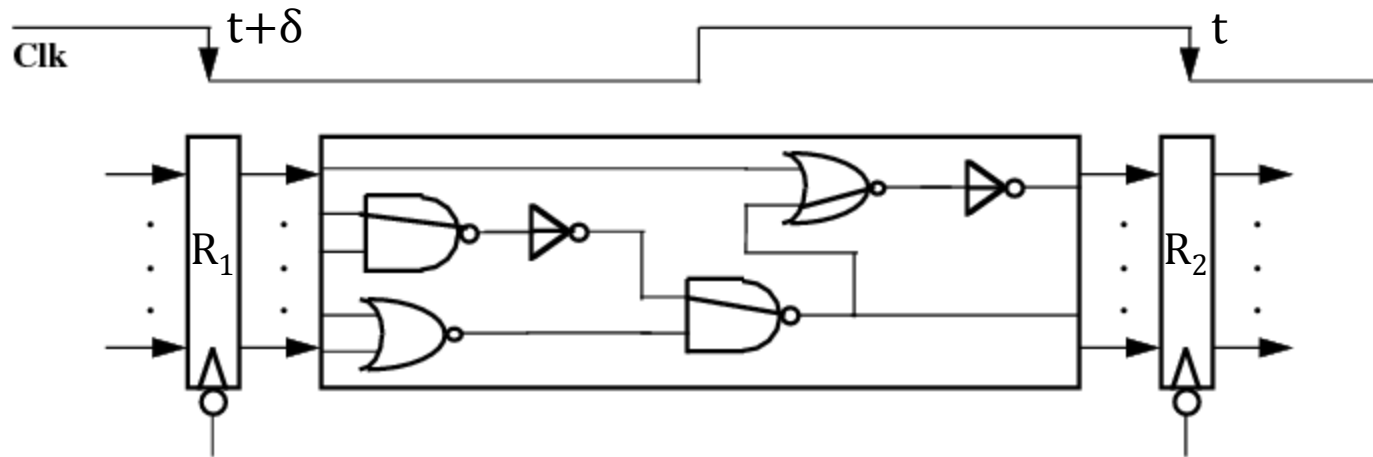
- ❑ **Setup Time:** Input must be stable BEFORE the trigger clock edge.
- ❑ **Hold Time:** Input must be stable AFTER the trigger clock edge.
- ❑ **Clock-to-Q time:** Output cannot change instantaneously at the trigger clock edge.
  - ❑ Similar to delay in logic gates.

# Clocking Methodology



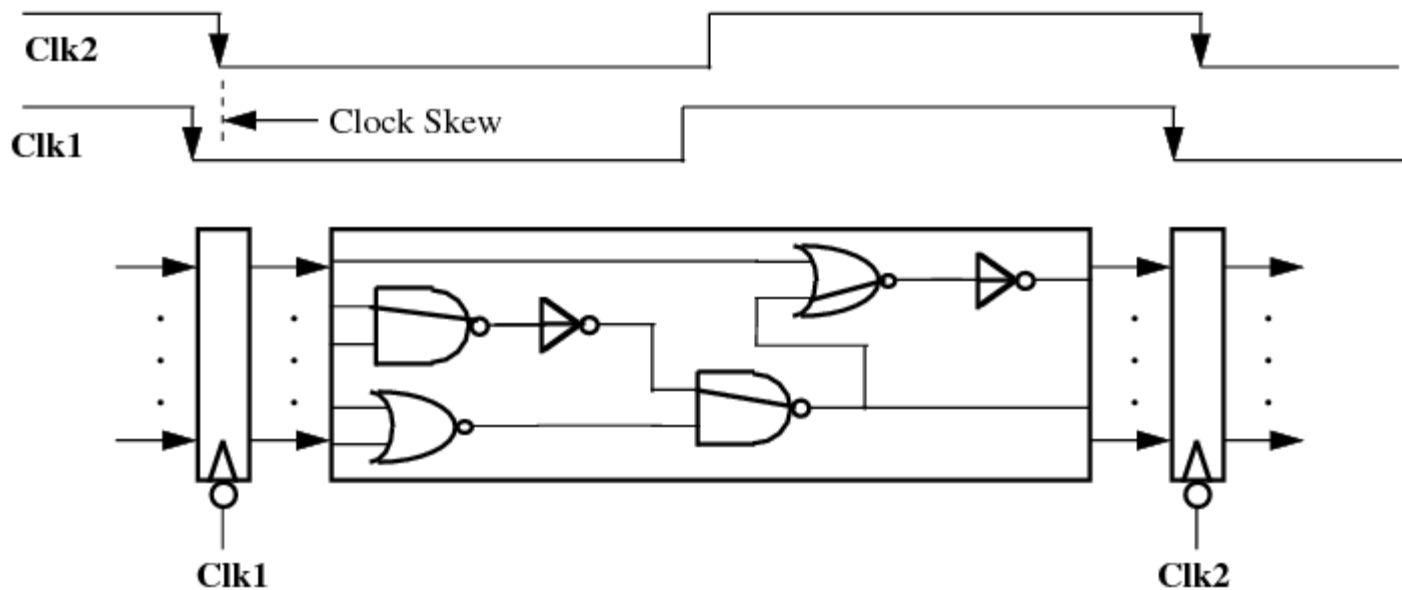
- All storage elements are clocked by the same clock edge
- The combination logic block's:
  - ▣ Inputs are updated at each clock tick
  - ▣ All outputs **MUST** be stable before the next clock tick

# Critical Path and Cycle Time



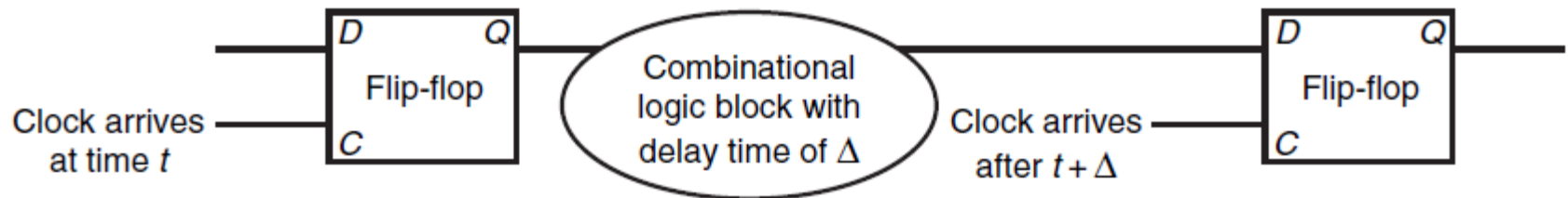
- ❑ **Critical Path:** Slowest path between any two storage devices
- ❑ Cycle time is a function of critical path
- ❑ More specifically, the cycle time must be greater than:
  - ❑ Clock-to-Q + Longest Path through the Combinational Logic + Setup Time

# Clock Skew's Effect on Cycle Time

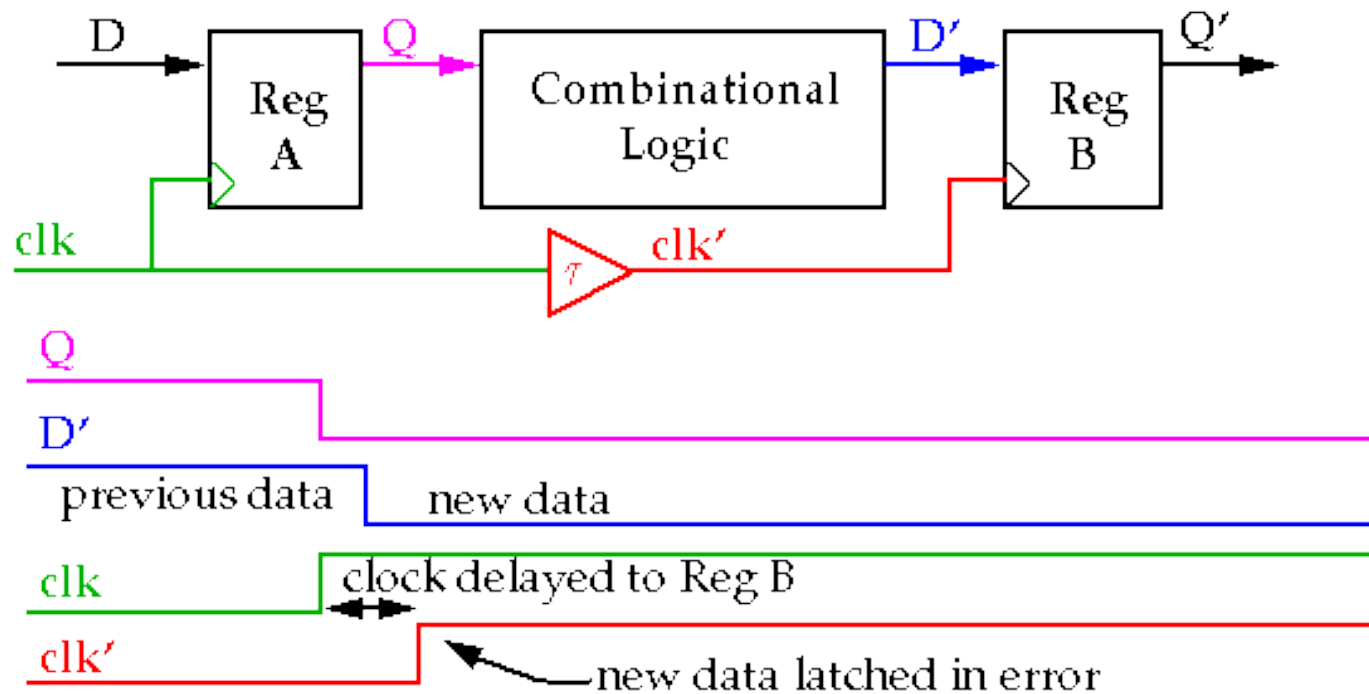


❑ How to take care of Clock Skew?

❑ We shall assume there is not Clock Skew.

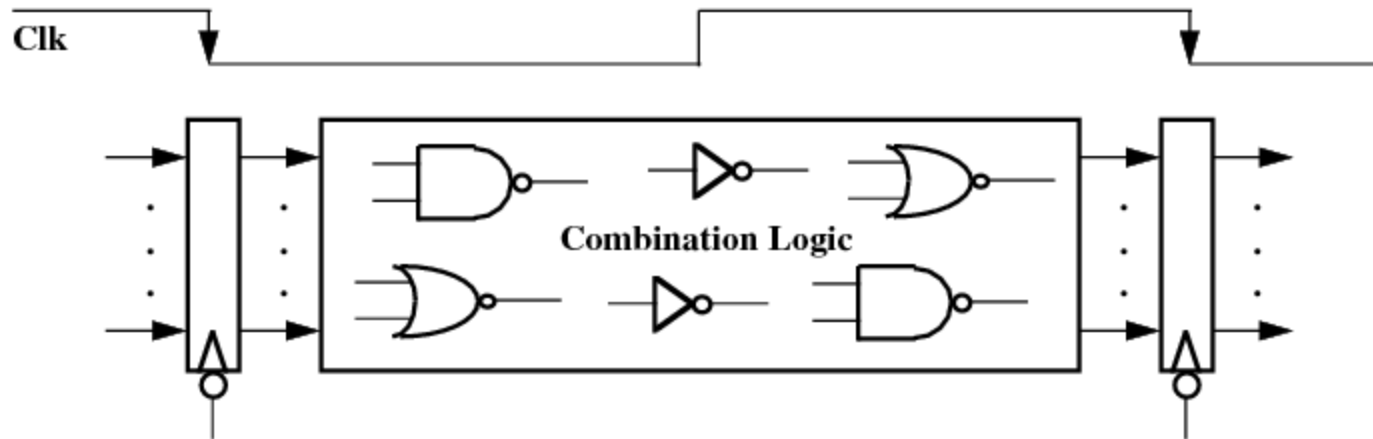


# Clock Skew





# How to Avoid Hold Time Violation?



- Hold time requirement:
  - ▣ Input to register must NOT change immediately after the clock tick.
- $\text{CLK-to-Q} + \text{Shortest Delay Path}$  must be greater than Hold Time