

# Field Programmable Analog Array

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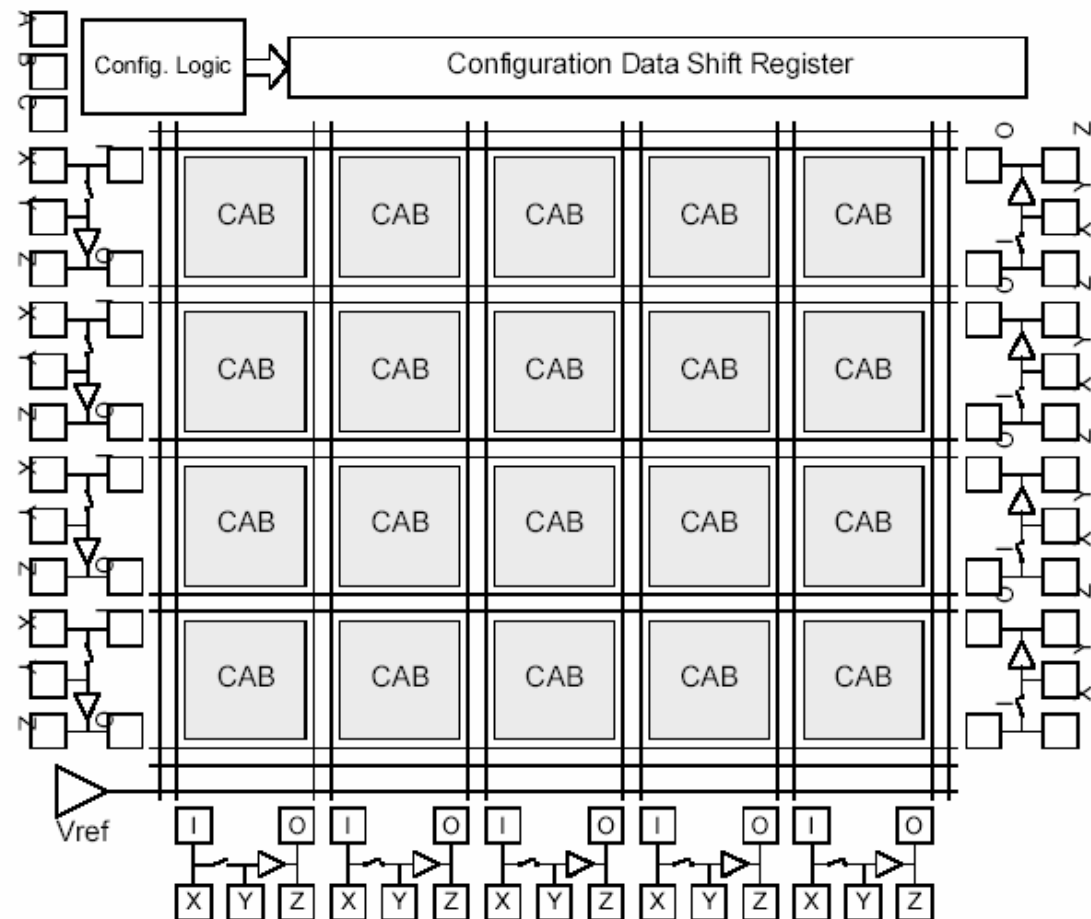
**CVEST, IIIT HYDERABAD**

# Why Programmable Analog?

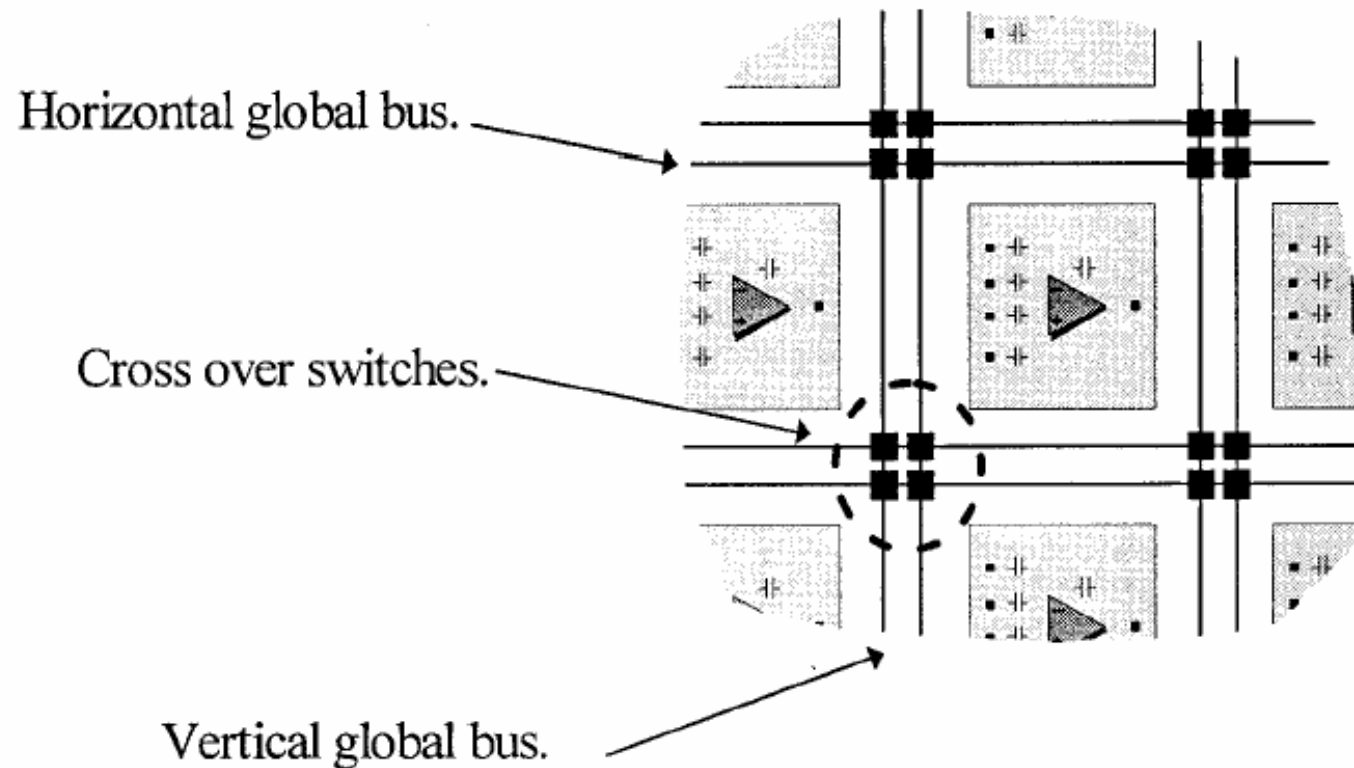
- Faster Prototyping
- Faster Time-to-Market
- Shorter Design Cycles
- Design integration
- Improved component matching



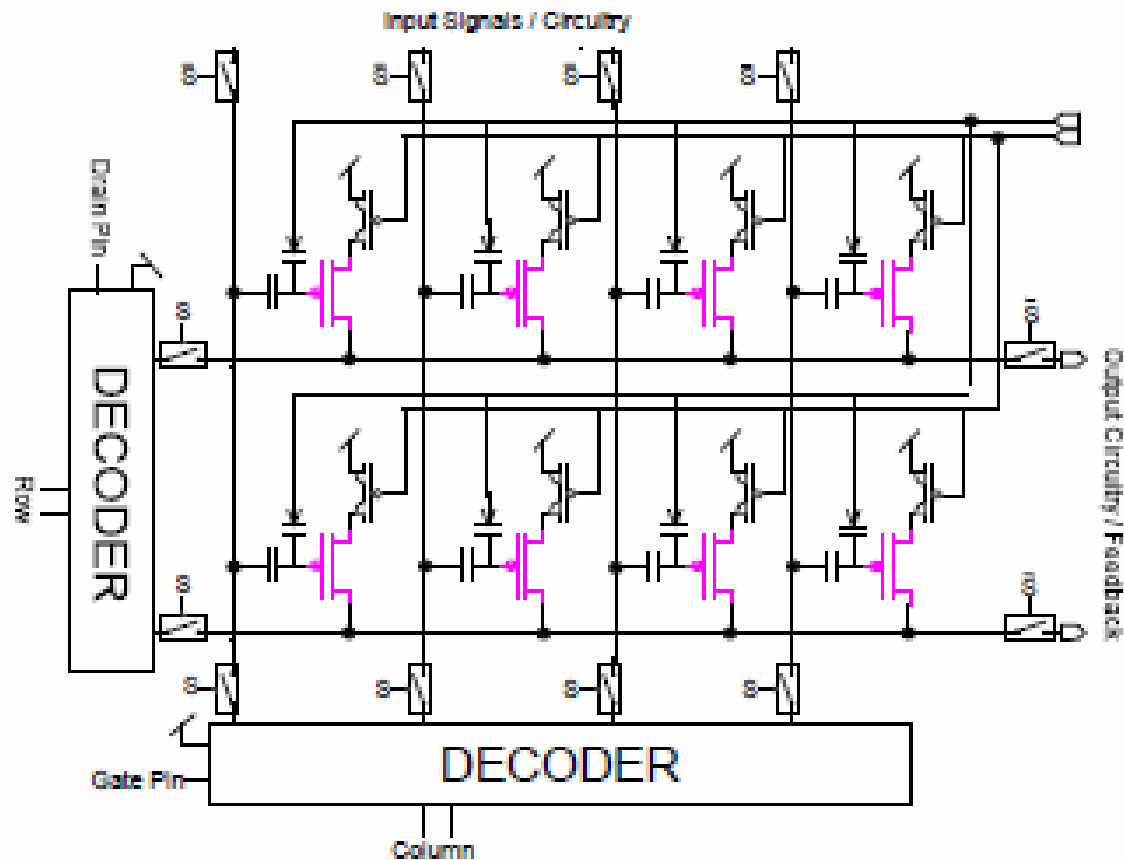
# Architecture of FPAA



# Routing Architecture



# Switching Matrix



# CAB Implementation

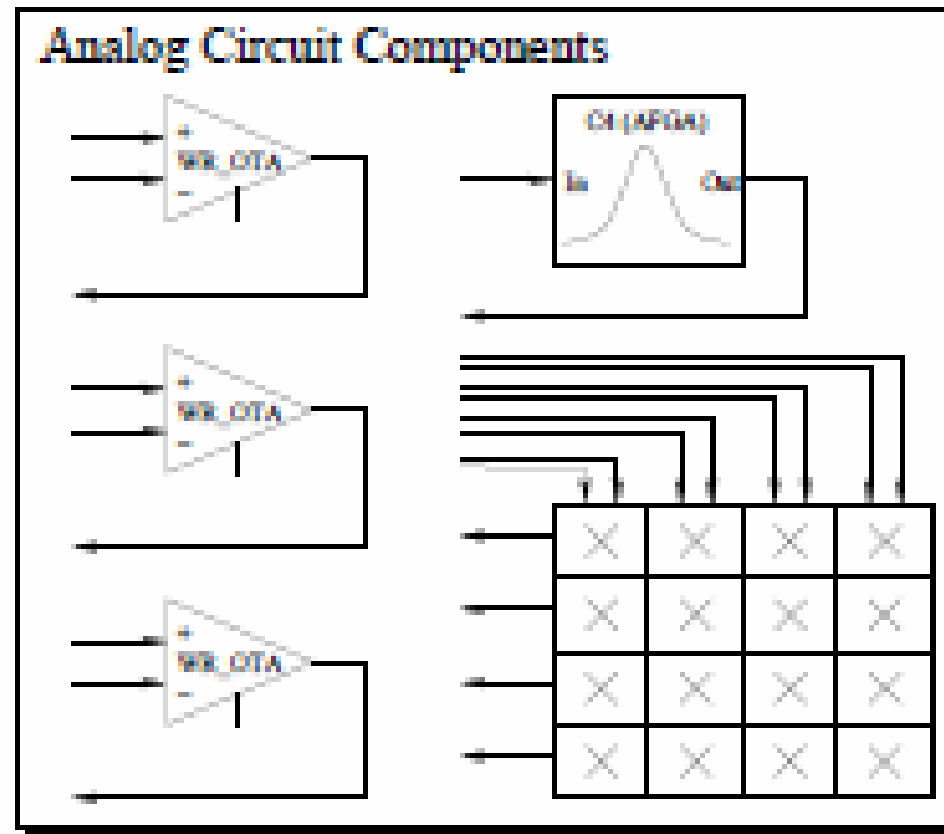
- Continuous Time vs. Discrete Time

## Discrete Time

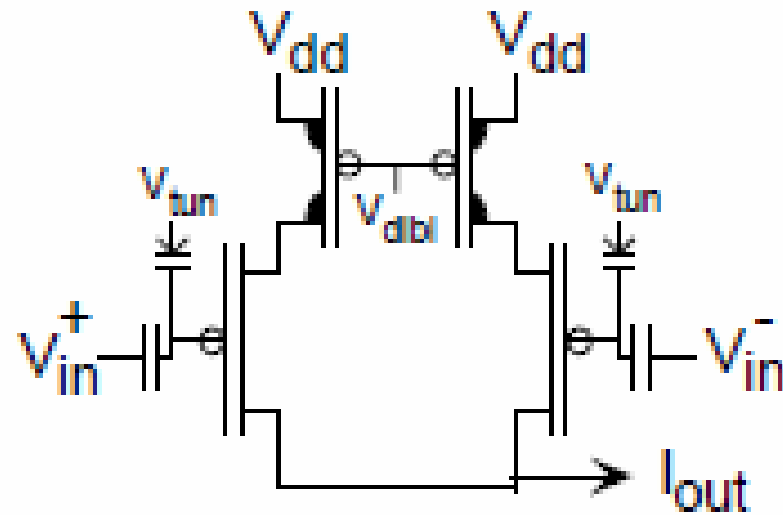
- Switched Capacitor Design (Current)
- Pulse Based Design (Under Research)



# Architecture of Configurable Analog Block

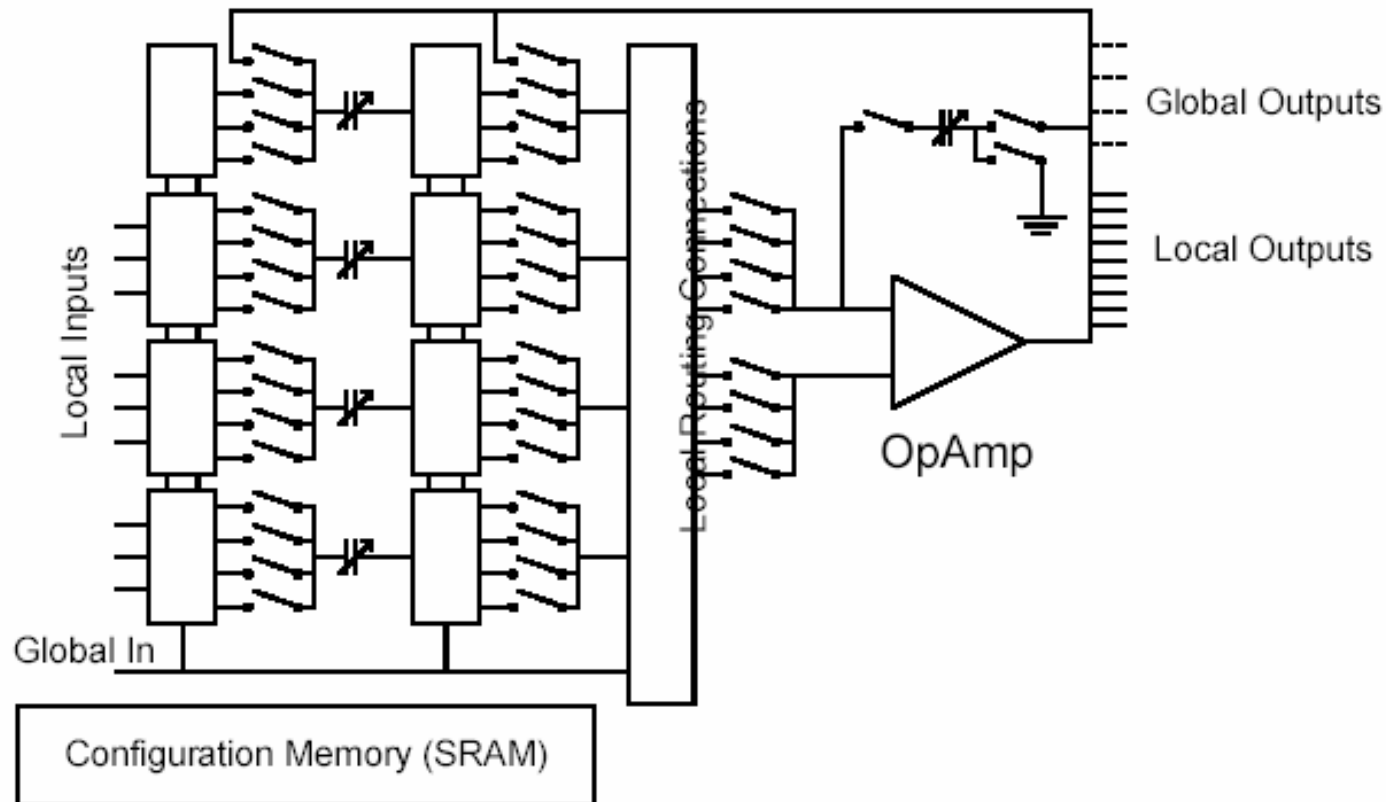


# Multiplication of an input by a constant

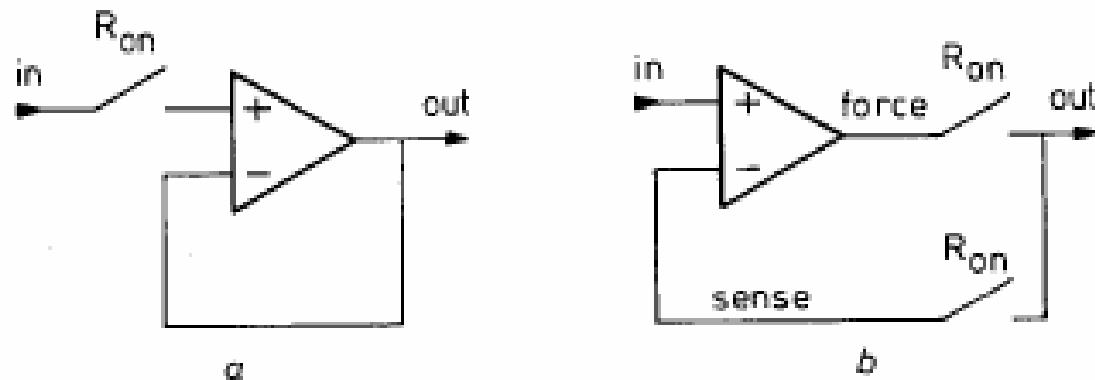




# Switched Capacitor based design



# Switches for input and output



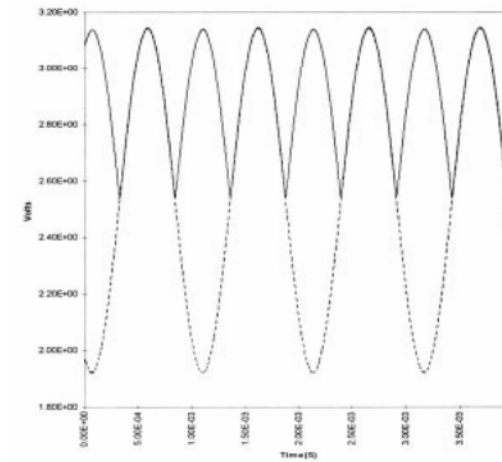
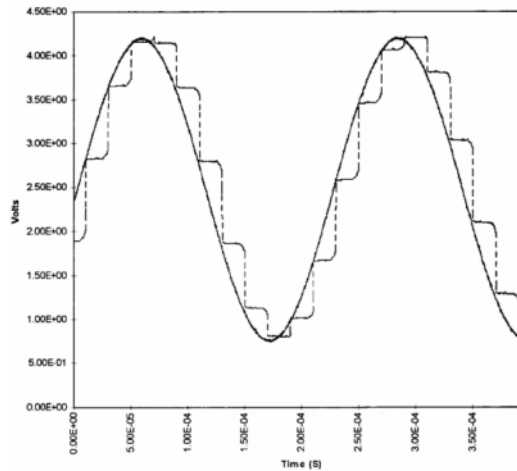
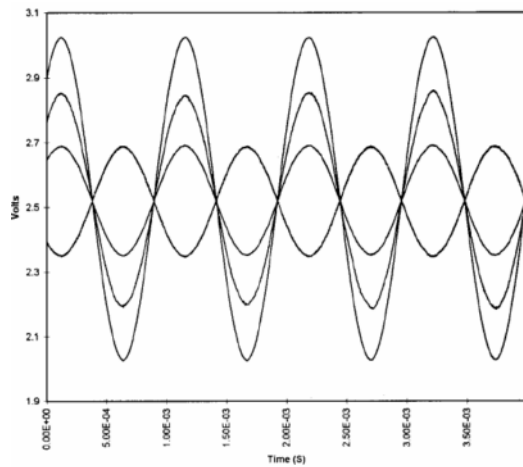
# Benefits of SC Design

- Design of SC circuits quite mature
- Switches already present in FPAA
- Allows for better accuracy than RC
  - 0.05% - 0.2% vs. 10% - 30%



# Performance of SC Design

- Currently limited to 1MHz
- Versatile design possibilities



# Problems with SC Design

- Limitations on switching frequency
  - Require non-overlapping clocks
- Voltage used to represent signal
  - Signal still susceptible to noise
- Increased mixed signal noise

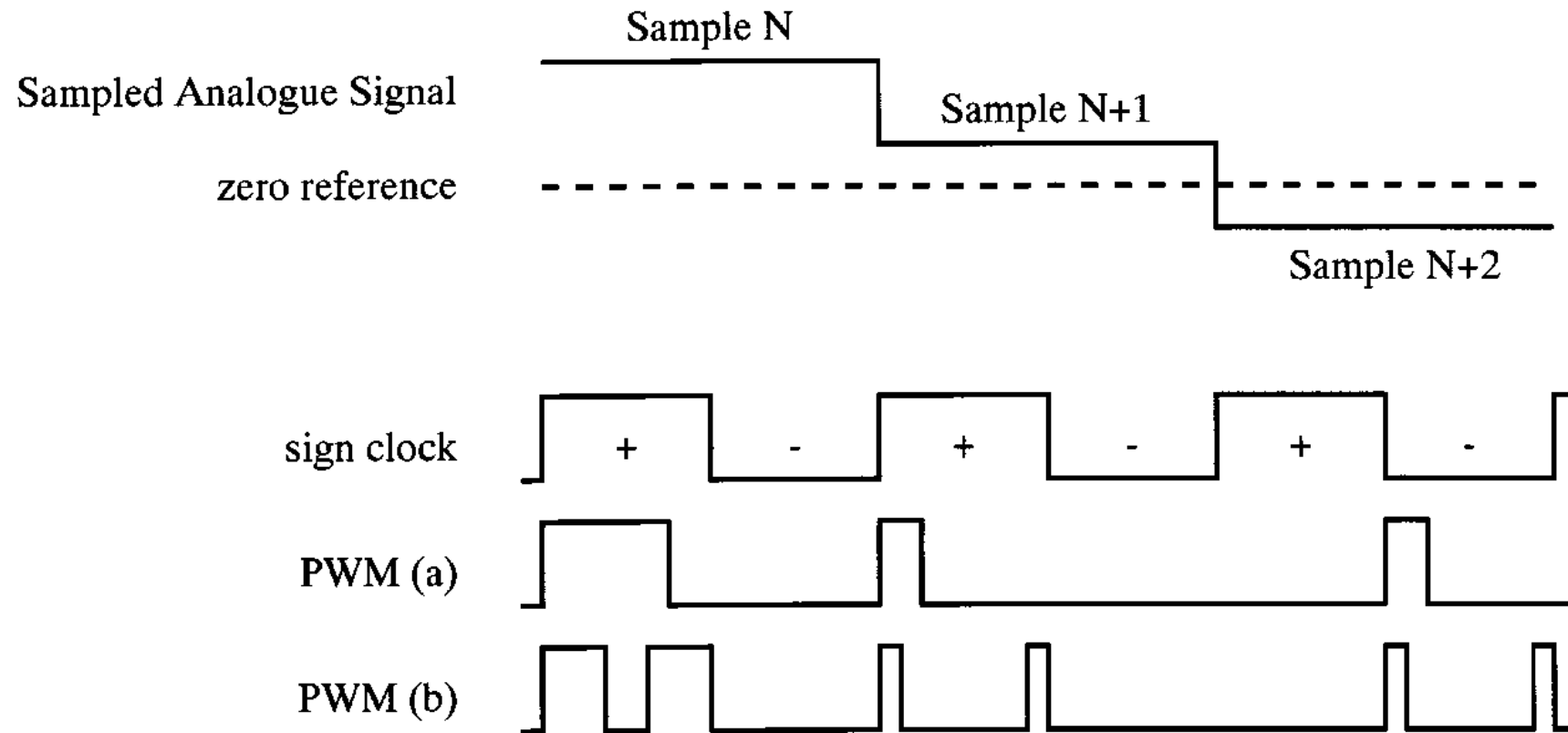


# Pulse based design of CAB

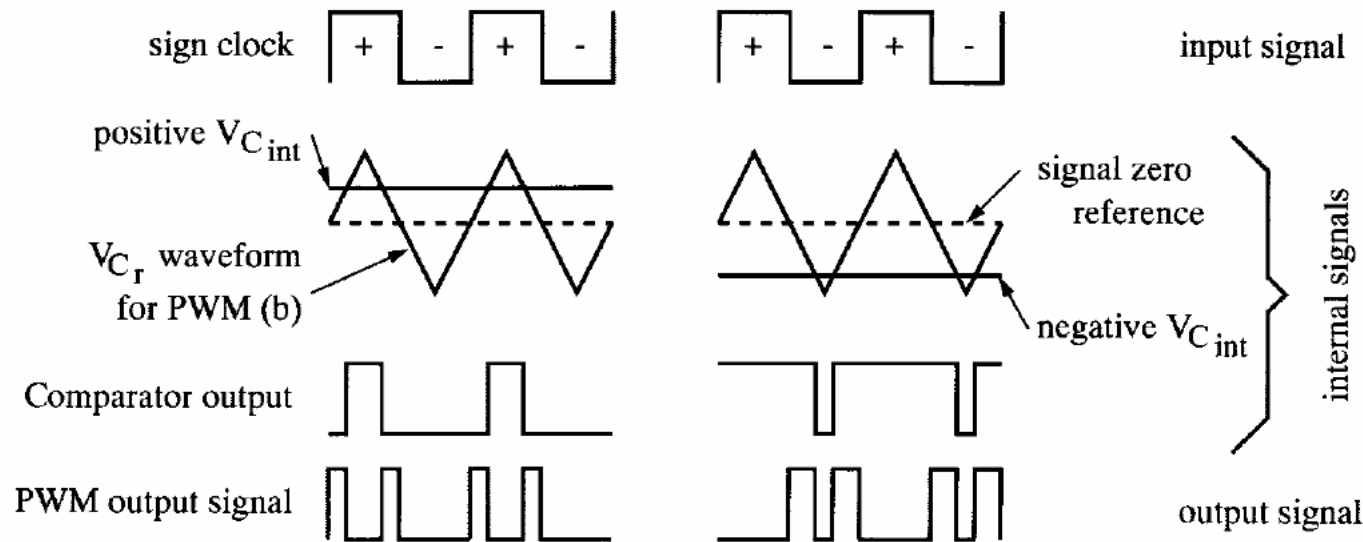
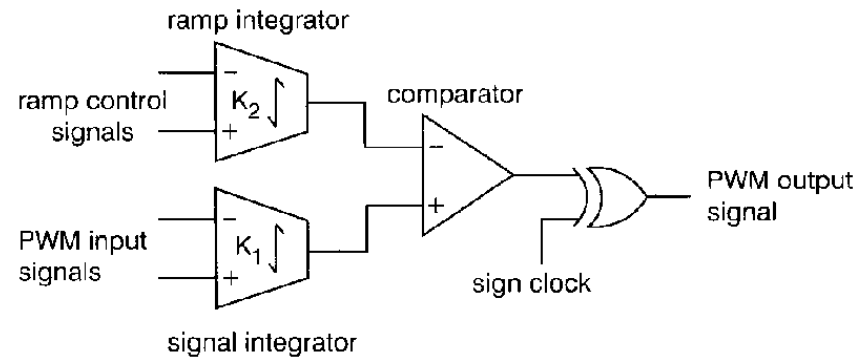
- Uses time to represent transmitted signal in the form of PWM
- Uses of digital signals levels
  - Noise immunity
- Relatively new area of research
  - Limited functionality
  - Complete design not yet available



# Two forms of PWM signals

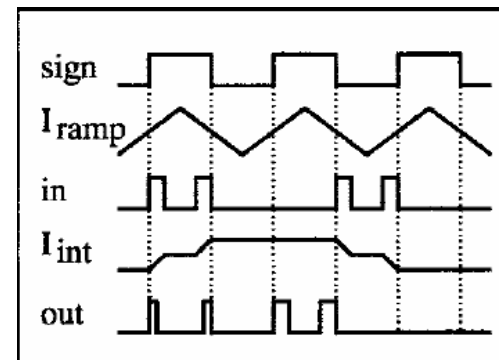
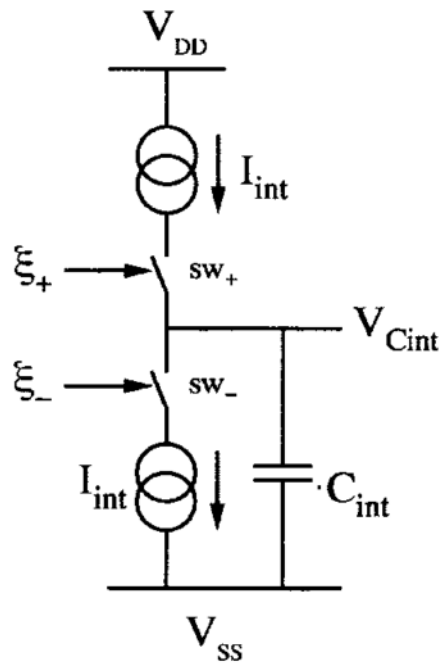


# Pulse Signals

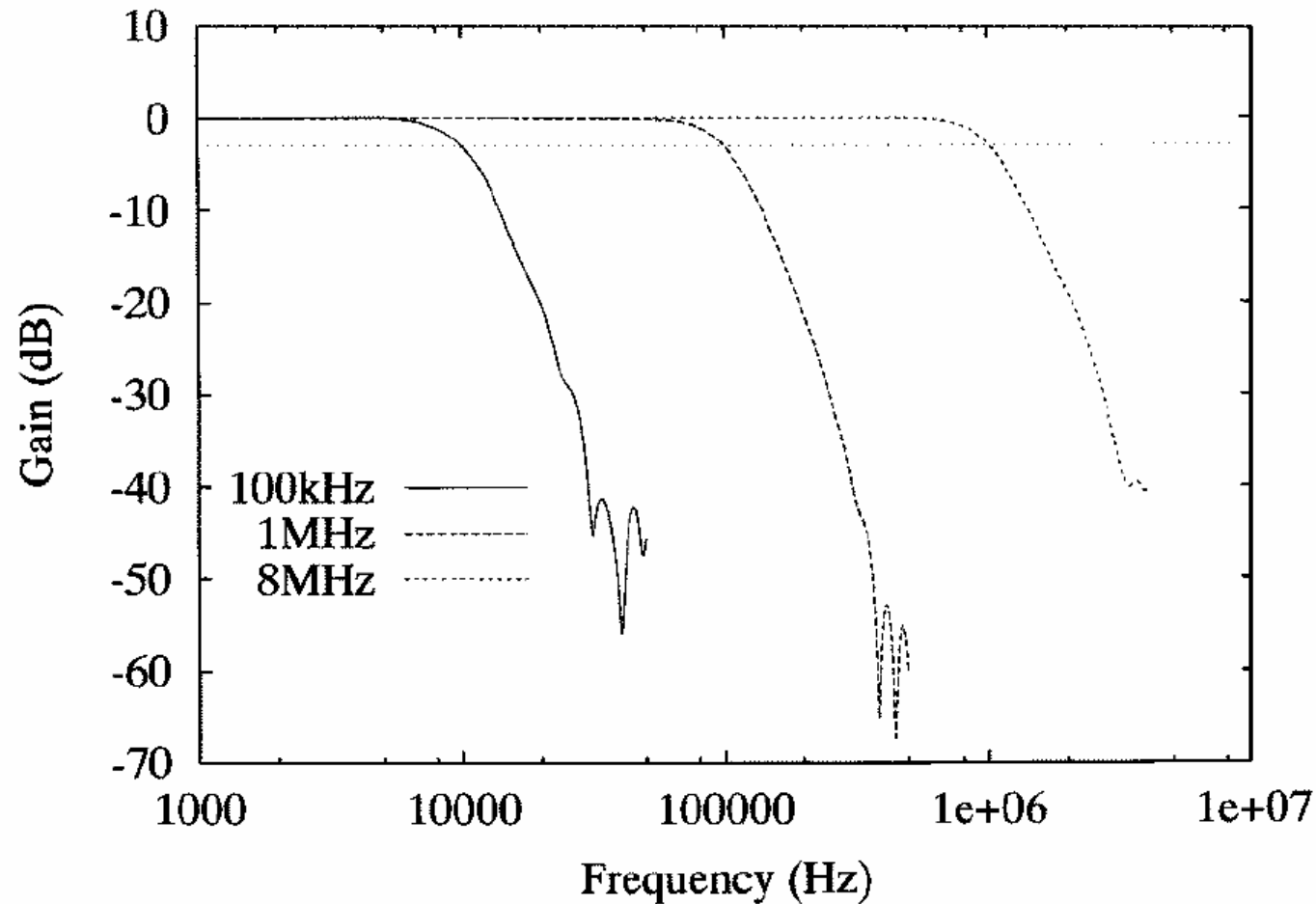




# Pulse based Integrator



# Pulse based Performance



# Future of FPAA's

- SC designs will dominate commercially
  - Improvements must be achieved
- FPAA's may lead to FPMAs
  - Natural evolution of mixed-signal design
- Question of viability must be answered
  - FPAA's vs. FPGA comparison
  - 8MHz vs. +1Gbps



# Questions?

