Single Cycle ALU Control Logic Design

Suresh Purini, IIIT-H

Consider the following Arithmetic and Logic Unit whose functional specification is given in the table adjacent to it.

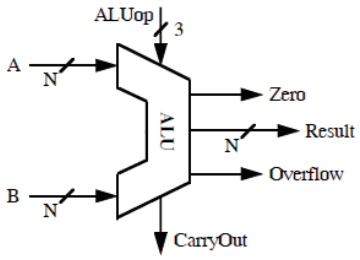

Figure 1: Arithmetic and Logic Unit

ALU Control Lines (ALUop)	Function
000	ADD
001	SUB
010	OR
011	AND

Figure 2: Functional Specification of ALU

Figure 3 shows the high-level picture of the control logic circuitry which is organized into two stages: Main Control and ALU Control.

op	00 0000	00 1101	10 0011	10 1011	00 0100	00 0010
	R-type	ori	lw	sw	beq	jump
RegDst	1	0	0	x	x	x
ALUSrc	0	1	1	1	0	x
MemtoReg	0	0	1	x	x	x
RegWrite	1	1	1	0	0	0
MemWrite	0	0	0	1	0	0
Branch	0	0	0	0	1	0
Jump	0	0	0	0	0	1
ExtOp	x	0	1	1	x	x
ALUop (Symbolic)	"R-type"	Or	Add	Add	Subtract	xxx
ALUop <2>	1	0	0	0	0	x
ALUop <1>	0	1	0	0	0	x
ALUop <0>	0	0	0	0	1	x

Figure 3: Control Path

Main Control will generate all the control signals except the ALUop control signals. If the

instruction is an R-type instruction, the Main Control will indicate that fact to the ALU control circuit (by generating signal 100). In this case, the ALU control logic would check the *funct* bits and generate the appropriate ALUop control signals. If the current instruction is not an R-type instruction, the control logic itself would generate appropriate ALUop control signals which are communicated to the ALU Control Logic and it will in turn communicate the same to the ALU.

Homework Question: Design the ALU Control Logic?