VLSI Architectural Optimization

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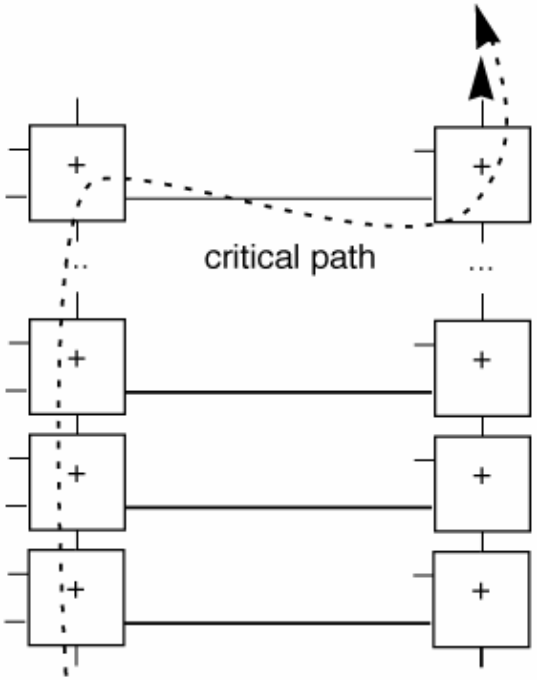
Single Cycle Operation

Some high level synthesis allows multiple computations being done on single clock cycle. The principle of performing more than operations in one clock cycle is called operator chaining.

Operator chaining

- May execute several operations in sequence in one cycle—operator chaining.
- Delay through function units may not be additive, such as through several adders.



Control implementation

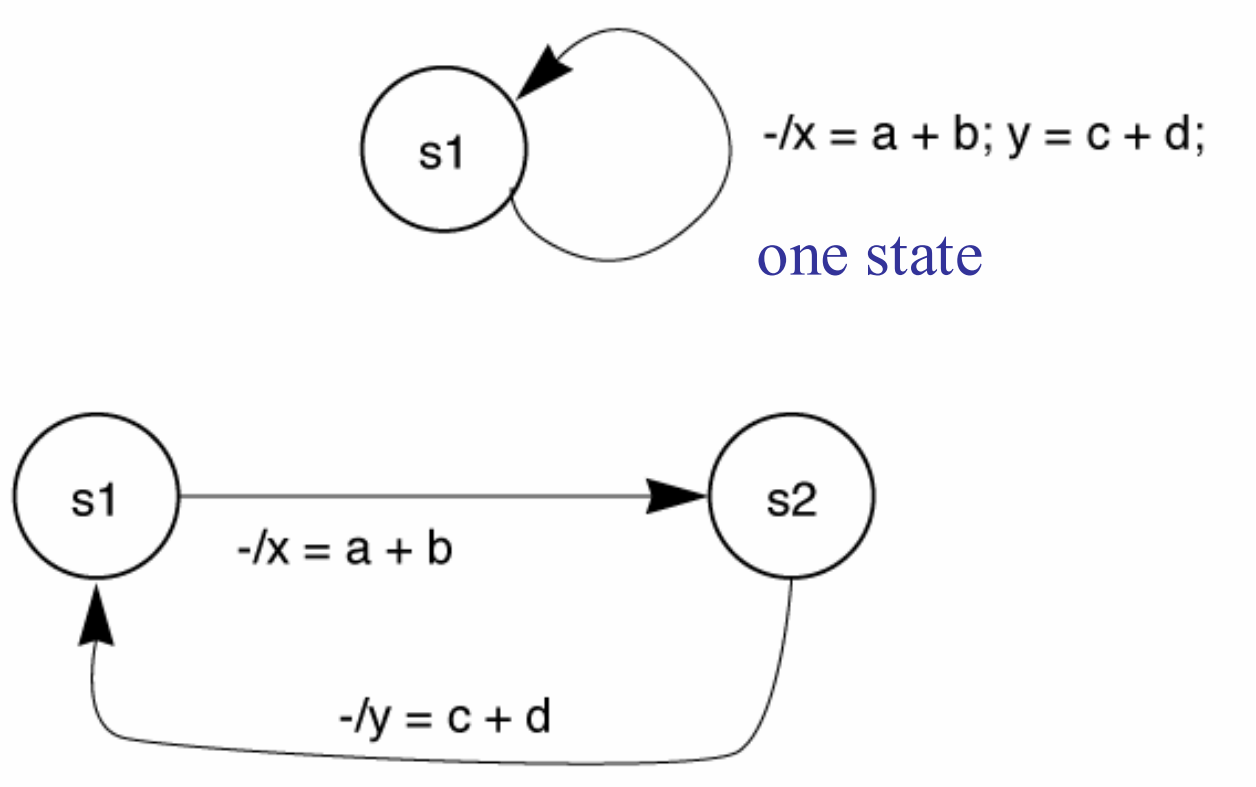
- Clock cycles are also known as control steps.
- Longer schedule means more states in controller.
- Cost of controller may be hard to judge from casual inspection of state transition graph.

Controllers and scheduling

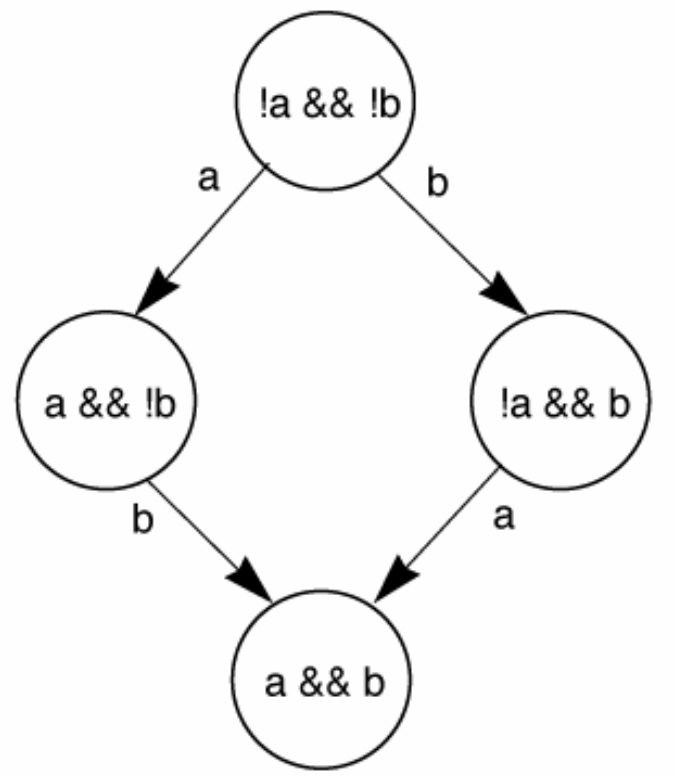
functional model:

x <= a + b;

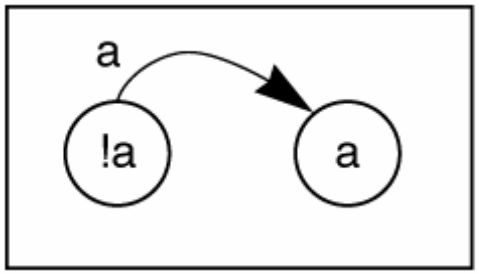
y <= c + d;

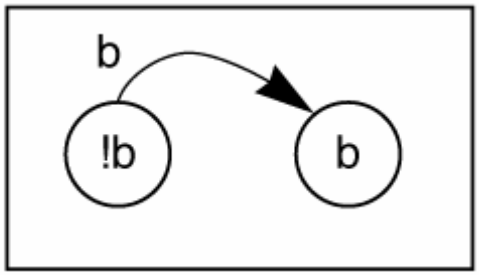


Distributed control



one centralized controller

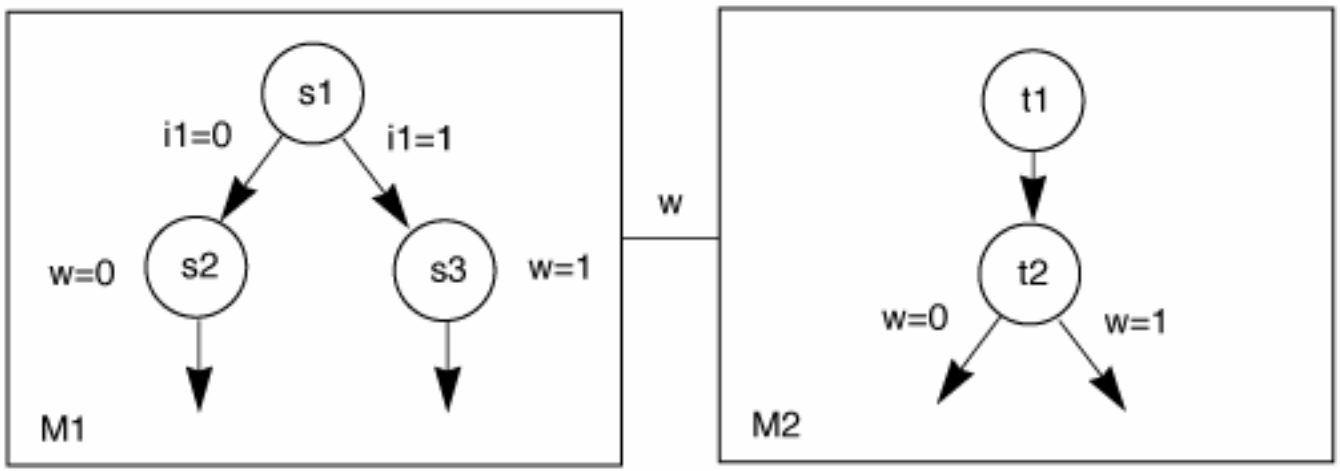




two distributed controllers

Synchronized communication between FSMs

To pass values between two machines, must schedule output of one machine to coincide with input expected by the other:

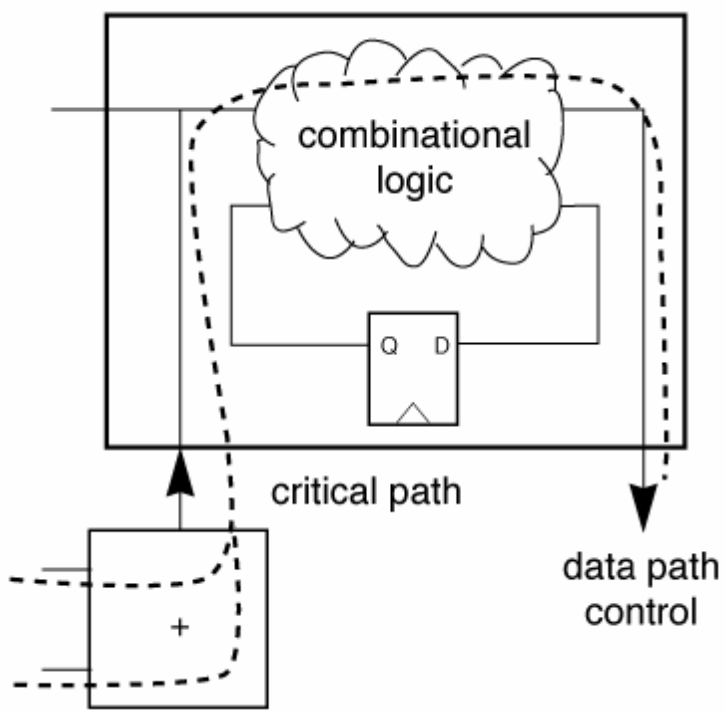


Hardwired vs. microcoded control

- Hardwired control has a state register and "random logic."
- A microcoded machine has a state register which points into a microcode memory.
- Styles are equivalent; choice depends on implementation considerations.

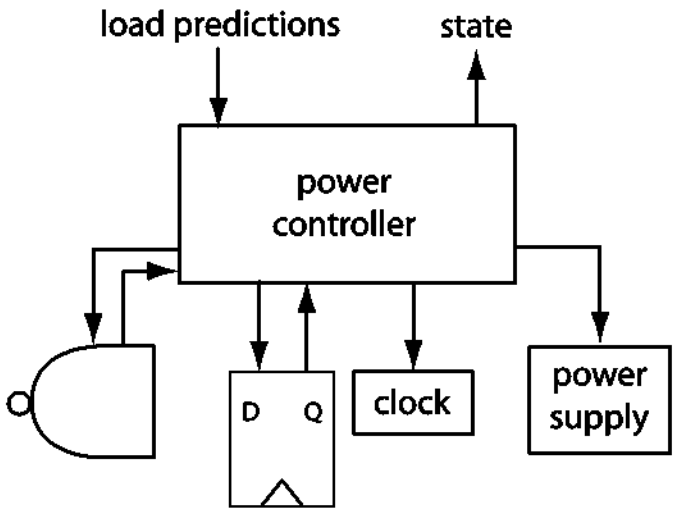
Data path-controller delay

Watch out for long delay paths created by combination of data path and controller:



Architectures for low power

- Power controller examines system state, controls subsystems.

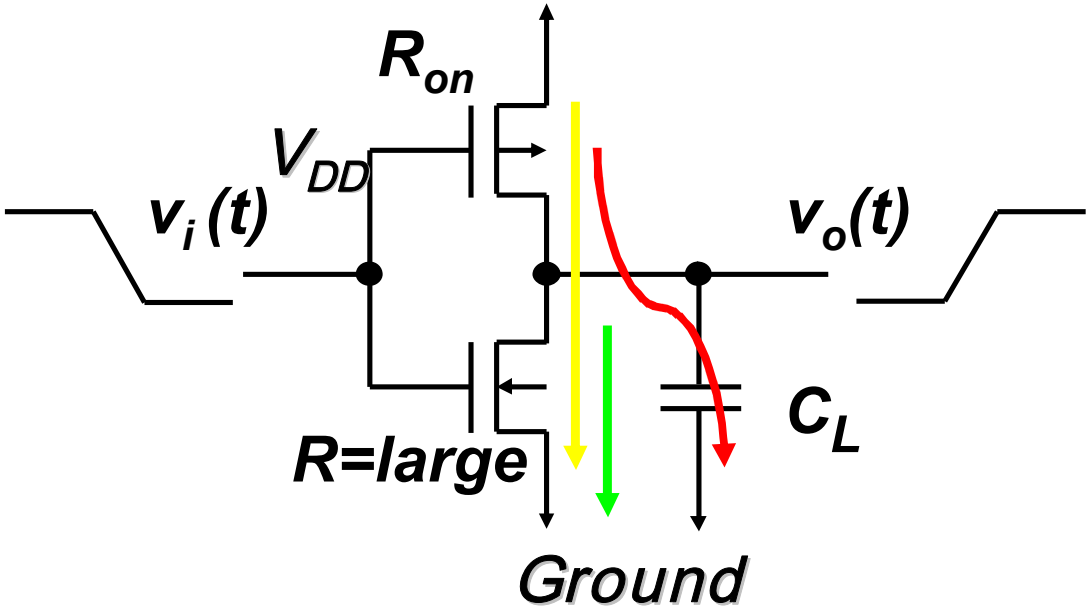


Power components in CMOS circuit

Dynamic power

Leakage power

Short circuit power



$Power = CV_{DD}^2$

Power-down modes

- CMOS doesn't consume power when not transitioning. Many systems can incorporate power-down modes:
  - condition the clock on power-down mode;
  - add state to control for power-down mode;
  - modify the control logic to ensure that power-down/power-up don't corrupt control state.

Gate power control

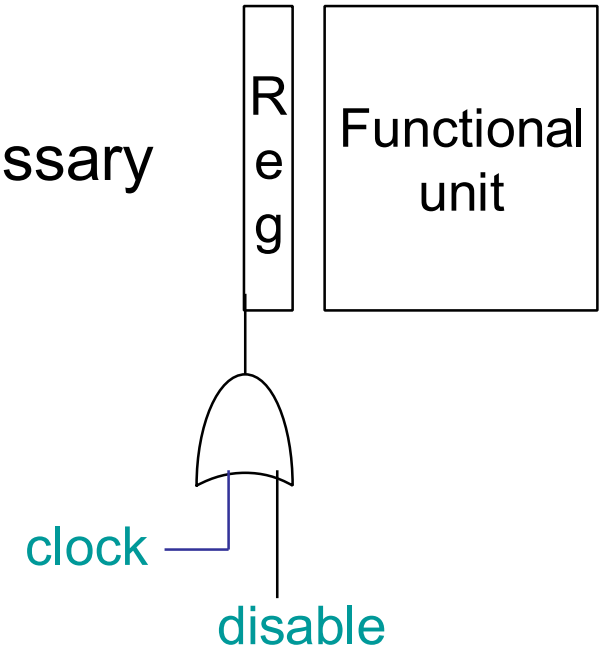
- Some gate types have low power modes.
  - Sleep transistor.
- Can also change substrate voltage in a region.

Data latching

- Store data in registers to avoid glitching in combinational logic.
- Use conditional clocks on existing latches to hold data when not in use.
- Avoid improper use of dynamic storage.

Clock Gating

- Most popular method for power reduction of clock signals and functional units
- Gate off clock to idle functional units
- Logic for generation of disable signal necessary
  - Higher complexity of control logic
  - Higher power consumption
  - Critical timing critical for avoiding of clock glitches at OR gate output
  - Additional gate delay on clock signal

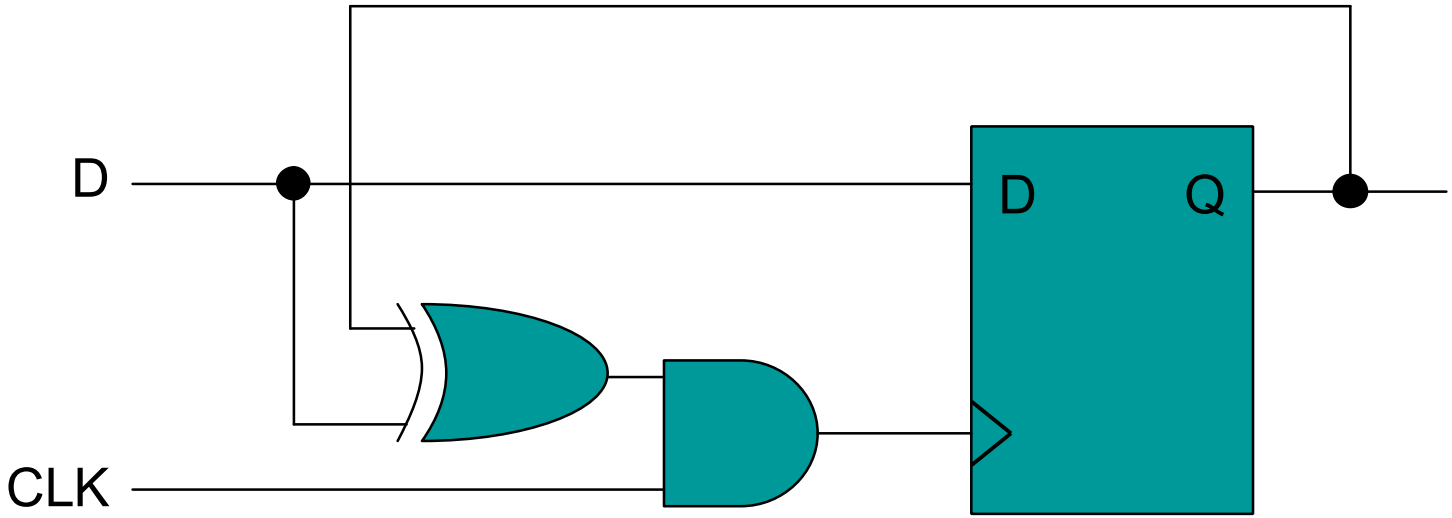


Clock gating

- Clock gating can cause clocked logic to freeze state.
- Must make sure that logic operates properly when frozen, when turned back on.
- Must carefully design clock network with gating to avoid skew, etc.

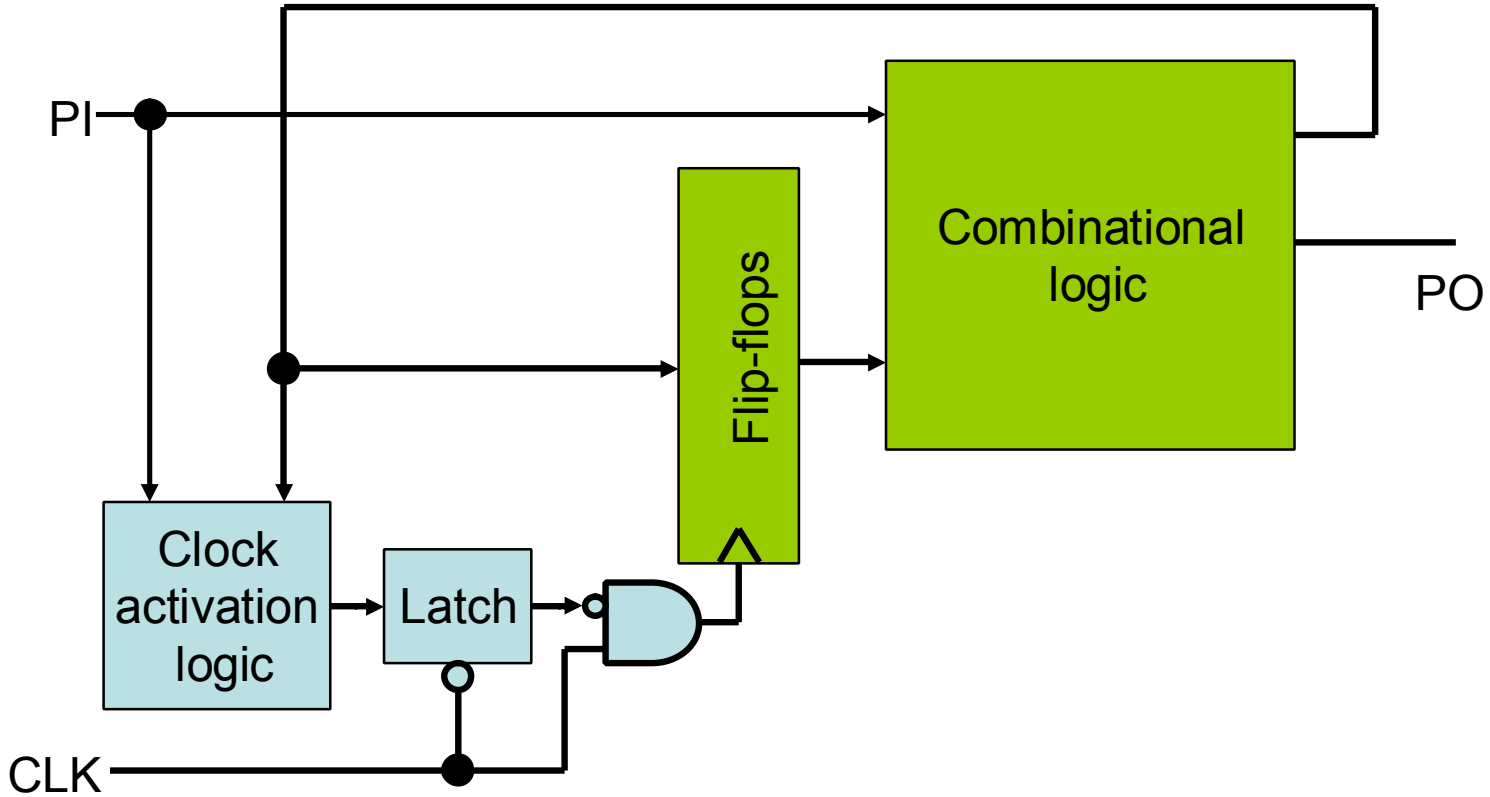
Clock Gating

- Clock-Gating in Low-Power Flip-Flop

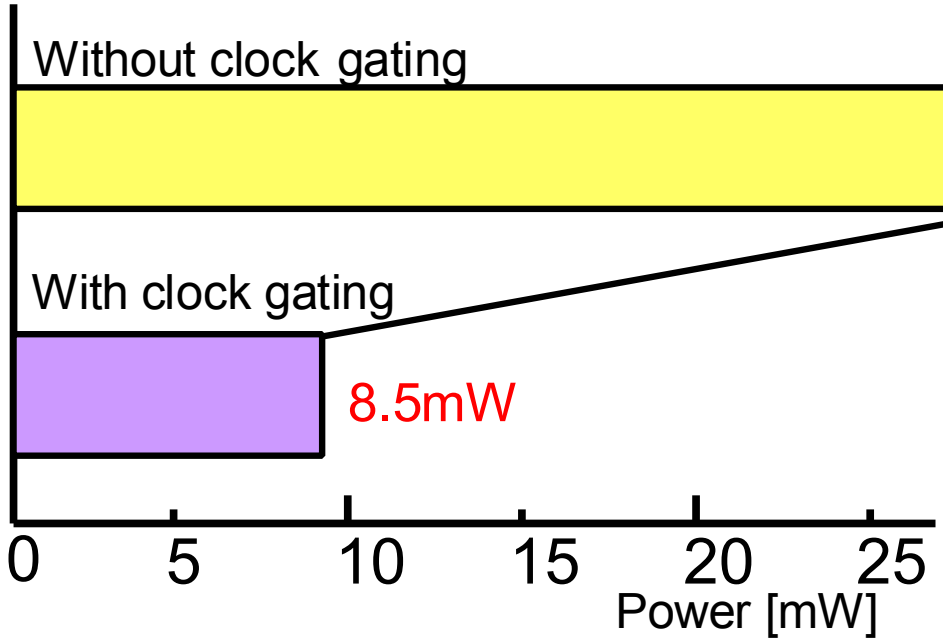


Clock Gating

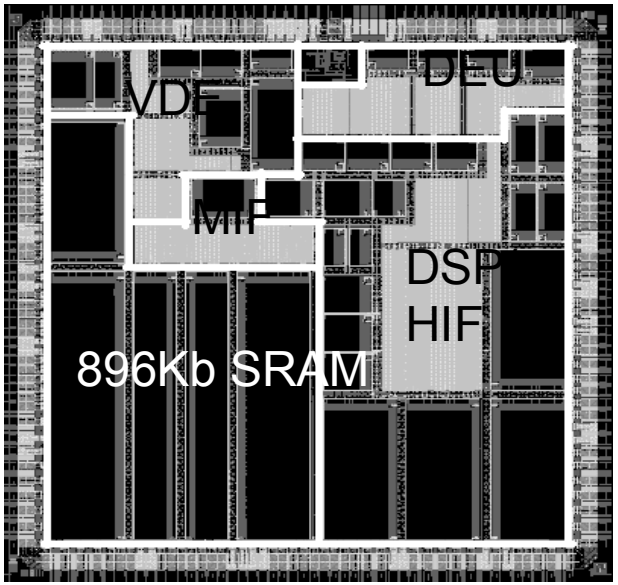
- Clock gating over consideration of state in Finite-State-Machines (FSM)



Clock Gating: Example



- 90% of FlipFlops clock-gated
- 70% power reduction by clock-gating

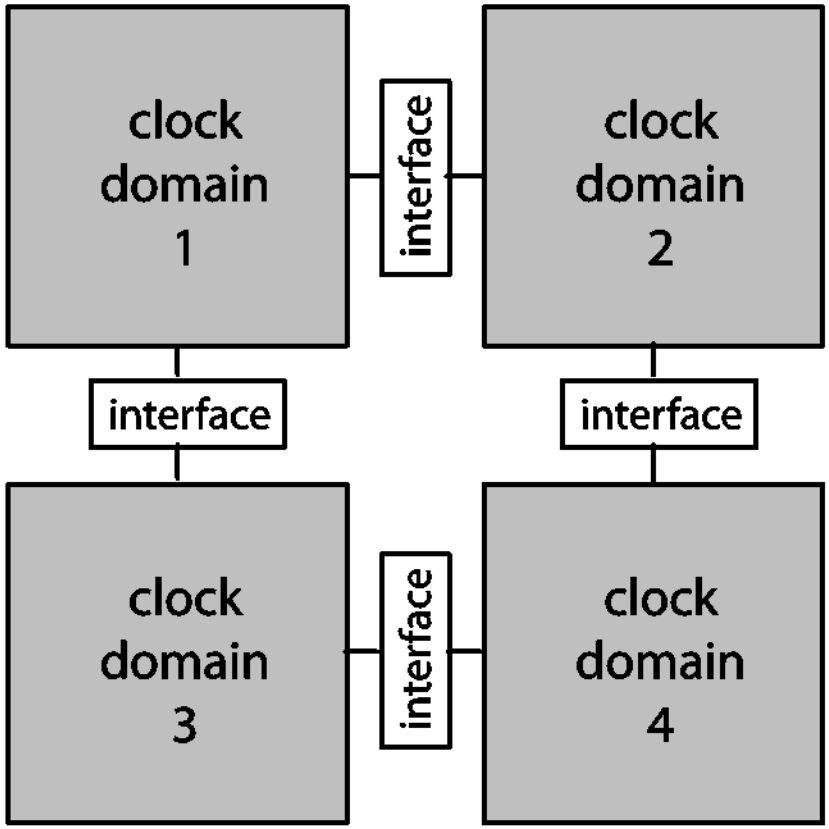


MPEG4 decoder

GALS design

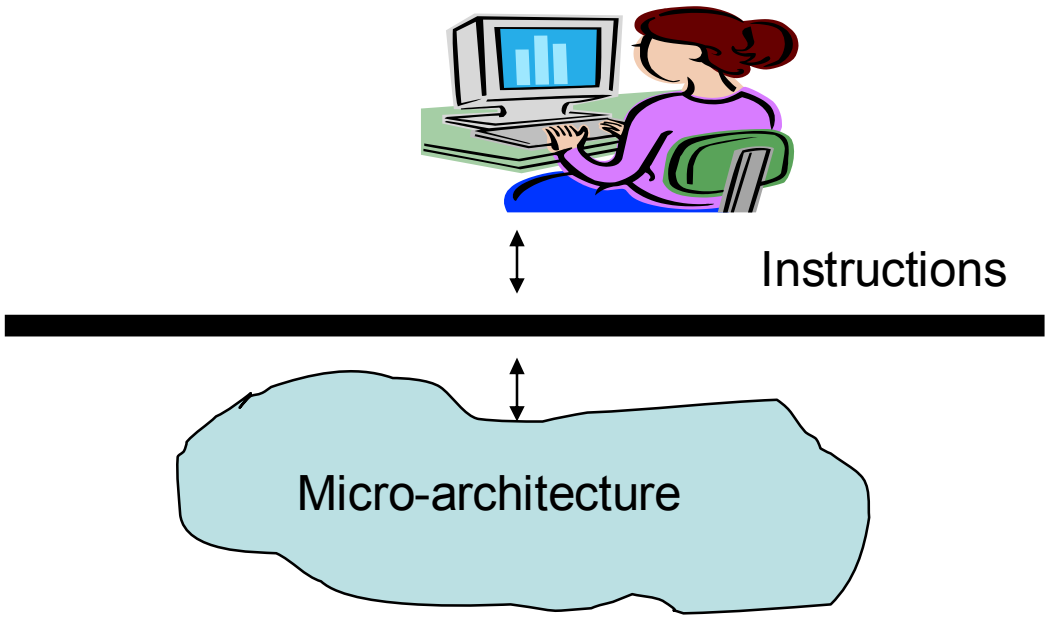
- Globally asynchronous, locally synchronous design uses different clock domains for different parts of the chips.
- Styles:
  - Pausable clocks.
  - Asynchronous interfaces.
  - Loosely synchronous interfaces.

GALS structure



Processors: What is different?

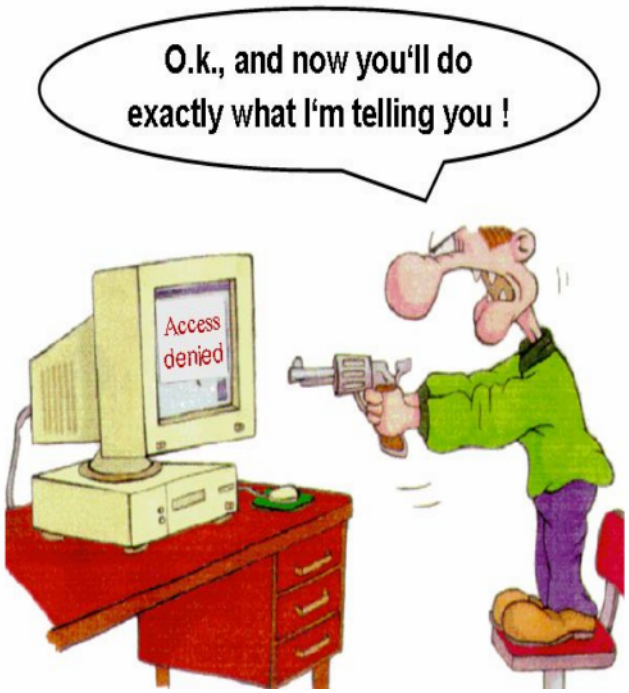
- Processors vis-à-vis ASICs are distinguished (or identified) by “instructions” being associated with control
- These instructions “isolate” the user from the micro-architectural details and provide an easy programming paradigm



Dynamic voltage and frequency scaling

- Technique for microprocessors:
  - Control power supply voltage and clock.
  - Clock frequency must be in legal range for power supply voltage setting.
- Relies on dynamic workload---microprocessor may not need to run at full speed.
- DVFS controller sets power supply, clock.

Users don't like bugs



Simulation expertice helps

Thank You !!!