

VLSI ARCHITECTURES:

ASSIGNMENT 4:

1. Design and simulate an 8 bit X 8 bit array multiplier using TSMC 180nm CMOS process. Estimate its area, delay and power dissipation.

Ans:

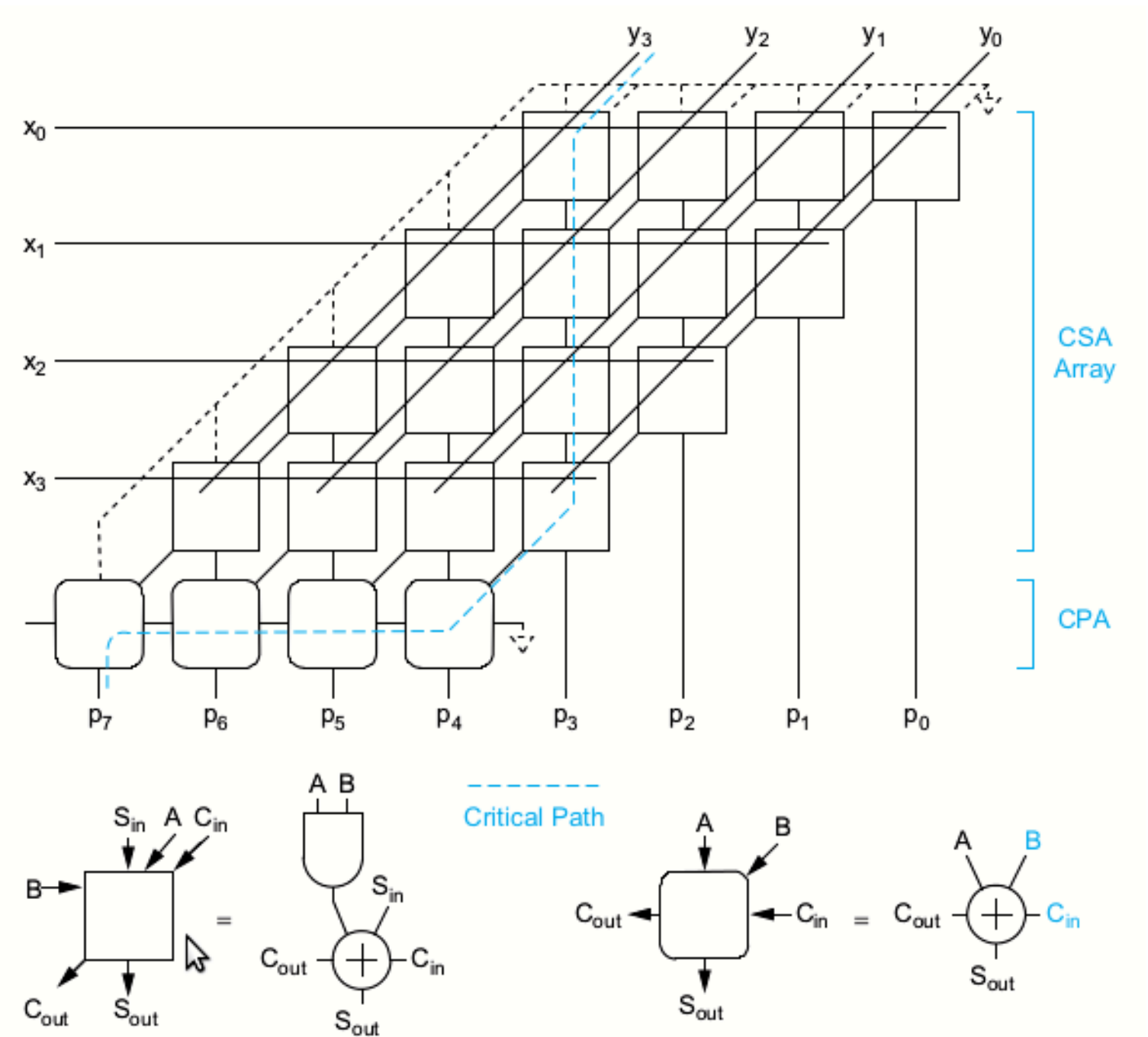


fig: Array multiplier block daigram

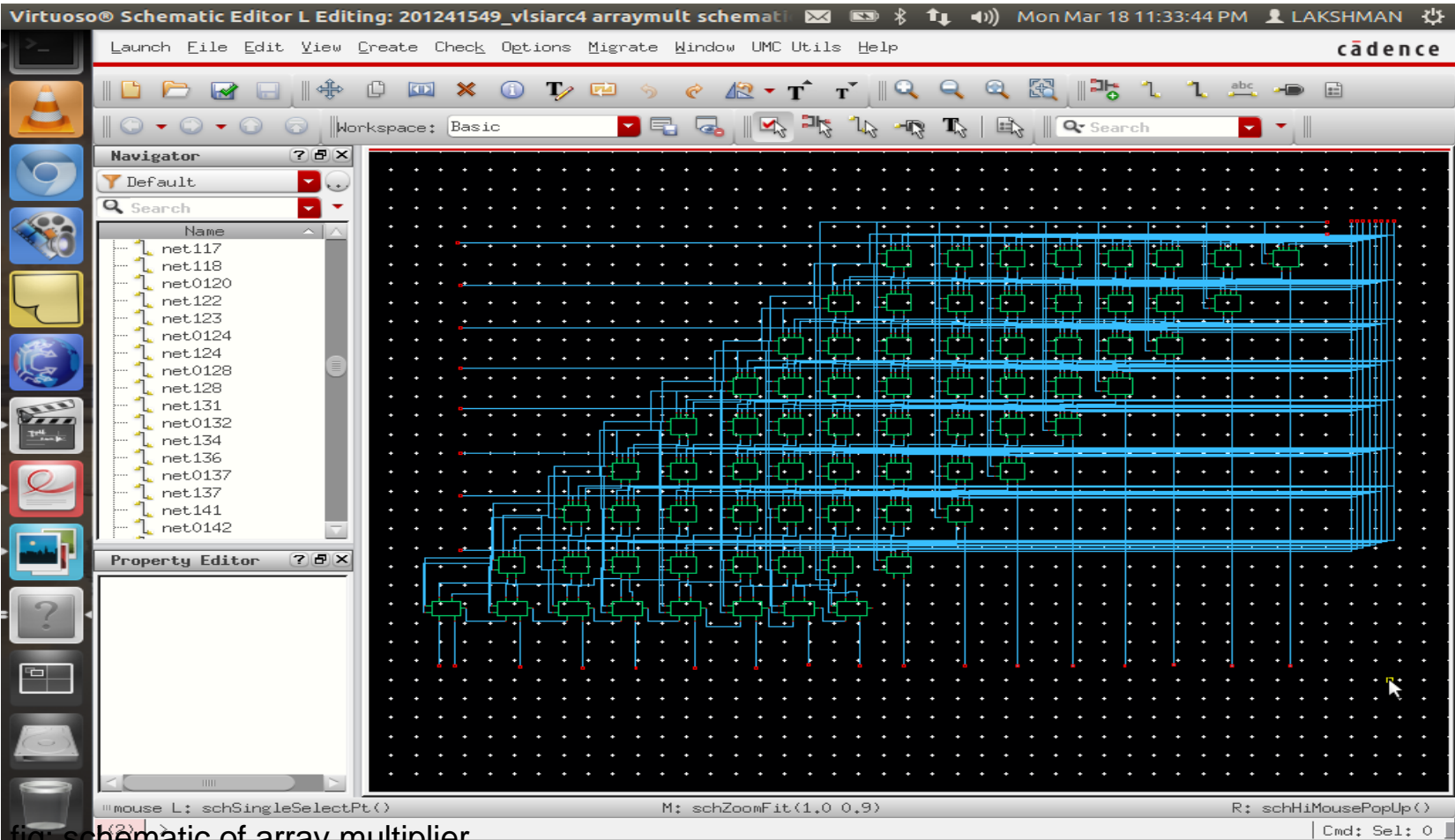
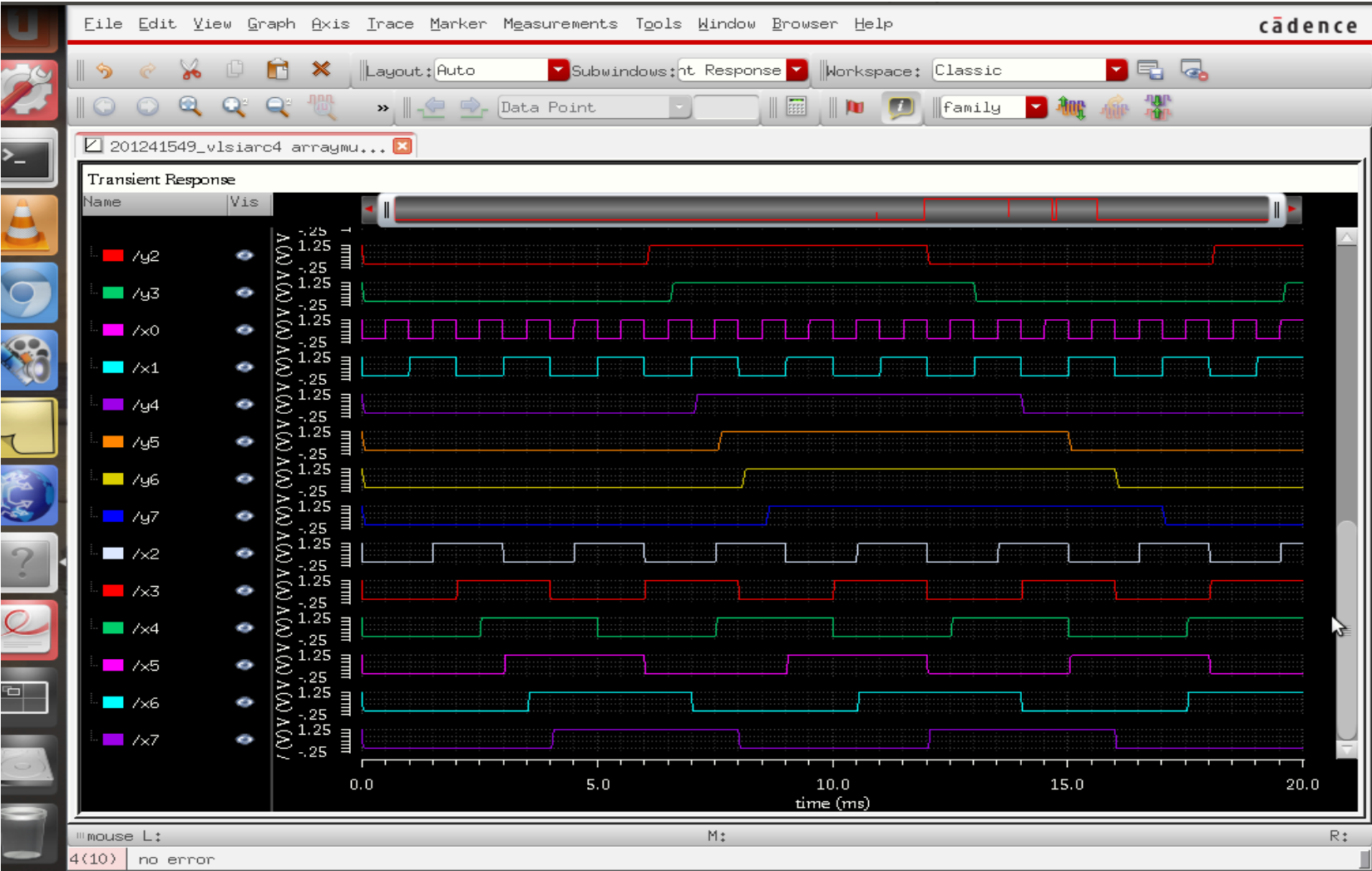
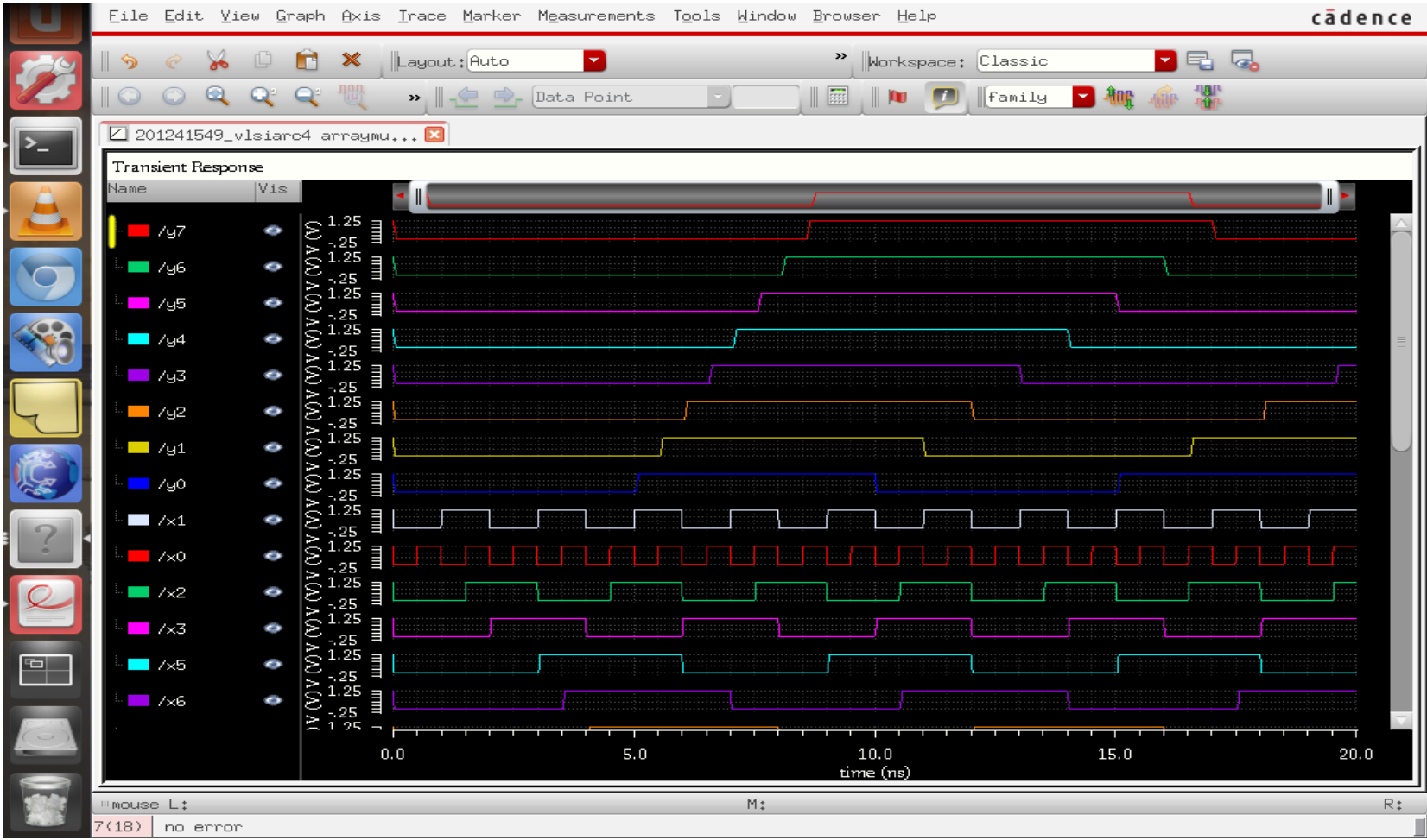
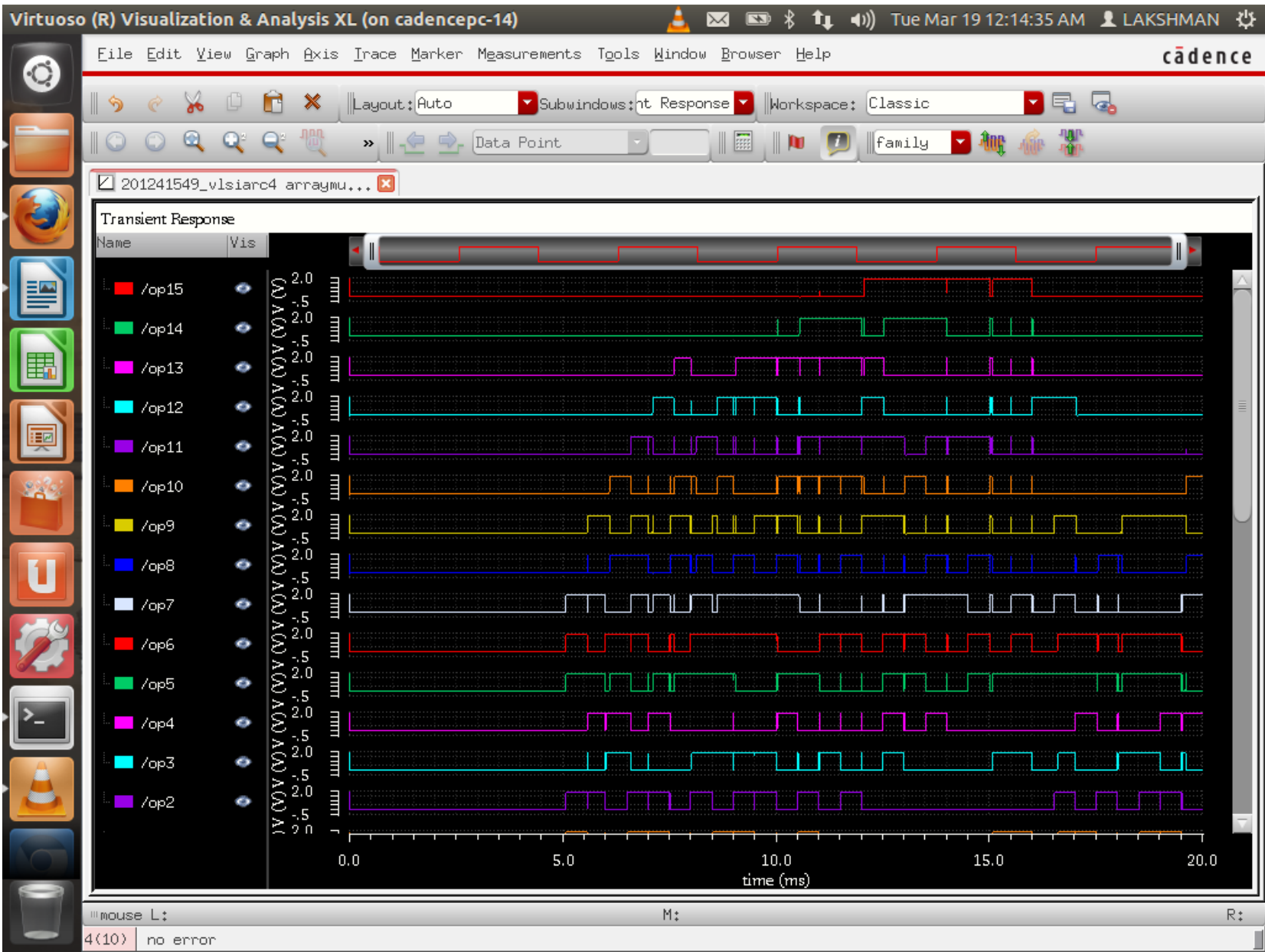


fig. schematic of array multiplier.





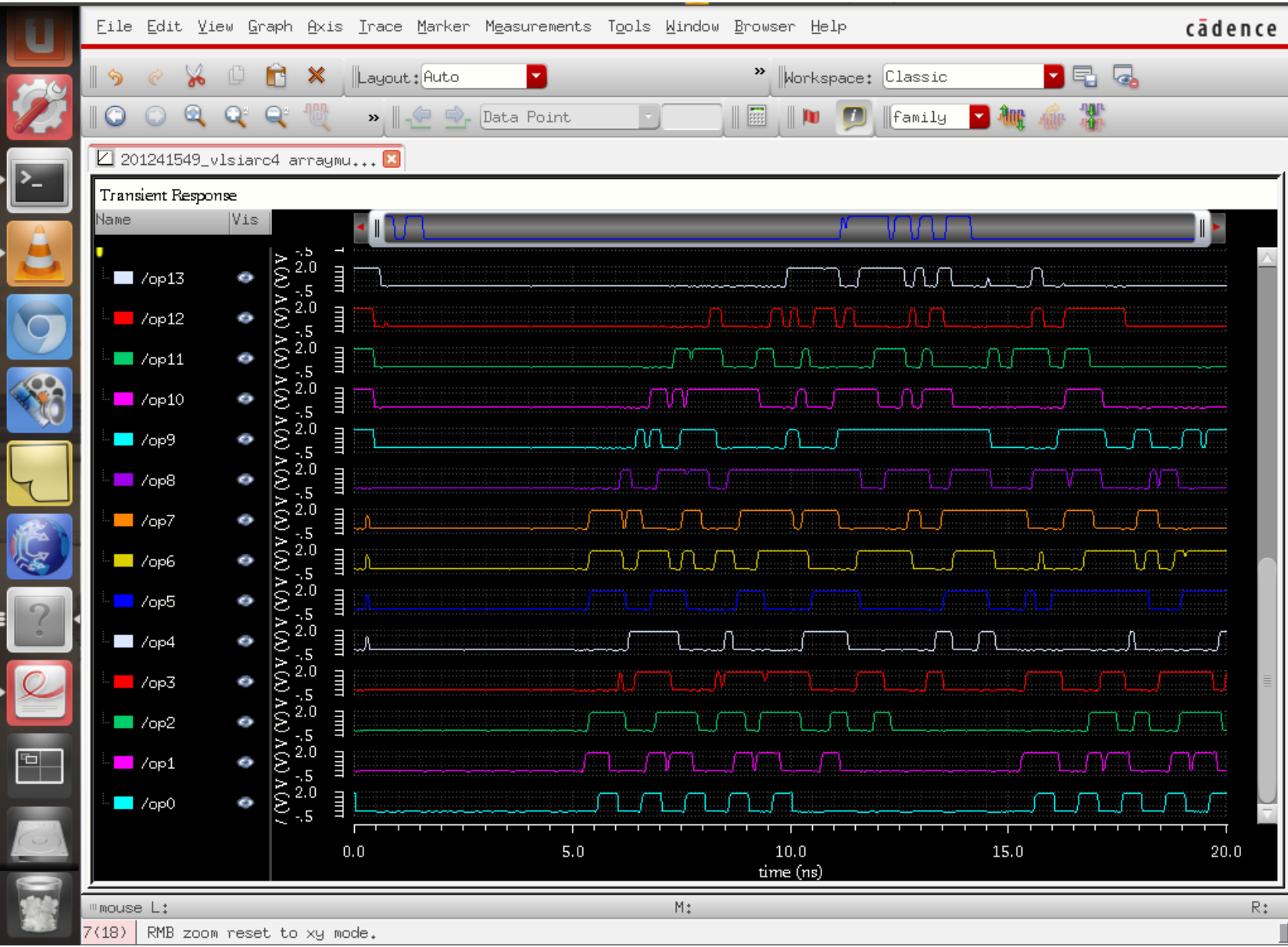


Fig: output wavefoms.

2. Consider the 8 bit multiplicand and multipliers in the previous problem to be signed binary numbers. Implement the multiplier based on Booth’s algorithm using

- a. cascaded linear sequence of carry save adders.
- b. optimized Wallace tree adders

Compare the performances of the two multipliers in terms of area, speed and power dissipation

Ans:

fig:booth Encoder and booth selector.

x_{i+2}	x_{i+1}	x_i	x_{i-1}	Partial Product
0	0	0	0	0
0	0	0	1	Y
0	0	1	0	Y
0	0	1	1	2Y
0	1	0	0	2Y
0	1	0	1	3Y
0	1	1	0	3Y
0	1	1	1	4Y
1	0	0	0	-4Y
1	0	0	1	-3Y
1	0	1	0	-3Y
1	0	1	1	-2Y
1	1	0	0	-2Y
1	1	0	1	-Y
1	1	1	0	-Y
1	1	1	1	-0

Fig: booth encoding table.

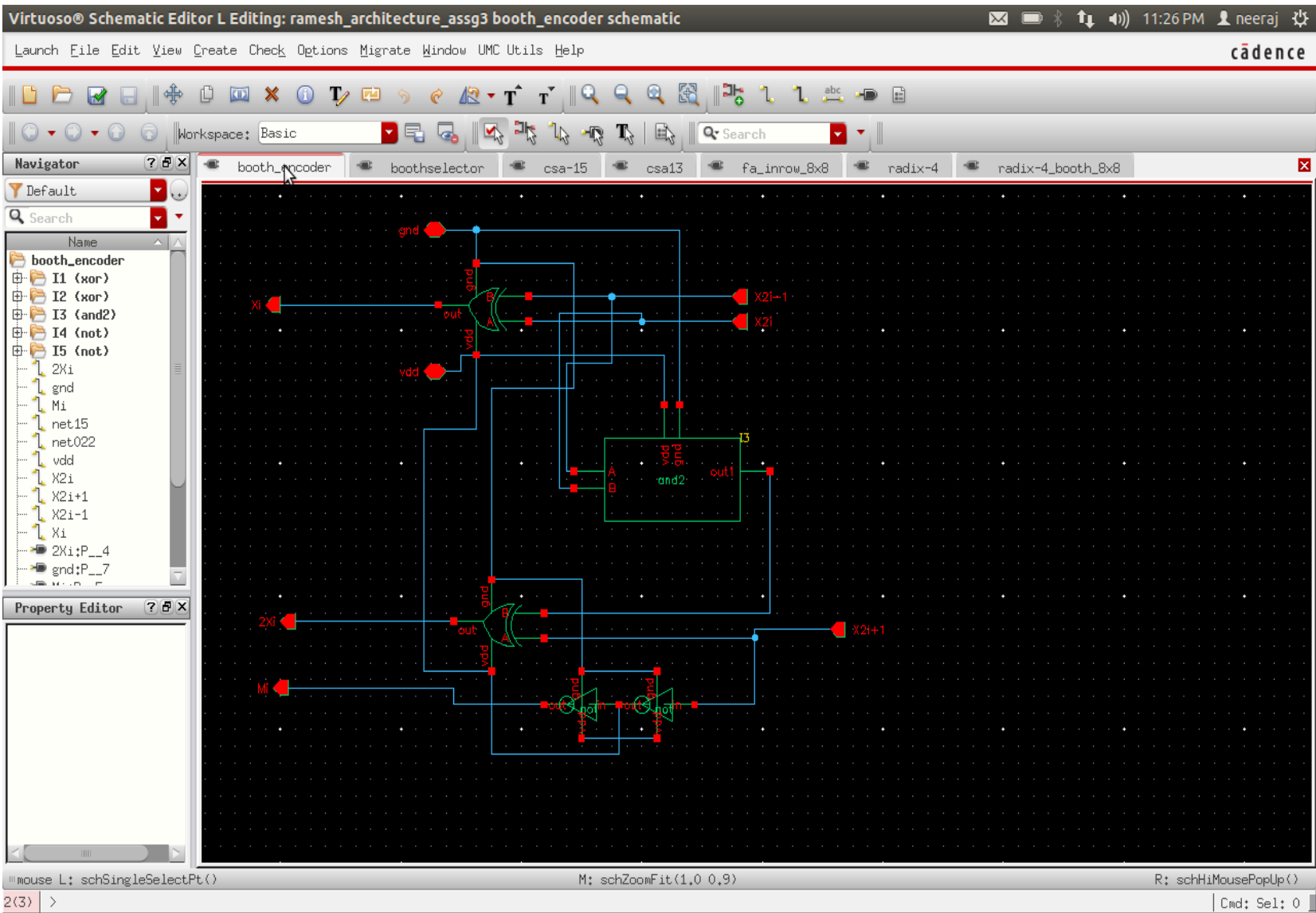


Fig: booth Encoder.

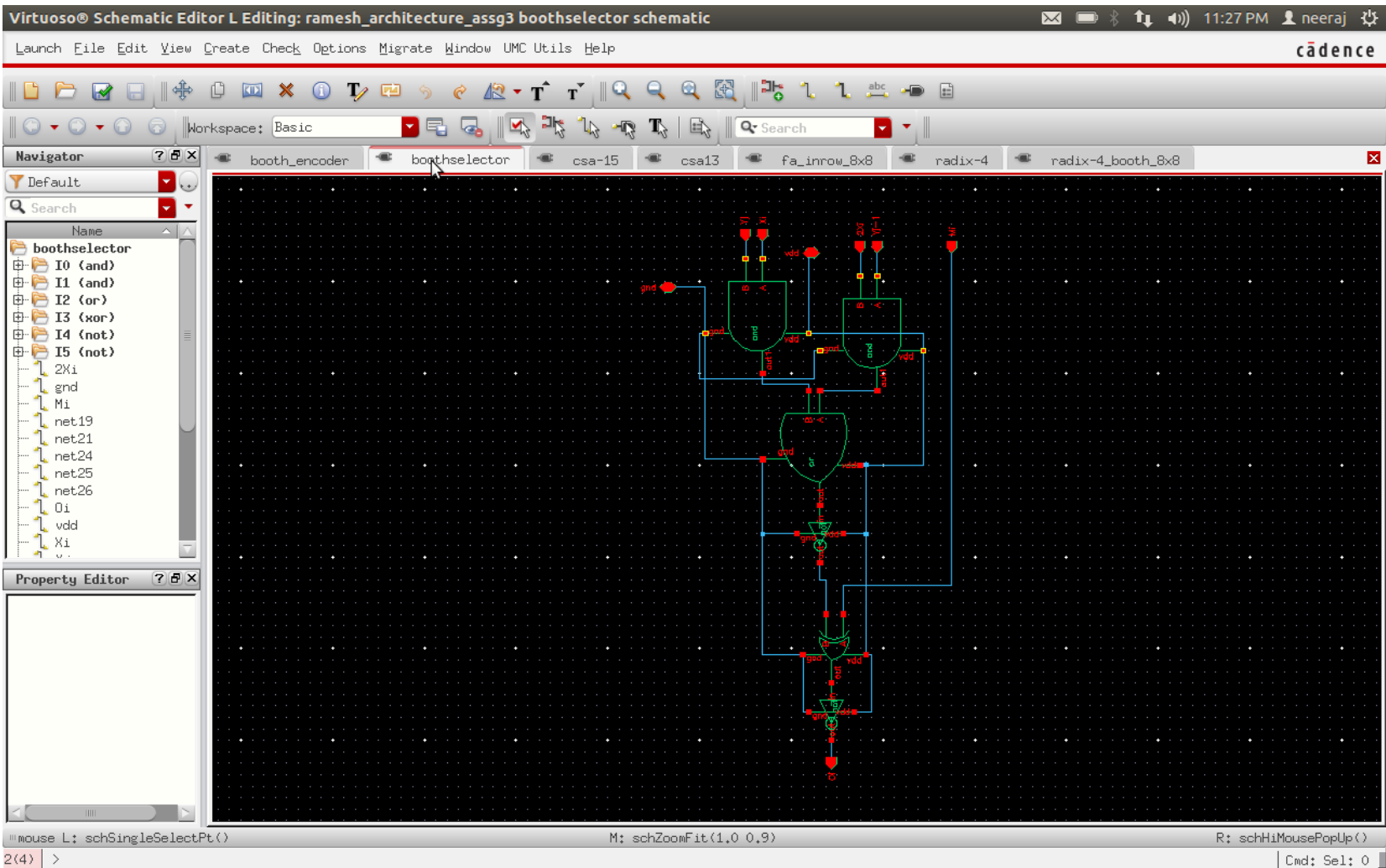


Fig:booth selector

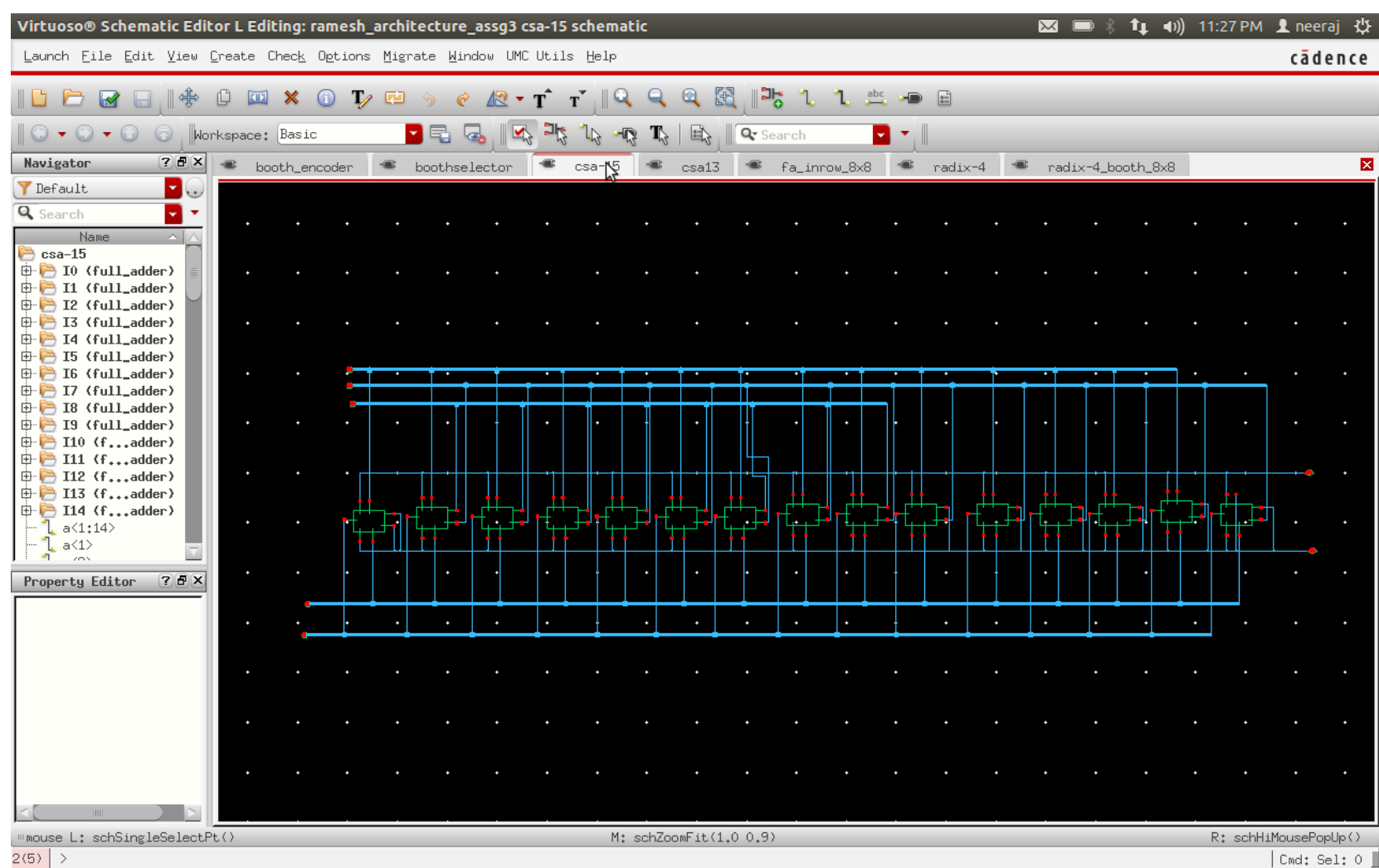


fig: 15 bit cay save adder

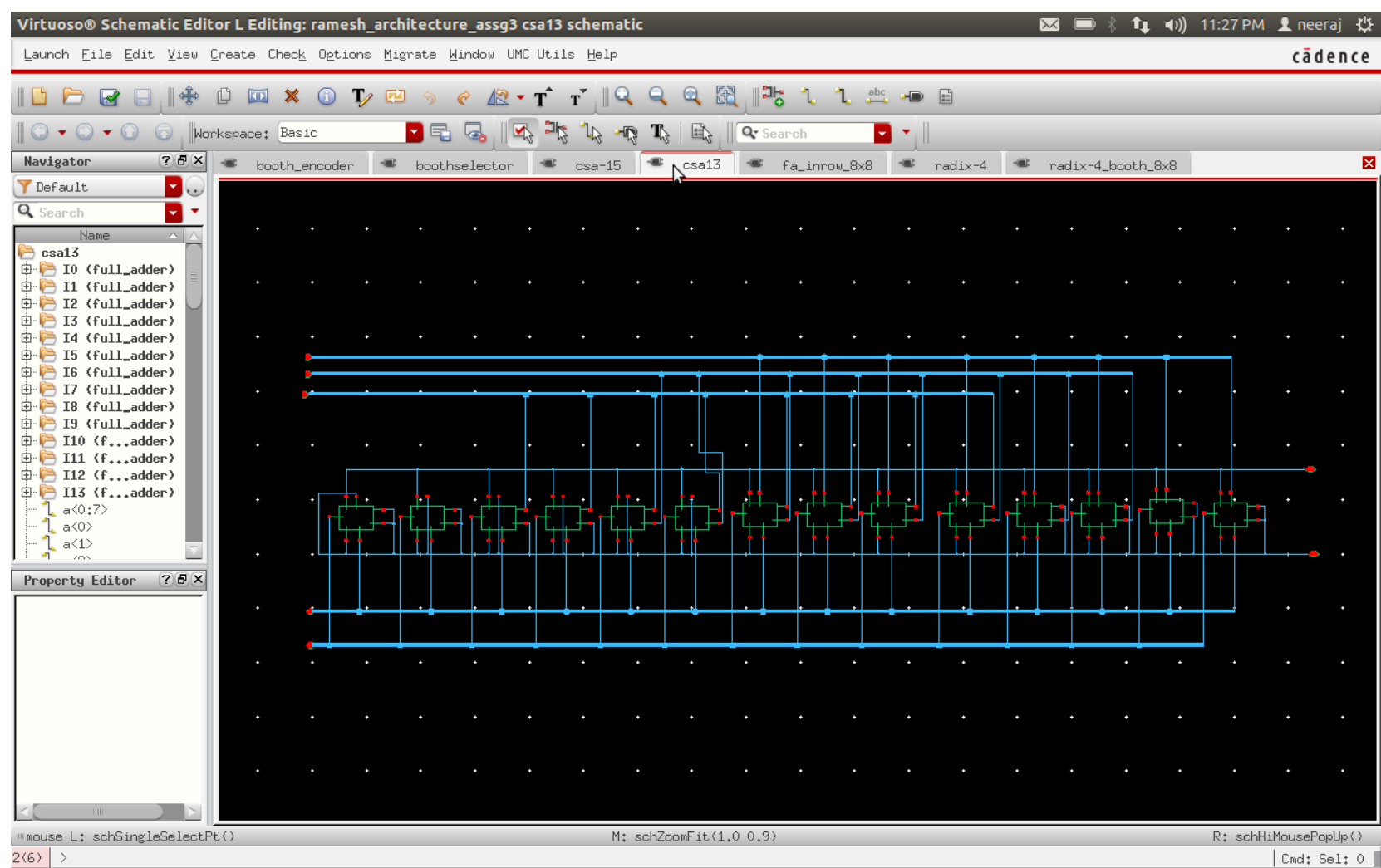


fig: carry save adder 14-bit.

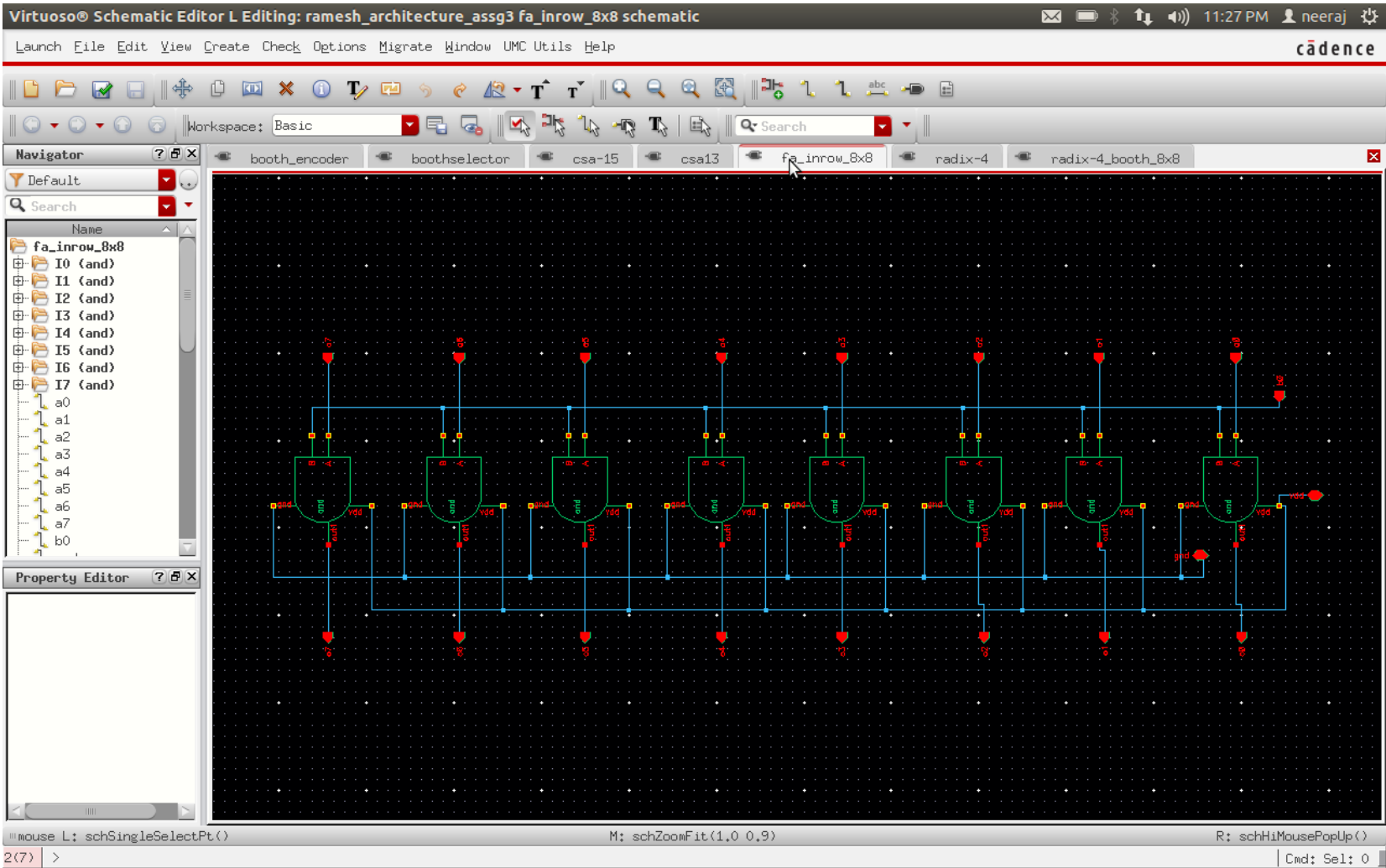
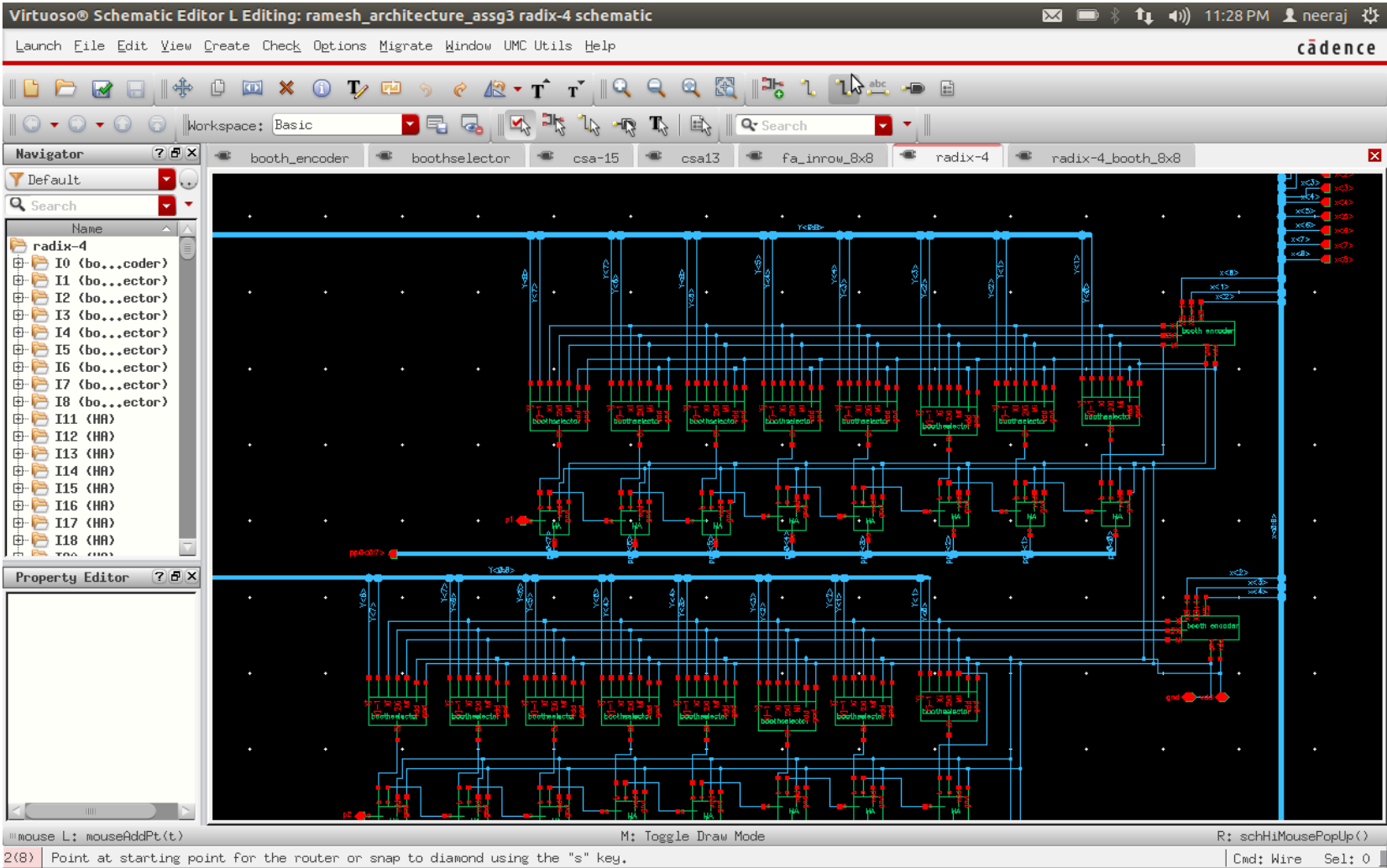


Fig: 8-bit carry save adders.



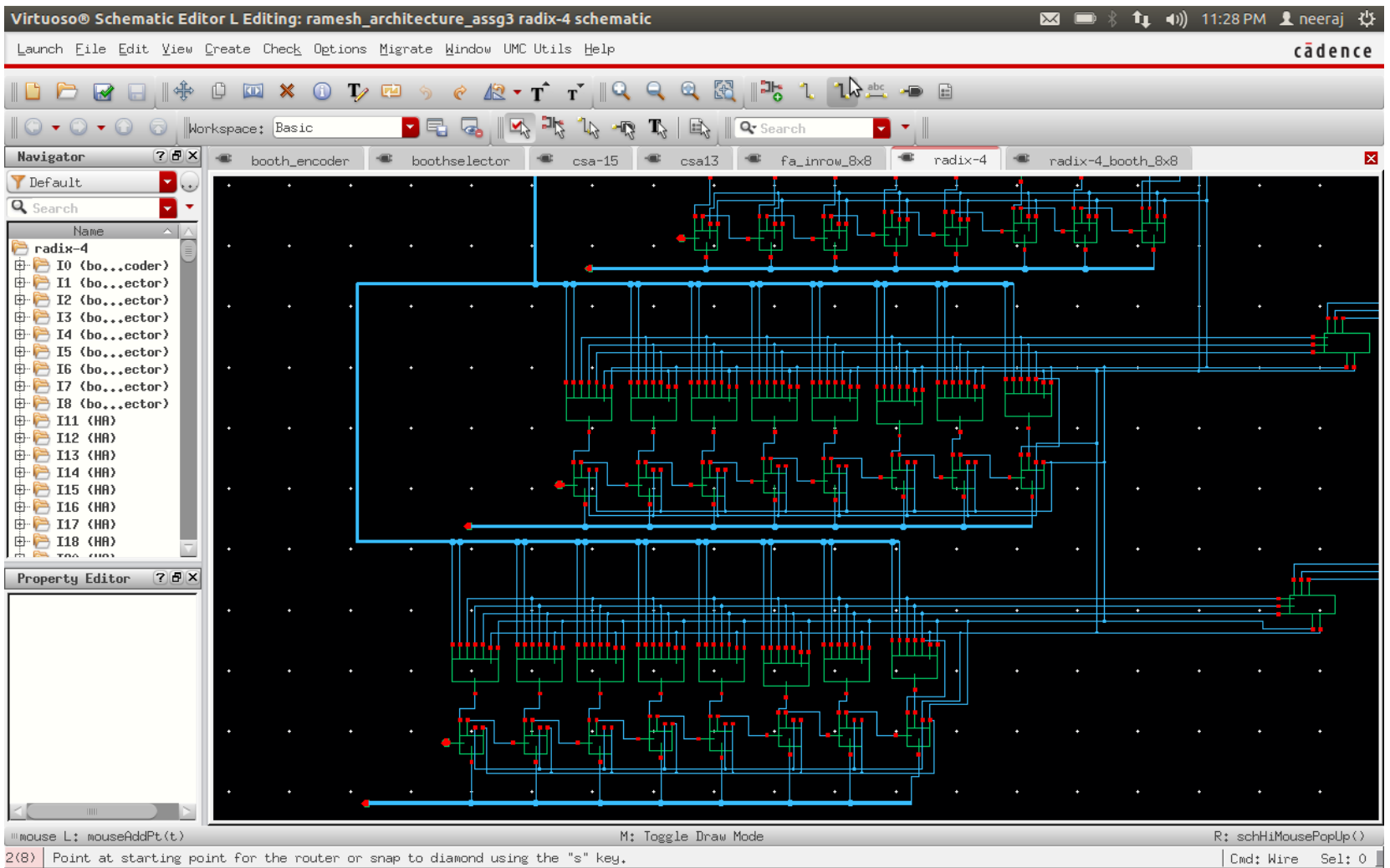


Fig: radix-4 booth multiplier.

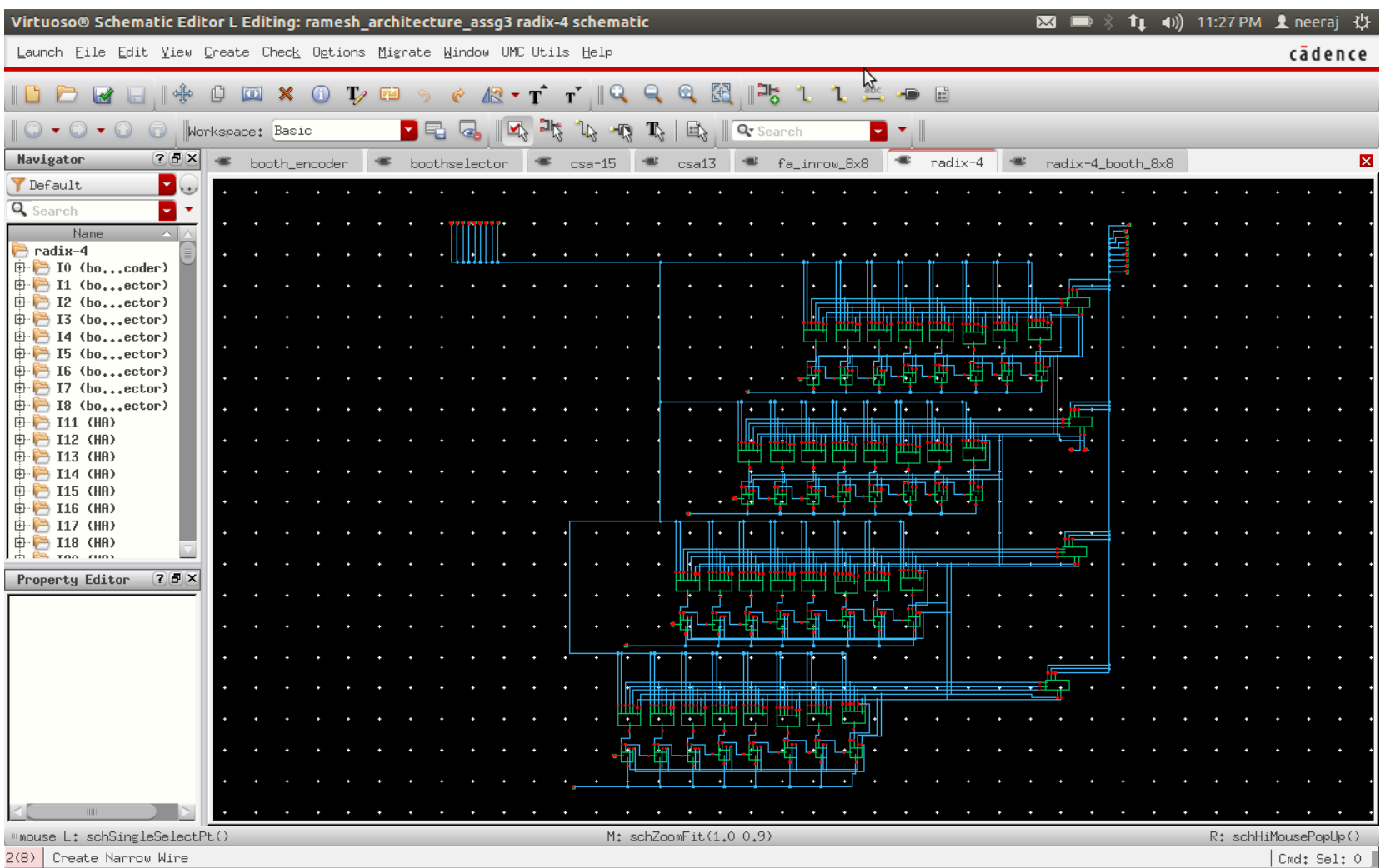


Fig:radix booth multiplier.

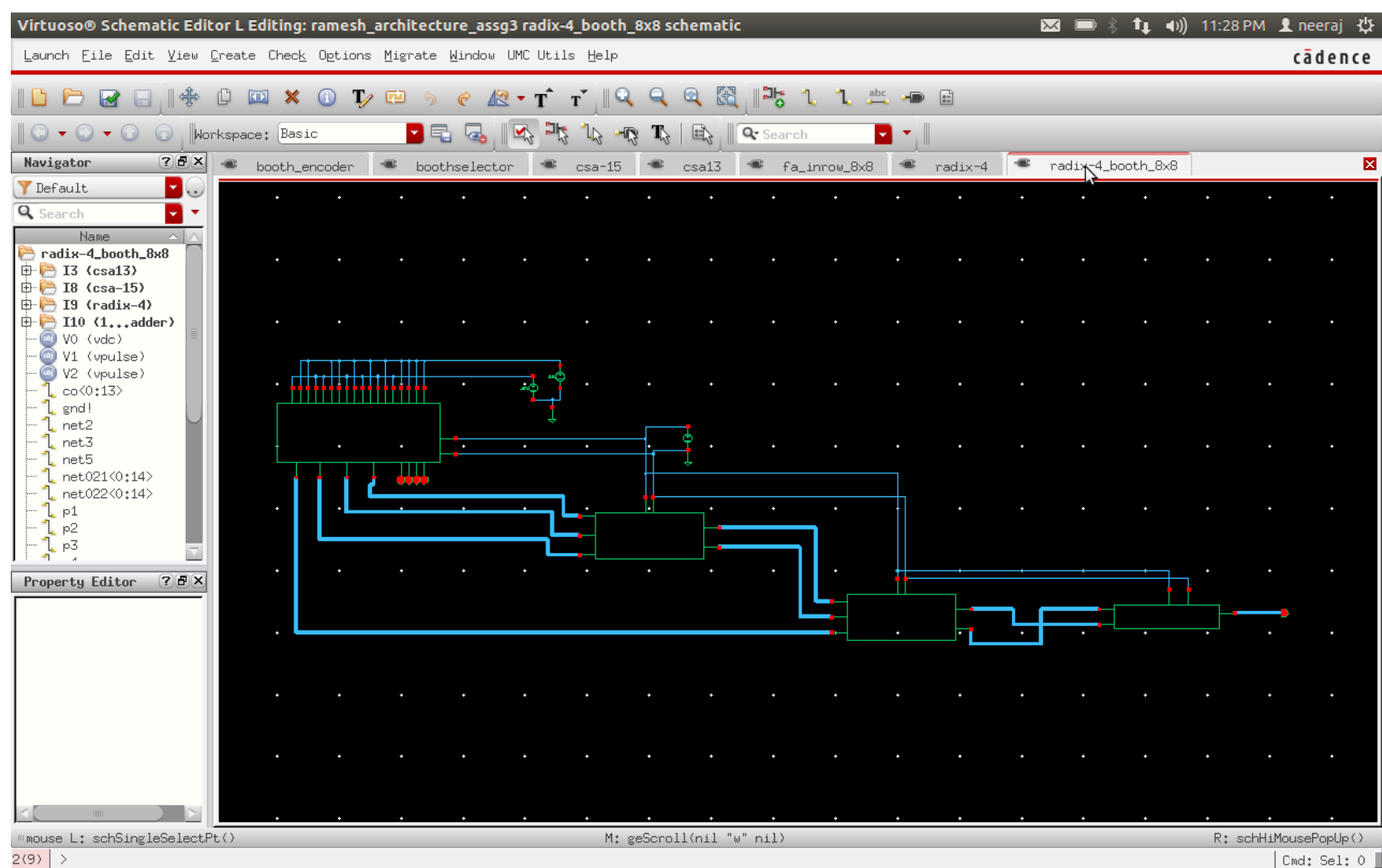
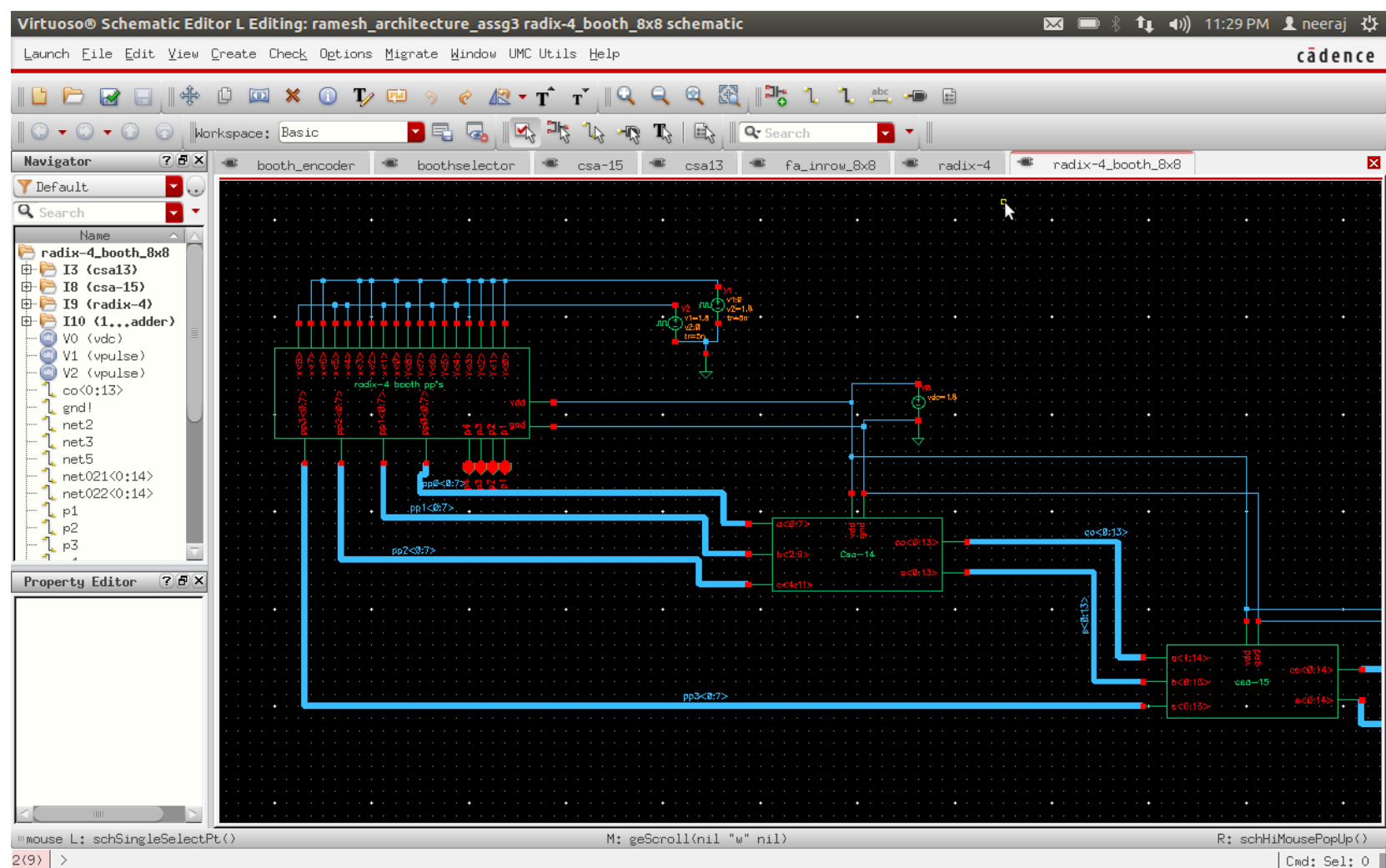


Fig: 8x8 radix booth multiplier.

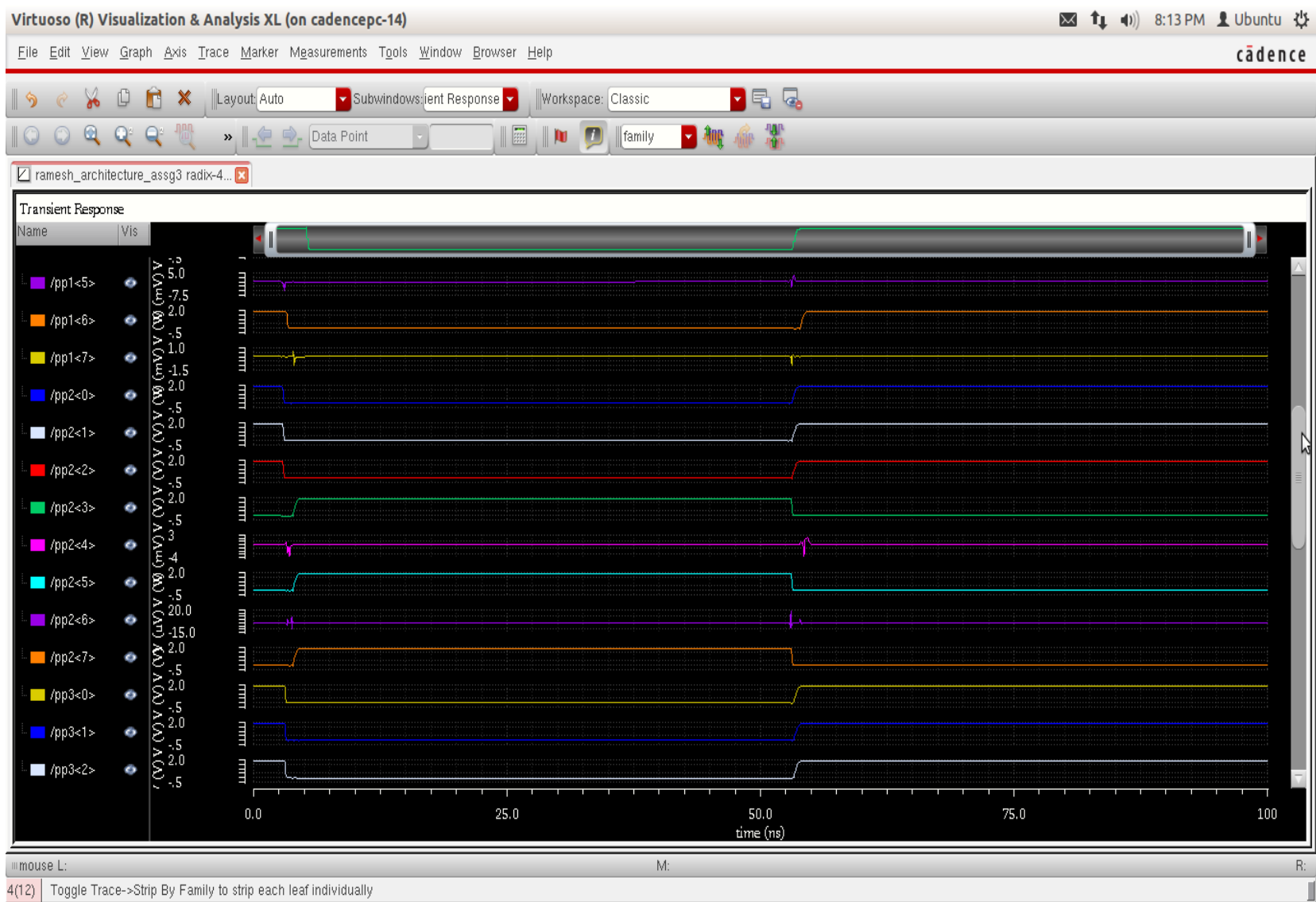
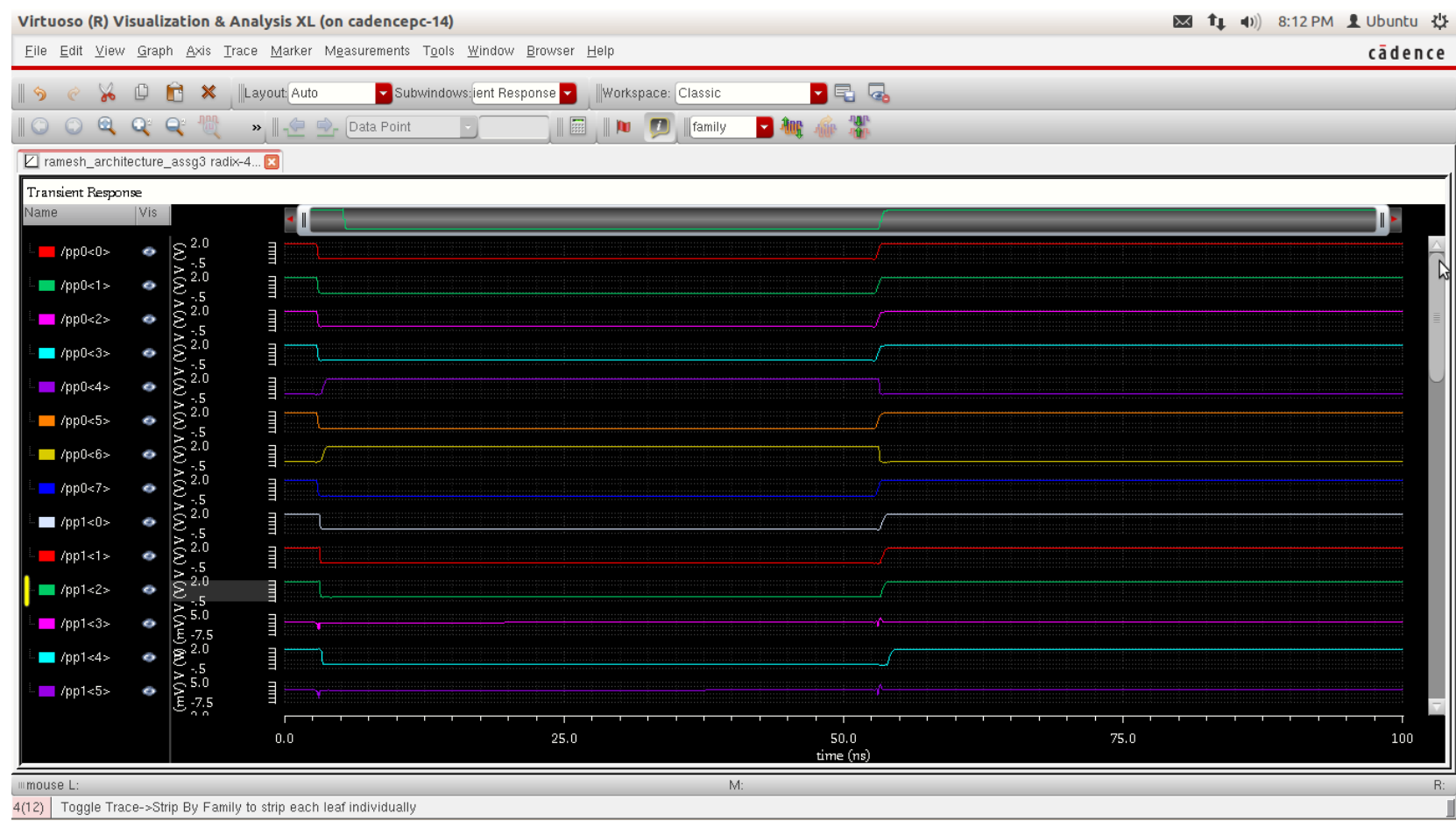


Fig:output waveform.

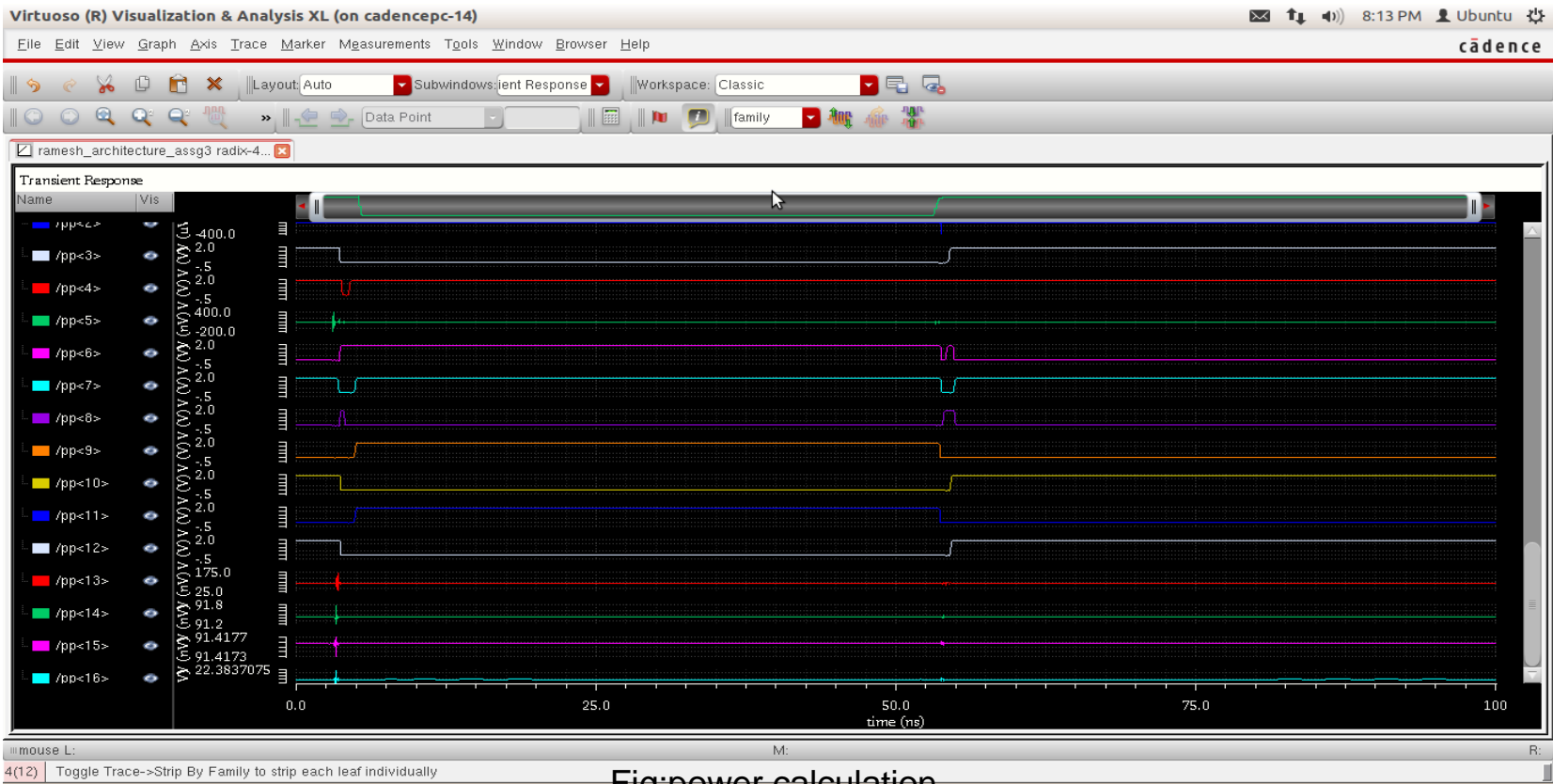


Fig:power calculation.

power=(lavg*Vdd)/T=(-76.75x10⁻¹²*1.8)/200n = 690 mW.

