

Design for Testability

1. Since $\frac{\partial f(x)}{\partial x_i} = f(x_{n-1}, x_{n-2}, \dots, x_{i+1}, 0, x_{i-1}, \dots, x_1, x_0) \oplus f(x_{n-1}, x_{n-2}, \dots, x_{i+1}, 1, x_{i-1}, \dots, x_1, x_0)$

and x_i is a Boolean variable, i.e. $x_i \in \{0, 1\}$, hence we can write,

$$\frac{\partial f(x)}{\partial x_i} = f(x_{n-1}, x_{n-2}, \dots, x_{i+1}, x_i, x_{i-1}, \dots, x_1, x_0) \oplus f(x_{n-1}, x_{n-2}, \dots, x_{i+1}, \bar{x}_i, x_{i-1}, \dots, x_1, x_0)$$

Hence, when $\frac{\partial f(x)}{\partial x_i} = 1$, it means $f(x_{n-1}, x_{n-2}, \dots, x_i, \dots, x_1, x_0) \neq f(x_{n-1}, x_{n-2}, \dots, \bar{x}_i, \dots, x_1, x_0)$, which implies $f(x)$ is dependent on variable x_i . As a result, in order to test stuck at fault at net x_i , it is necessary to find an input combination such that $\frac{\partial f(x)}{\partial x_i} = 1$. Hence, to test the stuck at 0 fault at net x_i , it is required to compute $x_i \frac{\partial f(x)}{\partial x_i} = 1$.

Similarly, to test the stuck at 1 fault at net x_i , it is required to compute $x_i' \frac{\partial f(x)}{\partial x_i} = 1$.
(Proved).

2. Total power dissipation in the circuit is

$$P_t = \begin{cases} P_{sf} + P_{st}, & \text{during scan.} \quad (1) \\ P_{cf} + P_{ct}, & \text{during capture.} \quad (2) \end{cases}$$

In case of gated flip flop output $P_{st} = 0$.

Given that $P_{ct} = \alpha P_{cf}$ and $P_{sf} \approx 0$.

Hence, $P_t = (1 + \alpha)P_{cf}$. (using (2)) (Proved).

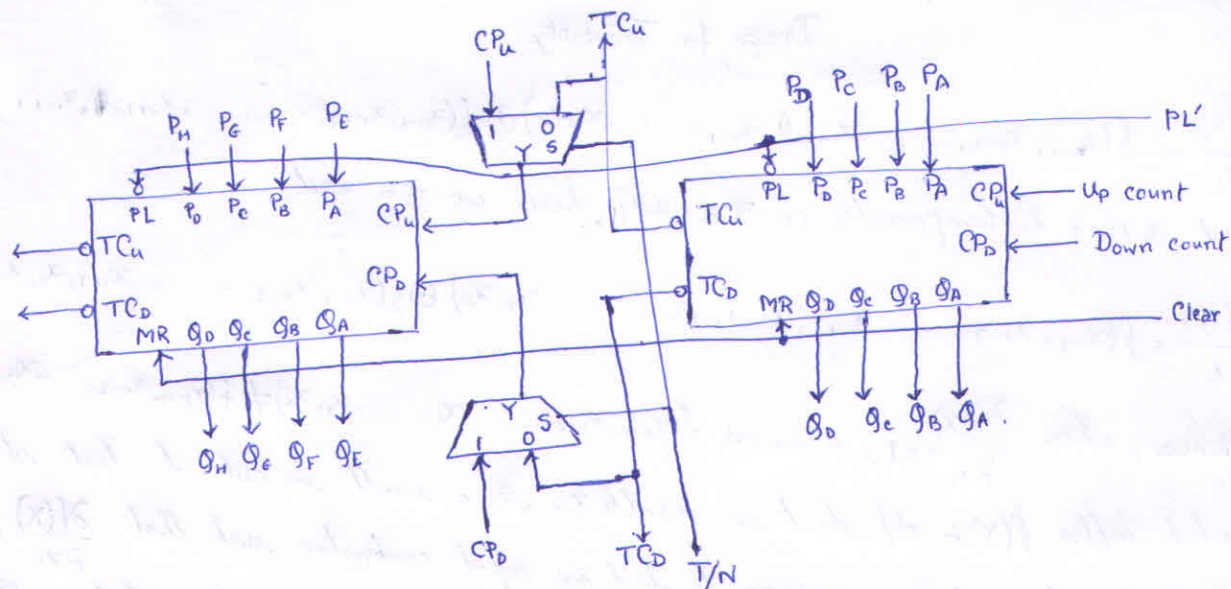
The test access mechanism (TAM) transports test patterns from ATE to the core and test response from the cores to ATE. The wrapper connects the core's functional inputs and outputs to the TAM and to the rest of the SoC. Assuming that K TAM wires are used for core j , the first capture cycle of core j with K TAM wires occurs at clock cycle $\max\{\forall_k (L_{in_k}^j + L_{sc_k}^j)\}$ and subsequent capture cycles occur at first capture cycle + $(n-1) * \max\{\forall_k (\max(L_{in_k}^j, L_{out_k}^j) + L_{sc_k}^j)\}$ for $0 < n \leq \text{no. of test vectors}$. The period of capture cycle would be $\max\{\forall_k (\max(L_{in_k}^j, L_{out_k}^j) + L_{sc_k}^j)\}$.

Hence n^{th} capture cycle of j^{th} core, TC_n^j would occur at

$$TC_n^j = \max\{\forall_k (L_{in_k}^j + L_{sc_k}^j)\} + (n-1) * \max\{\forall_k (\max(L_{in_k}^j, L_{out_k}^j) + L_{sc_k}^j)\}$$

(Proved).

3.



4. Fault coverage of the test, $FC = \frac{m}{n}$.

Process yield is defined as $Y = (1-p)^n = P(A)$.

$$P(B) = (1-p)^m$$

$$P(A \cap B) = P(A) = (1-p)^n$$

$$P(A|B) = P(A \cap B) / P(B) = (1-p)^n / (1-p)^m = (1-p)^{n(1-m/n)} \quad (\text{Proved}).$$

5. The given function is $G_{n-1}(x) = S_{n-1}(0) + S_{n-1}(1)x + \dots + S_{n-1}(j)x^j + \dots$

$$= \sum_{j=0}^{\infty} S_{n-1}(j)x^j \quad \dots \dots \dots (1)$$

Values at the outputs of different stages of an internal-XOR LFSR with $\phi_n = 1$ satisfy the following relations:

$$S_{n-1}(j) = \phi_{n-1} S_{n-1}(j-1) + S_{n-2}(j-1)$$

$$S_{n-2}(j-1) = \phi_{n-2} S_{n-2}(j-2) + S_{n-3}(j-2)$$

$$S_1(j-n+2) = \phi_1 S_{n-1}(j-n+1) + S_0(j-n+1), \text{ and}$$

$$S_0(j-n+1) = \phi_0 S_{n-1}(j-n)$$

$$S_{n-1}(j) = \sum_{i=0}^{n-1} \phi_i S_{n-1}(j-n+i) \quad \dots \dots \dots (2)$$

Generalizing, we can write, $S_{n-1}(j)$ at the j^{th} clock cycle in terms of values appearing at S_{n-1} at some previous clock cycles. Putting (2) in (1), we get,

$$G_{n-1}(x) = \sum_{j=0}^{\infty} \left[\sum_{i=0}^{n-1} \phi_i S_{n-1}(j-n+i) \right] x^j$$

$$= \sum_{i=0}^{n-1} \phi_i x^{n-i} \sum_{j=0}^{\infty} S_{n-1}(j-n+i) x^{j-n+i}$$

$$= \sum_{i=0}^{n-1} \phi_i x^{n-i} \left[S_{n-1}(-n+i) x^{-n+i} + \dots + S_{n-1}(-1) x^{-1} + S_{n-1}(0) + S_{n-1}(1)x + \dots \right] \quad \dots \dots \dots (3)$$

$$= \sum_{i=0}^{n-1} \phi_i x^{n-i} \left[S_{n-1}(-n+i) x^{-n+i} + \dots + S_{n-1}(-1) x^{-1} + G_{n-1}(x) \right] \quad \dots \dots \dots (3)$$

Hence we get, $\left[1 + \sum_{i=0}^{n-1} \phi_i x^{n-i}\right] G_{n-1}(x) = \sum_{i=0}^{n-1} \phi_i x^{n-i} \left[S_{n-1}(-n+i) x^{-n+i} + \dots + S_{n-1}(-1) x^{-1} \right]$

$$\Rightarrow G_{n-1}(x) = \frac{\sum_{i=0}^{n-1} \phi_i x^{n-i} \left[S_{n-1}(-n+i) x^{-n+i} + \dots + S_{n-1}(-1) x^{-1} \right]}{1 + \sum_{i=0}^{n-1} \phi_i x^{n-i}} \quad \dots (4)$$

The numerator of R.H.S. of equation (4) is a function of the initial states of LFSR flip flops represented in terms of $S_{n-1}(-n)$, $S_{n-1}(-n+1)$, \dots , $S_{n-1}(-1)$, i.e., the values appearing at the output of D_{n-1} in the n clock cycles preceding the 0^{th} cycle. Hence, the numerator captures the effects of the seed on the sequence of values appearing at the output of D_{n-1} . If the initial state of the LFSR is equivalent to appearance of the sequence $S_{n-1}(-n)=1$, $S_{n-1}(-n+1)=0$, \dots , $S_{n-1}(-1)=0$ at the output of D_{n-1} prior to the 0^{th} clock cycle, then for an LFSR with $\phi_0=1$ (non trivial LFSR) equation (4) may be rewritten as:

$$G_{n-1}(x) = \frac{1}{1 + \sum_{i=0}^{n-1} \phi_i x^{n-i}} \quad \dots (5).$$

The denominator of R.H.S. of equation (5) can be re-written in terms of feedback polynomial as $x^n \phi\left(\frac{1}{x}\right)$ since $\phi_n=1$ for n stage LFSR (non trivial LFSR).

Hence we get, $G_{n-1}(x) = \frac{1}{x^n \phi\left(\frac{1}{x}\right)}$.