A TV GHOST CANCELLER USING FPGA-BASED FIR FILTERS

Wanchalerm Pora and Pahol Siriluangtong

Electrical Engineering Department
Chulalongkorn University
Bangkok, Thailand 10330
Phone: +66-2218-6488
Email: Wanchalerm.P@Chula.ac.th

Electrical Engineering Department
Chulalongkorn University
Bangkok, Thailand 10330
Phone: +66-2218-6537
E-mail: jack@digital.ee.eng.chula.ac.th

ABSTRACT

This paper presents a PAL TV ghost canceller that employs a ghost cancellation reference signal (GCR signal) recommended in an ITU standard. The LMS algorithm is chosen to find the channel inverse, which is estimated by a 256-tap FIR filter. The emphasis is upon resource sharing technique, which increases utilization of multipliers by eight times. To test the canceller, a TV ghost emulator is constructed. From subjective tests, the canceller can remove the ghost whose power is lower than -6 dB compared to that of the main signal, providing its delay is lower than 10 μs.

1. INTRODUCTION

Even though the home theater concept has driven TV technologies a long way off, the most popular source of TV applications is still via analog broadcasting, which is subject to multipath propagation [1]. The signal from each path reaches TV receivers with different delays and powers; hence the duplicate horizontally-shifted pictures on the TV screens. This phenomenon is well-known as "ghost."

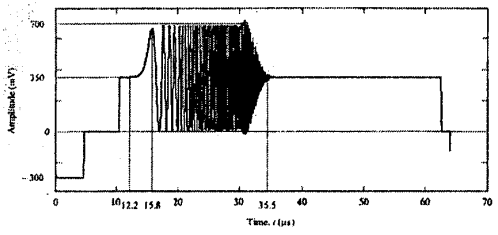
The ghost cannot be removed from the main picture using only conventional electronics. Signal processing must be incorporated, channel equalization in particular. Note that there were many attempts to implement ghost cancellers in the past twenty years [2]. However, they were very costly due to the cost of high performance signal processors. Ghost cancellation systems have, therefore, never been popular.

Advanced technologies have greatly increased the performance-cost of digital ICs. It is now worth reexamining the structure of a ghost canceller. The purpose of this paper is to propose a ghost cancellation system, which may be included within mid-range to high-end TV receivers. Its main components are a DSP processor and an FPGA that functions as a high-speed, long filter. Since DSP chip and FPGA are both reprogrammable, this combination provide other features, when equalization is not needed, such as noise cancellation, DTS decoder, etc.

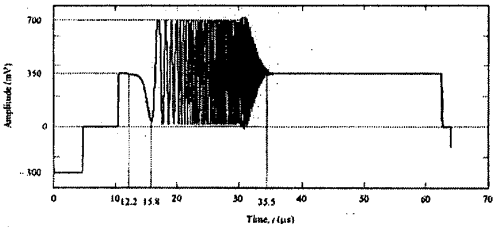
2. GHOST CANCELLATION REFERENCE (GCR) SIGNAL

In a ghost cancellation system, a GCR signal must be inserted onto a TV signal during its vertical blanking interval (VBI) [3] at a TV broadcaster. The ghost cancellers at the TV receivers exploit the knowledge of how the known GCR signal responds to the effect of the channel. They can then find an inverse of such effect that essentially removes the ghost from TV signals.

There were also many attempts to find "good" GCR patterns. Eventually, ITU gathered a few good GCR patterns in the Recommend ITU-R BT.1124 [4].



(a) Positive polarity



(b) Negative polarity

Figure 1 Patterns of the GCR-C Signal

In this research, we adopt an ITU standard GCR-C signal whose patterns are shown in Figure 1. The positive and negative polarity signals are alternately inserted onto line 318 of the composite video signal (CVS). Its figure

0-7803-7690-0/02/$17.00 ©2002 IEEE

looks alike that of a sinusoidal signal whose frequency increases temporally. This GCR signal has flat frequency response and smooth phase characteristic within a TV signal bandwidth. Moreover, its spectral characteristic is not much sensitive to selections of sampling frequency and word length of A/D converters [5].

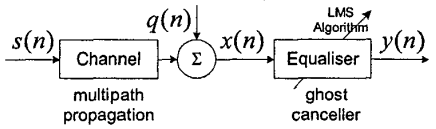


Figure 2 Signal propagates through channel and equalizer

3. EQUALIATION SCHEME

It is well known that a received signal, $x(n)$ traveled through a multipath propagation channel, as shown in Figure 2, can be estimated in discrete-time domain as

$$x(n) = \sum_{i=0}^{N} c_i s(n-i) + q(n) \qquad (1)$$

where c_i, $i = 0,...,N$ are parameters of the channel, $s(n)$ is the TV signal with GCR signal during the VBI and $q(n)$ is the additive noise. The channel length is denoted by N.

Without equalization, the received signal, $x(n)$ is a summation of some delayed transmitted signals, i.e., $x(n)$ is a ghosted signal. Intuitively, the desired response of the equalizer (or ghost canceller in this case) shall reverse the channel effect without amplifying noise.

If an FIR filter is used to estimate the inverse of the channel then, the equalized (deghosted) signal, $y(n)$ is

$$y(n) = \sum_{j=0}^{M} w_j x(n-j) \qquad (2)$$

where w_j, $j = 0,...,M$ are parameters of the filter and M denotes the filter length.

The LMS algorithm is chosen to find such parameters due to its computational complexity and robustness [6]. It tries to adapt the parameters such that the mean squared difference between $s(n)$ and $y(n)$ is minimized (only when $s(n)$ is the known GCR signal). If the algorithm converges, the filter, therefore, cancels the channel effect.

4. PROPOSED TV GHOST CANCELLER

A TV ghost canceller, as shown in Figure 3, consists of a sync separator, an A/D and a D/A converters, a digital signal processor and an FPGA which functions as an FIR filter and a GCR separator. Each part will be described as follows:

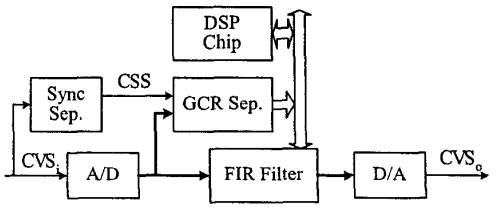


Figure 3 Structure of the proposed ghost canceller

4.1 Sync Separator (LM1881)

LM1881 separates composite sync. signal (CSS) from CVS input (CVS_i). Moreover, its internal clamp circuit always keeps DC voltage of the sync. tip level, the lowest voltage level of the CVS_i, at 1.5 V.

4.2 A/D converter (THS1031)

Typically, a CVS signal is $1V_{p\text{-}p}$, so the clamped CVS_i may vary within a range of 1.5-2.5V. The converter is, therefore, set to convert an analog input signal to 8-bit unsigned data with middle reference voltage at 2V. To maximize the length of the filter in continuous-time domain, whilst avoiding the alias effect, the sampling rate is chosen to be 12 Msamples/s.

4.3 GCR data separator

Implemented in a Xilinx FPGA [7], GCR data separator prepares GCR sequence for the DSP chip. It synchronizes the horizontal and vertical time bases with the CSS signal [2]. It then keeps the effect of the channel on the GCR by storing some parts of line 317 and 319 and the whole line of 318 in its FIFO. Recall that the transmitter inserts the GCR signal onto line 318 of the CVS signal.

4.4 Digital signal processor (TMS320C6211)

The DSP Chip performs the LMS algorithm. It gets the channel effect on GCR sequence by reading FIFO inside the GCR separator, searches the optimized parameters, and then readjusts the FIR parameters.

To improve picture stability, DSP chip stops updating the parameters, if summation of squared error [6] is less than a threshold, and resumes updating again when such value is higher than another higher threshold.

4.5 D/A converter (THS5641)

After equalization or ghost cancellation, deghosted digital data will be converted back to analog domain. THS5641 with an I-to-V amplifier converts 8-bit digital data to $1V_{p\text{-}p}$ analog CVS_o signal.

4.6 FIR Filter with Resource Sharing Technique

It is desirable to have an FIR filter whose length is as long as possible in order to cancel the ghost that has long

delay. In fact, to estimate the channel inverse with an FIR filter very well, the length of that FIR should be doubly longer than that of the channel [6], i.e., M (in Eq. (2)) should be greater than $2N$ (in Eq. (1)).

Since the filter operation is in a form of sum of products (see (2)), so each filter tap invokes multiplication and accumulation (MAC). Several DSP processors would be required to implement a long filter running at a high speed. For example, to implement a 256-tap filter running at 12 Msamples/s (approximately 3-billion MACs/s) requires at least 20 TMS320C6211s, hi-end DSP processors. This implementation is obviously not feasible.

Dedicated hardware such as FPGA seems to be a better choice. From its implementation report shown in Table 1, Xilinx XCV300E spends 54% of its hardware resource (about 160,000 gates) to construct a 32-tap FIR filter. This filter can process data up to 75.7 Msamples/s. However, if pipeline multipliers [8] are employed, it will spend a bit more resource but it can work almost doubly faster than the conventional one.

Table 1 Resource- performance of 32-tap FIR filter, implemented on XCV300E

Technique	Resource	Speed
Conventional Multiplier	54%	75.7 MHz
Pipeline Multiplier	60%	144.4 MHz

Since the speed of the filter implemented on the FPGA is several times faster than the sampling rate of 12 Msamples/s. It is therefore possible to design a structure of the filter such that a multiple filter taps access one MAC at different time every 12 MHz. This is a concept of resource sharing, which lengthens the filter significantly with small additional resource.

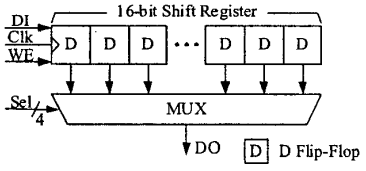


Figure 4 Structure of SRL16x1E, a primitive component of XCV300E

4.6.1 8-bit 8-to-1 Data Multiplexer and Shifter

We decide to reuse the MAC unit eight times over 12MHz cycle, so both sampled data, $x(n-8j+k)$ and filter parameters, w_{8j-k}, must be divided into groups eights where j denotes group number and $k=8,...,1$ is the group member index, which runs eight times faster than the sampling index n. Hence there must be circuits that select 1-of-8 pairs of $x(n-8j+k)$ and w_{8j-k}, in order to prepare operands for the MAC unit number j.

A primitive component, SRL16x1E, of the selected FPGA perfectly satisfies this requirement. Illustrated in Figure 4, it is composed of a 16-bit shift register and a multiplexer. In this design, only lower eight bits are utilized. A group of eight SRL16x1E, called SRL16x8E, represents eight bits of eight $x(n-8j+k)$ or w_{8j-k}.

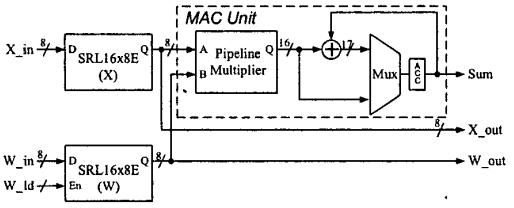


Figure 5 8-tap FIR filter using resource sharing

4.6.2 8-tap FIR Filters

An 8-tap filter j shown in Figure 5 is composed of two SRL16x8E and one MAC. One SRL16x8E is to keep $x(n-8j+k)$ and the other is to keep w_{8j-k}. Intuitively, after reducing k from eight down to one, while keeping n fixed, the accumulator should have a value of $\sum_{k=8}^{1} w_{8j-k}x(n-8j+k)$. Then k changes its value back from one to eight, n increases $(n=n+1)$, i.e. the eight registers inside SRL16x8E must be shifted. This can be done using the shift register inside SRL16x8E without additional hardware.

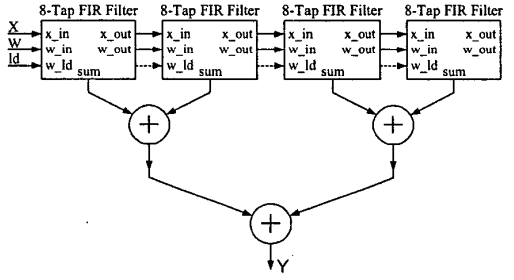


Figure 6 32-tap FIR filter

Value of $w_j, j=0...M$ can be updated by shifting too. When DSP chip wants to adjust filter parameters, it will activate W_ld signal and send w_M first and w_0 last, at each rising edge clock, w_j will propagate via shift register and seat in its designated position eventually after $M+1$ clocks.

To complete the whole filter, each 8-tap FIR filter is connected sequentially. Shown in Figure 6 is an example of a 32-tap FIR filter

A design of filters using resource sharing technique can

save lots of resource of FPGA. As shown in Table 2, a 256-tap filter consumes only 73% of resource in XCV300E or about 219,000 gates and the speed of the filter can run up to 141.9 MHz. Since the resource is reused eight times, the data rate can be up to 17.7 Msamples/s. Notice that resource sharing requires resource *six times* less than the conventional one.

Table 2 Resource-performance comparison between conventional FIR filter and FIR filter using resource sharing implemented on XCV300E

Technique	Length (taps)	Resource	Speed (MHz)	
			Circuit	Data
Conventional	32	54%	75.7	75.7
Pipeline Multiplier and Resource sharing	32	9%	147.1	18.3
Pipeline Multiplier and Resource sharing	256	73%	141.9	17.7

Finally, after synthesized and implemented together with the GCR separator, Xilinx Foundation 3.3i software reports that these circuits use up 99% of slices (a slice is a group of primitive components of Xilinx FPGA.)

5. PERFORMANCES

The effect of ghost can vary in many patterns depending upon the terrain of TV broadcasters and that of TV receivers. Hence we developed a ghost generator which consists of 64 270ns-delay-lines, amplifiers/attenuators and a combiner in order to emulate such effect thoroughly. The longest delay this emulator can generate is 17.3 μs. However, in unusual terrain, the ghost may have longer delay than this.

Figure 7 shows a deghosted TV screen, which demonstrates a visual test. In this example, we used two ghosts, whose delays are 1.08 μs and 4.05 μs, and powers are -12dB and -20dB, compared to the main signal respectively.

Thorough subjective tests have been conducted. The results are categorized according to the range of ghost delays as follows:

Delays between -1.3μs to 16μs: The canceller can visually remove the ghost completely within a few seconds when the total power of all delays is less than -12dB (1/4), compared to that of the main signal.

Delay between 0-10μs: Limitation of the range helps the filter to estimate the channel inverse better. The total ghost power can be up to -3dB. However, if the ghost is stronger than -6dB, it may distort sync. signal too much such that sometimes the GCR separator cannot synchronize with the CVS signal, so it may take a few more seconds to find the optimal parameters

If the ghost is stronger or its delays are longer than stated above, the canceller may not remove the ghost completely; it may be able to remove strong ghost but induces ghost at another position. If the ghost is too much strong, TV receivers will lose sync.

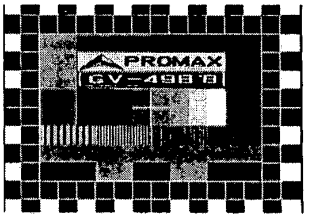


Figure 7 TV screen after ghost has been removed

6. CONCLUSIONS

We developed A PAL TV ghost canceller using a DSP chip and an FPGA. Resource sharing technique was employed. From our experiments, the ghost canceller can visually cancel the ghost within a few seconds if the total ghost power is not more than -6 dB compared to the main signal and the delays are within a specific range.

ACKNOWLEDGEMENTS

This paper is financially supported by National Electronics and Computer Center, and the Development of Faculty Staff Fund, Chulalongkorn University, Thailand.

REFERENCES

[1] Mary Louise Bucher, "Simulation of multipath fading/ghosting for analog and digital television transmission in broadcast channels," IEEE Transactions on broadcasting, Vol. 38 (December 1992), pp. 256-262

[2] K. Kim, J. Oh et al, " New Ghost Cancellation System," Consumer Electronics IEEE Inter. Conf. on 1994, pp. 288-289 1994

[3] H.V. Sims, "Principles of PAL Colour Television and Related Systems," 2nd ed. , Hiffe books, 1969

[4] Recommendation ITU-R BT.1124-3. "Reference signals for ghost cancelling in analogue television system," ITU 2001

[5] Report ITU-R BT.2018, "Study of the system C ghost canceling reference signal for the evaluation and correction of linear distortion in the television chain." ITU 1998

[6] Simon Haykin, "Adaptive Filter Theory," 3rd ed. New Jersey : Prentice-Hall, 1996

[7] Xilinx Incorporation. "The Programmable Logic Data Book 2000," 2000.

[8] Xilinx Inc. "Multiply Generator v3.1," May 2001