Clock circuits

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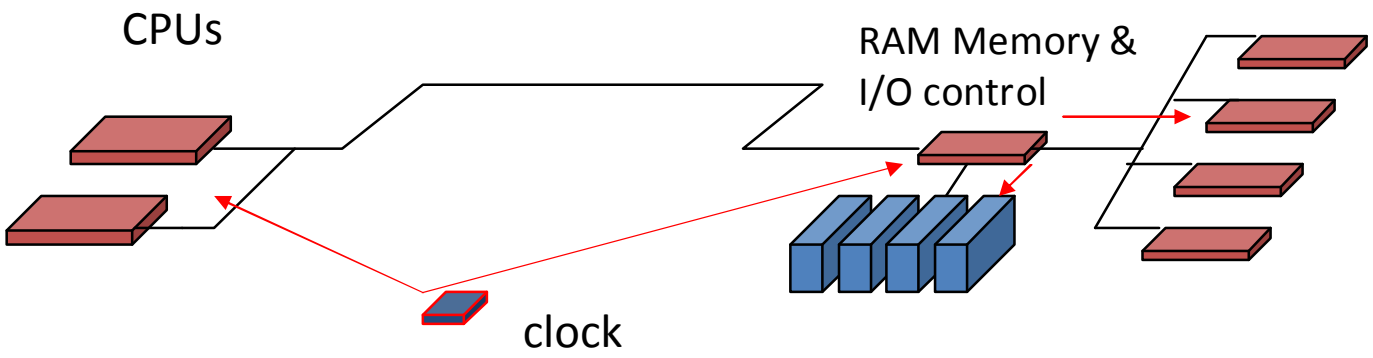
Clock generation in external chips

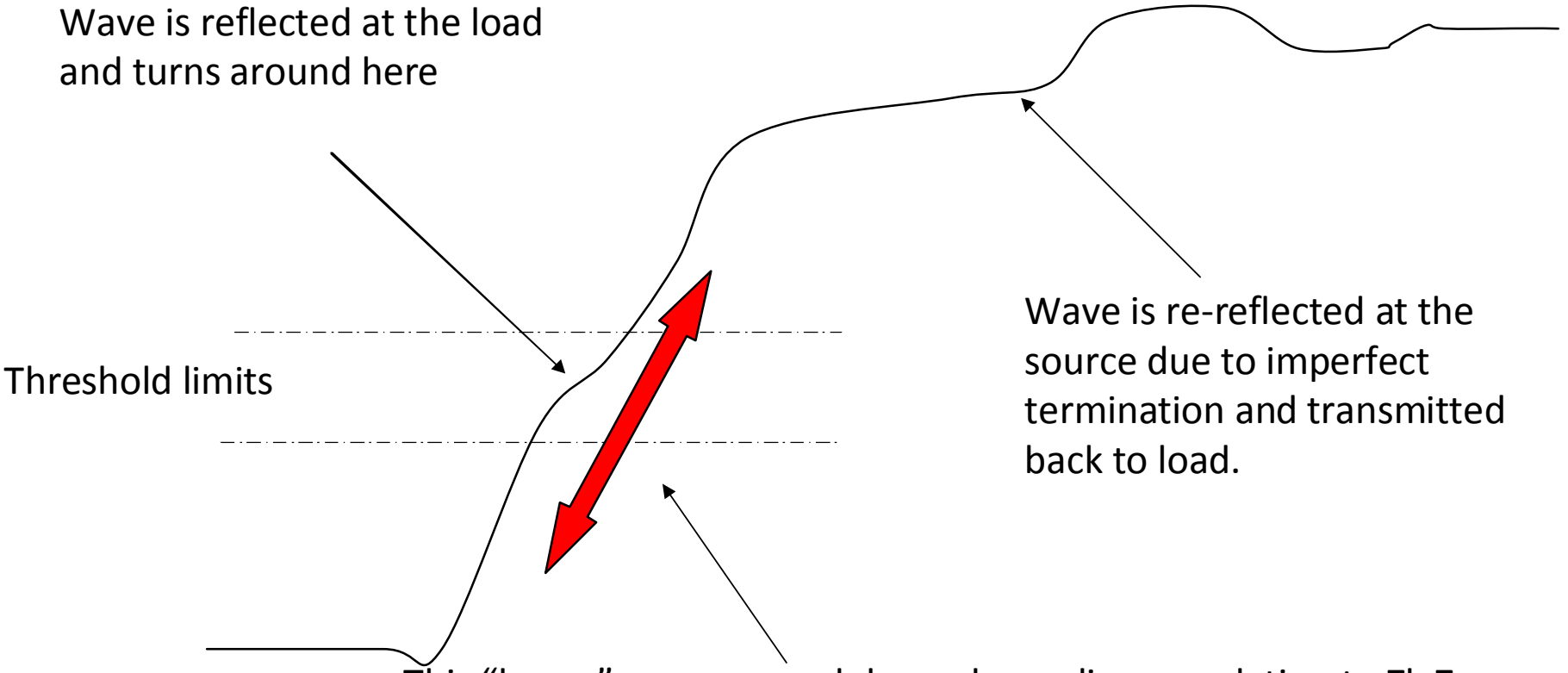


- The idea assumption is that the clock edge are synchronized at each device
- A digital clock signal is ideally a 50% duty cycle square wave
- A "***clock domain***" is comprised of the a set of signals that are referenced to the same idea clock signal.

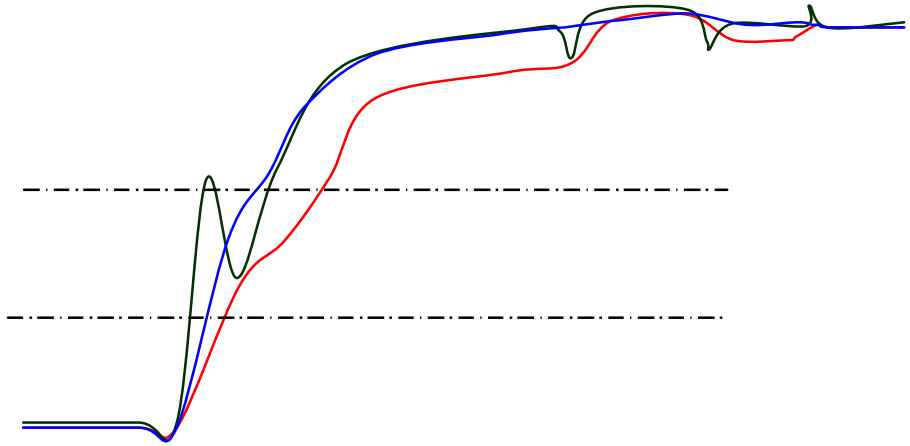
Clock Signal Requirements

- Monotonic edges
  - Avoid double clocking and meta-stable behavior.
  - Controlled with distribution topology
- Fast edges
  - Reduce uncertainty from slew rate
  - Controlled by length
- Low Skew
  - Controlled by topology, loading, and receiver sensitivity.
- Low Jitter
  - Mostly a clock generation issue.
- High fan-out - Topology
  - Includes cpu's, i/o chips, expansion connectors, memory chips, control chips

Non-monotonic series terminated effects

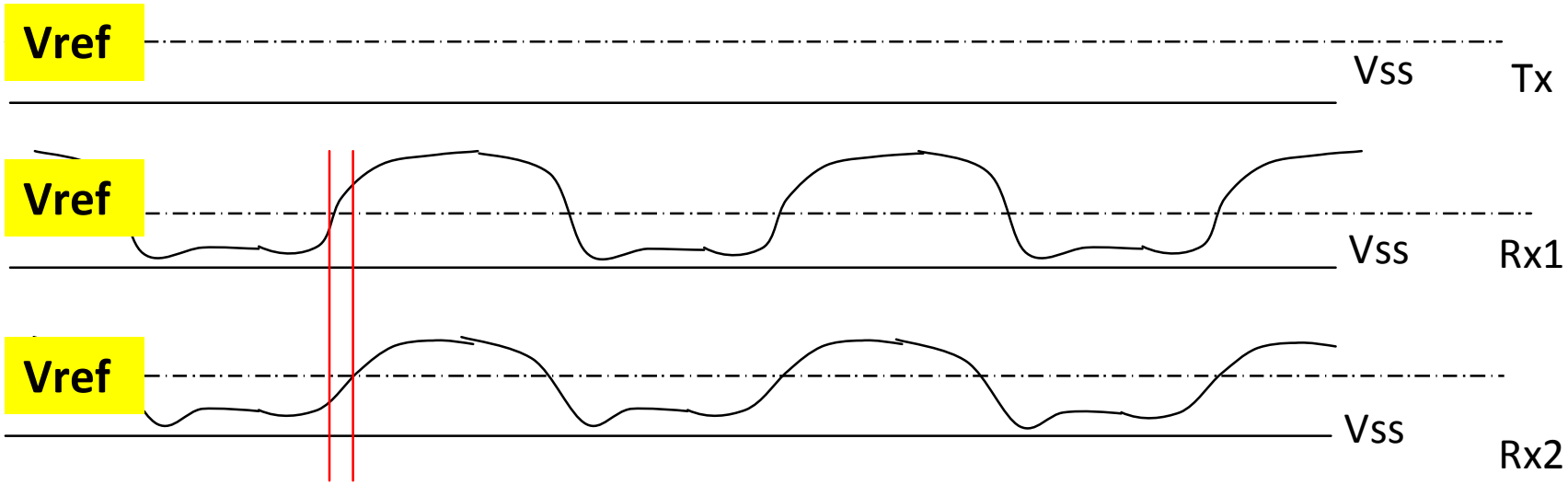


Fast Edge Reduce Skew



- Fast edges can reduce the time uncertainty through the thresholds
- However stub and packages can make fast edges more susceptible to ringing which can cause double clocking of the data

Issues with single ended threshold sensitivity

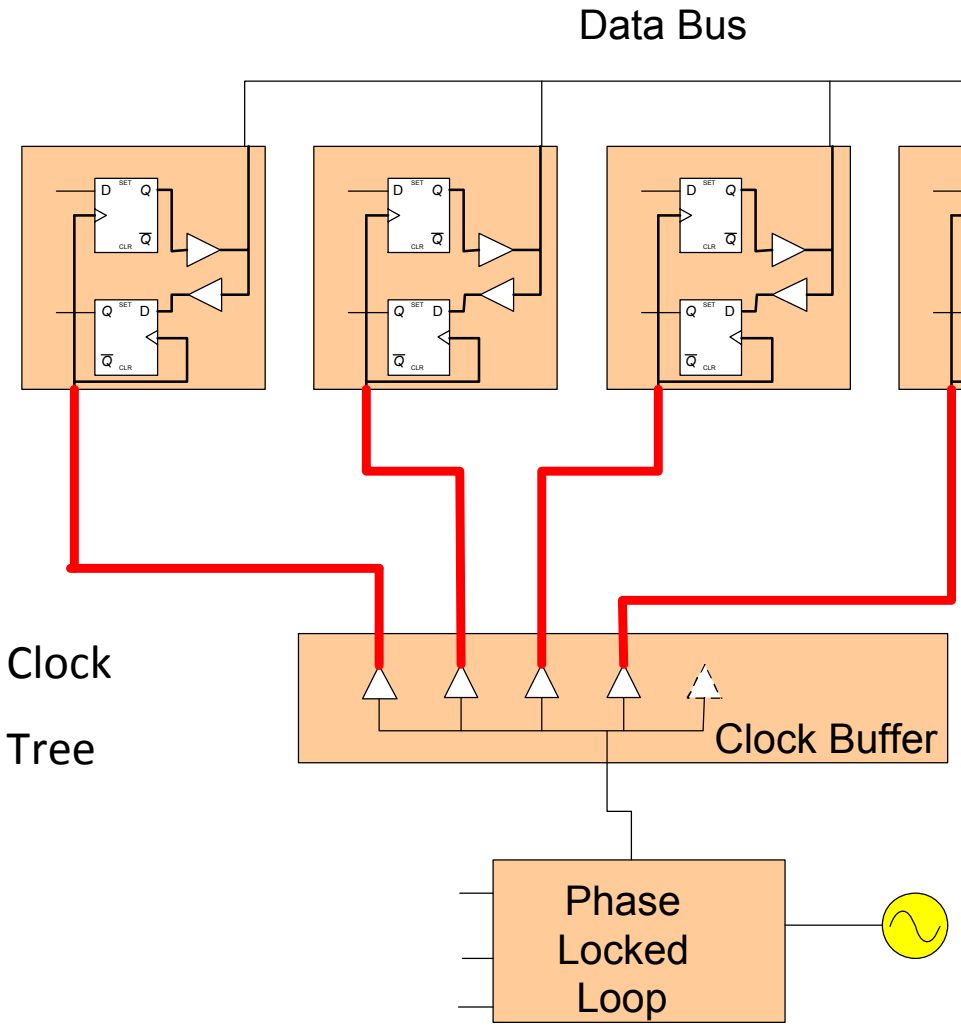


- The wave is referenced to either Vcc or Vss. Consequently the effective DC value of the wave will be tied to one of these rails.
- The wave is attenuated around the effective DC component of the waveform, but the reference does not change accordingly. Hence the clock trigger point between various clock load points is very sensitive to distortion and attenuation.

Differential Clocking vs Single Ended Clocking

- For a **Single ended (SE) clock,** the buffer drives the clock signal on one trace.
- For a **Differential (Diff) clock,** the buffer drives two traces in equal but in opposite directions. The signal are received at the load end with a differential amplifier. This means that the qualifying “clock” waveform is the difference of the signals on the two traces.
- Single ended signaling requires a threshold reference voltage.
  - This voltage is generated either on or off of the die.
  - The problem with single ended clocking is that is sensitive to more to attenuation and edge distortion.

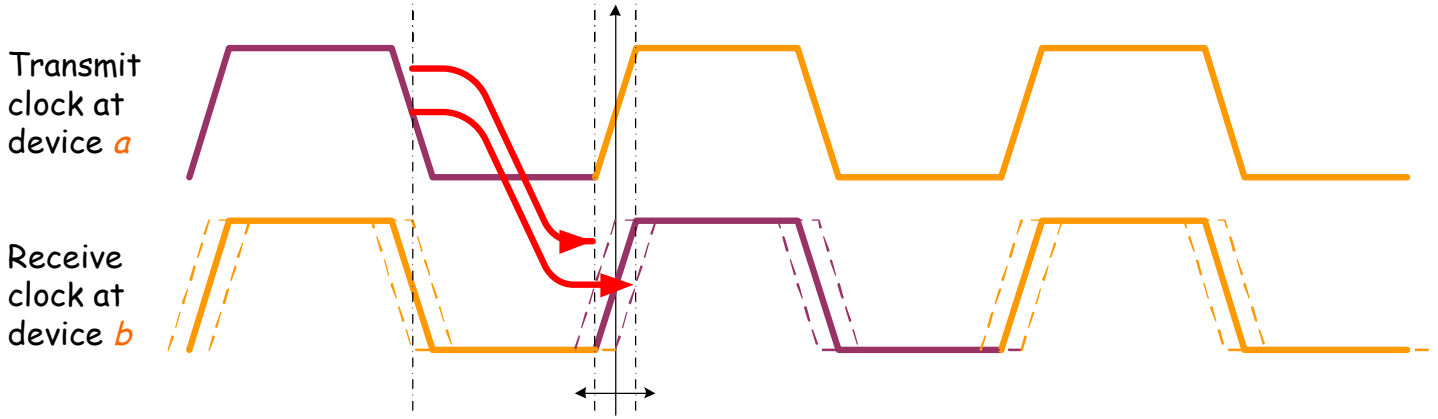
Clock skew due to path length mismatch



Skew Factors

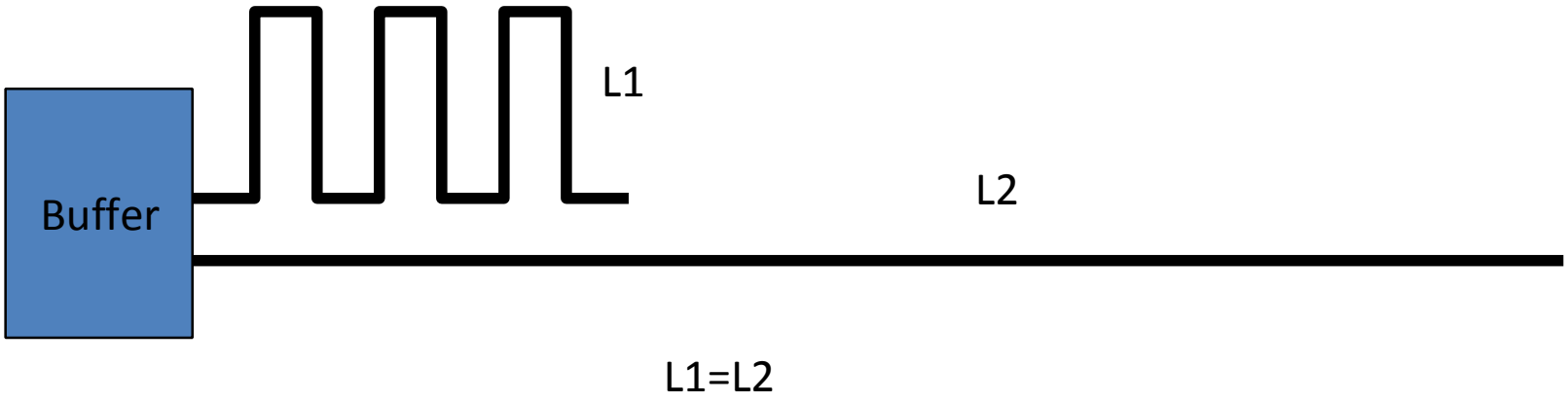
- Clock path arrival mis-match
- Clock buffer Tco pin to pin skew
- Receiver loading

Review of Clock Skew



- **Clock Skew:** pin-to-pin variation in the timing of input clock at each agent (source & destination, in our example) on a bus.
- The net effect of clock skew is that it can
  - reduce the total delay that signals are allowed to have for a given frequency target.
  - require larger minimum signal delays in order to avoid logic errors. (We'll cover this in more detail shortly.)

Serpentine Routing is used to adjust for lengths

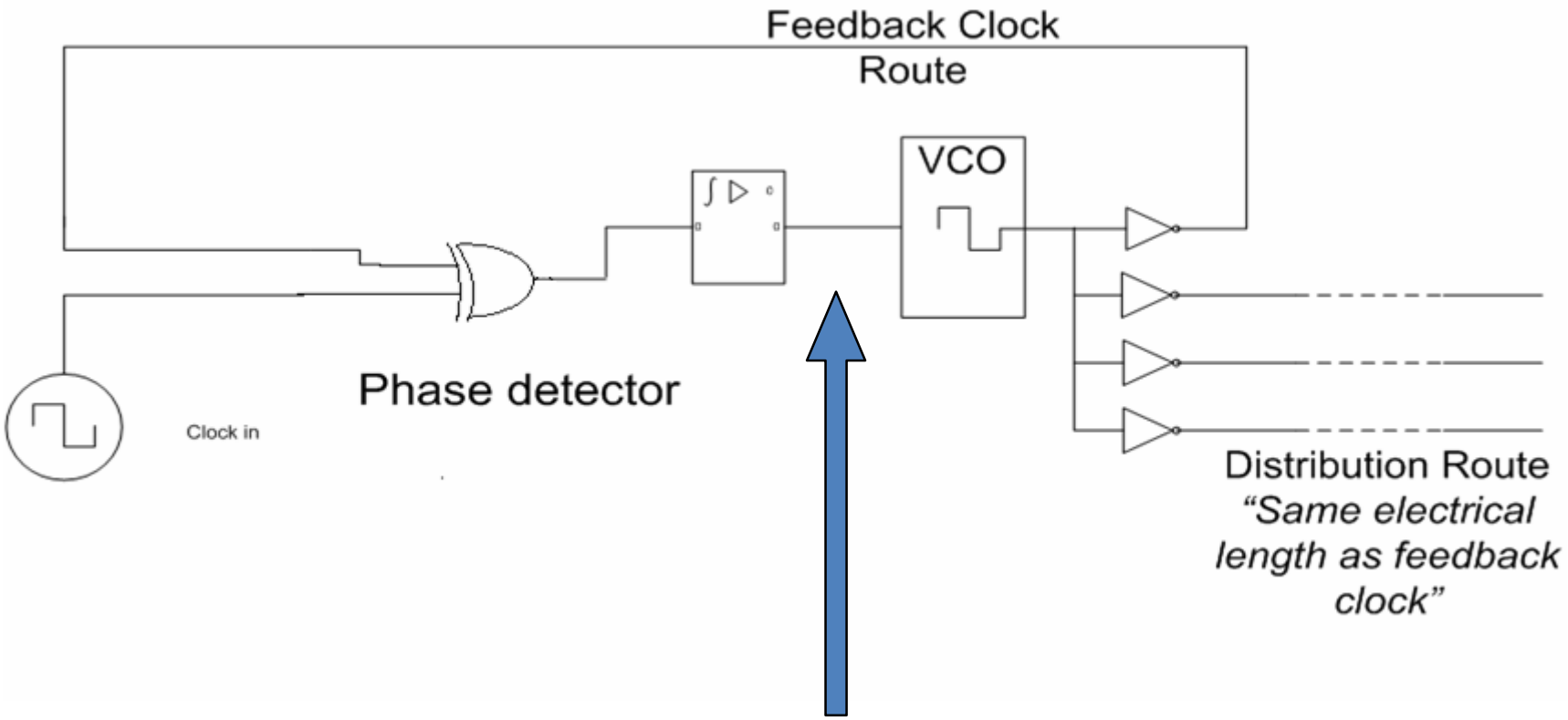


- Space between serpentine traces should be minimum of 3x the dielectric height for stripline and 5x the dielectric height for microstrip.
- We can estimate the effect using the coupling coefficient from a 2 D field solvers.

Clock Source

- The traceable reference for most clocks sources is a crystal oscillator.
- A phase locked loop (PLL) regenerates clocks for distribution.
  - The primary purpose of a phase lock loop is to synchronize signal edges.
  - PLLs may be the main clock domain source
  - PLLs may be used within each chip to synchronizes internal nodes and external clock references.
- PLLs are feedback amplifiers and subject to stability criteria. This especially true when PLLs cascaded.

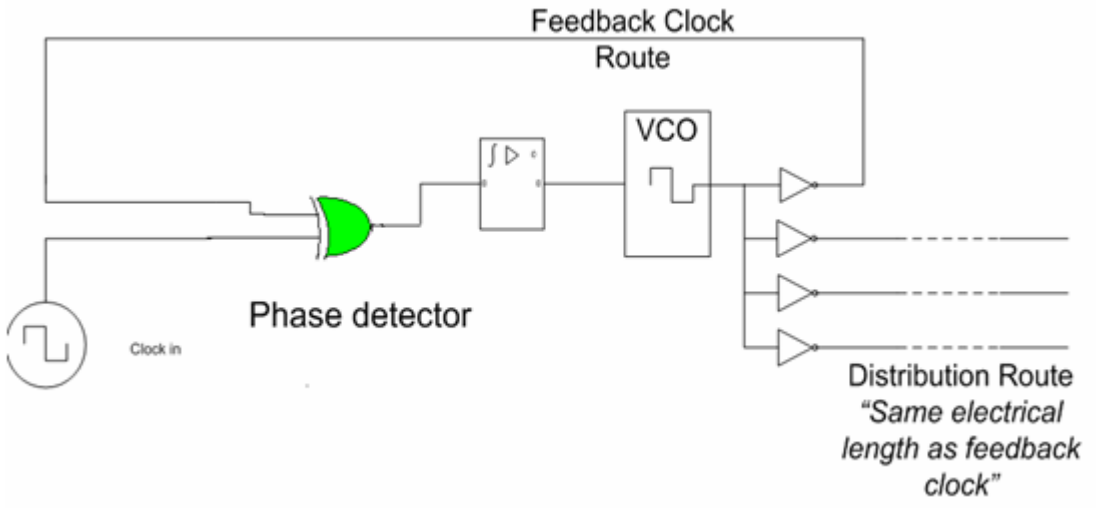
Phase Locked Loop



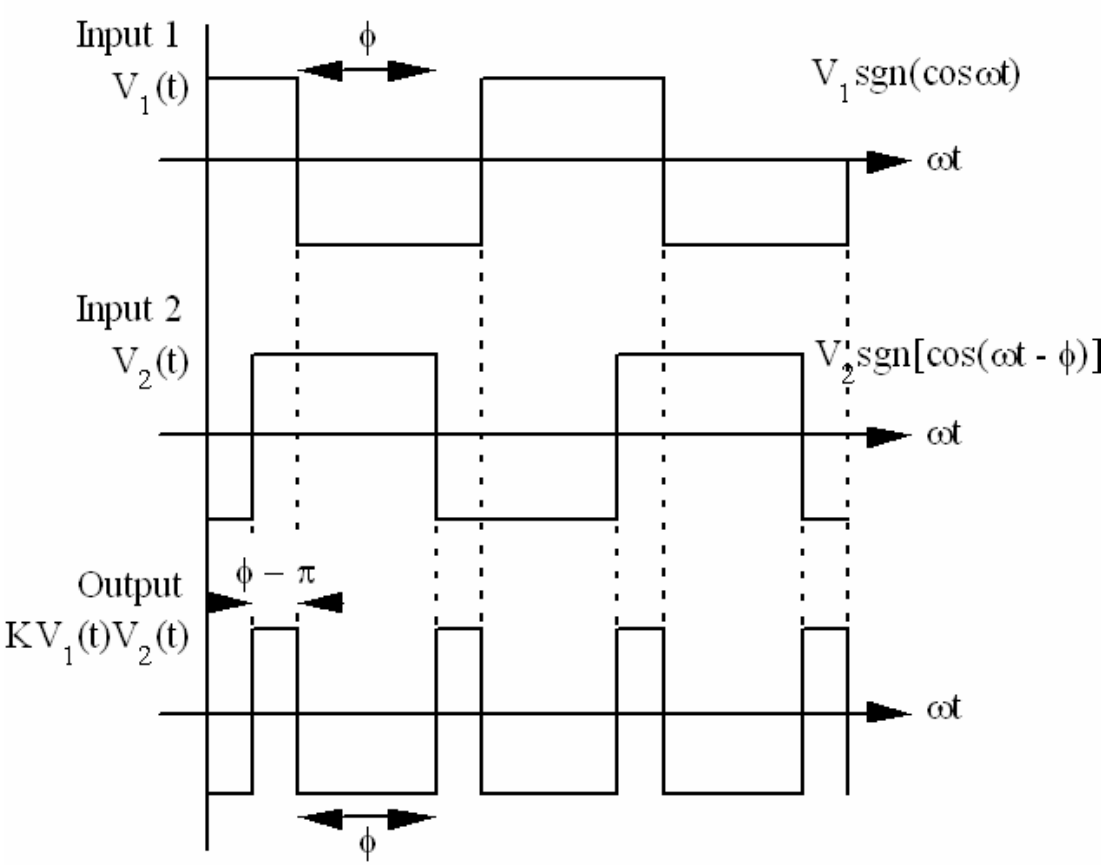
When this point is 0 V the distribution clocks are in phase with the "clock in"

Phase Detector

- Phase Detector
  - Acts as comparator
  - Produces a voltage proportional to the phase difference between input and output signal
  - Voltage becomes a control signal

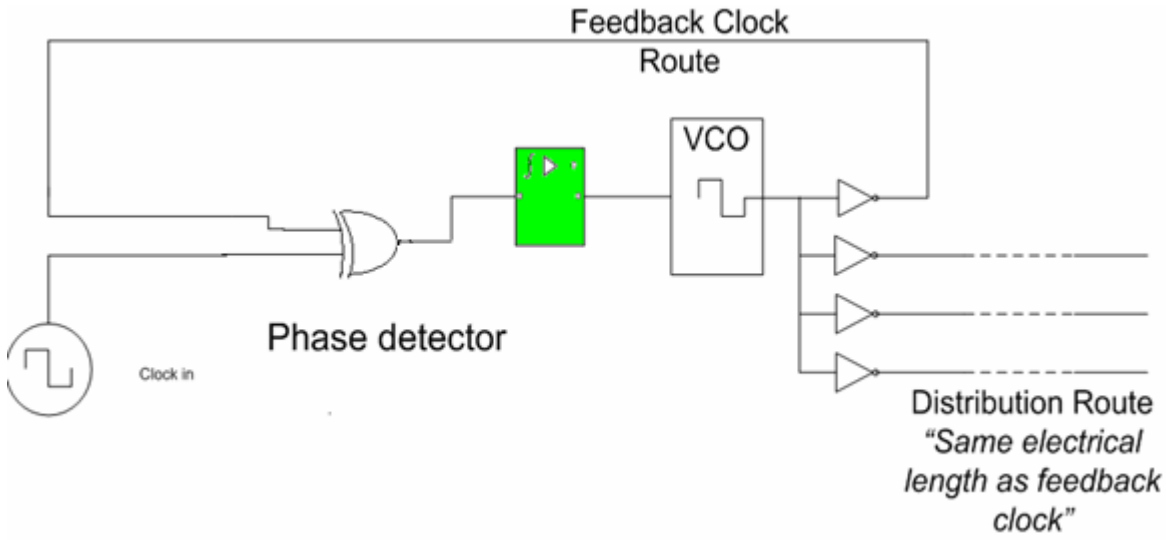


Phase detection



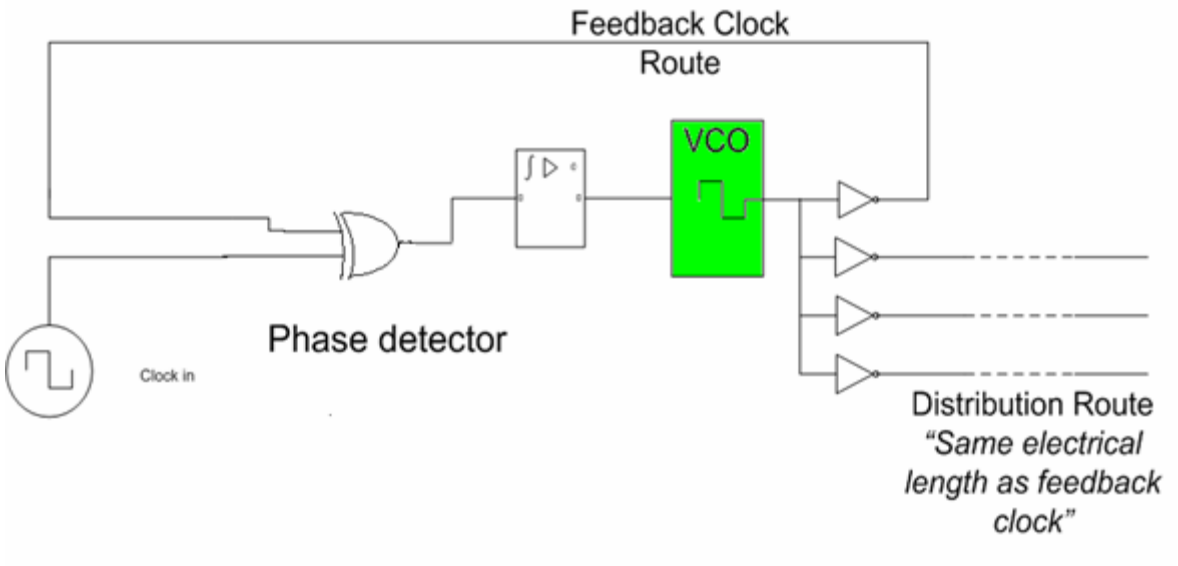
Loop Filter

- Filter
  - Determines dynamic characteristics of PLL
    - » Specify Capture Range (bandwidth)
    - » Specify Tracking Range
  - Receives signal from Phase Detector and filters accordingly



Voltage Controlled Oscillator

- Voltage Controlled Oscillator
  - Set tuning range
  - Set noise margin
  - Creates low noise clock oscillation



Thank you