Assignment-4

Multiplier Architectures

1. Design and simulate an 8 bit X 8 bit array multiplier using TSMC 180nm CMOS process. Estimate its area, delay and power dissipation.
2. Consider the 8 bit multiplicand and multipliers in the previous problem to be signed binary numbers. Implement the multiplier based on Booth's algorithm using
    a. cascaded linear sequence of carry save adders
    b. optimized Wallace tree adders

    Compare the performances of the two multipliers in terms of area, speed and power dissipation