Laboratory Assignments on Design Verification using VHDL

Sessional Practice #2

After completing this assignment, you will be able to:

i. Get familiarized with finite state machines.
ii. Model sequentially logic circuits by considering them as finite state machines.
iii. Understand the usage of functions in hardware modeling.

1. Consider a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z whenever $w = 1$ or $w = 0$ for four consecutive clock pulses the value of z has to be 1; otherwise, $z = 0$. Overlapping sequences are allowed, so that if $w = 1$ for five consecutive clock pulses the output z will be equal to 1 after the fourth and fifth pulses. Figure 1 illustrates the required relationship between w and z.

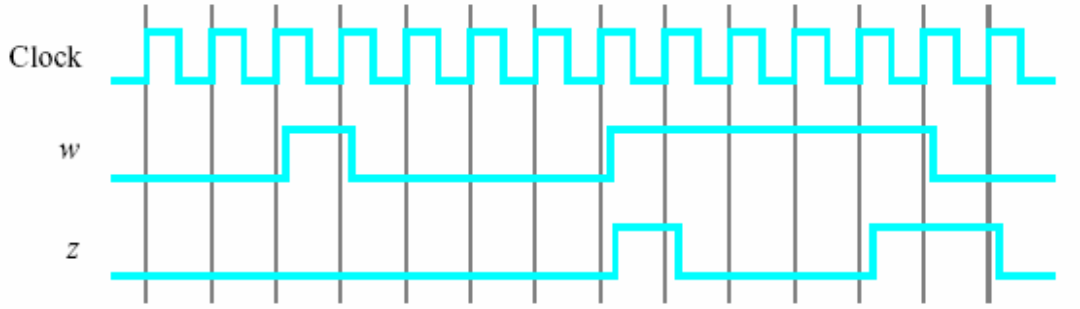

Figure 1. Required timing for the output z.

Draw a state diagram for this finite state machine. Behaviorally model the finite state machine using VHDL. Now draw the sequential circuit corresponding to this finite state machine. Structurally model the finite state machine using VHDL.

2. Build a package to perform 4 bit parallel addition with the help of a function. Use the package to model a 4 bit parallel adder.