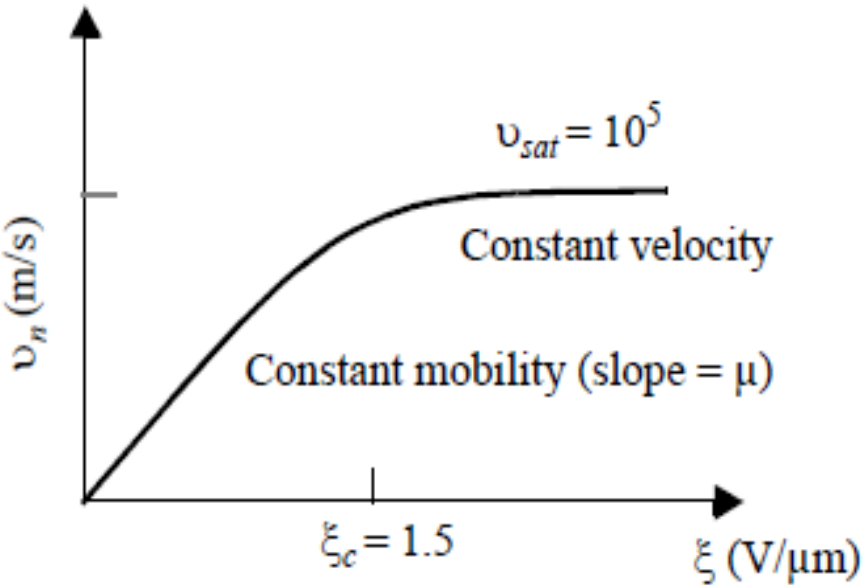
Process Variations

Devices parameters vary between runs and even on the same die!

Variations in the process parameters, such as impurity concentration densities, oxide thicknesses, and diffusion depths. These are caused by nonuniform conditions during the deposition and/or the diffusion of the impurities. This introduces variations in the sheet resistances and transistor parameters such as the threshold voltage.

Variations in the dimensions of the devices, mainly resulting from the limited resolution of the photolithographic process. This causes (W/L) variations in MOS transistors and mismatches in the emitter areas of bipolar devices.

Velocity Saturation



$$\upsilon_n = -\mu_n \xi(x) = \mu_n \frac{dV}{dx}$$

scattering effects (collisions suffered by the carriers)

For *p*-type silicon, the critical field at which electron saturation occurs is 1.5 V/μm

saturation velocity υ_{sat} approximately equals 10^5 m/s

$$\upsilon = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for} \quad \xi \le \xi_c$$

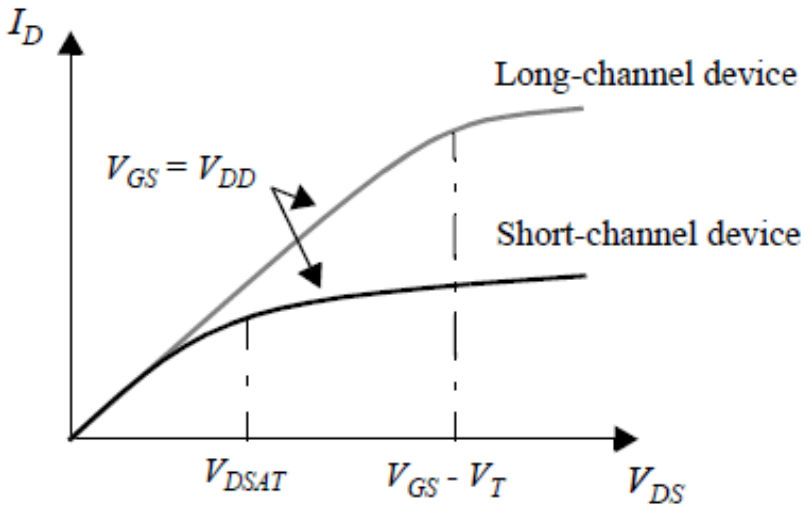
$$= \upsilon_{sat} \quad \text{for} \quad \xi \ge \xi_c$$

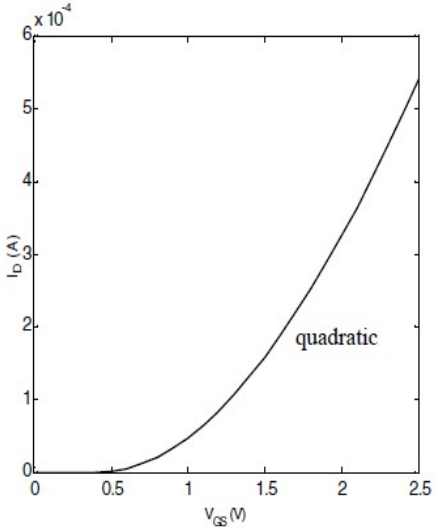
drain current in the resistive region

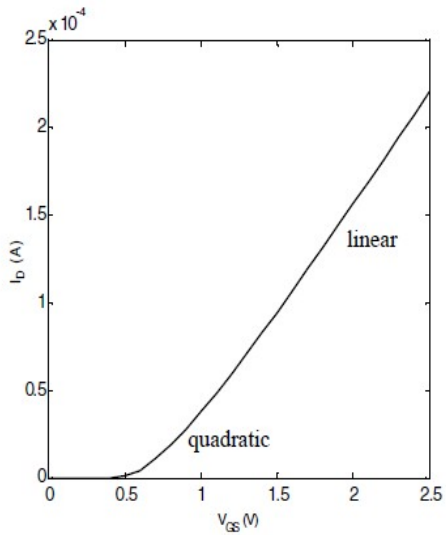
$$I_D = \kappa(V_{DS})\mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

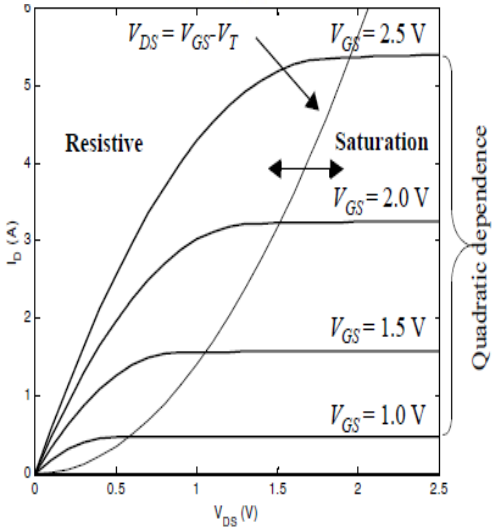
For short-channel devices, κ is smaller tha

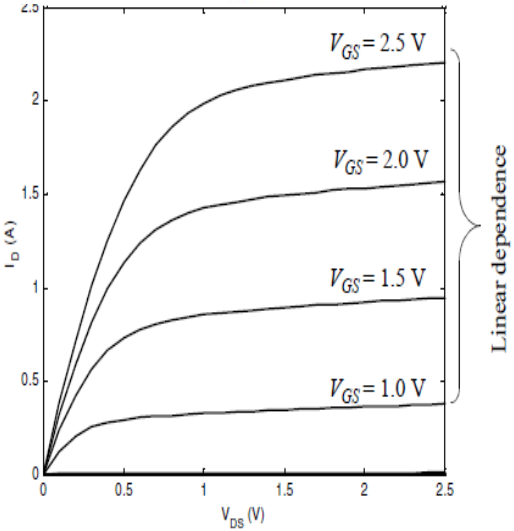
$$\kappa(V) = \frac{1}{1+(V/\xi_c L)}$$











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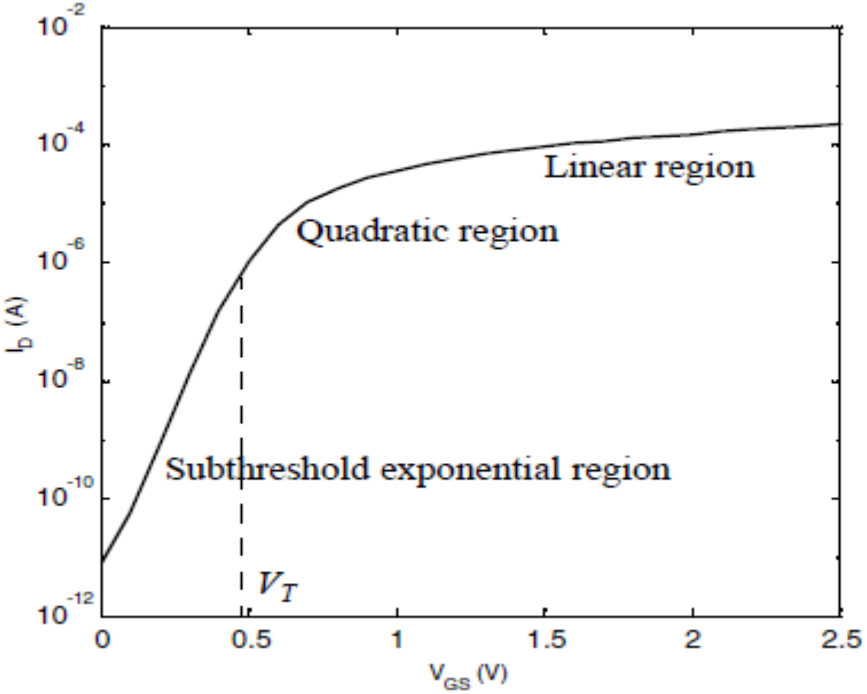
Subthreshold Conduction



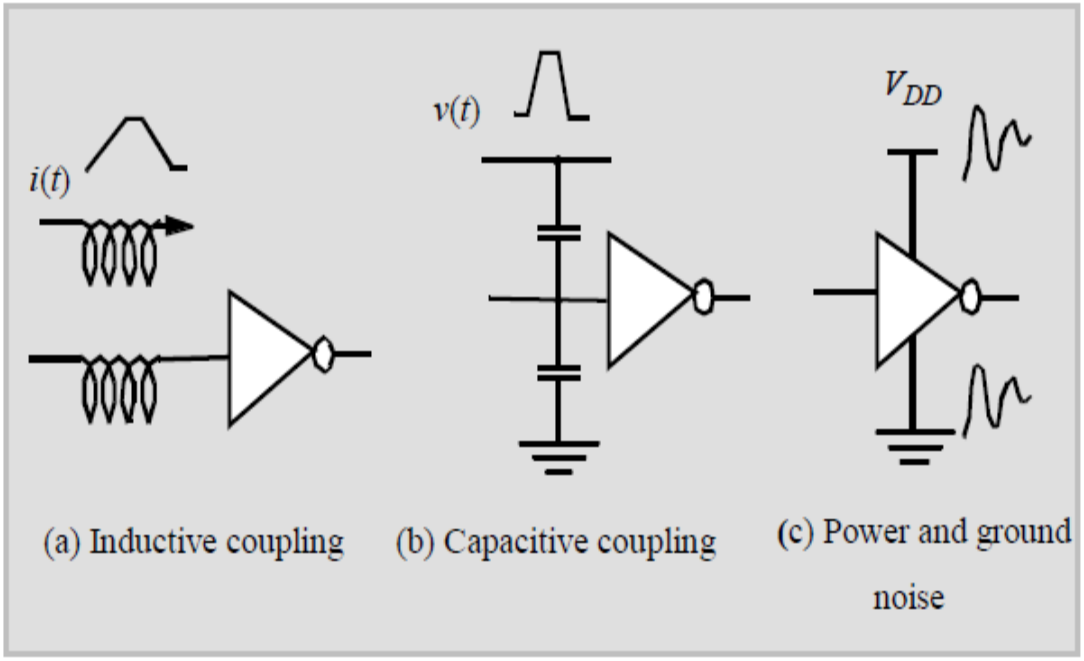
$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)$$

measures by how much V_{GS} has to be reduced for the drain current to drop by a factor $S = n\left(\frac{kT}{q}\right)\ln(10)$

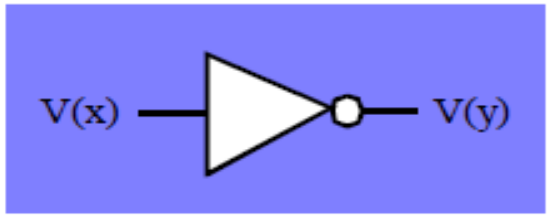
DIGITAL GATES
Fundamental Parameters

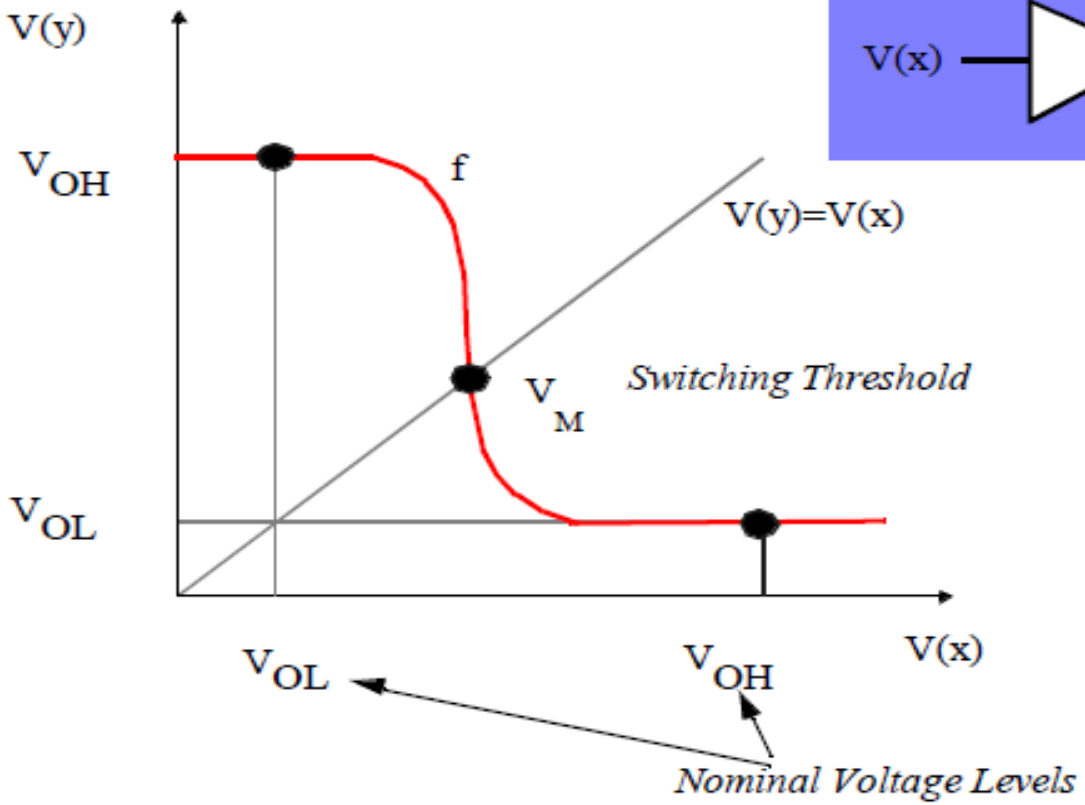
- Functionality
- Reliability, Robustness
- Area
- Performance
  - » Speed (delay)
  - » Power Consumption
  - » Energy

Noise in Digital Integrated Circuits

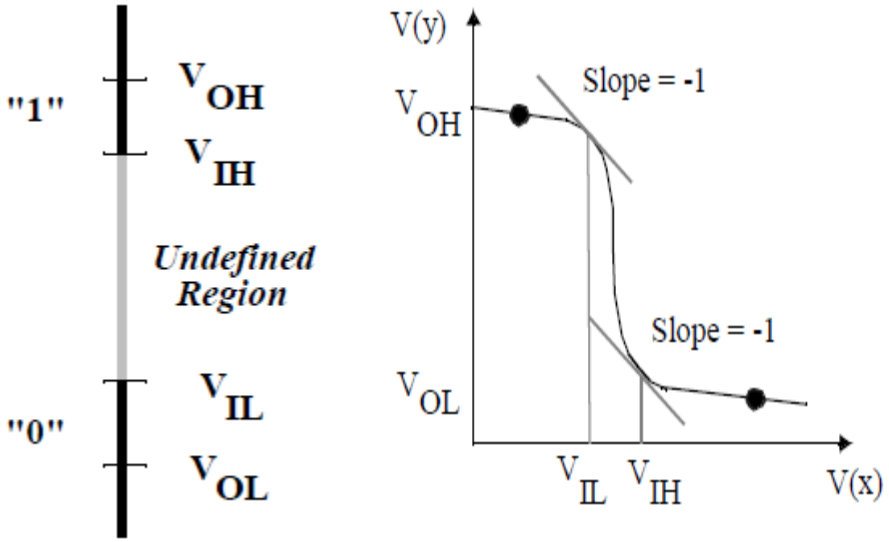


DC Operation: Voltage Transfer Characteristic



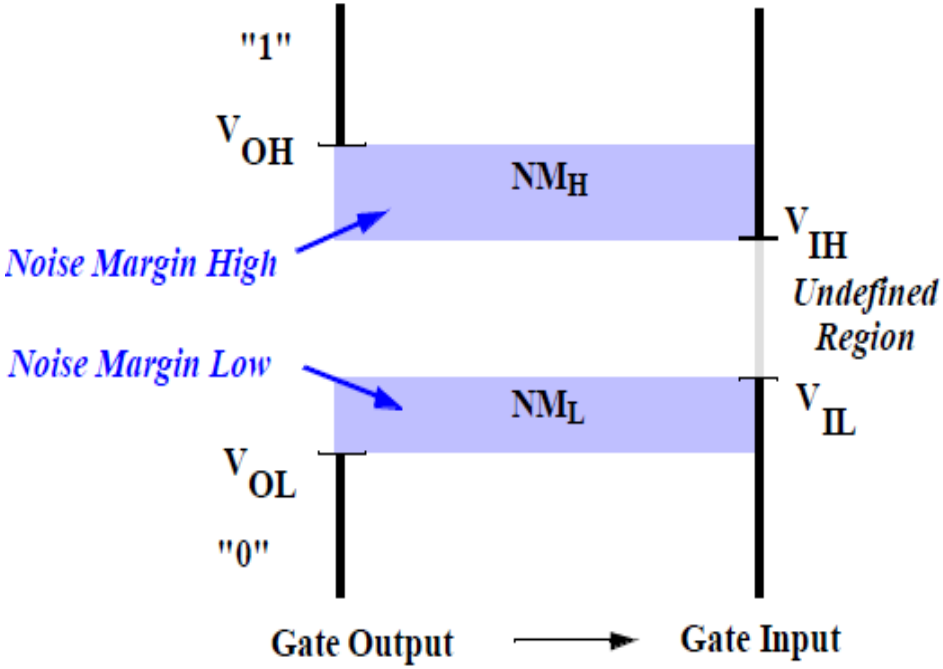


Mapping between analog and digital signals



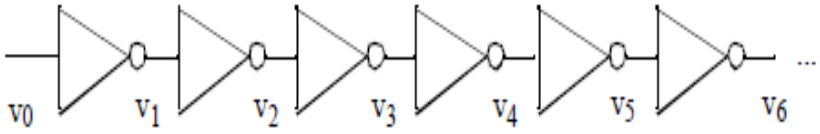
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

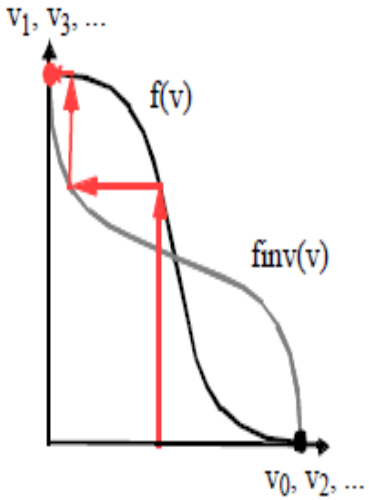


Definition of Noise Margins

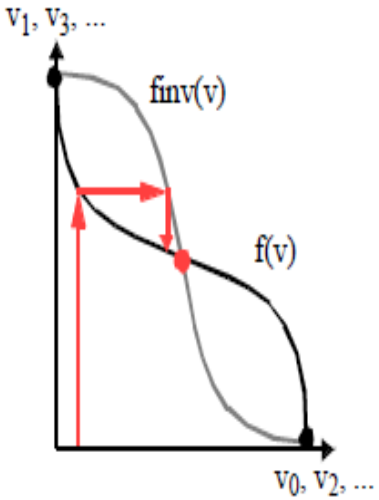
The Regenerative Property



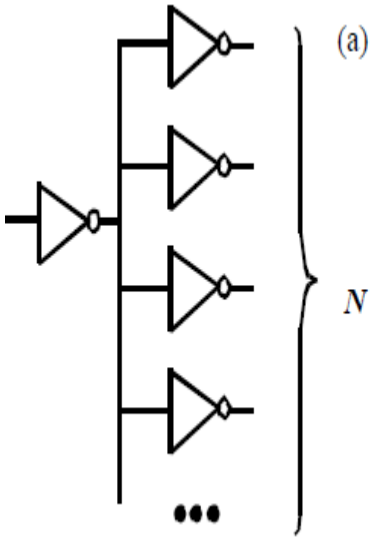
(a) A chain of inverters.

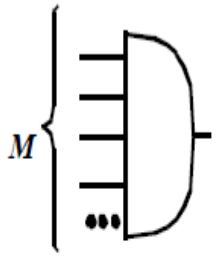


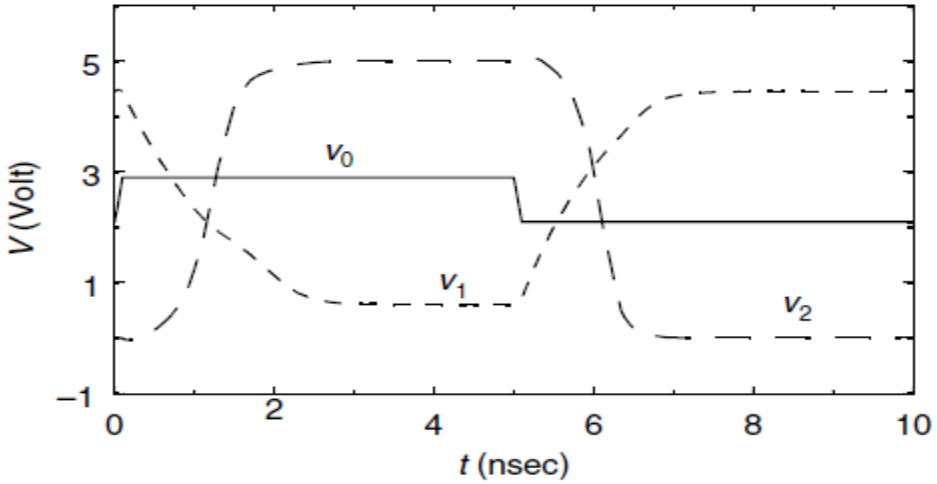
(b) Regenerative gate



(c) Non-regenerative gate







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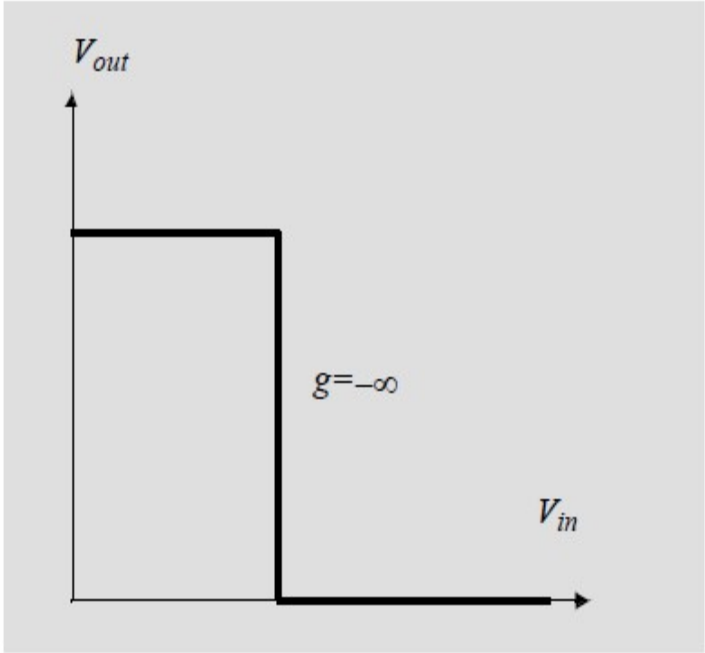
Noise Immunity

- proportional to the signal swing V_{sw}. The impact on the signal node is expressed as g V_{sw}.
- fixed. The impact on the signal node equals f V_{Nf}, with V_{nf} the amplitude of the noise source, and f the transfer function from noise to signal node.

$$V_{NM} = \frac{V_{sw}}{2} \geq \sum_i f_i V_{Nfi} + \sum_j g_j V_{sw}$$

$$V_{sw} \geq \frac{2\sum_i f_i V_{Nfi}}{1 - 2\sum_j g_j}$$

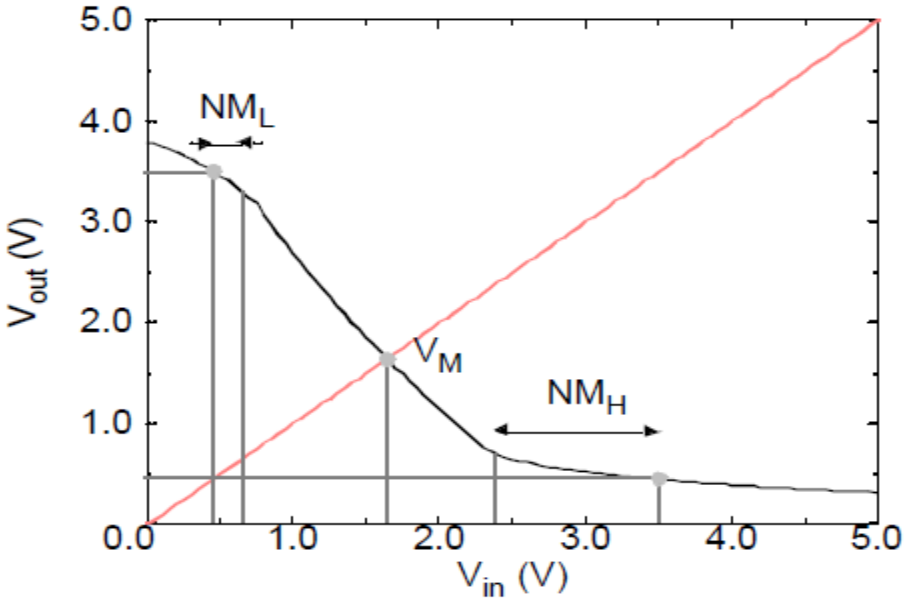
The Ideal Gate



$R_i = \infty$

$R_o = 0$

VTC of Real Inverter



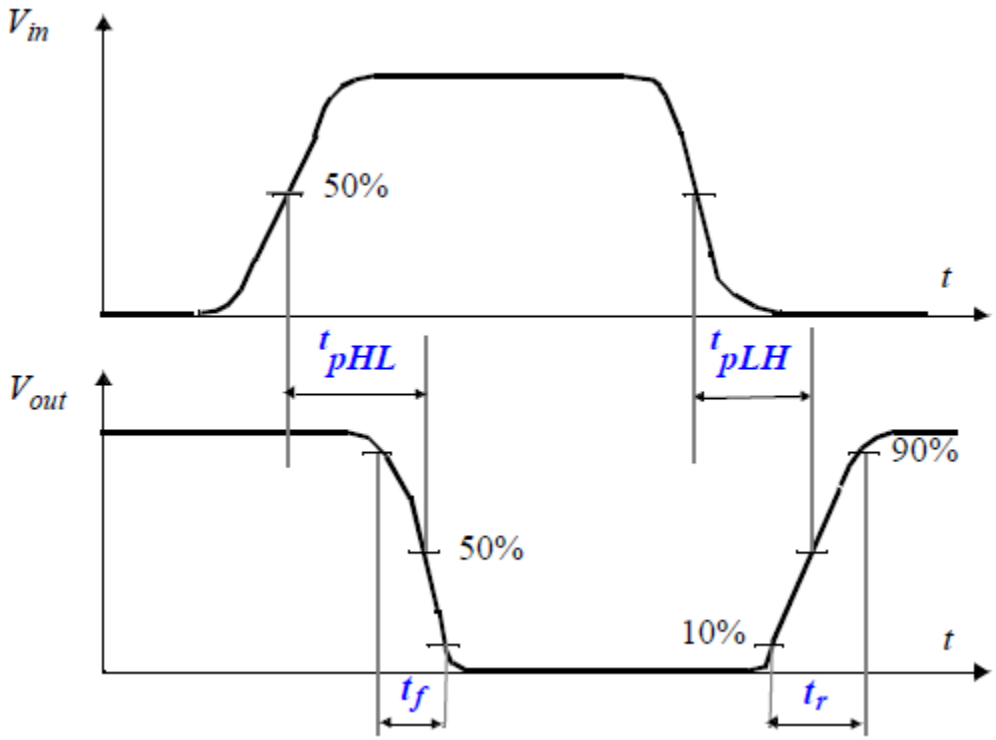
$V_{OH} = 3.5$ V; $V_{OL} = 0.45$ V

$V_{IH} = 2.35$ V; $V_{IL} = 0.66$ V

$V_M = 1.64$ V

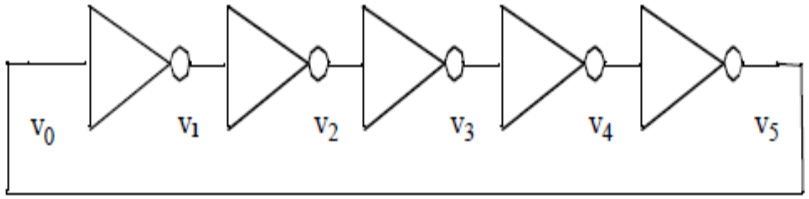
$NM_H = 1.15$ V; $NM_L = 0.21$ V

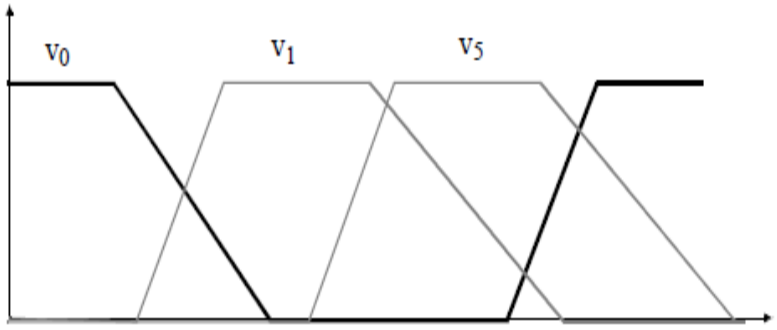
Delay Definitions



$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

Ring Oscillator





$$T = 2 \times t_p \times N$$

$$2Nt_p >> t_f + t_r$$

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Power Dissipation

$$P_{peak} = i_{peak} V_{supply} = max(p(t))$$

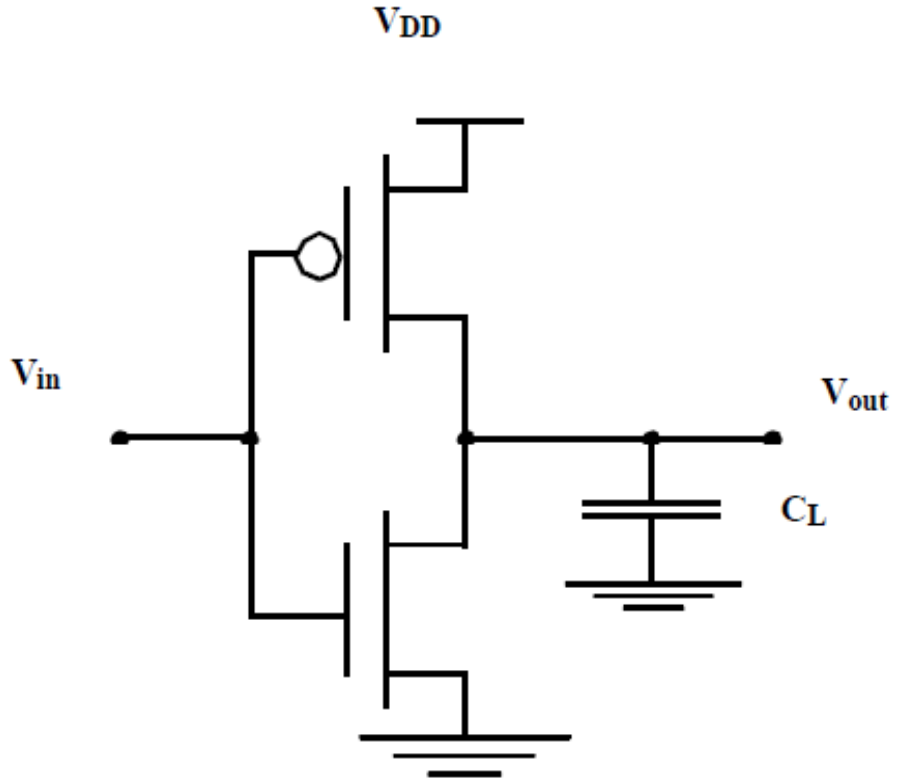
$$P_{av} = \frac{1}{T}\int_0^T p(t)dt = \frac{V_{supply}}{T}\int_0^T i_{supply}(t)dt$$

Power-Delay Product

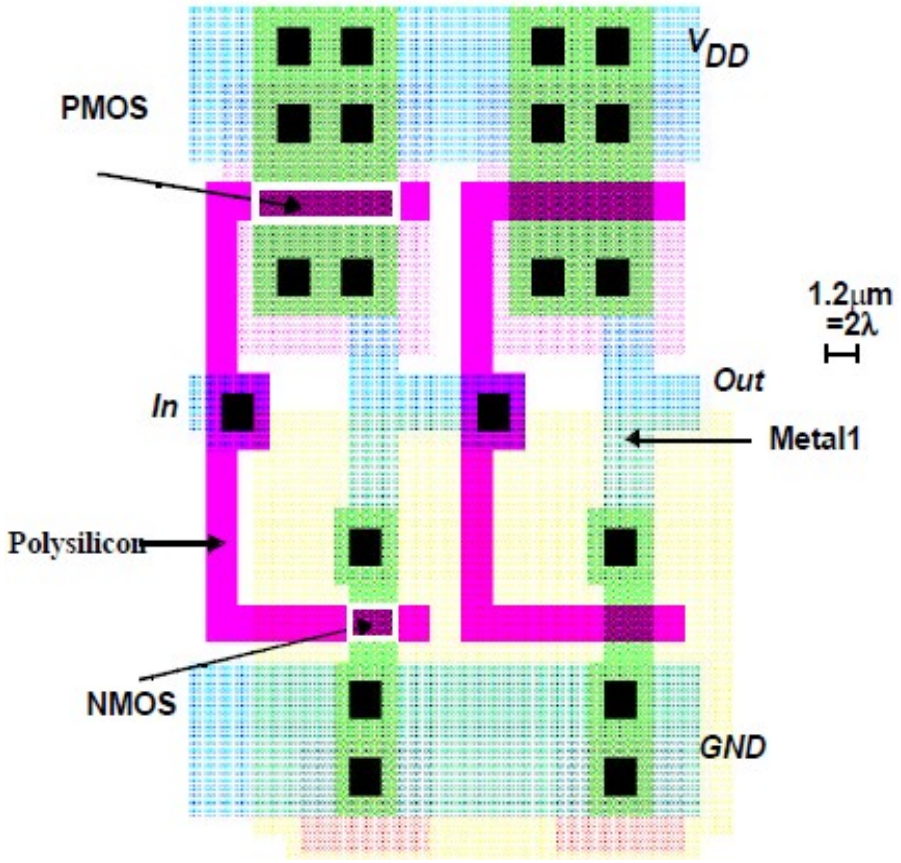
$$PDP = t_p \times P_{av}$$

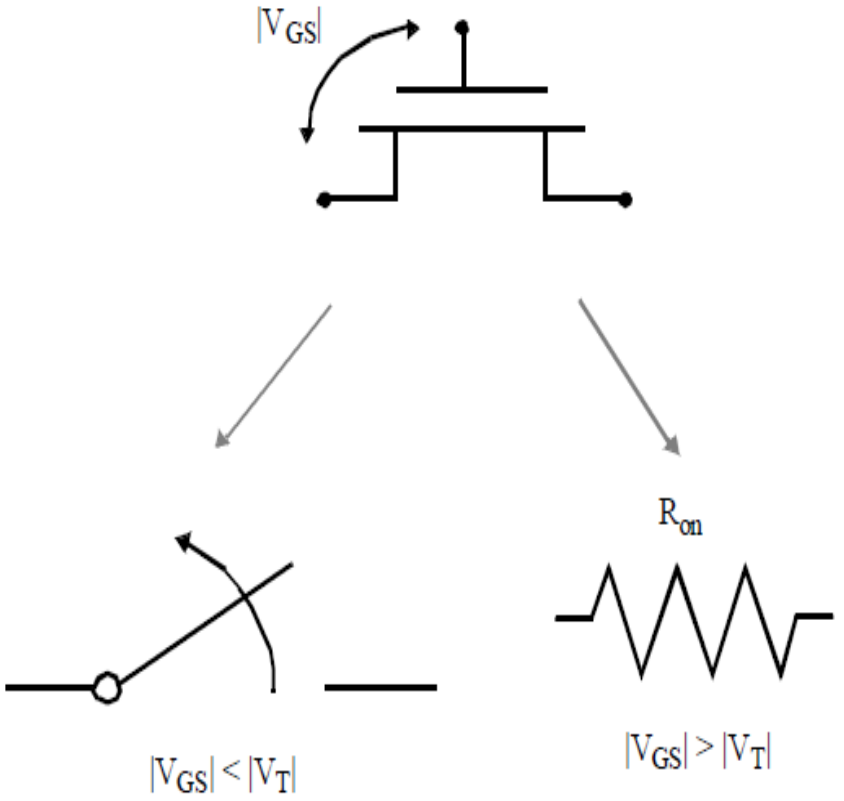
= Energy dissipated per operation

The CMOS Inverter



CMOS Inverters





Switch Model of CMOS Transistor

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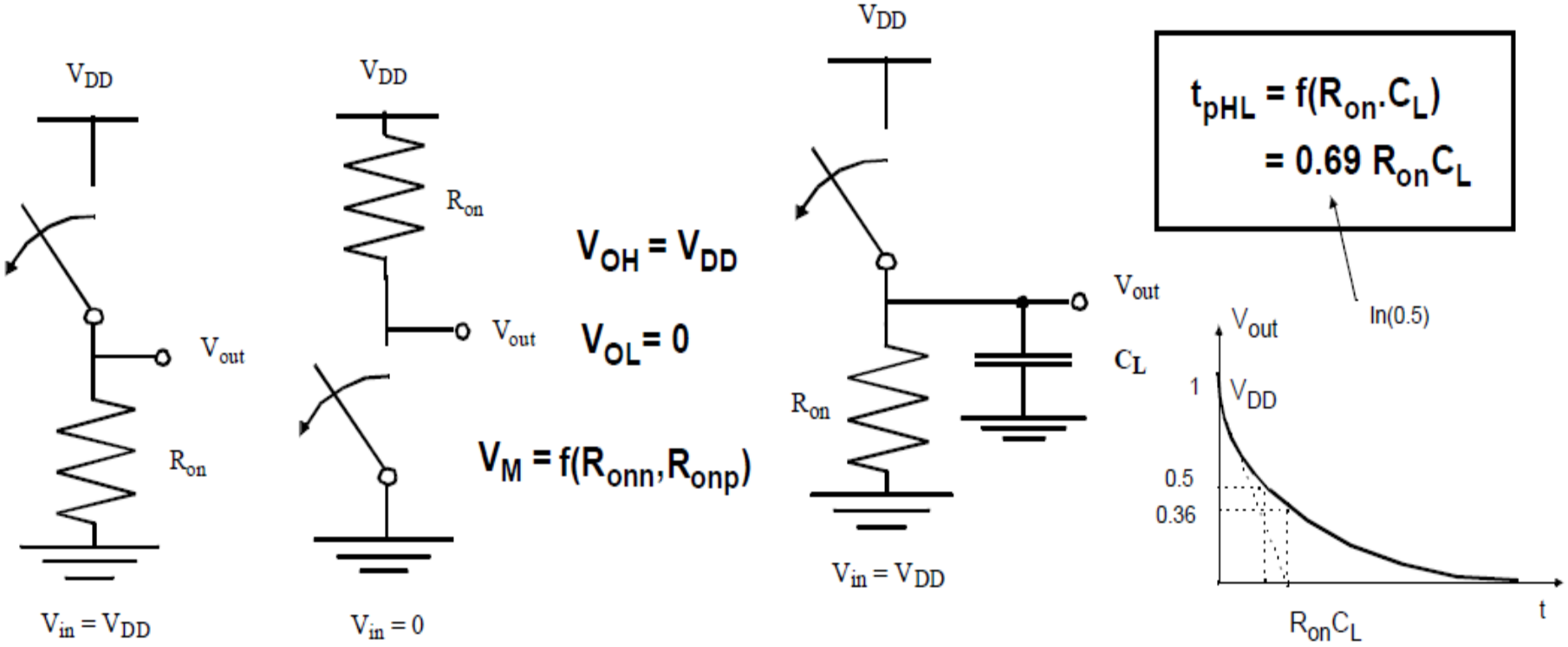
Some points to note .....

- The high and low output levels equal V_{DD} and *GND*, respectively; in other words, the voltage swing is equal to the supply voltage. This results in high noise margins.
- The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size. Gates with this property are called *ratioless*. This is in contrast with *ratioed logic*, where logic levels are determined by the relative dimensions of the composing transistors.
- In steady state, there always exists a path with finite resistance between the output and either V_{DD} or *GND*. A well-designed CMOS inverter, therefore, has a *low output impedance*, which makes it less sensitive to noise and disturbances. Typical values of the output resistance are in kΩ range.
- The *input resistance* of the CMOS inverter is extremely high, as the gate of an MOS transistor is a virtually perfect insulator and draws no dc input current. Since the input node of the inverter only connects to transistor gates, the steady-state input current is nearly zero. A single inverter can theoretically drive an infinite number of gates (or have an infinite fan-out) and still be functionally operational; however, increasing the fan-out also increases the propagation delay, as will become clear below. So, although fan-out does not have any effect on the steady-state behavior, it degrades the transient response.

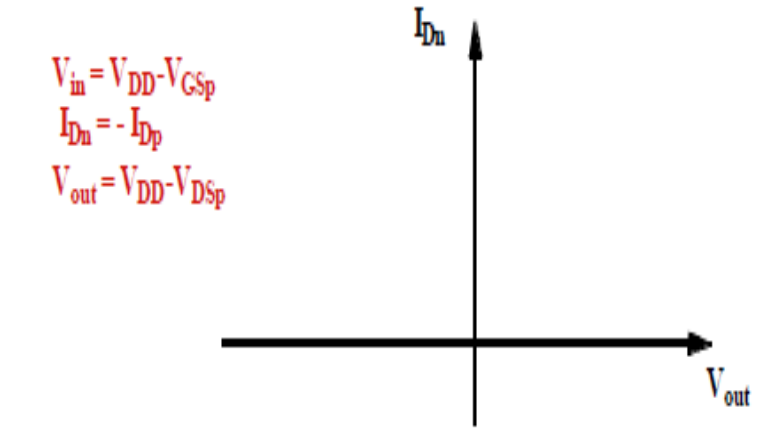
CMOS Inverter: Steady State Response



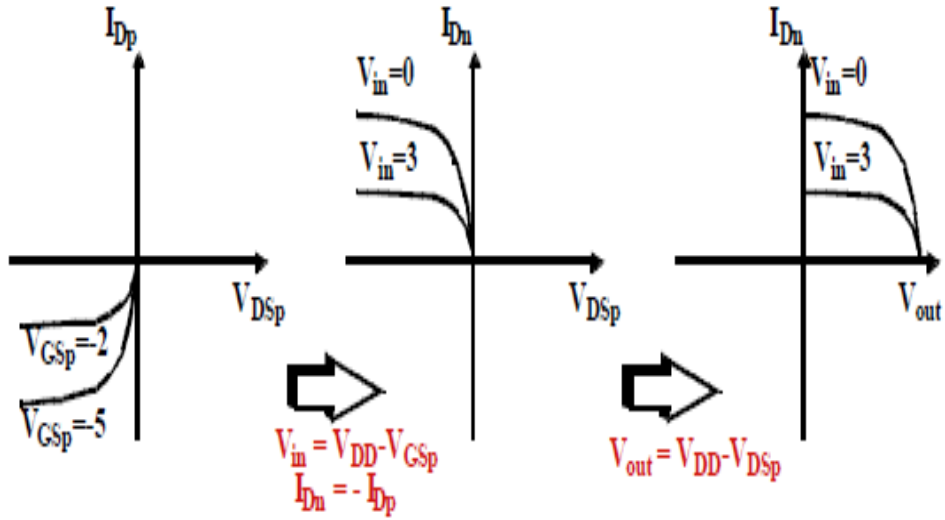
CMOS Inverter: Transient Response

CMOS Properties

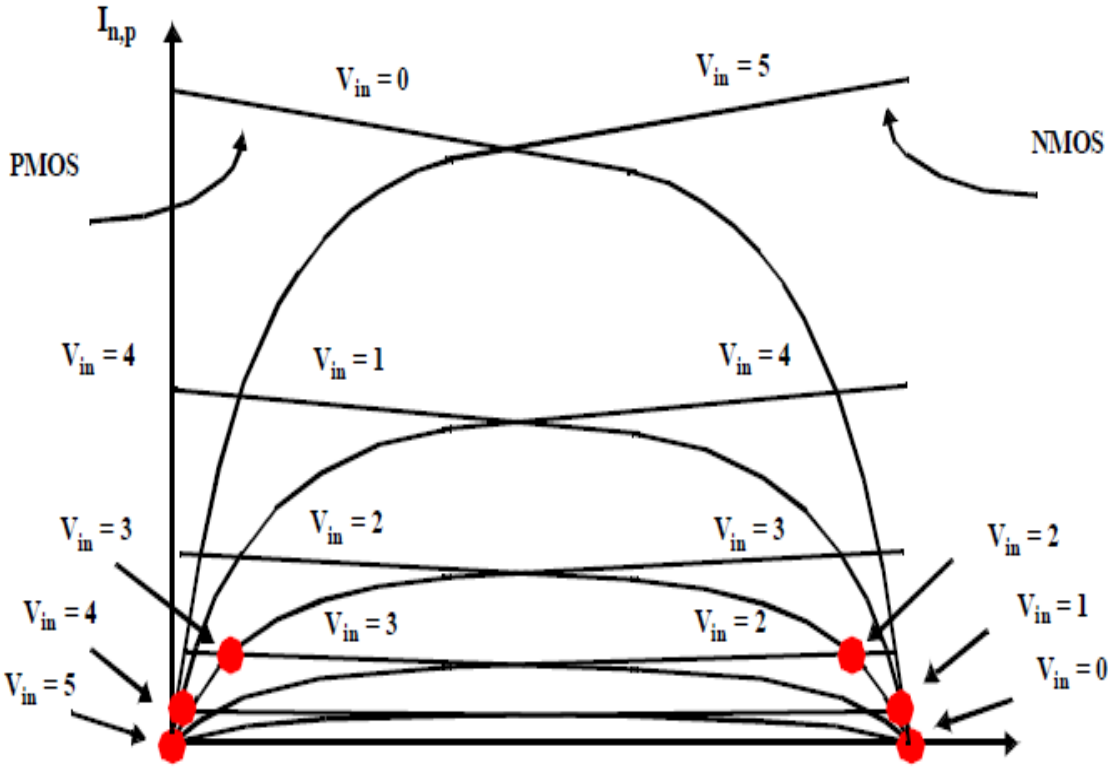
- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching



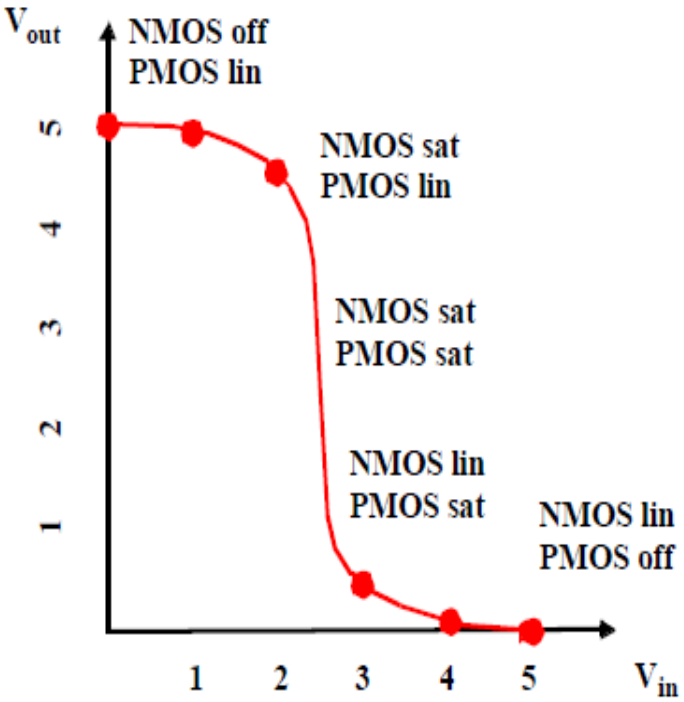
PMOS Load Lines



CMOS Inverter Load Characteristics



CMOS Inverter VTC



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CMOS Inverter: The Static Behavior

The switching threshold, V_M, is defined as the point where $V_{in} = V_{out}$.

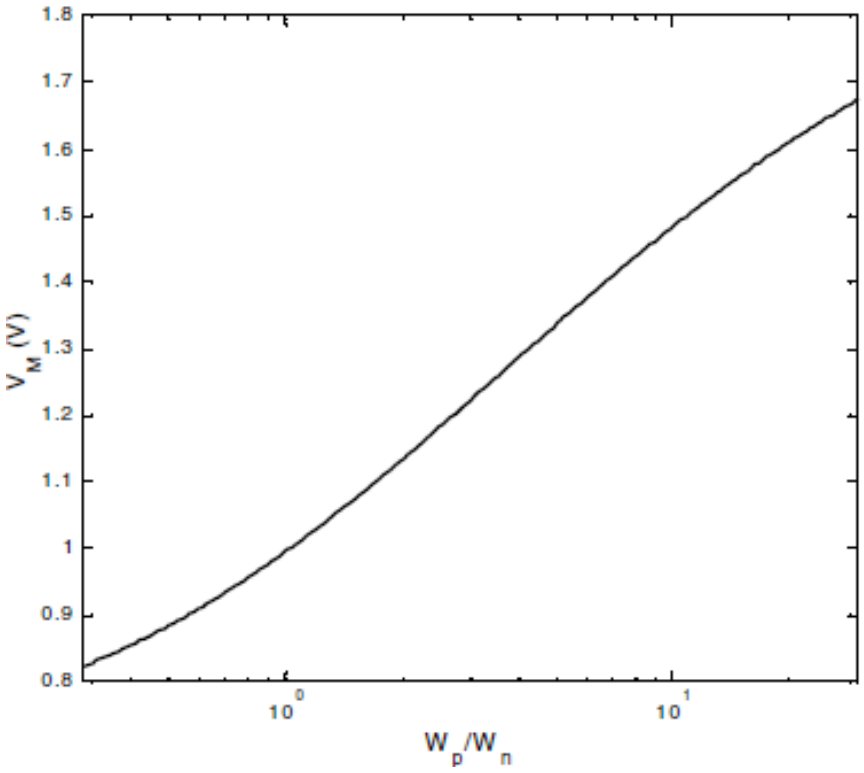
$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right) = 0$$

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1 + r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$$

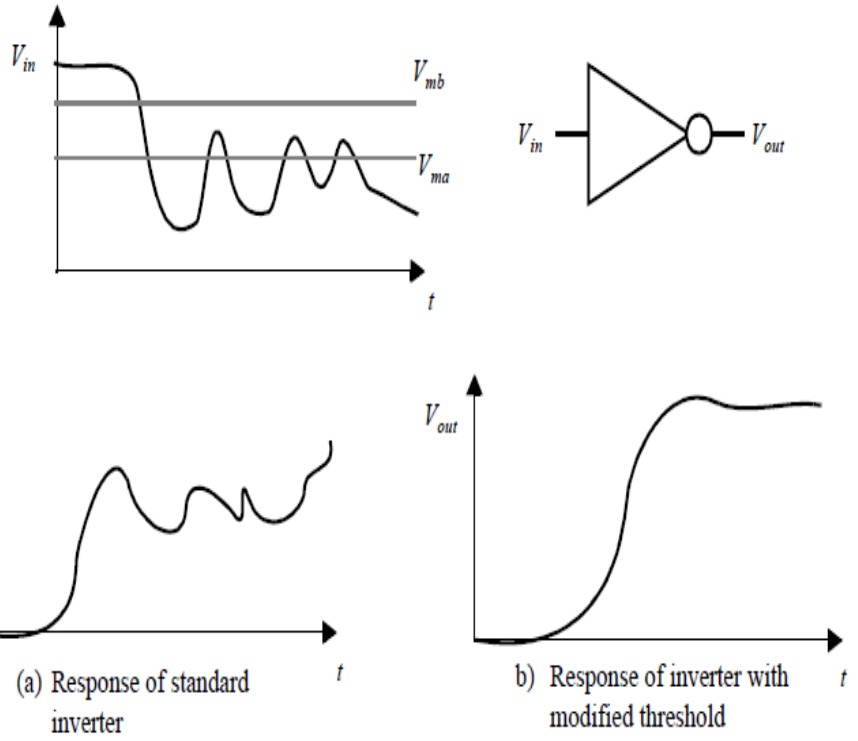
$$V_M \approx \frac{r V_{DD}}{1 + r}$$

$$(W/L)_p = (W/L)_n \times (V_{DSATn} k'_n)/(V_{DSATn} k'_p)$$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k'_p V_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)}$$



Changing the inverter threshold can improve the circuit reliability



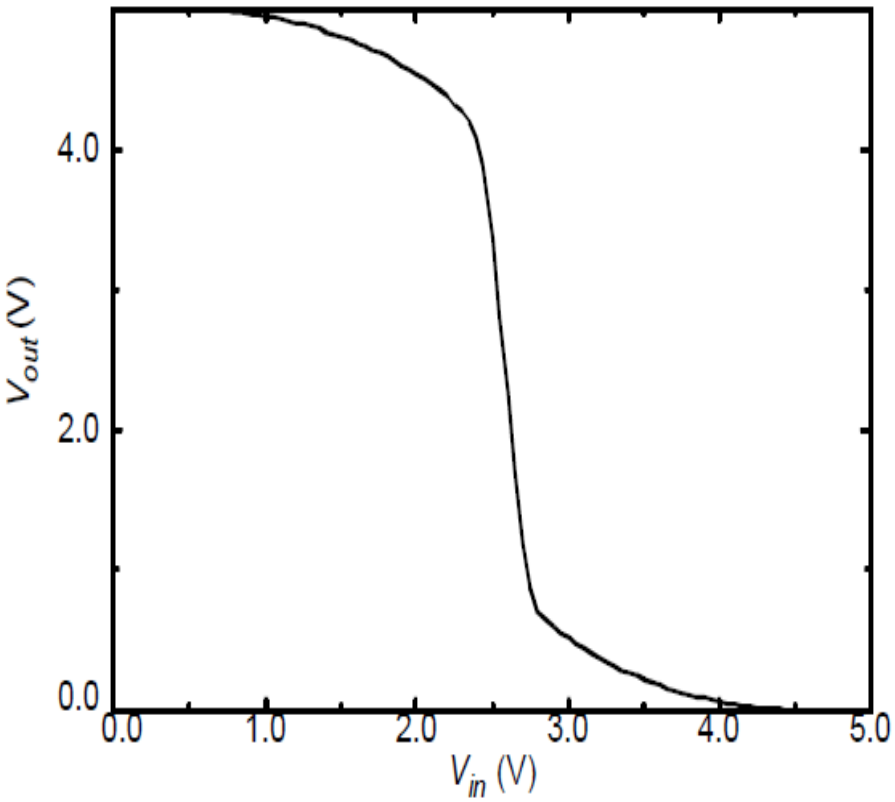
(a) Response of standard inverter

b) Response of inverter with modified threshold

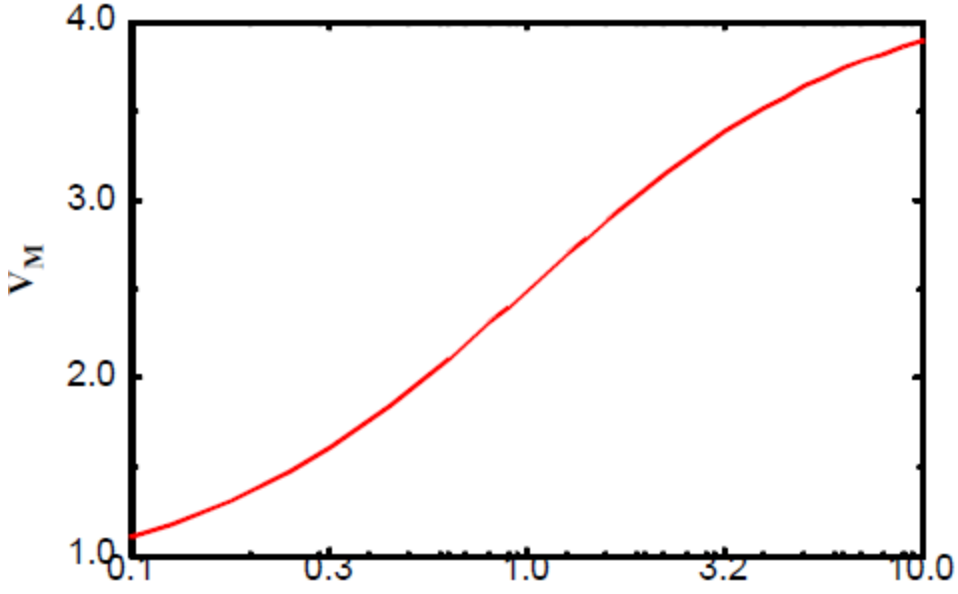
V_M is relatively insensitive to variations in the device ratio

The effect of changing the W_p/W_n ratio is to shift the transient region of the VTC

Simulated VTC



Gate Switching Threshold



$$V_M = \frac{r(V_{DD} - |V_{Tp}|) + V_{Tn}}{1 + r} \quad \text{with} \quad r = \sqrt{\frac{k_p}{k_n}}$$

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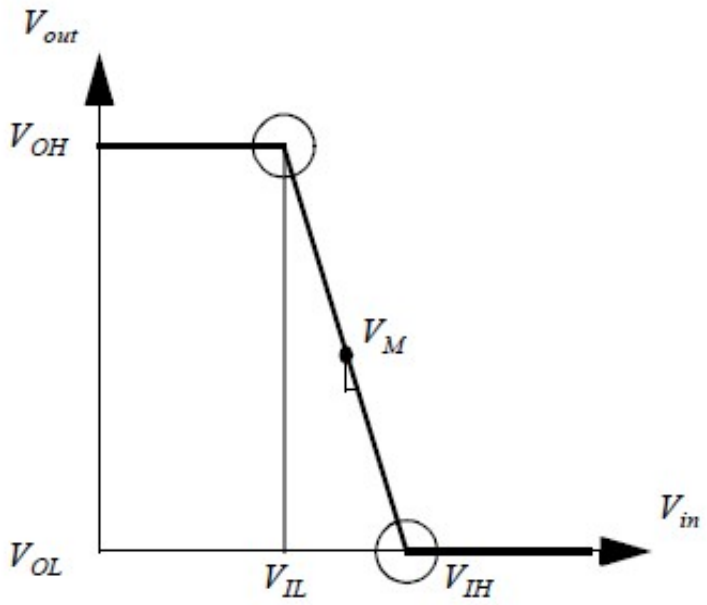
Noise Margins

V_{IH} and V_{IL} are the operational points of the inverter where $\frac{dV_{out}}{dV_{in}} = -1$



$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

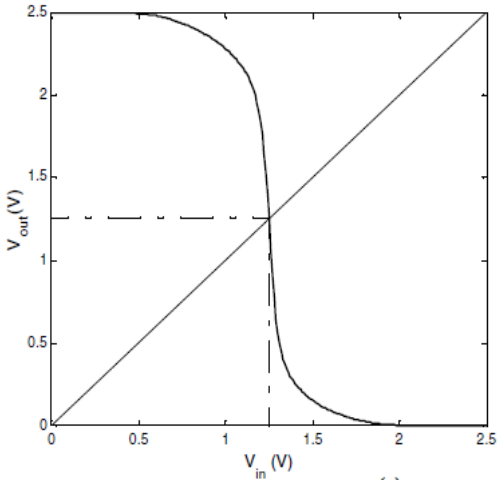
$$k_n V_{DSATn}\left(V_{in} - V_{Tn} - \frac{V_{DSATn}}{2}\right)(1 + \lambda_n V_{out}) +$$

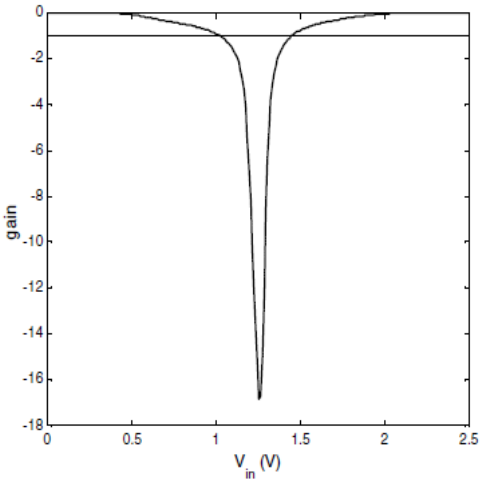
$$k_p V_{DSATp}\left(V_{in} - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)(1 + \lambda_p V_{out} - \lambda_p V_{DD}) = 0$$

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n V_{DSATn}(1 + \lambda_n V_{out}) + k_p V_{DSATp}(1 + \lambda_p V_{out} - \lambda_p V_{DD})}{\lambda_n k_n V_{DSATn}(V_{in} - V_{Tn} - V_{DSATn}/2) + \lambda_p k_p V_{DSATp}(V_{in} - V_{DD} - V_{Tp} - V_{DSATp}/2)}$$

$$g = -\frac{1}{I_D(V_M)}\frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$

$$\approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$





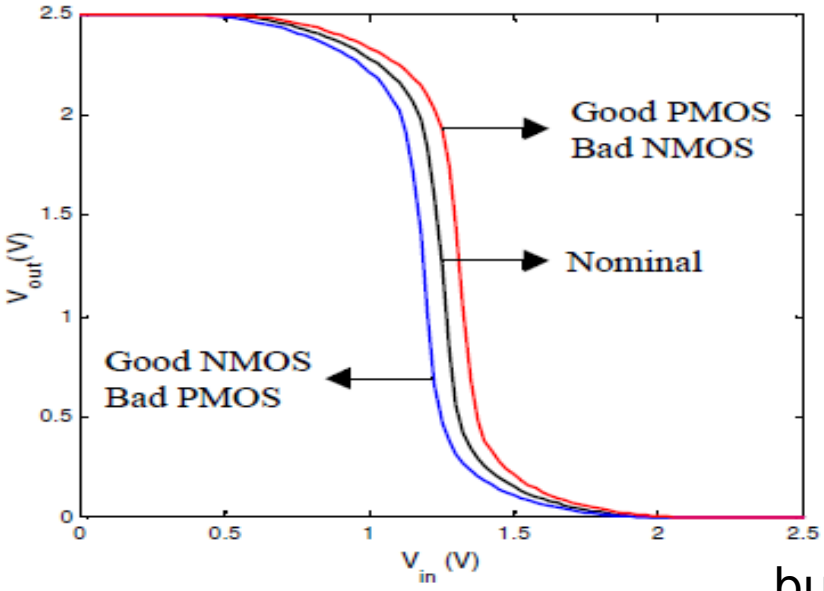
Assume an inverter in the generic 0.25 μm CMOS technology designed with a PMOS/NMOS ratio of 3.4 and with the NMOS transistor minimum size ($W = 0.375$ μm, $L = 0.25$ μm, $W/L = 1.5$). We first compute the gain at V_M (= 1.25 V),

$$I_D(V_M) = 1.5 \times 115 \times 10^{-6} \times 0.63 \times (1.25 - 0.43 - 0.63/2) \times (1 + 0.06 \times 1.25) = 59 \times 10^{-6}\ \text{A}$$

$$g = -\frac{1}{59 \times 10^{-6}}\frac{1.5 \times 115 \times 10^{-6} \times 0.63 + 1.5 \times 3.4 \times 30 \times 10^{-6} \times 1.0}{0.06 + 0.1} = -27.5$$

This yields the following values for V_{IL}, V_{IH}, NM_L, NM_H:

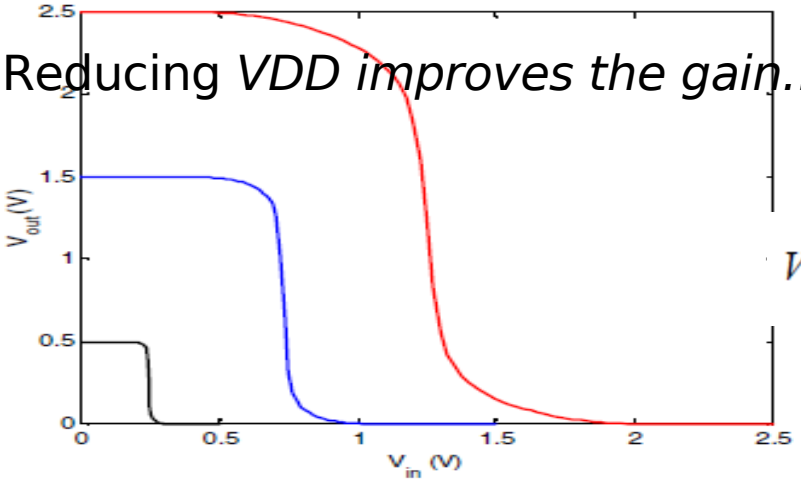
$$V_{IL} = 1.2\ \text{V},\ V_{IH} = 1.3\ \text{V},\ NM_L = NM_H = 1.2.$$



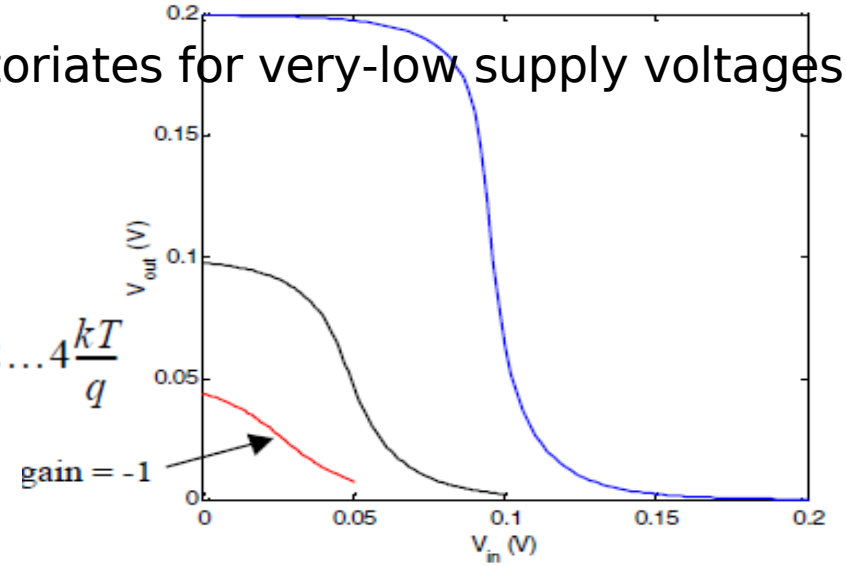
Impact of device variations on static CMOS inverter VTC. The "good" device has a smaller oxide thickness (- 3nm), a smaller length (-25 nm), a higher width (+30 nm), and a smaller threshold (-60 mV). The opposite is true for the "bad" transistor.

but it detoriates for very-low supply voltages

Reducing *VDD improves the gain...*



$$V_{DDmin} > 2 \ldots 4\frac{kT}{q}$$



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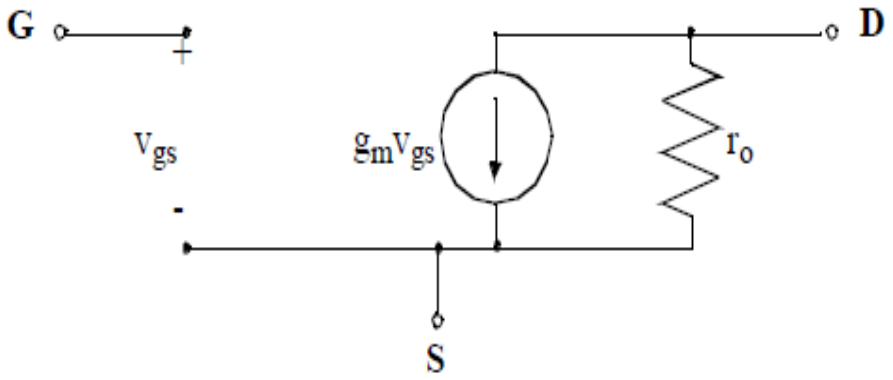
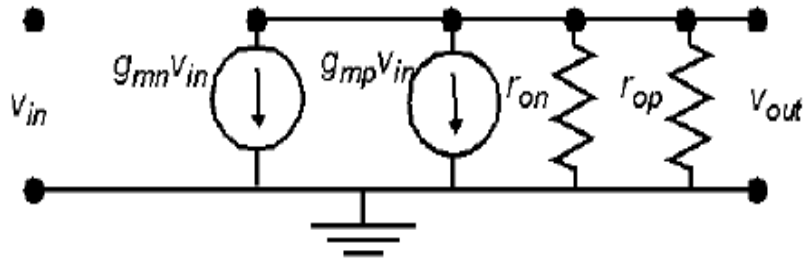
MOS Transistor Small Signal Model



	g_m	r_o
linear	kV_{DS}	$[k(V_{GS}-V_T-V_{DS})]^{-1}$
saturation	$k(V_{GS}-V_T)$	$1/\lambda I_D$

At V_{IH} (V_{IL}): $\frac{\partial V_{out}}{\partial V_{in}} = -1$

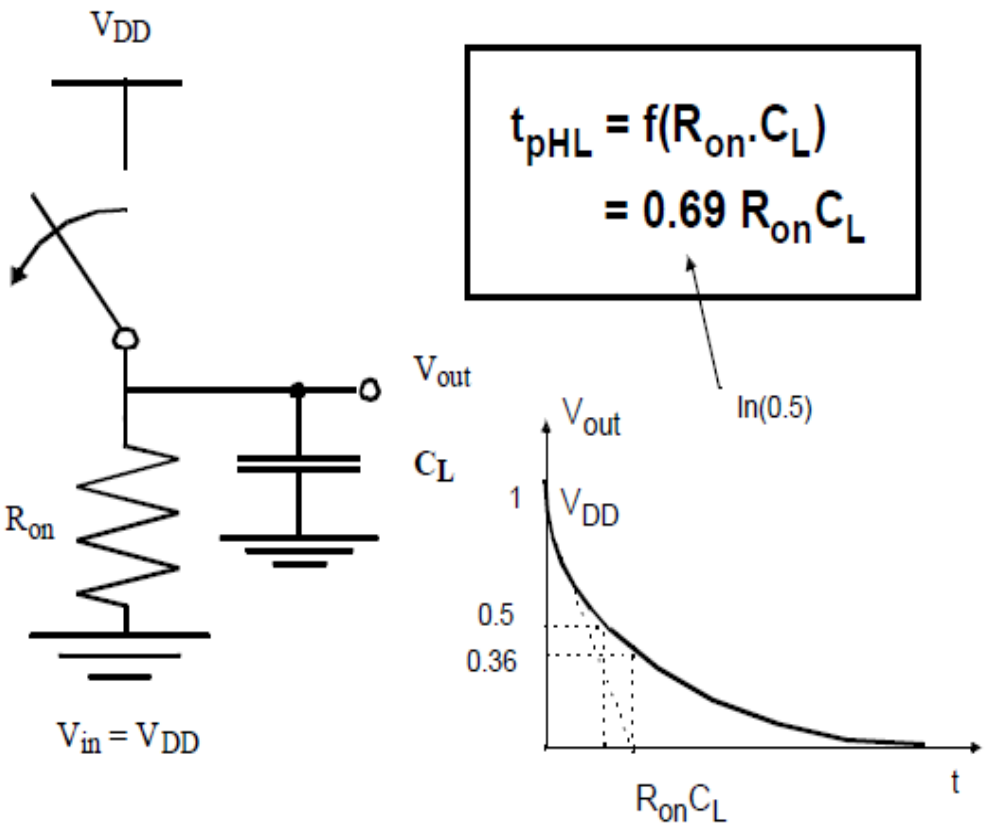
small-signal model of inverter



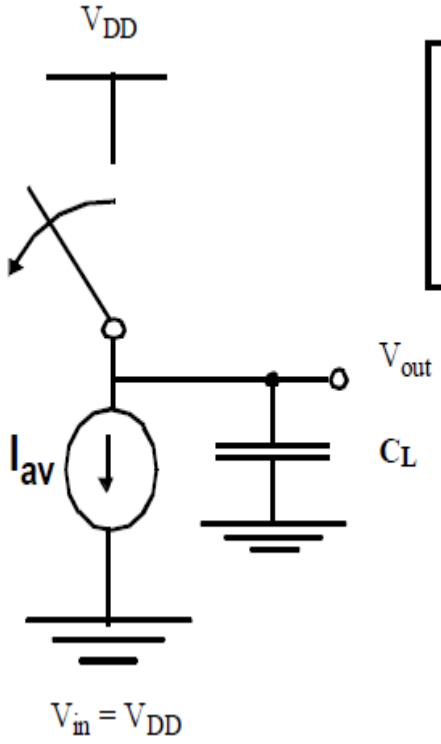
$$g = \frac{v_{out}}{v_{in}} = -(g_{mn} + g_{mp}) \times (r_{on} \| r_{op}) = -1$$

Determining V_{IH} and V_{IL}

CMOS Inverter: Transient Response



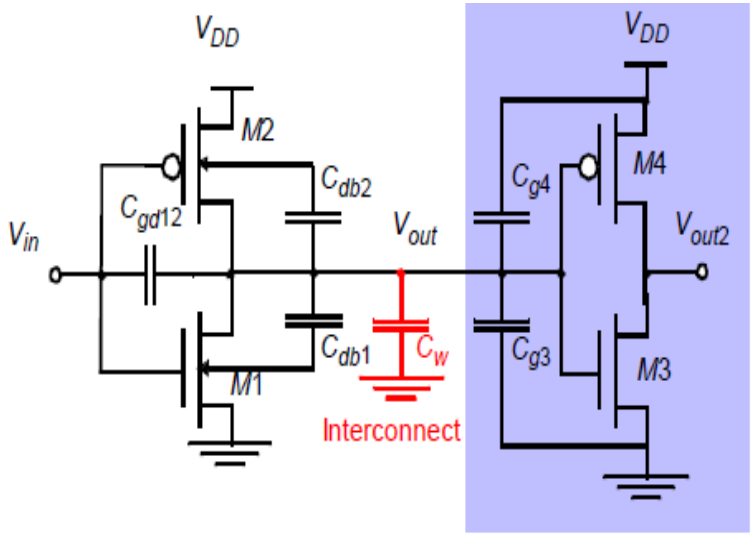
$$t_{pHL} = f(R_{on}.C_L) = 0.69\, R_{on} C_L$$



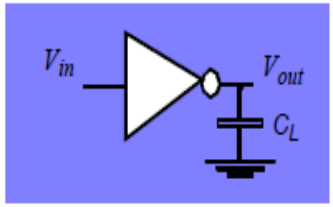
$$t_{pHL} = \frac{C_L V_{swing}/2}{I_{av}} \sim \frac{C_L}{k_n V_{DD}}$$

CMOS Inverter Propagation Delay

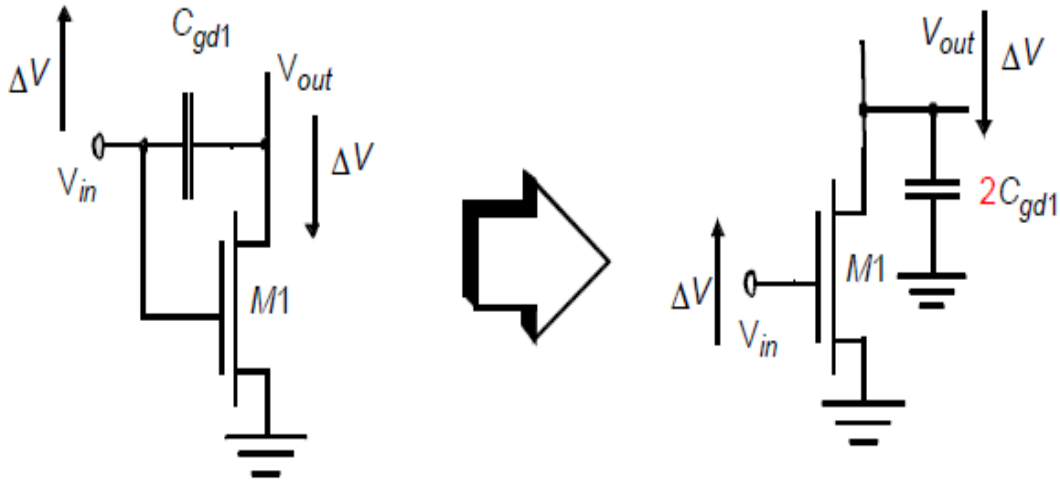
Computing the Capacitances



Simplified Model



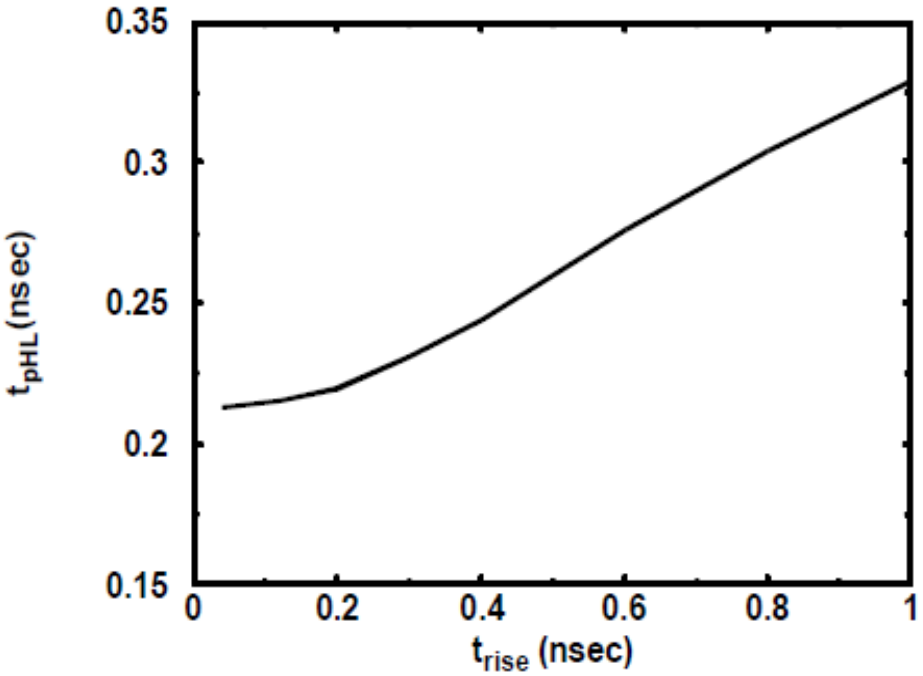
The Miller Effect



"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."

Computing the Capacitances

Capacitor	Expression
C_{gd1}	2 CGD0 W_n
C_{gd2}	2 CGD0 W_p
C_{db1}	K_{eqn} (AD_n CJ + PD_n CJSW)
C_{db2}	K_{eqp} (AD_p CJ + PD_p CJSW)
C_{g3}	C_{ox} W_n L_n
C_{g4}	C_{ox} W_p L_p
C_w	From Extraction
C_L	Σ



$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

Impact of Rise Time on Delay

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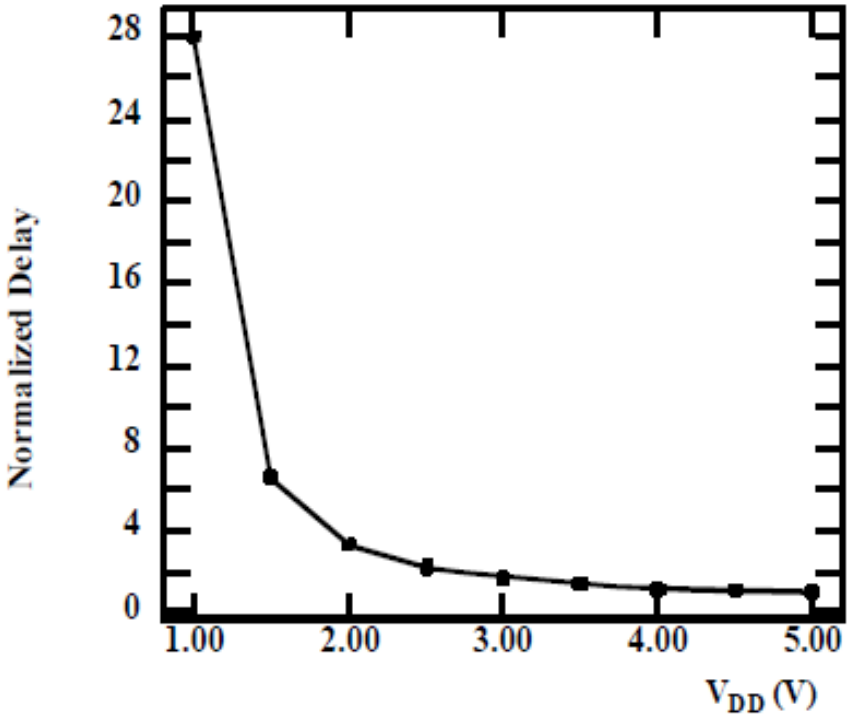
Delay as a function of V_{DD}



Where Does Power Go in CMOS?

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

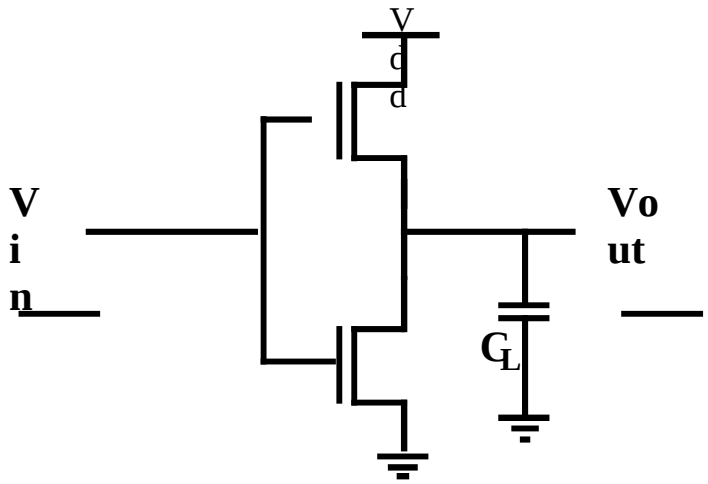
- **Short Circuit Currents**

  Short Circuit Path between Supply Rails during Switching

- **Leakage**

  Leaking diodes and transistors

Dynamic Power Dissipation

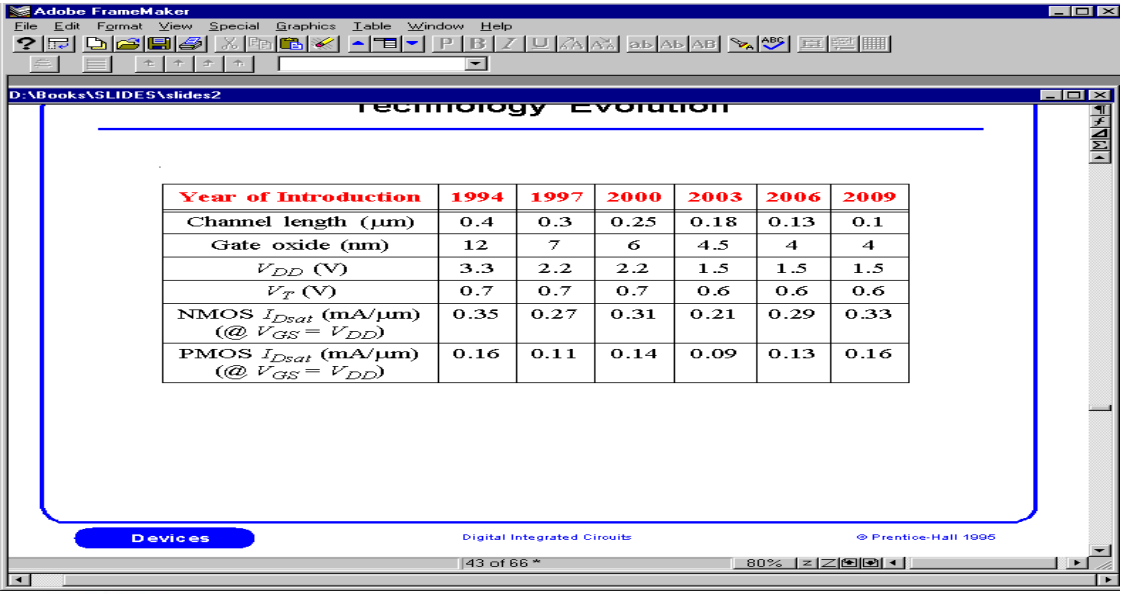


Energy/transition = $C_L * V_{dd}^2$

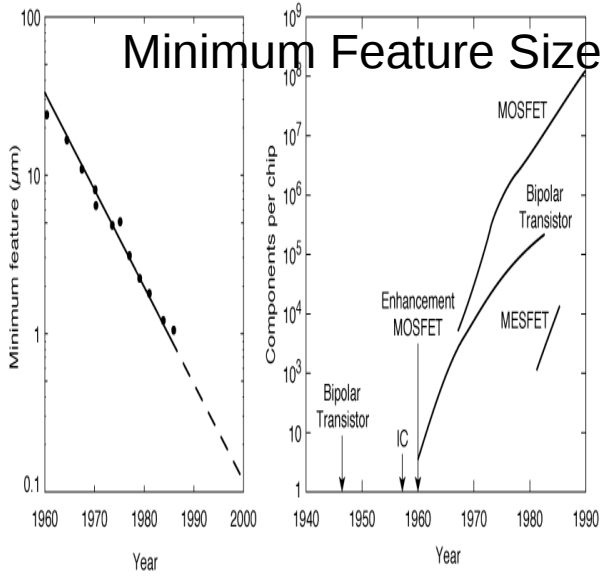
Power = Energy/transition * f = $C_L * V_{dd}^2 * f$

Not a function of transistor sizes!

Need to reduce C_L, V_{dd}, and f to reduce power.



Year of Introduction	1994	1997	2000	2003	2006	2009
Channel length (μm)	0.4	0.3	0.25	0.18	0.13	0.1
Gate oxide (nm)	12	7	6	4.5	4	4
V_{DD} (V)	3.3	2.2	2.2	1.5	1.5	1.5
V_T (V)	0.7	0.7	0.7	0.6	0.6	0.6
NMOS I_{Dsat} (mA/μm) (@ $V_{GS} = V_{DD}$)	0.35	0.27	0.31	0.21	0.29	0.33
PMOS I_{Dsat} (mA/μm) (@ $V_{GS} = V_{DD}$)	0.16	0.11	0.14	0.09	0.13	0.16



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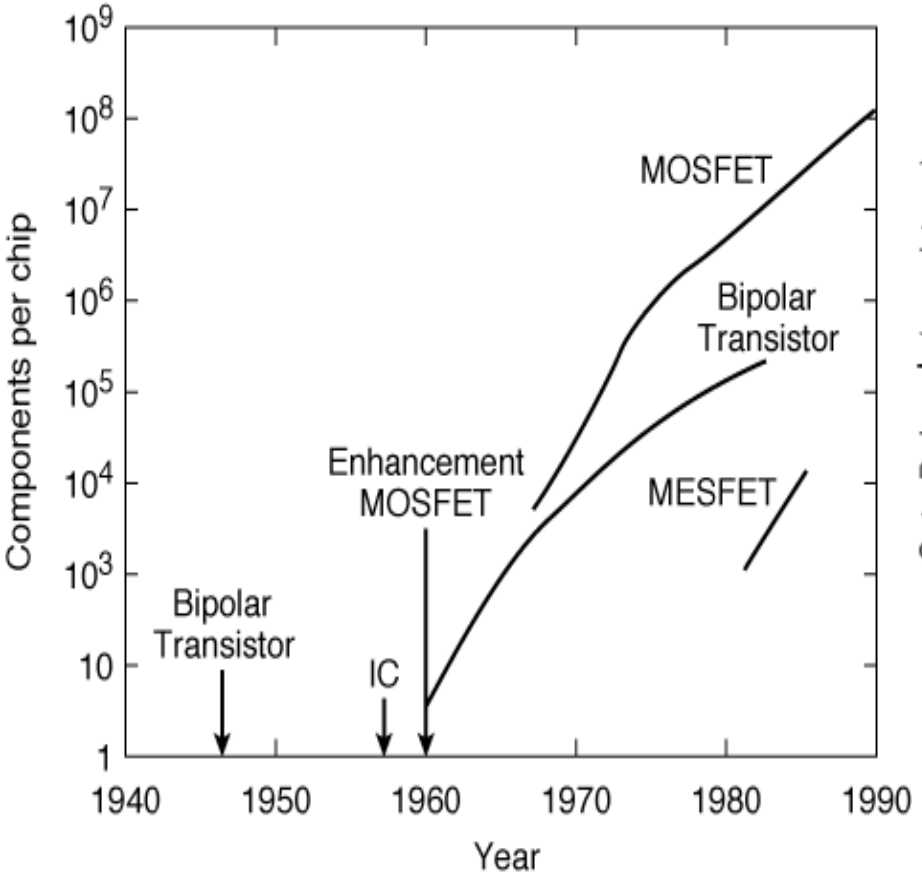
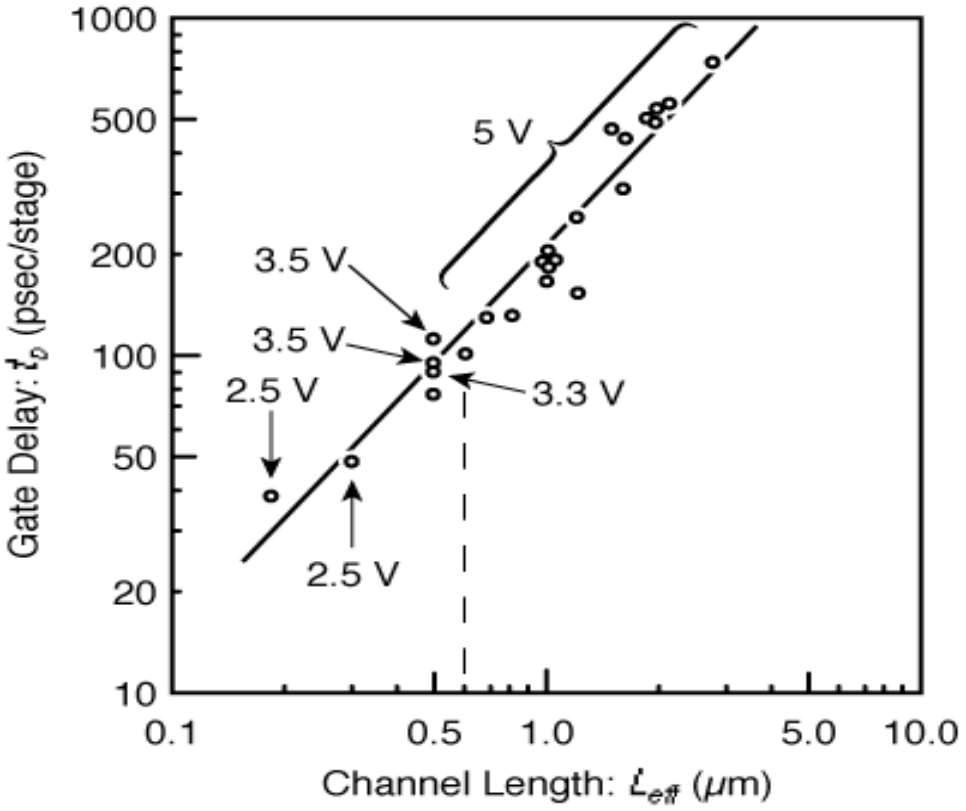
Number of components per chip



Propagation Delay Scaling



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Technology Scaling Models

- **Full Scaling (Constant Electrical Field)**

  ideal model — dimensions and voltage scale together by the same factor *S*

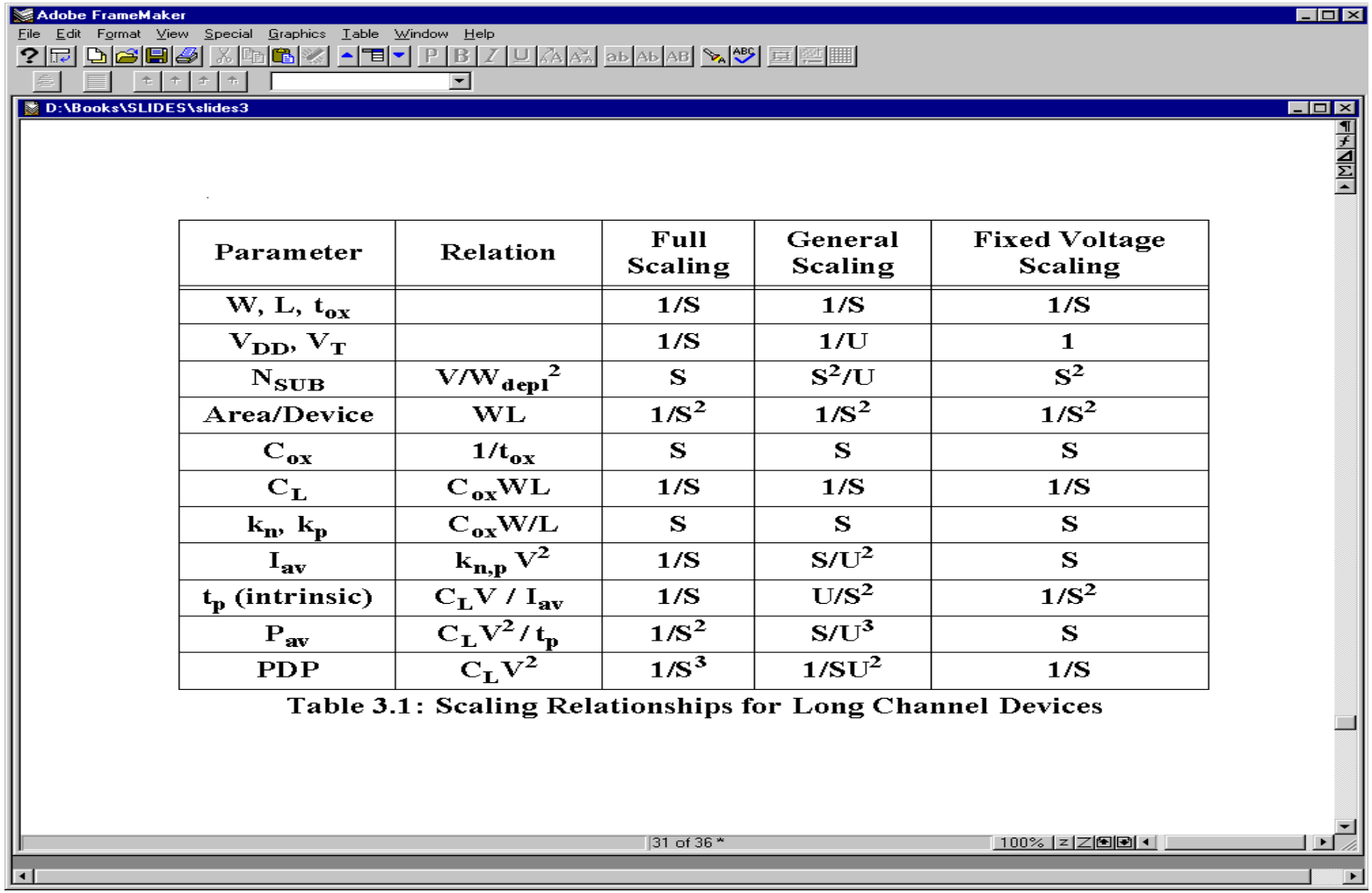
- **Fixed Voltage Scaling**

  most common model until recently — only dimensions scale, voltages remain constant

- **General Scaling**

  most realistic for todays situation — voltages and dimensions scale with different factors

Scaling Relationships for Long Channel Devices



Parameter	Relation	Full Scaling	General Scaling	Fixed Voltage Scaling
W, L, t_{ox}		1/S	1/S	1/S
V_{DD}, V_T		1/S	1/U	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
Area/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_L	$C_{ox}WL$	1/S	1/S	1/S
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{av}	$k_{n,p} V^2$	1/S	S/U^2	S
t_p (intrinsic)	$C_L V / I_{av}$	1/S	U/S^2	$1/S^2$
P_{av}	$C_L V^2 / t_p$	$1/S^2$	S/U^3	S
PDP	$C_L V^2$	$1/S^3$	$1/SU^2$	1/S

Table 3.1: Scaling Relationships for Long Channel Devices

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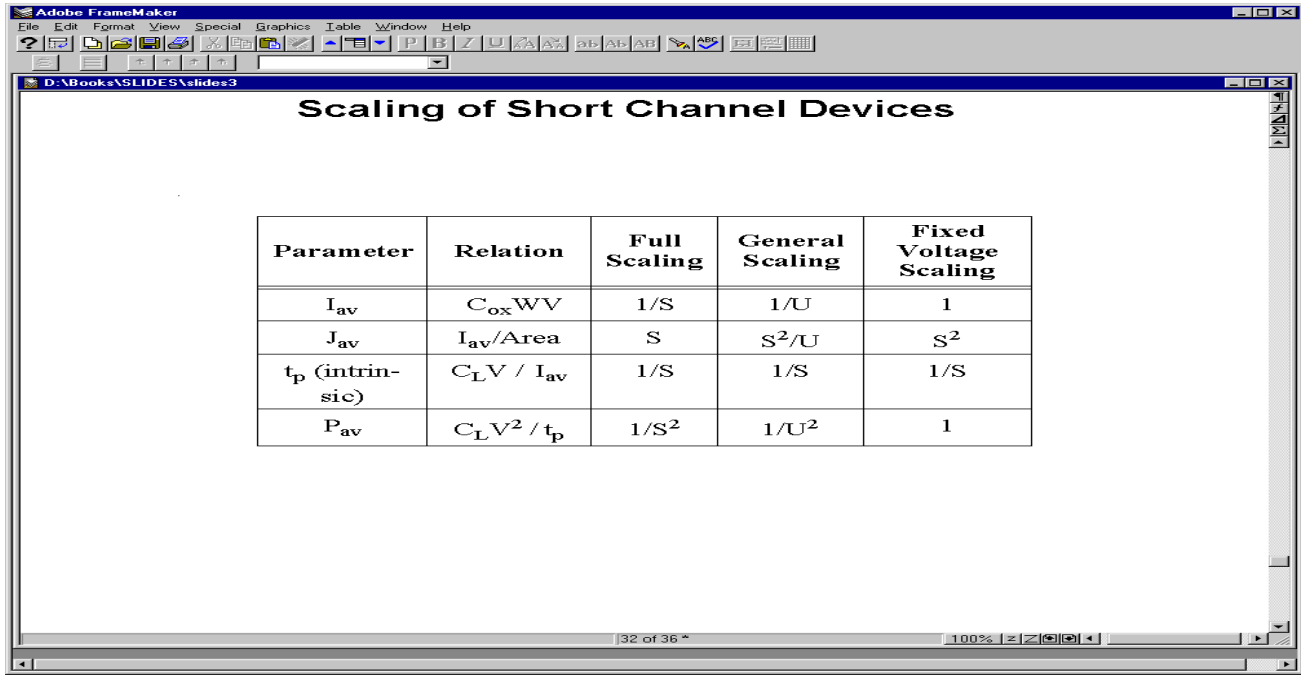
Scaling of Short Channel Devices



Parameter	Relation	Full Scaling	General Scaling	Fixed Voltage Scaling
I_{av}	$C_{ox}WV$	1/S	1/U	1
J_{av}	I_{av}/Area	S	S^2/U	S^2
t_p (intrin-sic)	C_LV / I_{av}	1/S	1/S	1/S
P_{av}	C_LV^2 / t_p	$1/S^2$	$1/U^2$	1

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