Fault models

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Fault Modeling

- Fault modeling is the translation of physical defects into a **mathematical construct** that can be operated upon **algorithmically and understood** by a **software simulator** for the purposes of providing a **metric for quality measurement**.

- The most common fault models supported in **modern VLSI and core-based digital design** are:

    - *Single Stuck-at DC Model*
    - *Transition-Delay and Path-Delay AC Models*
    - *Pseudo-Stuck-at and Toggle Current Measurement Models*

Open Circuit Fault

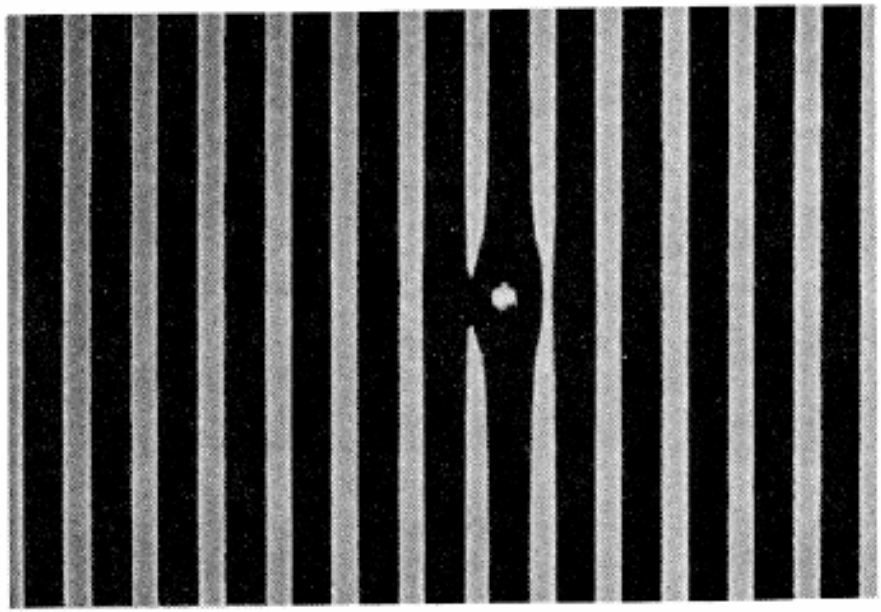


Figure 1: Example of a break in a metal line.

Reference: W. Maly, "Realistic Fault Modeling for VLSI Testing", Proceedings of the 24th ACM/IEEE Design Automation Conference, 1987, Miami Beach, Florida, Pages: 173-180

Bridging Defects

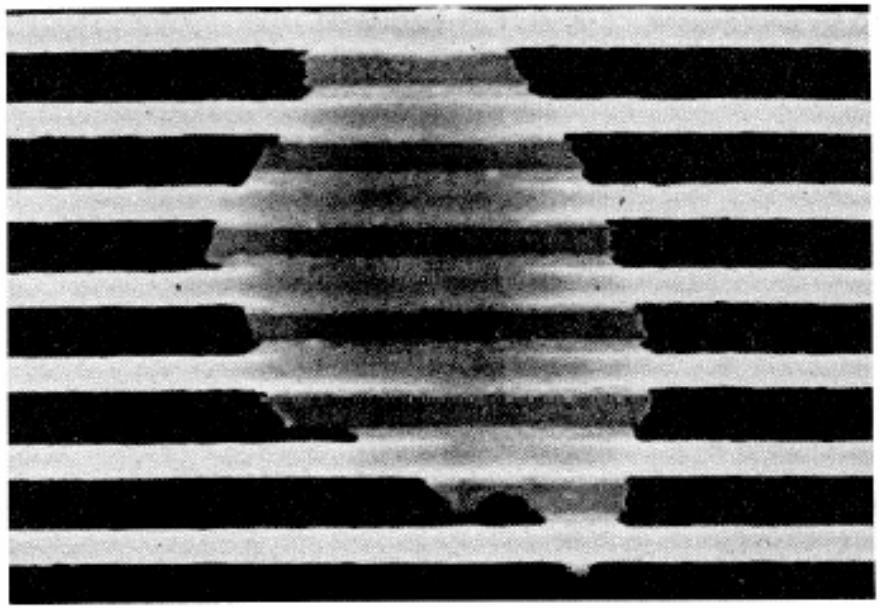


Figure 3: Example of a short of 7 metal lines caused by unexposed photo resist.

Reference: W. Maly, "Realistic Fault Modeling for VLSI Testing", Proceedings of the 24th ACM/IEEE Design Automation Conference, 1987, Miami Beach, Florida, Pages: 173-180

Latent Defects

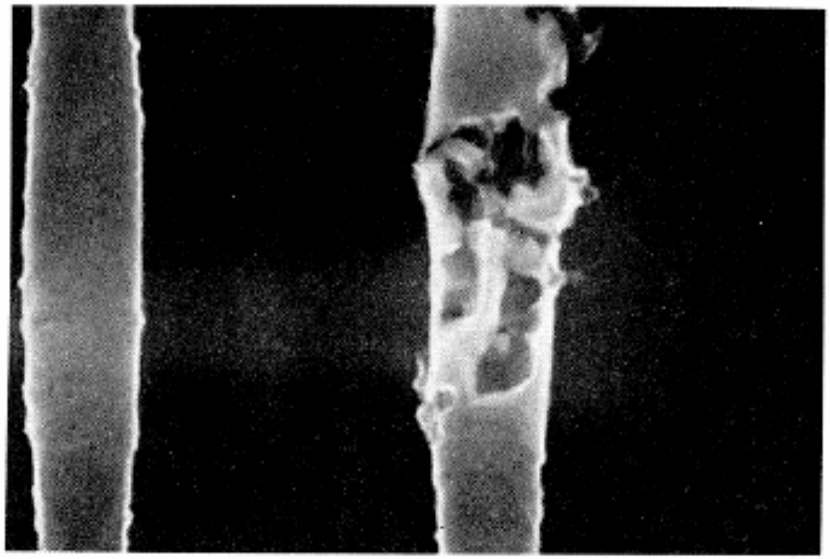
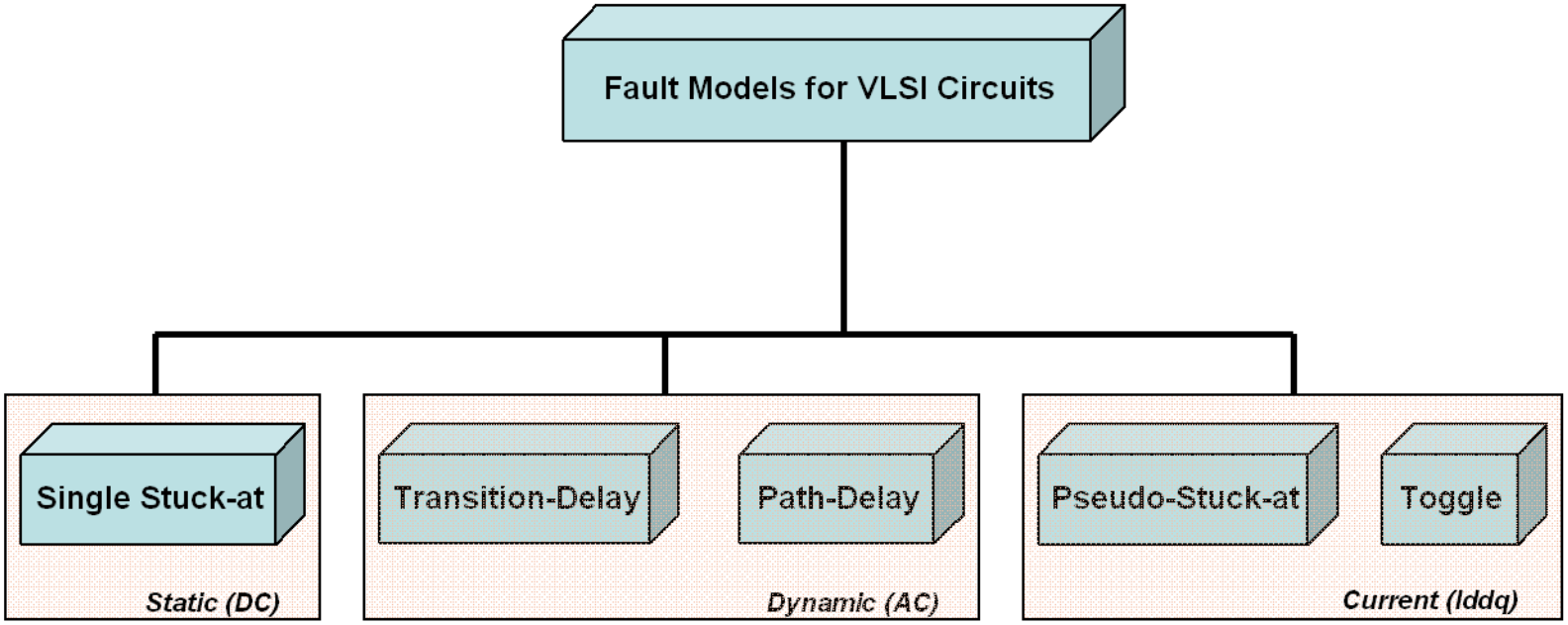


Figure 6: Example of metal line corrosion that eventually may result in breaks.

Reference: W. Maly, "Realistic Fault Modeling for VLSI Testing", Proceedings of the 24th ACM/IEEE Design Automation Conference, 1987, Miami Beach, Florida, Pages: 173-180

Fault Modeling



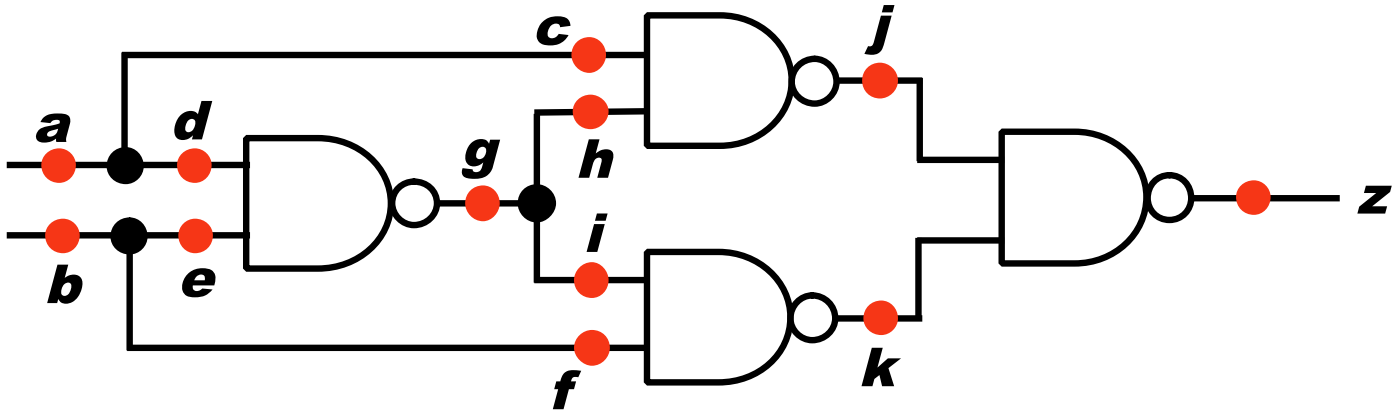
Single Stuck-at Fault

- Stuck-at Fault is a **DC (static) approximation** whereby all failures are represented as an individual gate-level pin or wire net connection that acts as if it were **shorted to Vdd or Vss**.
- This is a "**single-fault assumption**".
- This model is applied regardless of **frequency** or **time domain** considerations.
- This is the **most popular**, **industry-default** method.

Single Stuck-at Fault

- Three properties define a single stuck-at fault
  - *Only one line is faulty*
  - *The faulty line is permanently set to 0 or 1*
  - *The fault can be at an input or output of a gate*

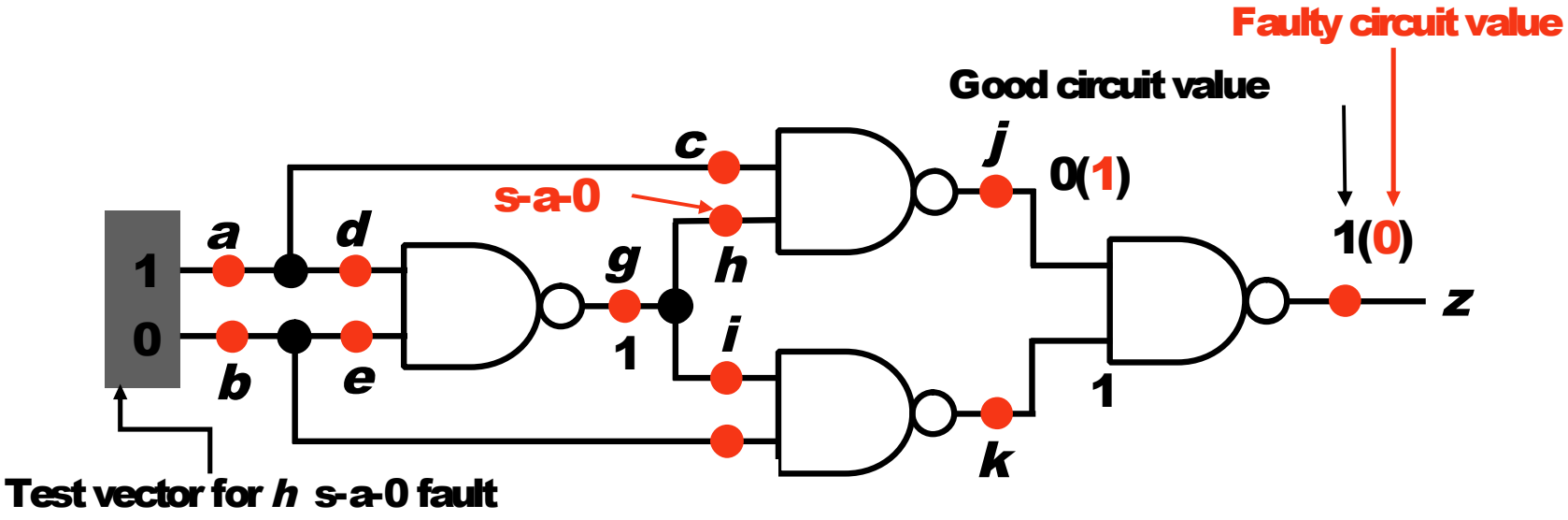
- Example: XOR circuit has **12** fault sites (●) and **24** single stuck-at faults



Single Stuck-at Fault

- Three properties define a single stuck-at fault
  - *Only one line is faulty at a time*
  - *The faulty line is permanently set to 0 or 1*
  - *The fault can be at an input or output of a gate*

- Example: XOR circuit has **12** fault sites (●) and **24** single stuck-at faults



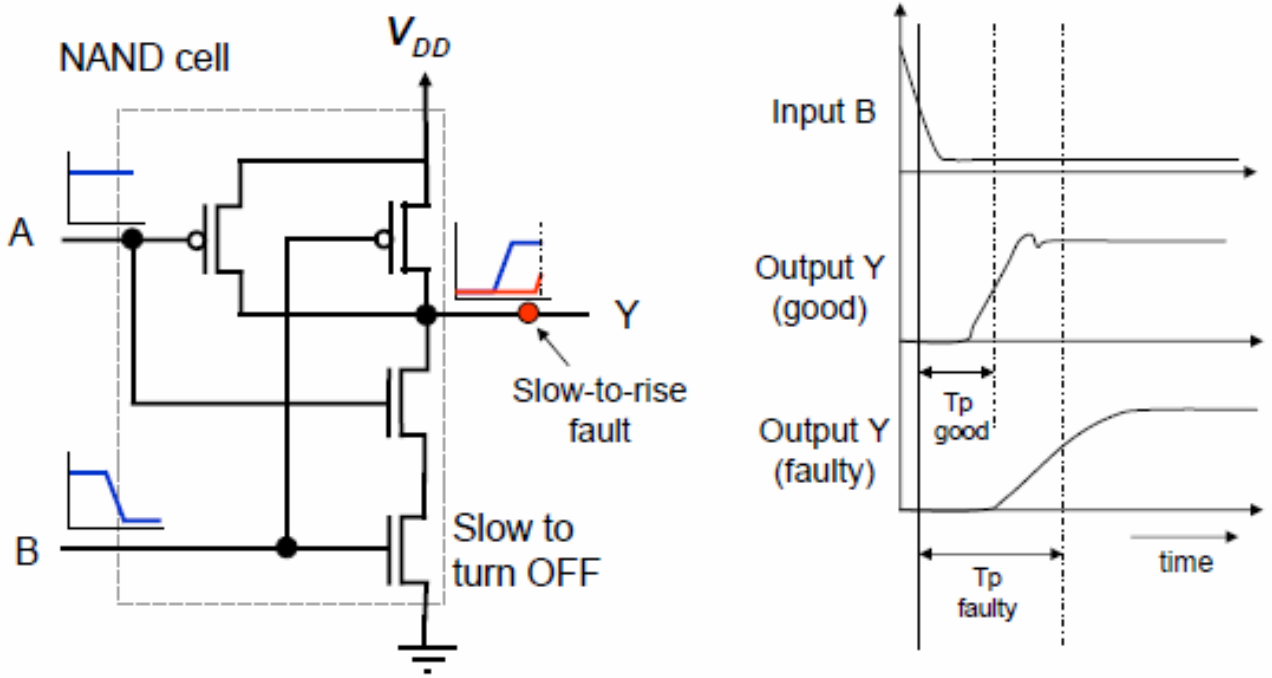
Transition-Delay Fault Model

- The application of the Transition-Delay Fault is **identical to the Stuck-at DC gate-level model**, **except** that the "**stuck-at-0**" and "**stuck-at-1**" values are now termed "**zero-to-one**" and "**one-to-zero**" transitions.

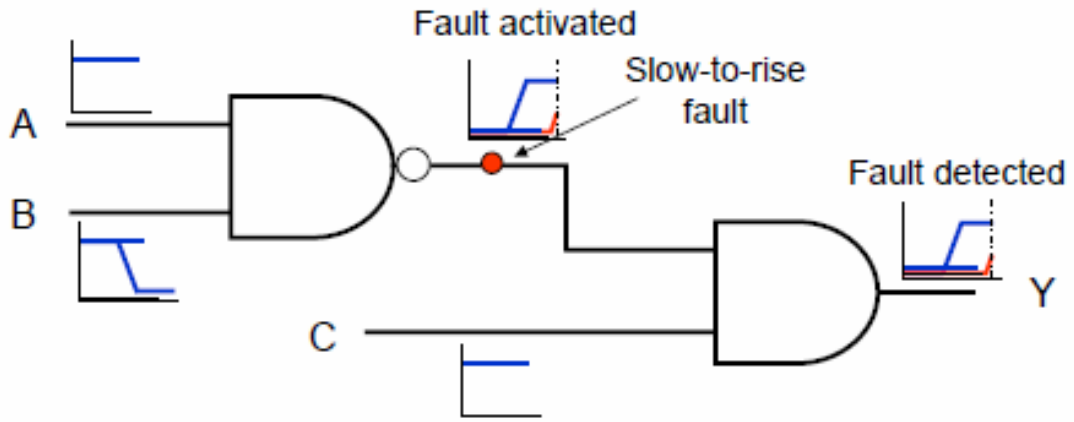
- It can be viewed as a **modified version of the Single Stuck-at DC Model** to allow it to be used to **assess the time domain**:
  - *the extra step is to force the gate-output to the expected fail value at some time period prior to the observation event, and then apply a transition and conduct the observation or sample event at a defined period of time.*

- This is the **simplest timing fault model**, also known as "**Gate-Delay Fault Model**", since the delay can be related directly to a gate in the modeling sense.

Transition-Delay Fault Model



Transition-Delay Fault Model



Path-Delay Fault Model

- This model is **similar** to the Transition Delay Model, but instead of a **single gate** pin or a wire net connection being targeted, an **entire path** made of multiple gate pins and wire net connections is the target of the fault model.

- This model can be viewed as the **sum of combinational gate transition delays along an identified circuit path**.

Pseudo-Stuck-at Fault Model

- Pseudo-Stuck-at Fault is also largely based on the Stuck-at fault model (**except for the observation event**).
- Pseudo-Stuck-at Fault is based on **current measurement**.
- Pseudo-Stuck-at Fault modeling is to only drive the fault effect to the **output of a gate** and then, conduct the observation event by performing a **current measurement** of the supply side (it may be measured from the return side of the power supply).

Toggle Fault Model

- Toggle Fault is also based on **current measurement**.
- Toggle Fault aims at being able to **place every node** to a logic “1” or logic “0” and then **measure the DC current consumption**.
- This is a very **simple and powerful** method.

Explicit and Implicit fault models

Logical fault model can be explicit or implicit.

- **Explicit fault model** – defines a fault universe in which each fault is individually identified
- **Implicit fault model** – defines a fault universe by collectively identifying the faults of interest

- **Fault universe** – set of all possible faults in the design.

Structural and Functional faults

- **Structural faults** – faults defined in conjunction with a structural model
  - Modify the interconnections among the components
- **Functional faults** – faults defined in conjunction with a functional model
  - Modify the truth table of the component or the model in which it is represented

Short and Open Structural faults

- Assumes that the faults are due to interconnects only and the components are fault free.
- Typical structural faults
  - Short – by connecting unnecessary nodes
  - Open – by breaking of a connection

For example shorting the inputs of a component or breaking the connection to supply or ground.

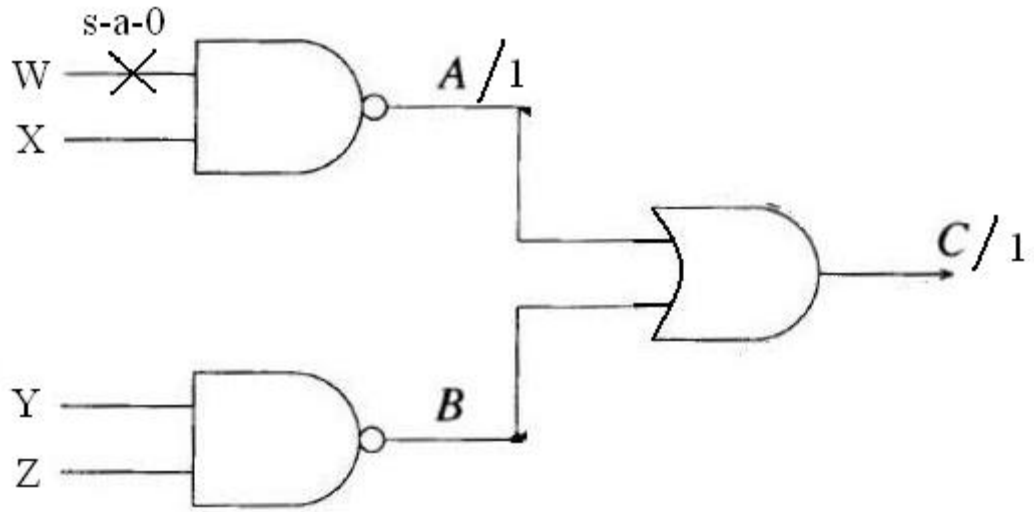
Stuck-at-faults

- A short between signal and supply or ground will make the node remain at a fixed voltage.
- The node is said to be stuck-at-voltage (v)
- V € {0,1}
- Represented by s-a-v.

- Any line X s-a-v € {0,1} represent following physical faults
  - X open
  - X shorted to ground or supply
  - Any internal fault in the component driving X that keeps its value at ‘v’.

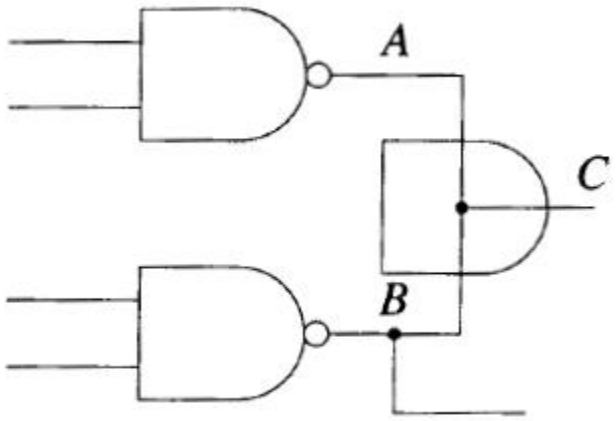
Example

- Suppose the line ‘W’ is unfortunately shorted to ground
- It can be represented as s-a-0
- One can observe the error at the output.

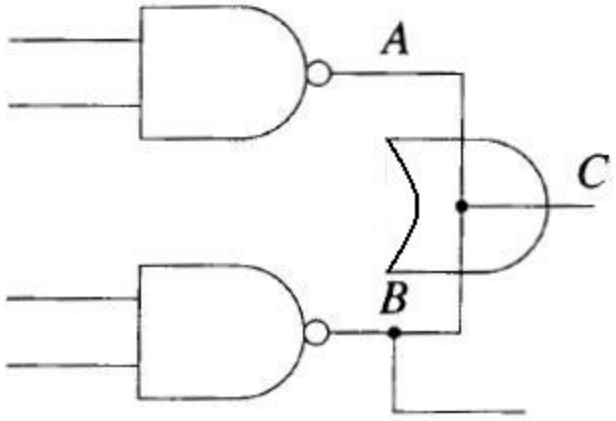


Bridging fault

- During fabrication, some unconnected signal lines may be shorted which can be represented by this fault.
- It is a logical fault representing a short between two signal lines which creates a new logic function.
- Depending on the function created, there are two types of bridging faults
  - AND bridging faults
  - OR bridging faults



AND bridging fault



OR bridging fault

Transistor Faults

- MOS transistor can be considered as an ideal switch.
- Two types of transistor faults
  - Stuck-open
  - Stuck-short

- **Stuck-open:** A transistor is permanently stuck in the open state.

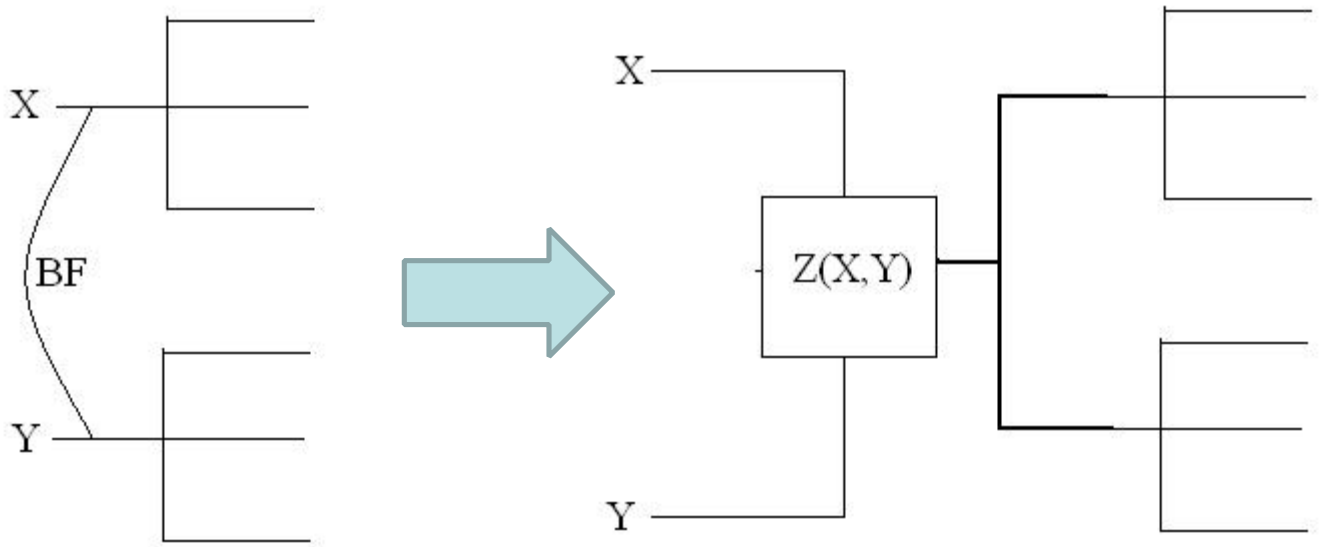
  Stuck-short: A transistor is permanently shorted irrespective of its gate voltage.

Bridging Fault

- One of the manufacturing defects that occur frequently in chips and on boards is **shortage of two unconnected signals**.
- The two signal lines become equipotential because of short.
- **Bridging fault** is a logical fault representing a short between two normally unconnected signal lines which creates a new logic function.

Representation of a Bridging fault

- Assume Bridging fault between signals X and Y.
- It is denoted by (X.Y) and the function generated by it as Z(X,Y)



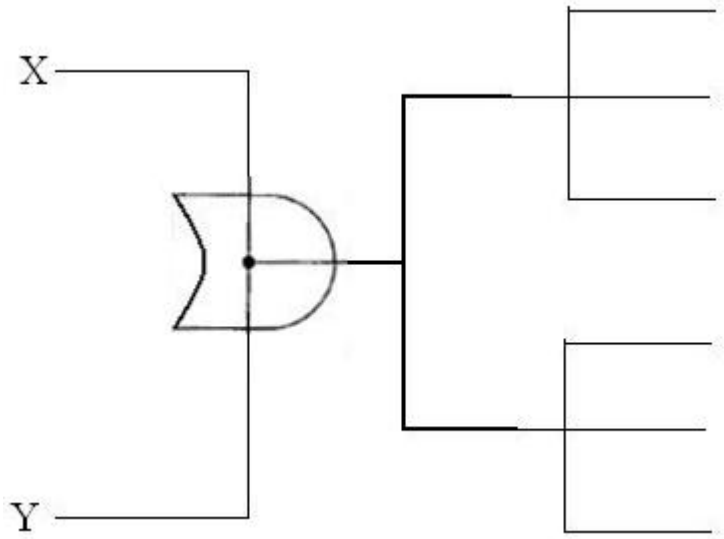
Bridging fault model

Function

- If both the shorted signal lines have the same value, then the response of the function will also be the same.
- If the signal lines have different values, either of the values will be driven, so output of the function can be
  - OR of the two signals – **OR bridging fault**, or
  - AND of the two signals – **AND bridging fault**

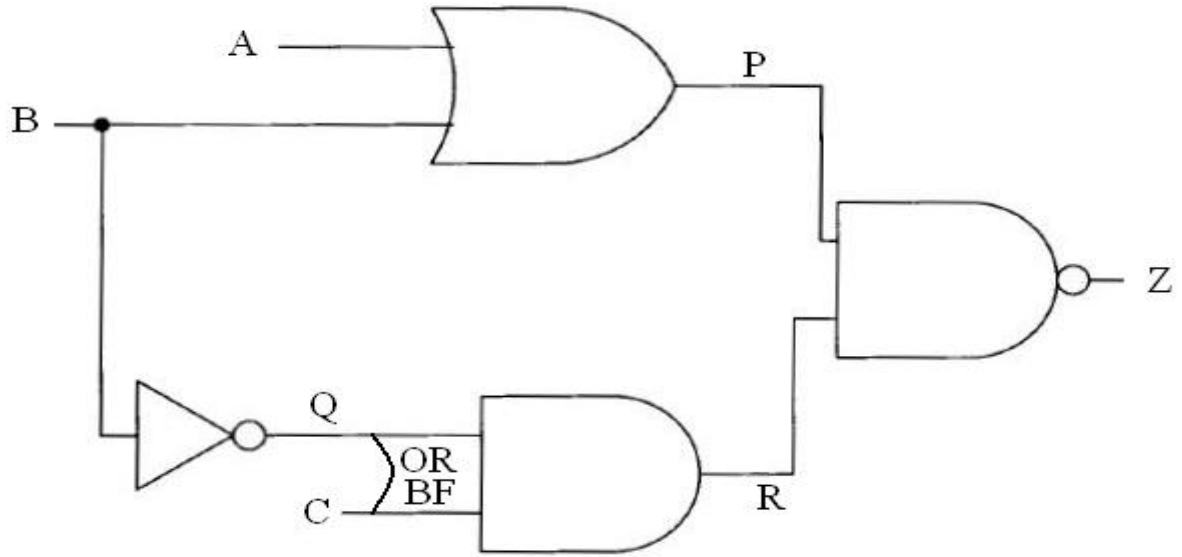
OR bridging fault

- If the function generated is OR, then we say, a OR bridging fault between the signal lines.
- OR(X,Y) will be driven to the next signal lines.



Example

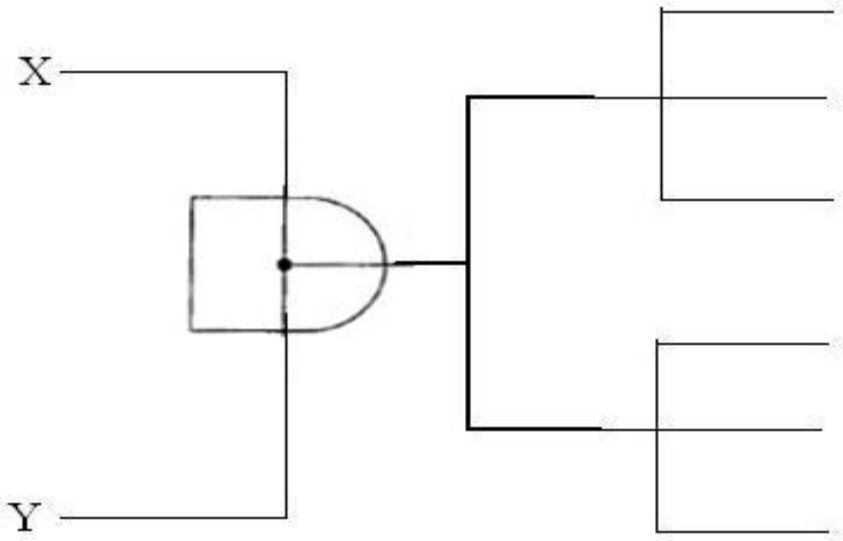
- Assume OR bridging fault between C & Q.



- Z = {(A+B).(B'.C)}'
- Z_F = {(A+B).[(B'+C).(B'+C)]}' = {(A+B).(B'+C)}'
- Test vector 100 can detect this fault and there can be many such test vectors
- Test vectors like 101, 110 cannot detect this fault

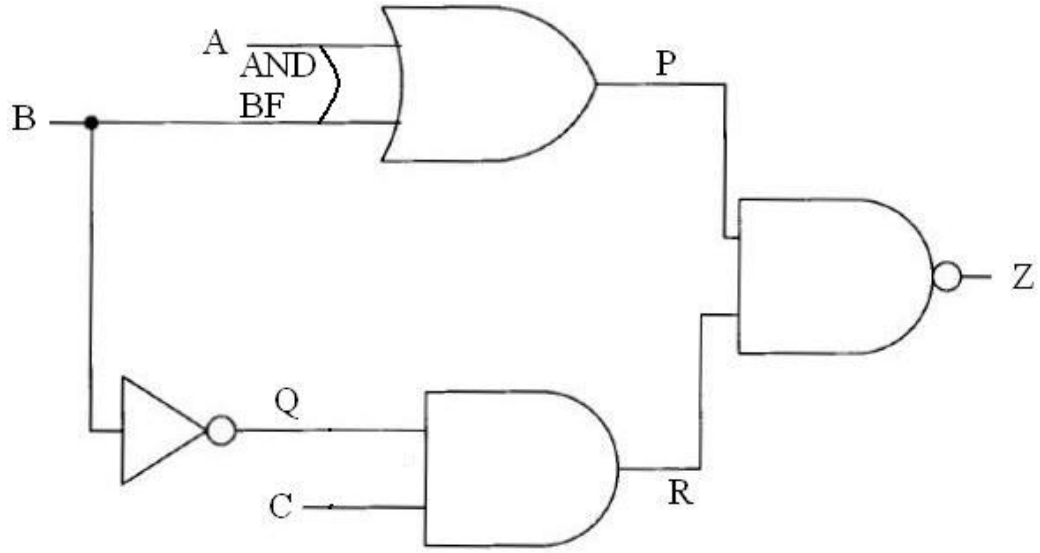
AND bridging fault

- If the function generated is AND, then we say, a AND bridging fault between the signal lines.
- AND(X,Y) will be driven to the next signal lines.



Example

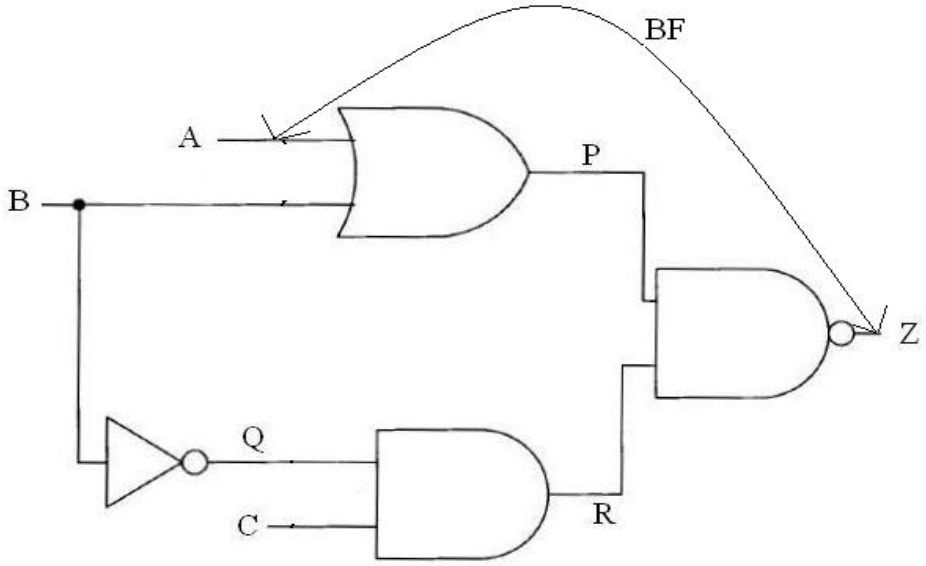
- Assume AND bridging fault between signal lines A & B.



- Z = {(A+B).(B'.C)}'
- Z_F = {[(A.B)+(A.B)].(B'.C)}' = {(A.B).(B'.C)}'
- Test vector 101 can detect this fault.
- Check for vectors 110, 010, 001

Feedback bridging faults

- A bridging fault that creates a feedback loop is referred to as feedback bridging fault (FBF).
- A FBF converts a combinational circuit to sequential circuit.



Example of FBF

Questions?