DESIGN FOR TESTABILITY
Assignment-1

1. Consider the circuit shown in figure 1.

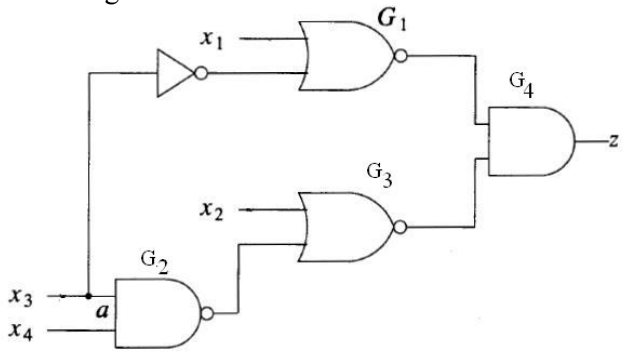


Figure 1

How many possible single stuck at faults does this circuit have? How many possible multiple stuck at faults does this circuit have?

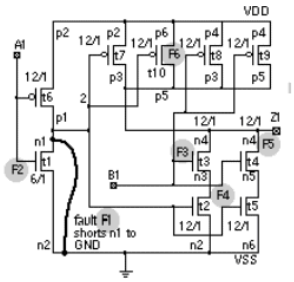
2. Consider again the circuit shown in figure 1. Determine the output function of the given circuit with the following faults:
a. OR bridge between inputs of gate G3
b. AND bridge between inputs of gate G1

3. Show by an example how a combinational logic circuit gets transformed into a sequential logic circuit in the presence of a bridging fault.

4. Generate a minimum set of test vectors to completely test an n-input NAND gate under the single stuck at fault model. How many test vectors are needed?

5. Generate a minimum set of test vectors to detect all single stuck at faults for a cascade of (n-1) exclusive OR gates for an n bit parity checker where each exclusive OR gate is implemented by elementary logic gates (AND, OR, NAND, NOR, NOT). How many test vectors are needed?

6. Physical fault can happen in many ways like shorting of wire, shortening of source and drain of a transistor, shortening of wire with Vdd or ground. A physical fault is converted into logical fault since testing for a logical fault is much easier than testing for a physical fault. Consider the circuit shown in figure 2. So given below is a circuit with different physical fault; convert it into logical fault. Model Faults F1,F2,F4,F6 and F7 as logical fault(stuck-at-fault).



1. F1 translates to node n1 being stuck at 0.
2. F2 will probably result in node n1 remaining high.
3. F4 is a bridging fault. Can we model it as stuck at fault?
4. F6 is short-circuit of source and drain of transistor t10.
5. Fault F7due to electromigration the cell could no longer pull Z1 up to VDD

Figure 2

7. The Stuck-at fault model has been successfully used for testing large-scale integration (LSI) and medium-size integration (MSI). Because these model cover variety of physical fault. The stuck-at-model is independent of the technology used and is independent of the relative importance of the fault in terms of circuit behavior. Stuck-at-fault can covers up to 85% of the physical faults in a given circuit. In a circuit if a line is stuck-at fault then some test vector may detect the fault and some test vector may not detect that fault. in view of this, for the given circuit below in figure 3, suggest a test vector that will detect the fault and a test vector that will not detect a fault.

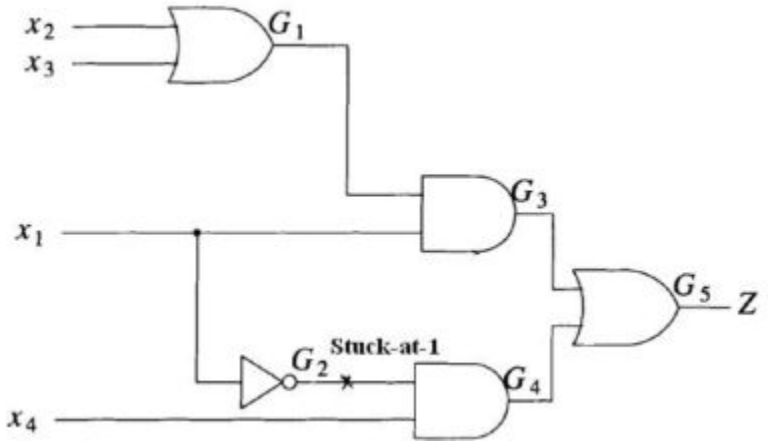


Figure 3

8. When two normally unconnected signal lines are shorted, either OR or AND bridging fault occurs between them. For the circuit shown below in figure 4, find the bridging faults that can be detected with the test vectors 1100, 0101, 0110, 0001.

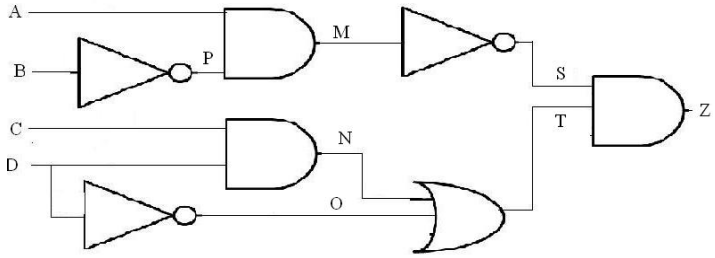


Figure 4

9. ALU is the basic execution unit of Microprocessor. Write an RTL code of an ALU whose description is given below. Simple processes are performed by the Arithmetic Logic Unit (ALU for short). The ALU is made up of devices called gates that receive one or more inputs and, based upon what function they are designed to perform, output a result. The ALU in our example performs one of seven functions:

a. Logical (NOT, AND, OR)
b. Shift operation (Left Shift, Right Shift)
c. Arithmetic operation (Add, Subtract)

The operation that is needed to perform depends on the control signal. The ALU takes two inputs, loaded from registers on the chip. Then the answer is stored back to a register.