

VLSI Architectures

ECE 465

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Course Content

- Introduction. Goals of VLSI Design: Optimization of Speed, Area, Power dissipation, cost and reliability. Review of VLSI design flow
- Algorithmic modeling of system
- Architectural design of VLSI circuits and systems : Resource utilization and time constraints
- Data-path subsystems: Adder and multiplier data-path architectures
- Array subsystems: Memory arrays and programmable gate arrays
- Logic level design and optimization
- Analog array architectures
- Low power and high speed analog and digital VLSI architectures
- Clock generators and clock routing for VLSI chips
- High speed interconnect design
- Digital Signal Processing using array architectures: Systolic array and Wave-front array
- Dynamically reconfigurable gate arrays
- Inexact computing: Probabilistic CMOS model based design architectures and probabilistic pruning



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The World's First Baby Computer



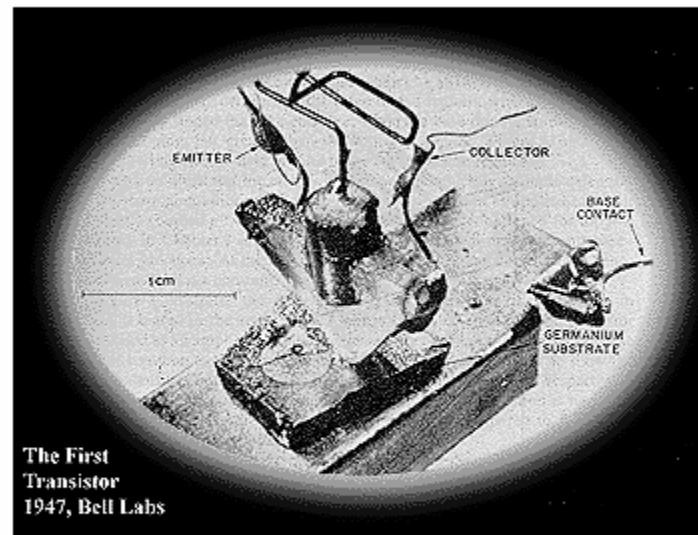
The world's first stored program computer, running for the first time on
June 21, 1948



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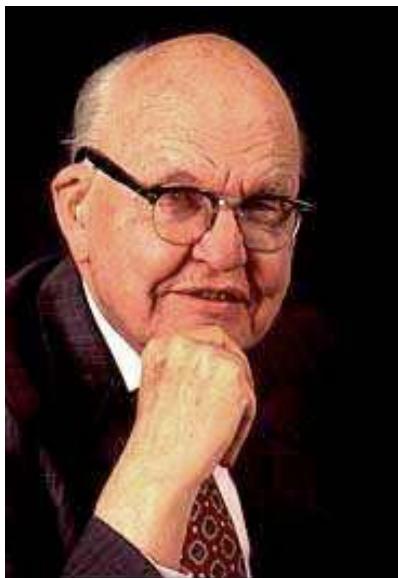
The First Transistor- Bell Labs (1947)



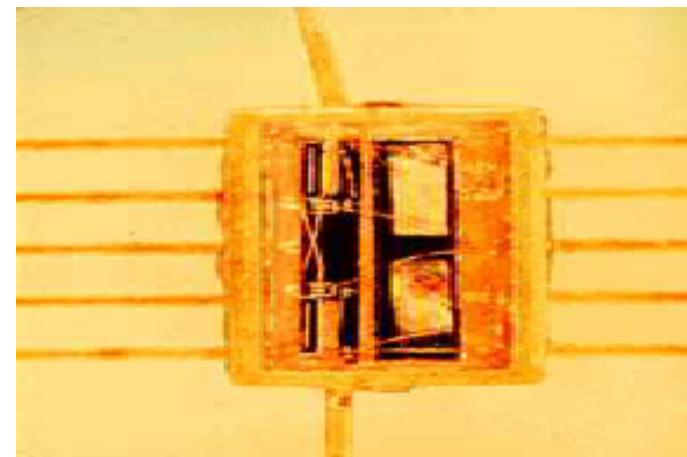
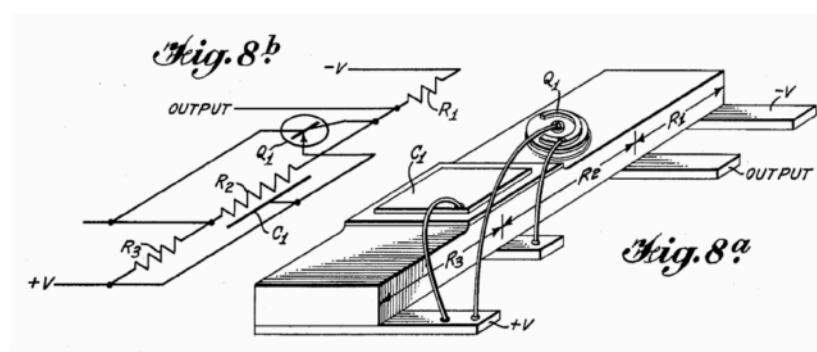
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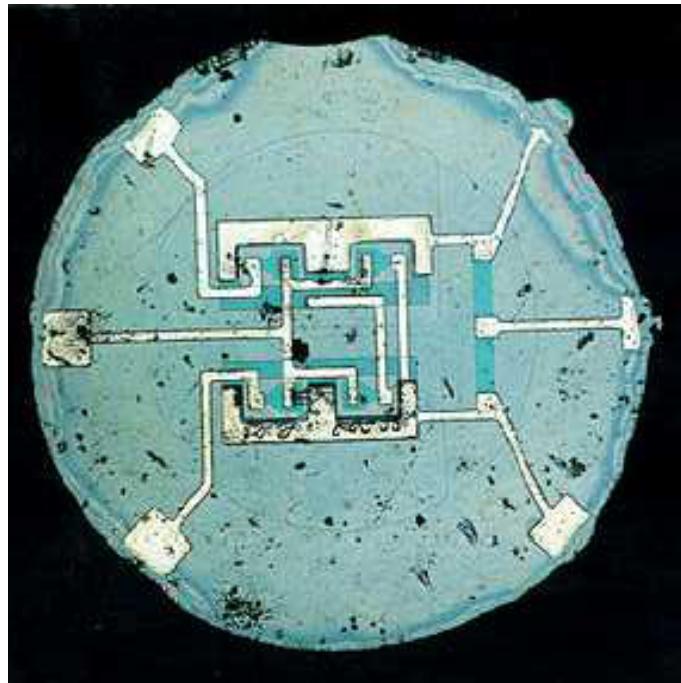
The First Integrated Circuit



- 1959: Jack Kilby, working at TI, dreams up the idea of a monolithic “integrated circuit”
 - Components connected by hand-soldered wires and isolated by “shaping”, PN-diodes used as resistors (U.S. Patent 3,138,743)



The first planar integrated circuit

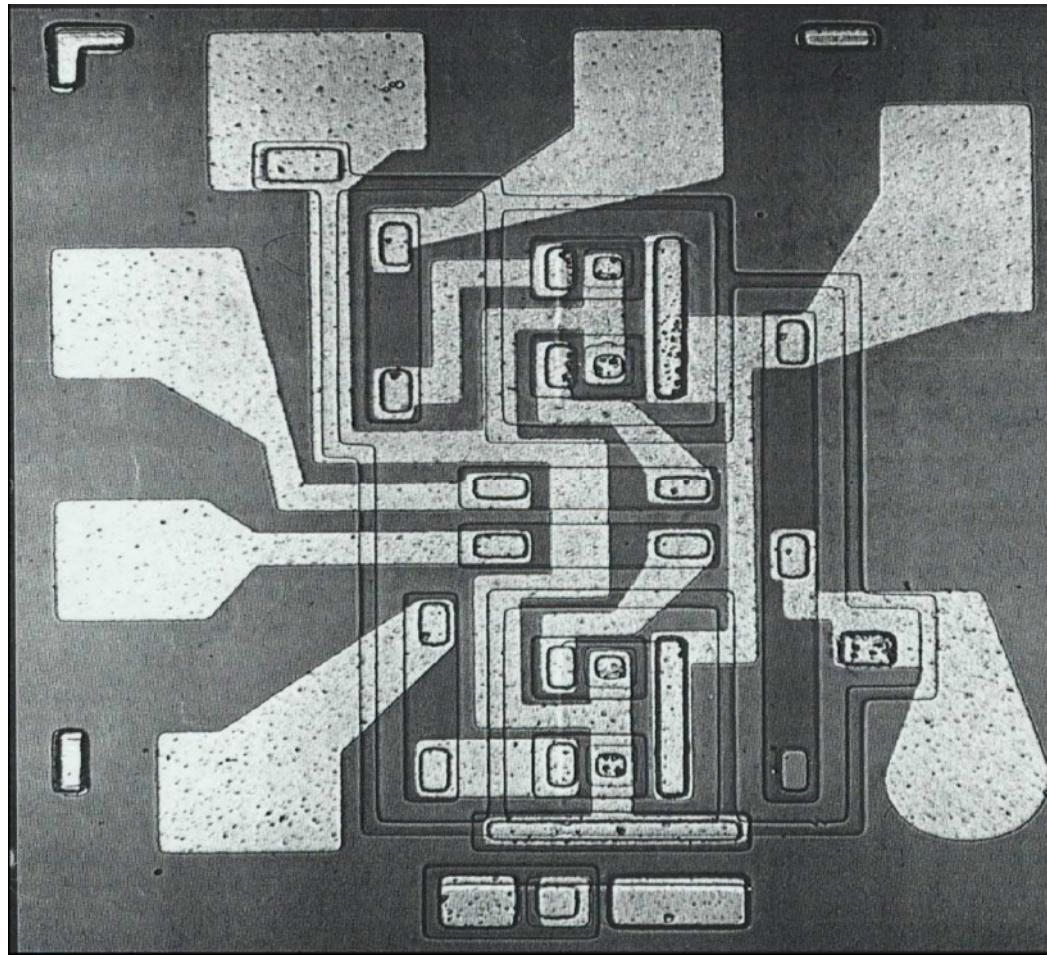


This device, developed by Robert Noyce in 1961, was the first commercially available integrated circuit (it was a Flip-Flop).

Courtesy:
Fairchild Semiconductor.



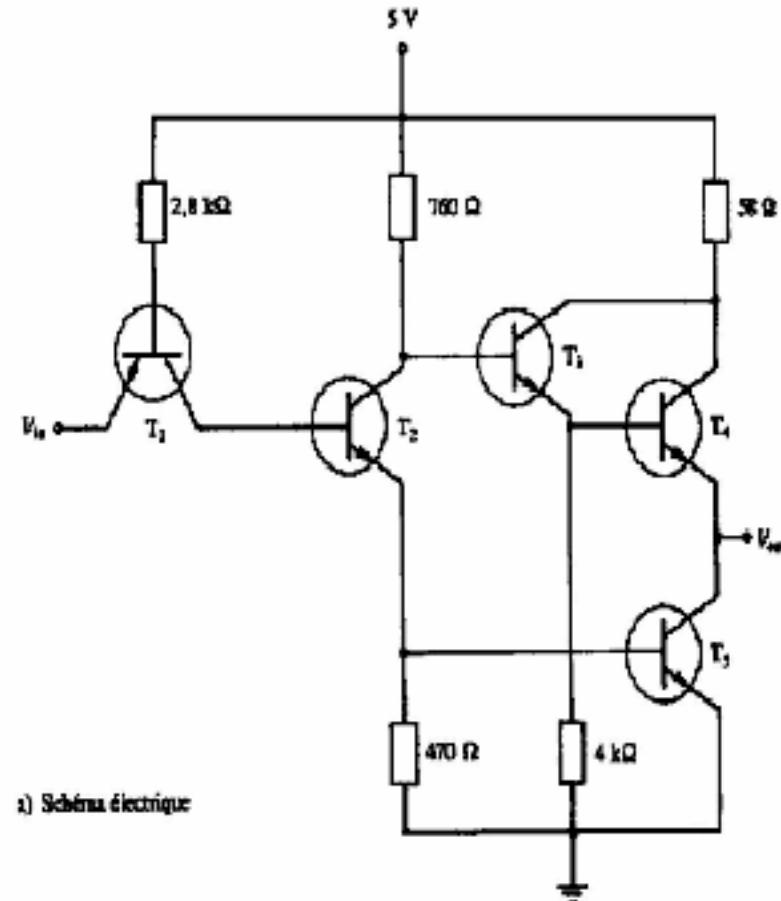
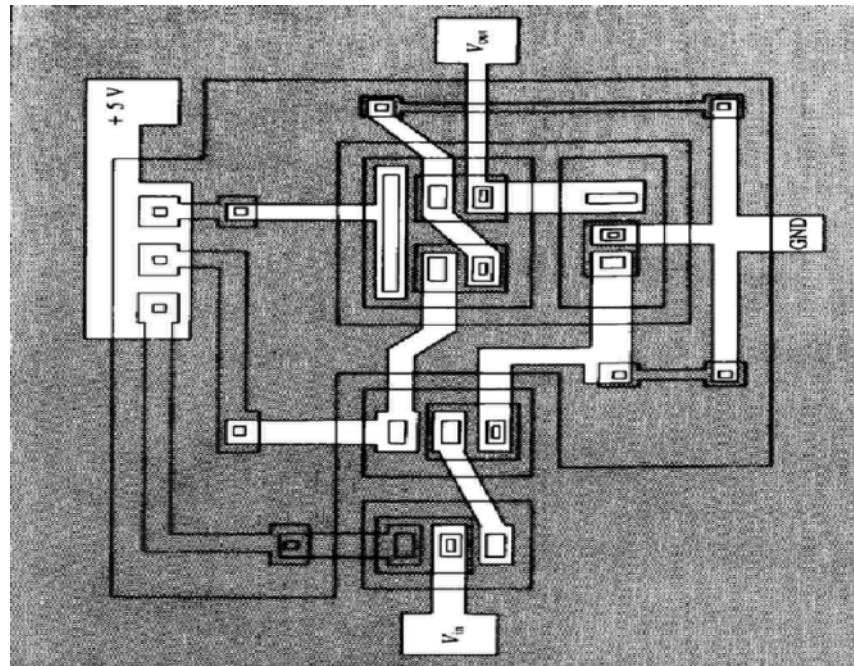
RTL Logic (1963)



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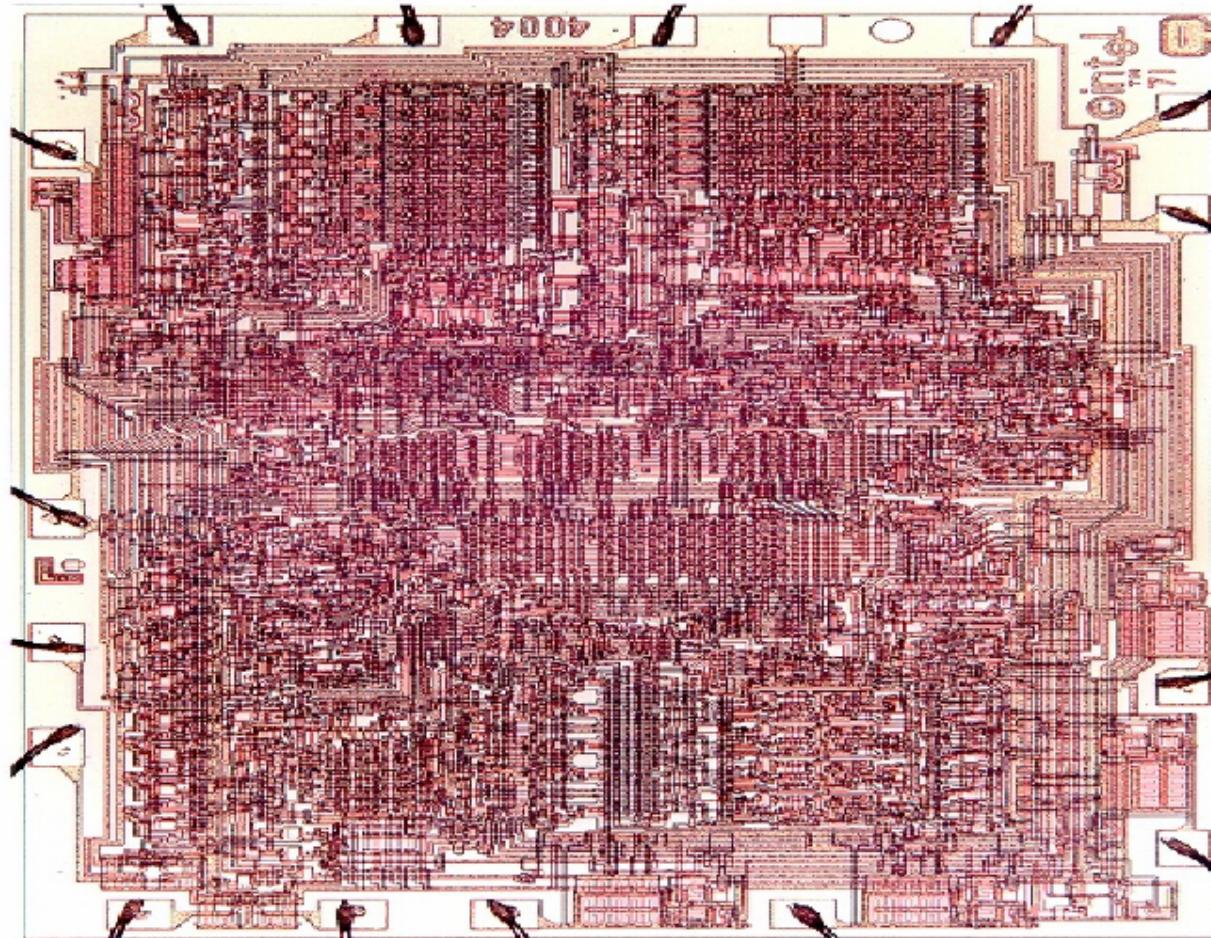
The TTL Inverter



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The Intel 4004 (1971)



Total no. of transistors=2300



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Ted Hoff, Bob Noyce, Gordon Moore



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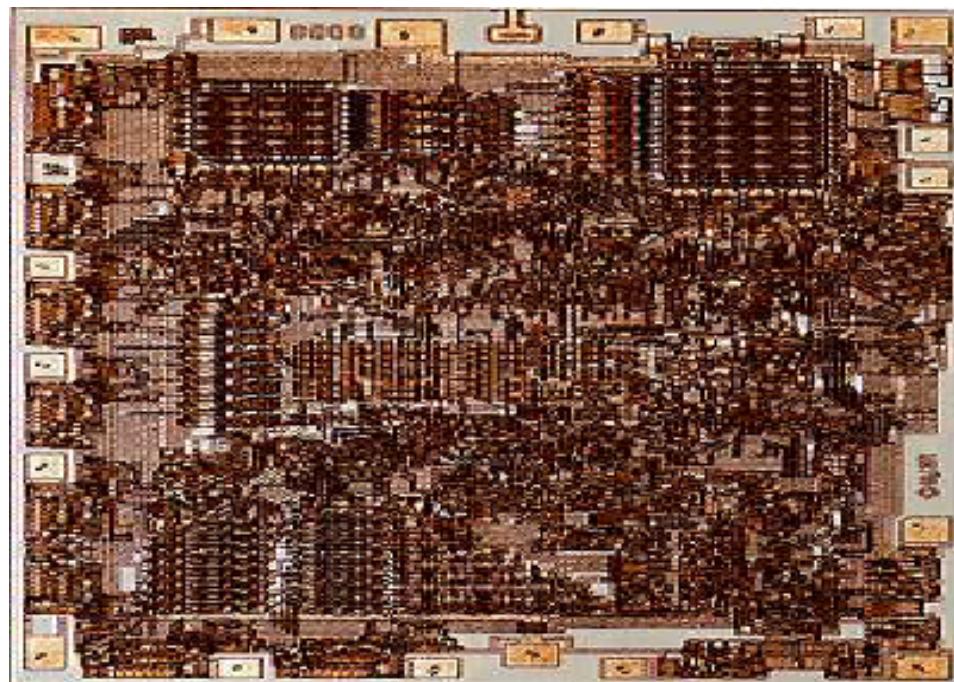
Moore's Law

The number of devices per chip increases exponentially.

It gets doubled in every two years and this trend will continue in the near future.

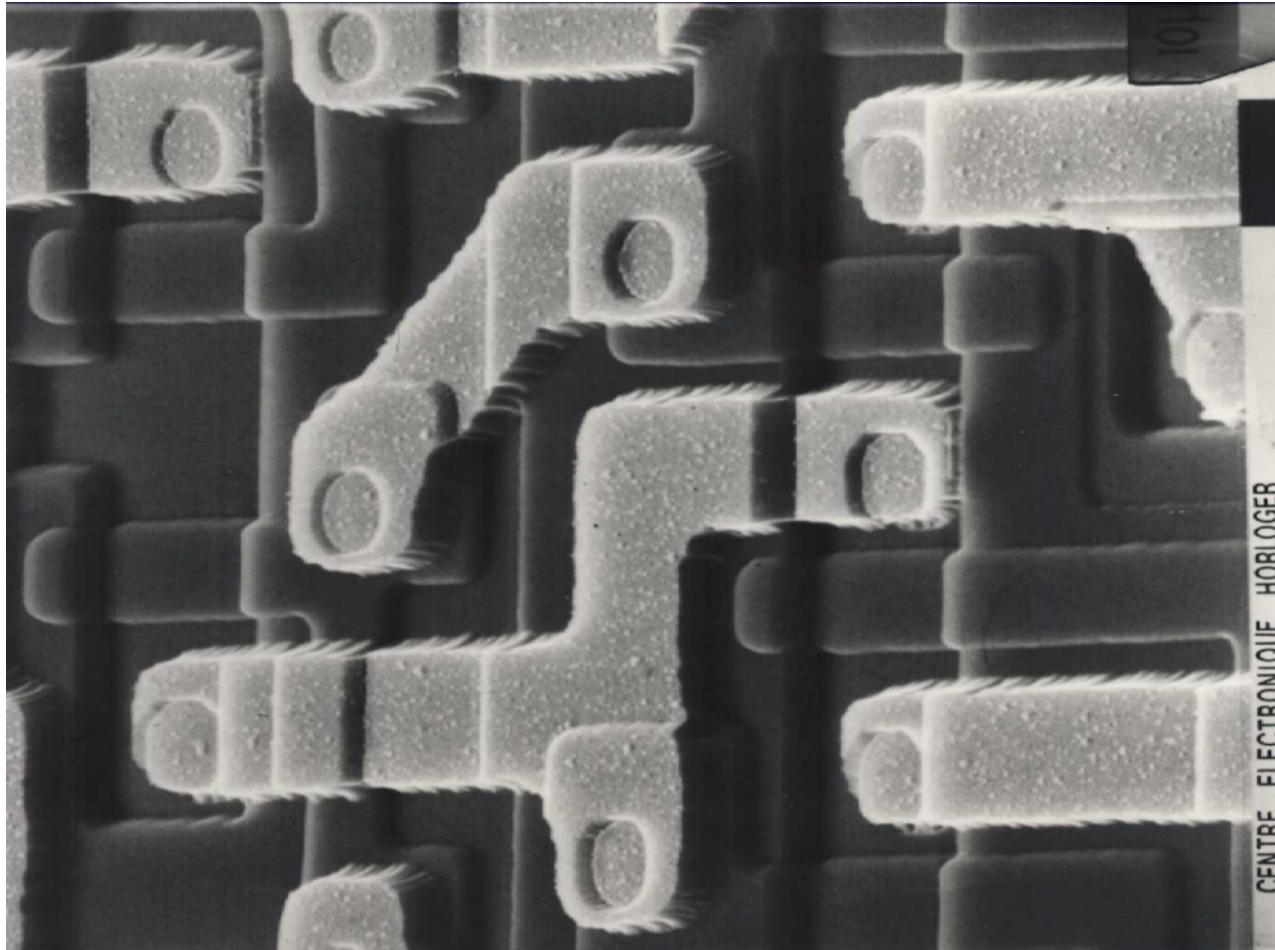


The Intel 8008 (1972)



Total no. of transistors=3500

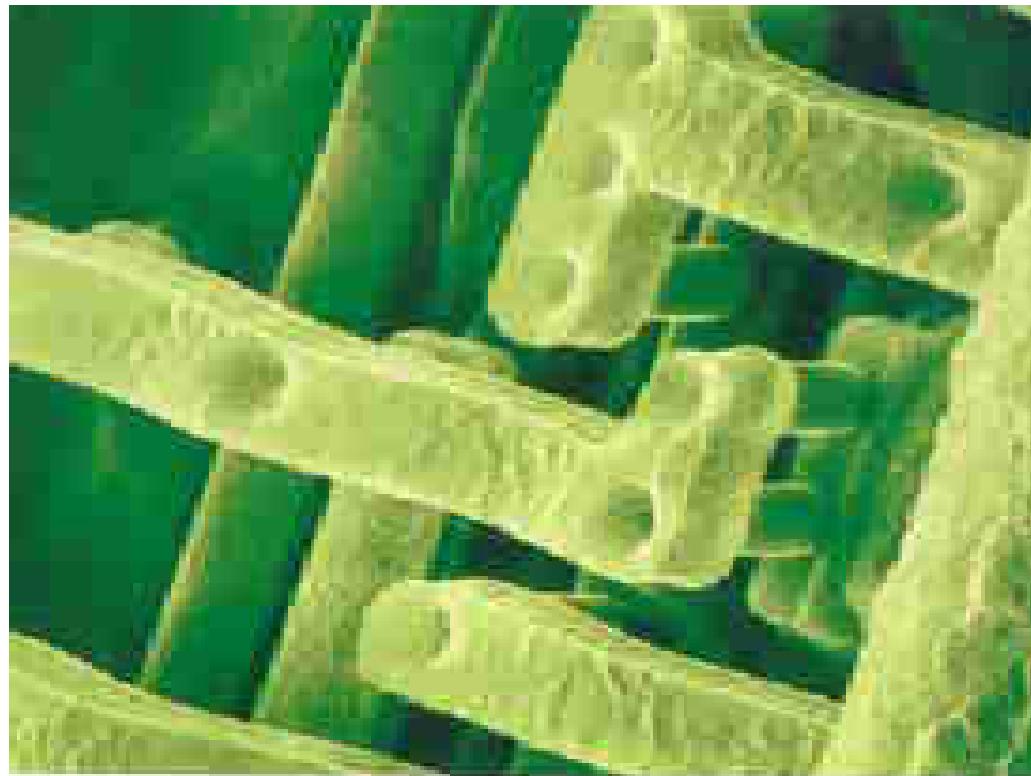
The CMOS Circuit (1972)



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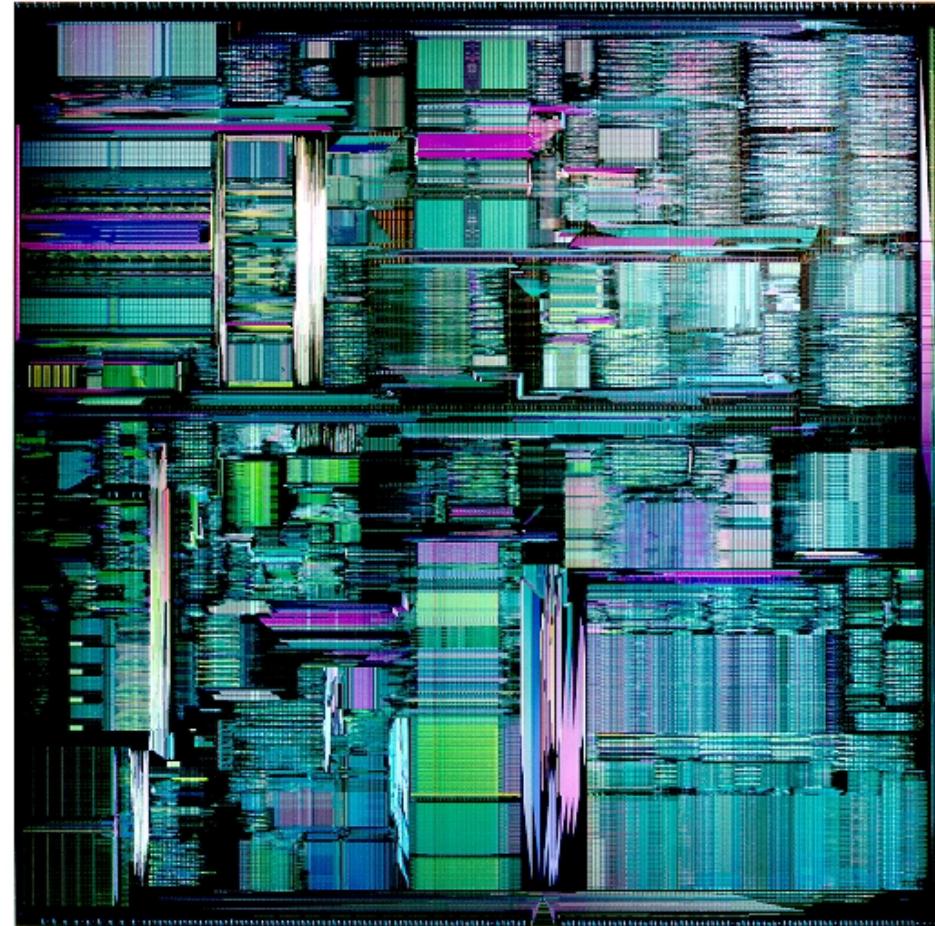
EPROM 4M



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The Intel Pentium Pro (1995)



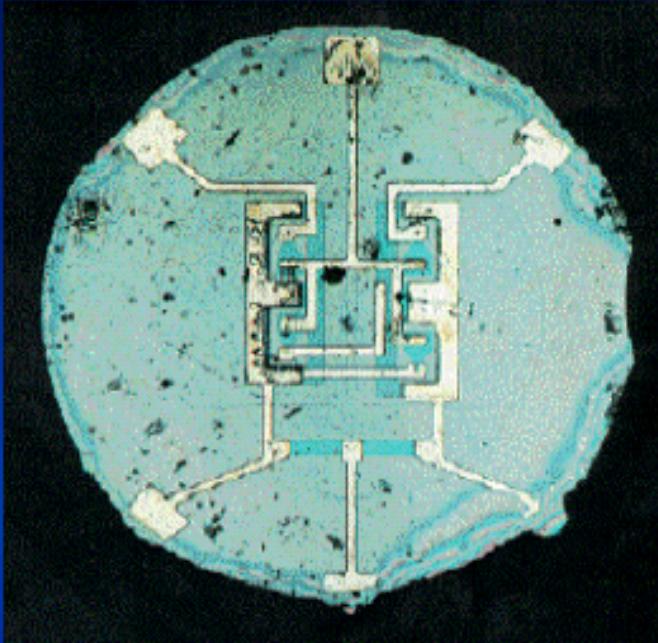
Total no. of transistors=5.5 million



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Four Decades of ICs



1961

First Planar Integrated Circuit
Two transistors

2001

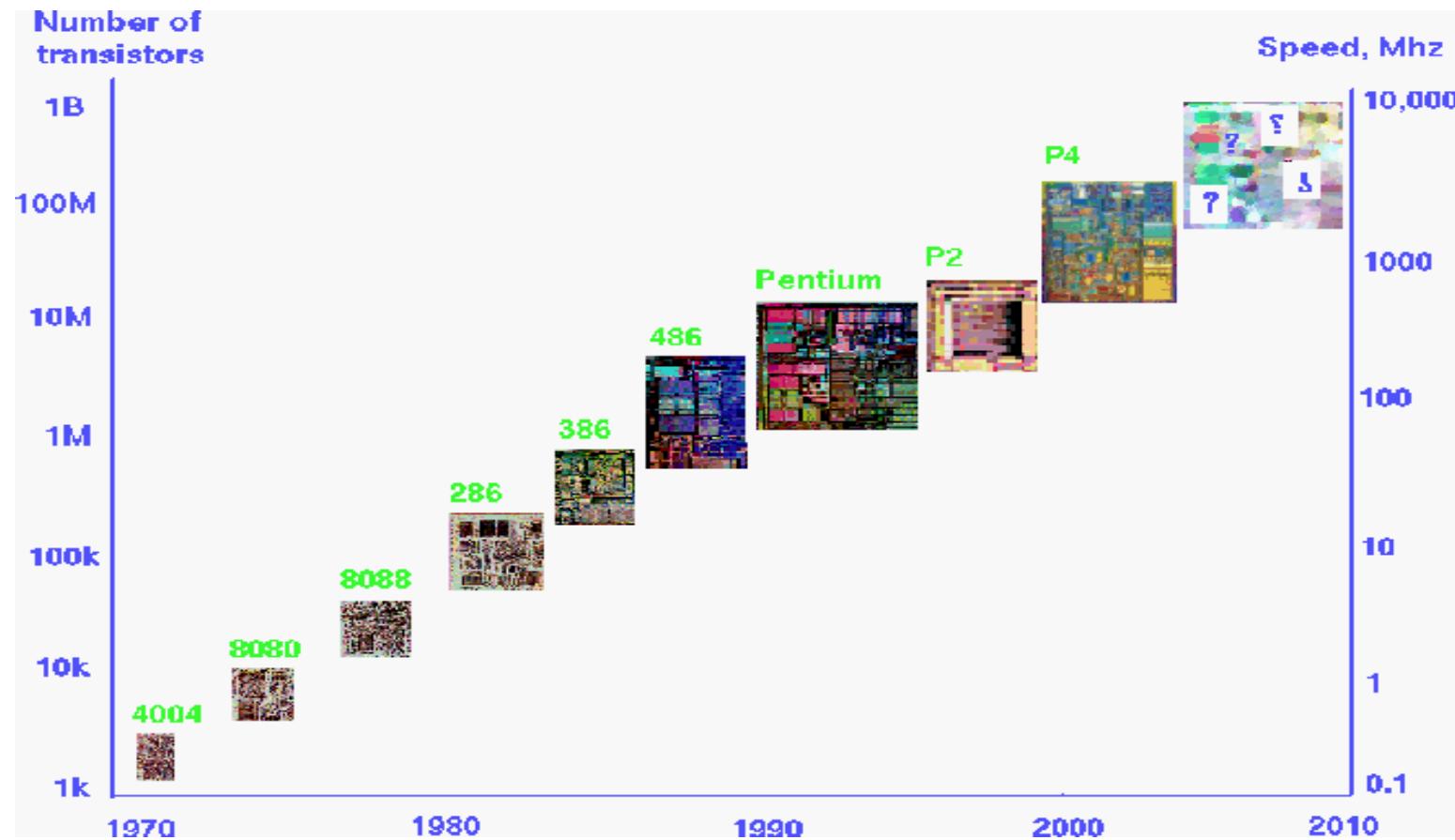
Pentium® 4 Processor
42 million transistors



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MOS Technology Trends



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ITRS (International Technology Roadmap)

Year	1997	1999	2002	2005	2008	2011	2014
Dense lines: Half pitch(μm)	0.25	0.18	0.13	0.10	0.07	0.05	0.0035
Shrink rate	-	0.72	0.72	0.77	0.70	0.7	0.71
Isolated lines: MPU gate(μm)	0.20	0.14	0.10	0.07	0.05	0.035	0.025
Shrink rate	-	0.70	0.71	0.70	0.71	0.70	0.70
DRAM @ introduction	256M	1G	4G	16G	64G	256G	1T
DRAM @ production	64M	256M	1G	4G	16G	64G	256G

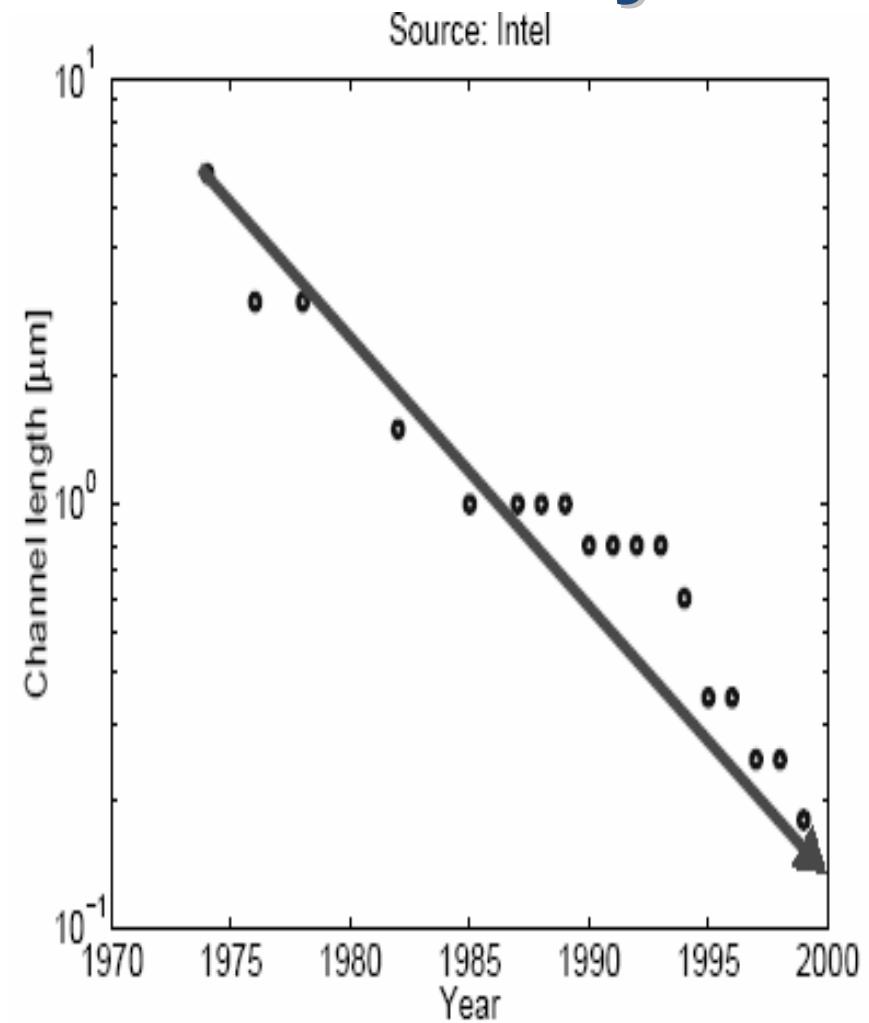


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Why miniaturization is necessary?

1. **Reduce gate delay.**
2. **Increase operating frequency.**
3. **Increase transistor density.**
4. **Reduce power dissipation.**



Why Miniaturization is Possible?

The functionality is not lost or reduced by downsizing!

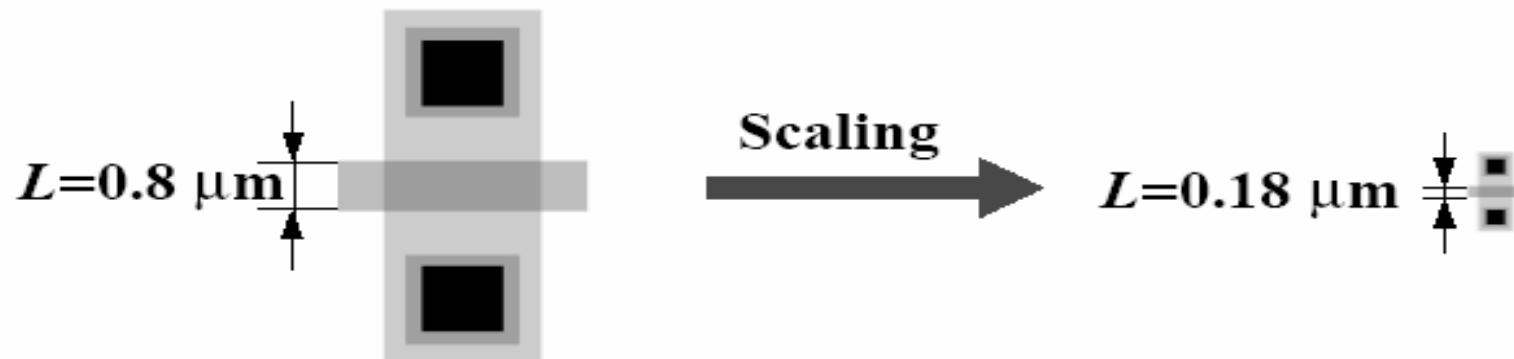
$$I = f(\text{Tech}) * (W/L) * f(\text{Voltage})$$

Reduce W, Reduce L.

Keep the ratio constant.

The functionality remains unaffected!

Scaling into deep submicron



Both these transistors have the same functionality



Why MOS technology is preferred to bipolar technology?

- Higher package density than bipolar transistors
- MOS has low power dissipation
- MOS is more noise immune
- It is possible to use MOS devices over a wide range of supply voltage

Bipolar Transistors: Are they too bad?

Bipolar transistors are faster.....



Microelectronics

Silicon

MOS

NMOS

PMOS

CMOS

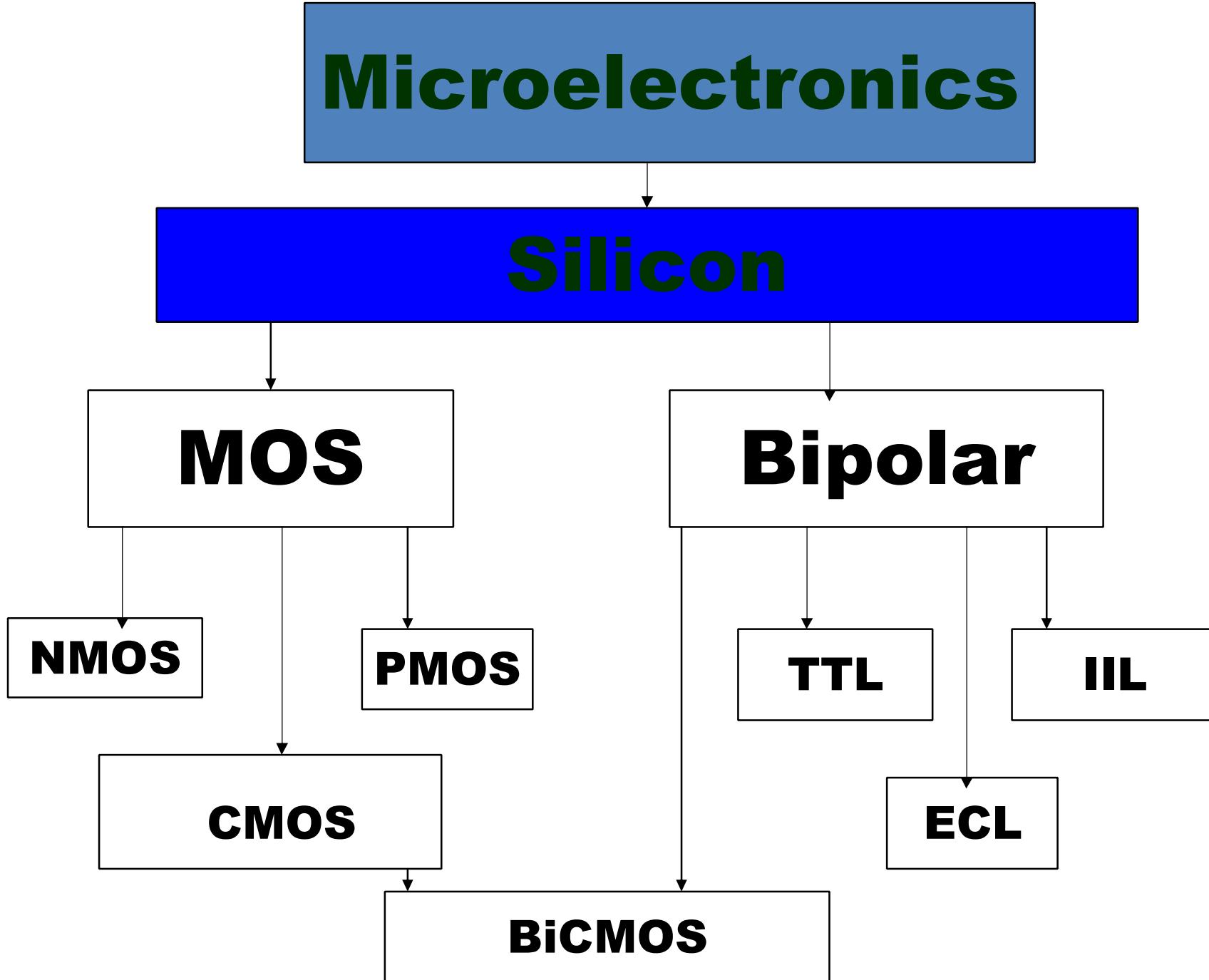
Bipolar

TTL

IIL

ECL

BiCMOS



Conventional design approach unacceptable

- 1. Efficiency must be improved.**
- 2. Large amount of design data associated with schematic, layout and simulation are to be efficiently handled.**
- 3. VLSICs are highly structured.**
- 4. Utilize a small number of basic circuits a large number of times.**

Hence Computer Aided Design.

Design Flow



Modern day design of chips are very challenging because of their high complexities.



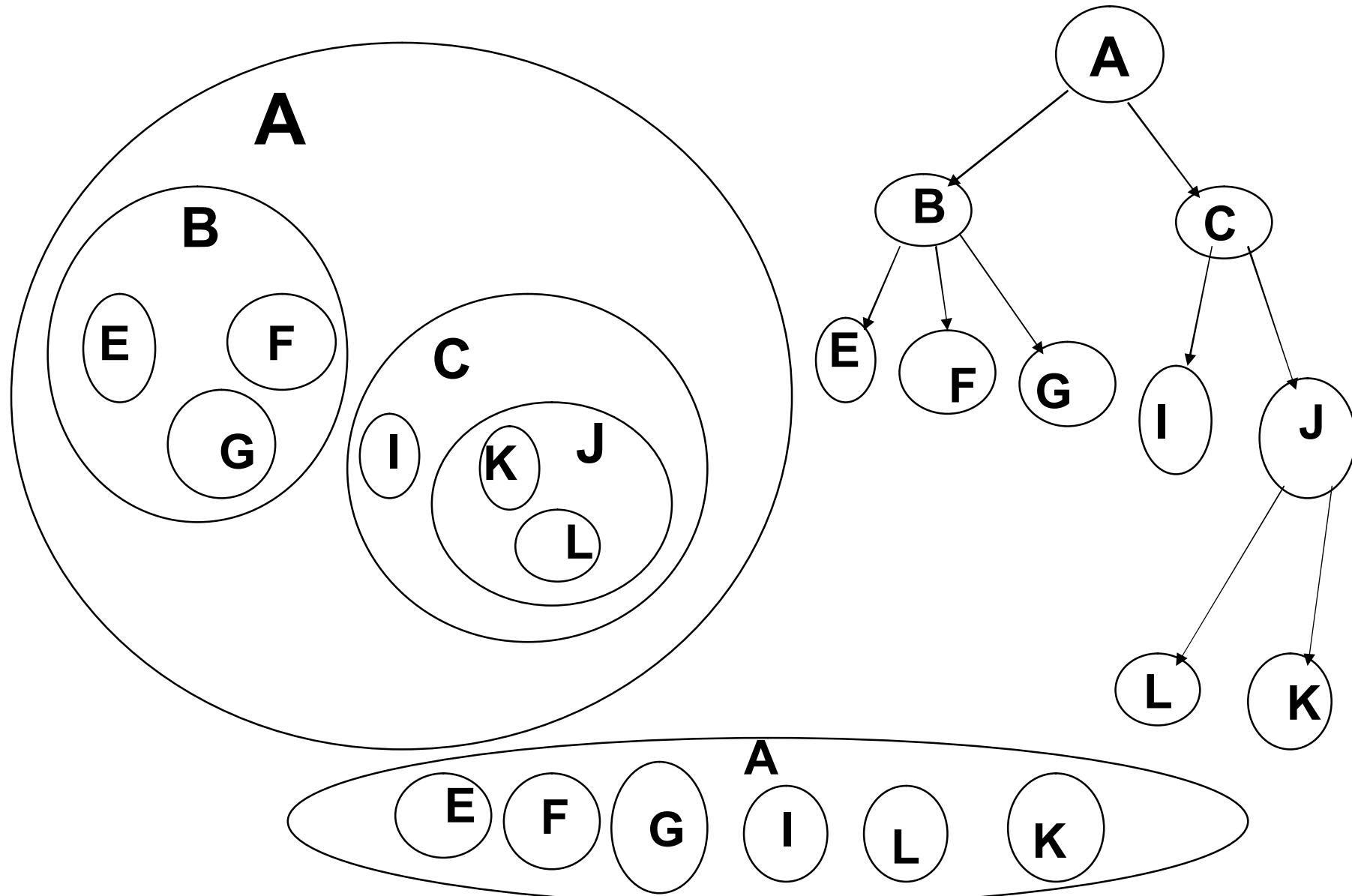
Most of the steps in a chip design are automated.



Integrating the various automation tools, corresponding to the different stages of the design, gives the design flow.

A design flow conveys the essential ideas that go into a typical design cycle, from specifications to manufacturing.

Hierarchy and Abstraction



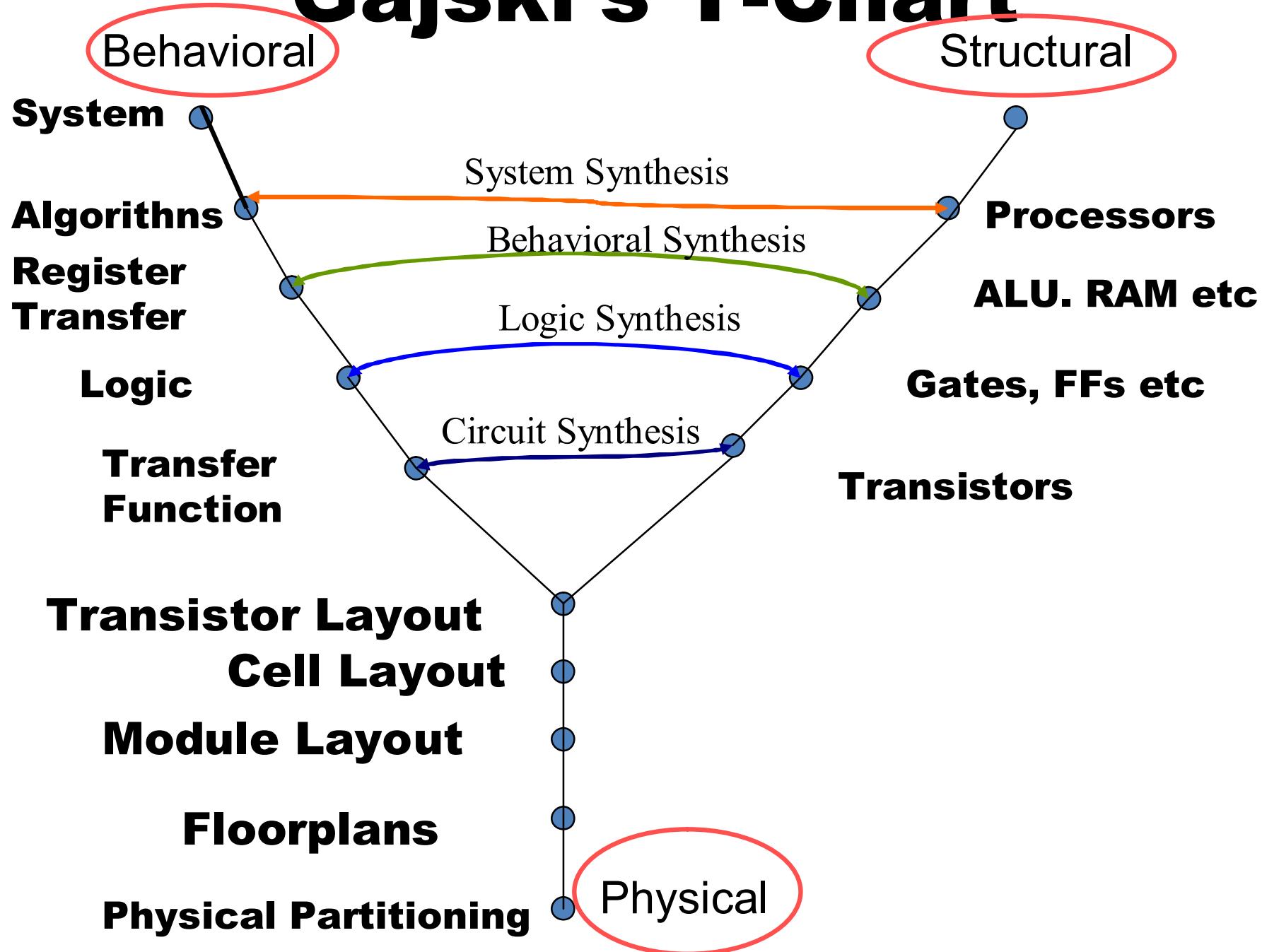
Design Domains

There are three fundamental aspects of any piece of IC hardware: Behavioral, Structural and Physical.

- The behavioral aspect deals with the ***behavior*** of hardware: ***what*** is the functionality and speed (without worrying about the constructional details).
- The structural aspect tells us about the hardware construction: ***which*** parts have been selected for construction and ***how*** they have been interconnected.
- The physical (or layout) aspect deals with the ***physical*** location of each element on a 2-dimensional plain.



Gajski's Y-Chart



VLSI Design Overview (1)

- VLSI design involves translating the given specifications into geometrical patterns that are used for fabricating chips.
- This translation task is very complex in nature and cannot be accomplished in one step.
- It is accomplished through a succession of translation steps of manageable complexity.
- Each translation step translates a more abstract (less detailed) design representation into a less abstract (more detailed) design representation.

Abstractions are the means of representing various views of the design with varying amounts of details



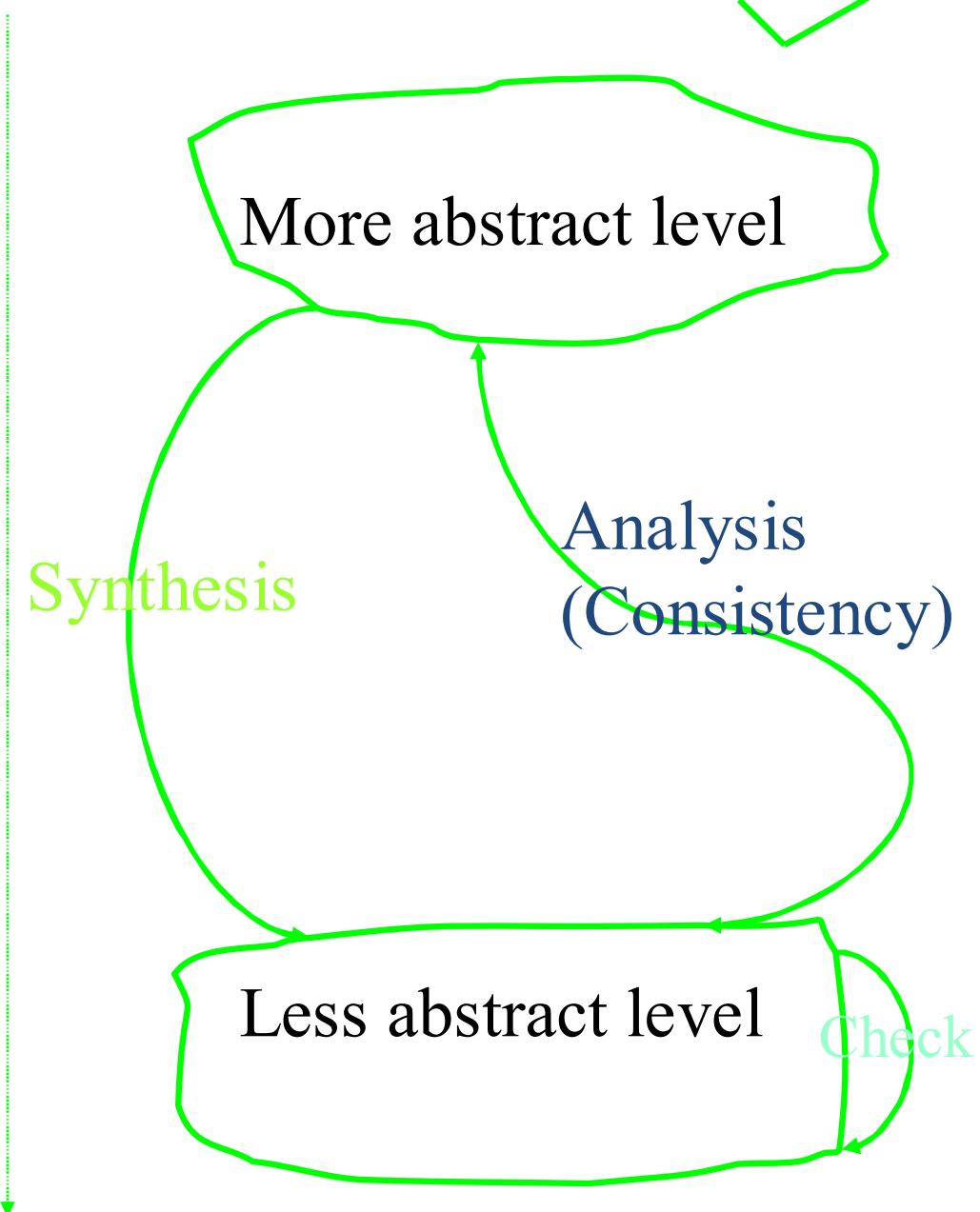
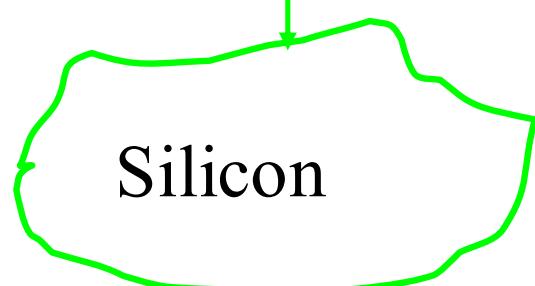
VLSI Design Overview

- Each translation step is a one-to-many mapping.
- For a given design description at any level of abstraction there are many valid design translations to the next lower level of abstraction, each with a different cost-performance thus offering trade-offs to the designer.
- Therefore, the central issue in VLSI design is one of managing *increasing complexity* and making *optimal choices* as one goes through successive translation steps to successive *lower levels of abstraction*.

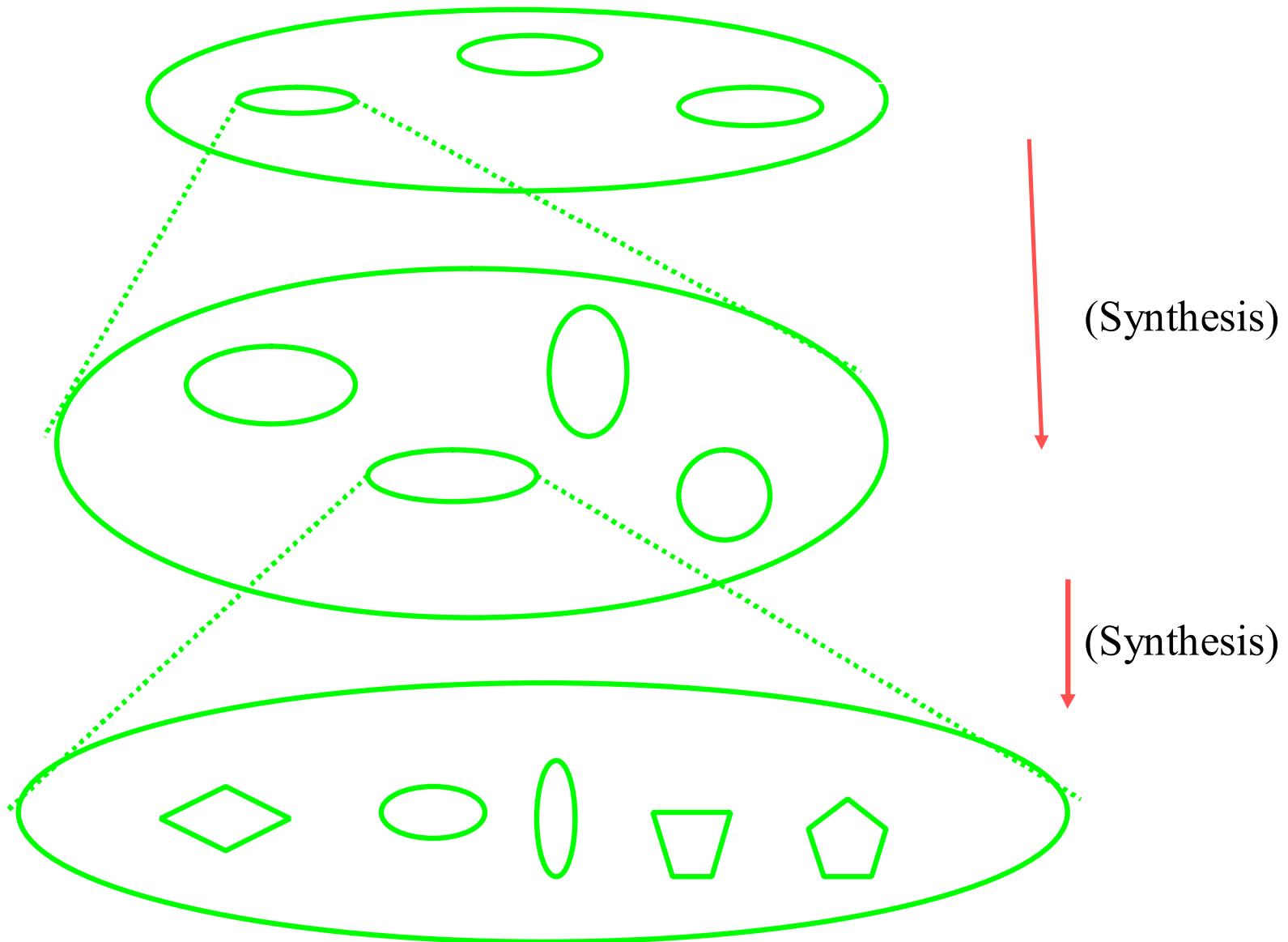




Giant translation step
to meet constraints



Design Translation



Design Actions

VLSI design involves different types of activities requiring different types of CAD tools.

☞ **Synthesis** ⇒ adds details to the current state of the design

☞ **Verification** ⇒ ensures that the synthesis step is correct.

☞ **Analysis** ⇒ provides data on the quality of the design.

☞ **Optimization** ⇒ Improves the quality of design

☞ **Design management tools.**



Optimization – Key Design Parameters

- **Area:** Results in less silicon area and higher yield.
- **Speed:** Results in more computations in less time.
Usually speed is a design constraint, while area needs to be optimized.
- **Power Dissipation:** Results in performance deterioration.
Usually traded with area.
- **Design Time:** Results in lower design costs. Aided by CAD tools and semi-custom design.
- **Testability:** Results in lower testing time. Usually traded with area.



Top-down approach

The designer

- 1. Repeatedly decomposes the system-level specifications into groups and subgroups of simpler tasks.**
- 2. The lowest-level tasks are implemented in silicon with standard circuits that have been previously designed and tested (Standard Cells)**



The Bottom-up Approach

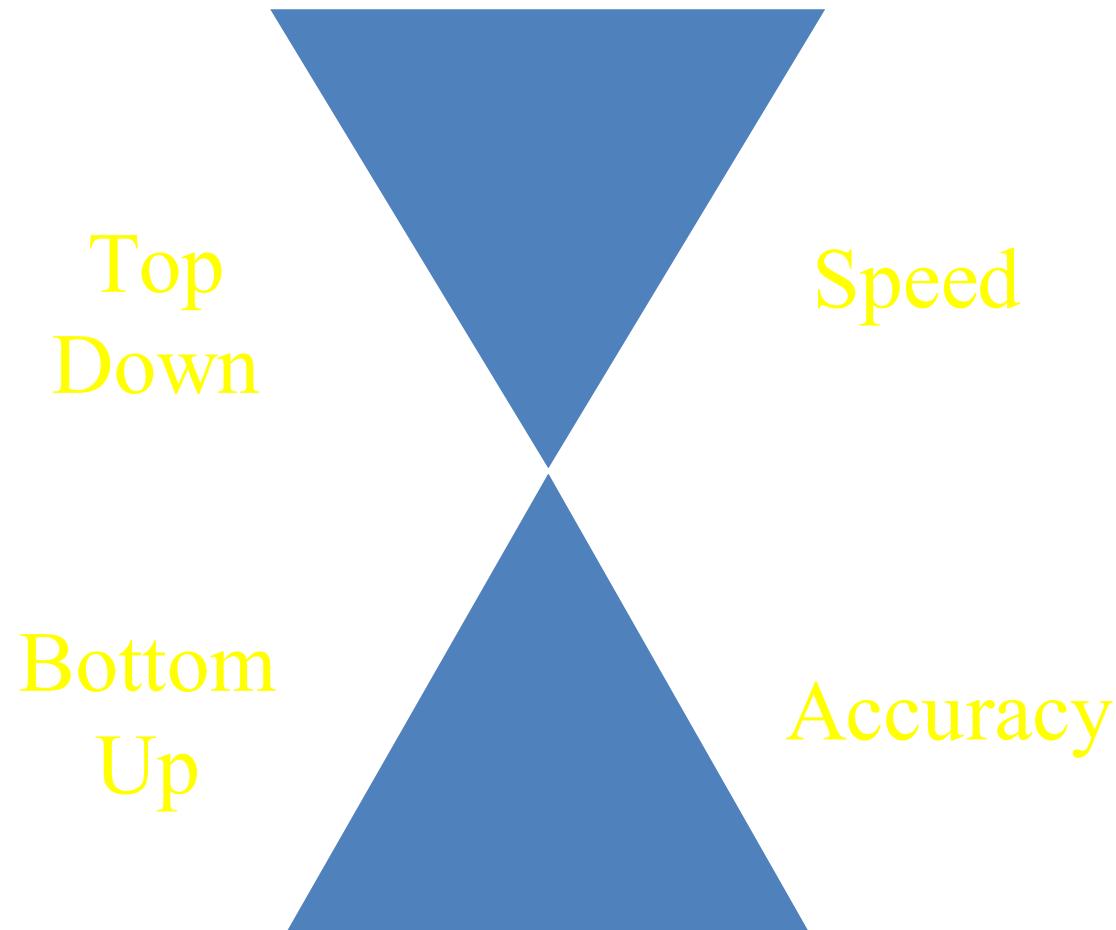
- 1. The designer starts at the transistor or gate level and designs sub-circuits of increasing complexity.**
- 2. These are interconnected to realize the required functionality.**

Top-down approach is better suited for digital design, bottom-up for analog.

Combination of both is the usual mode.



The Two Approaches



Algorithmic and System Design

- A formal description in HDL.
- Simulator to detect errors in specifications.
- Synthesizer to generate equivalent logic netlist.
- Hierarchical FSMs.
- Hardware-software codesign.
- Formal verification etc.



Structural and Logic Design

- Netlist from synthesis or schematic editor.
- Simulator to detect errors in design.
- Fault simulation.
- Automatic test vector generation etc.



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Transistor Level Design

High usage of simulation tools, depending on the accuracy needed.

- **Switch:** digital + signal strengths + capacitances.
- **Timing:** analog + piecewise linear transistor models.
- **Circuit:** accurate transistor models in terms of nonlinear differential equations.



Layout Design

- **Partitioning** keeps tightly connected subblocks in the same place and helps in floorplanning and placement.
- **Floorplanning and Placement** assigns space to each subblock.
- **Routing** generates wiring patterns for correct interconnections and aims for minimal area.
- **Design Rule Checkers** for checking mask geometries.
- **Circuit Extractors** are used for extracting the final circuit from the masks layout, and then simulated for verifying the functionality.



Importance of Simulation in VLSI Design Flow

- Simulation programs are tools for verifying IC design at different stages.
- They enable us to verify functionality and timing of the chip before fabrication (saving time and cost) and allow easy modification of circuit components .



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Why simulation?

Modern day VLSI circuits contain thousands of thousands of transistors.

P-III processor contains 65 million transistors, Itanium 320 million!

Traditional “Breadboard” method fails for VLSI (or even LSI and MSI) circuits.

God save me, my friends and my company, if an IC is fabricated only to be discovered during the test phase that the design is faulty!

70% of the total cost is in the design stage, i.e. before the silicon goes to the furnace.



**It has to be spiced before it is
cooked.**

And spiced well.

And many times.

Before each stage of the design.

And after each design step.

By simulation.

This is called analysis.

Analysis tests the quality of synthesis (design).

SPICE is a simulation program

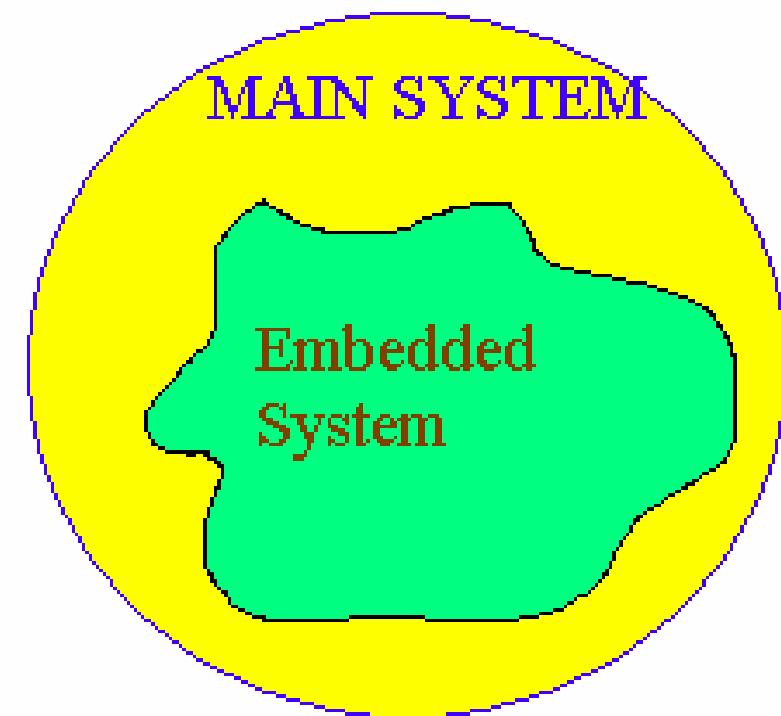
SPICE is an analysis tool.



Design Re-use

- Many system components are available as IP cores
- For example – if we want to design a system using a microprocessor, we don't have to design the μ P from scratch.

ENVIRONMENT



ASIC Design

The Ultimate goal

- Optimized design of the circuit
- Preferably a full custom design
- A huge gain in terms of area, speed and power
- What about the cost?



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Trends in ASIC Design

- Improvement in Device Technology
- Smaller Circuits
- Higher Performance
- More Devices on a Chip
- Higher Degree of Integration
- More Complex Systems
- Lower Cost
- Higher Reliability

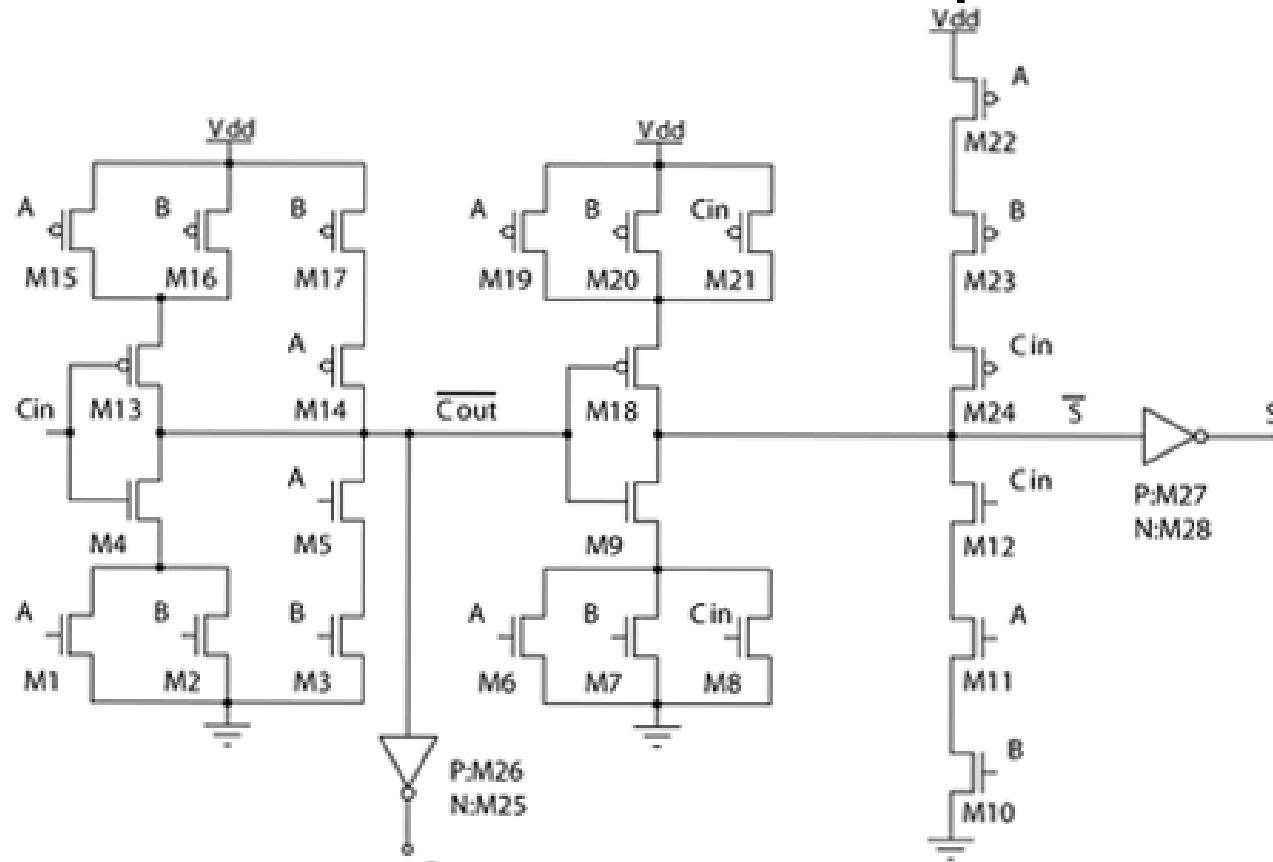


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Circuit size reduction by minimizing transistor count

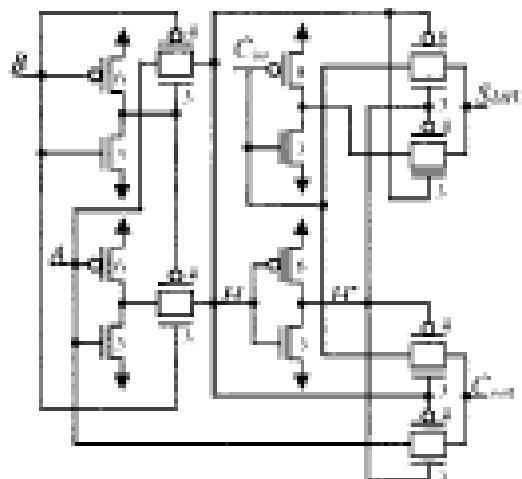
A Full Adder Example



28 Transistor Adder

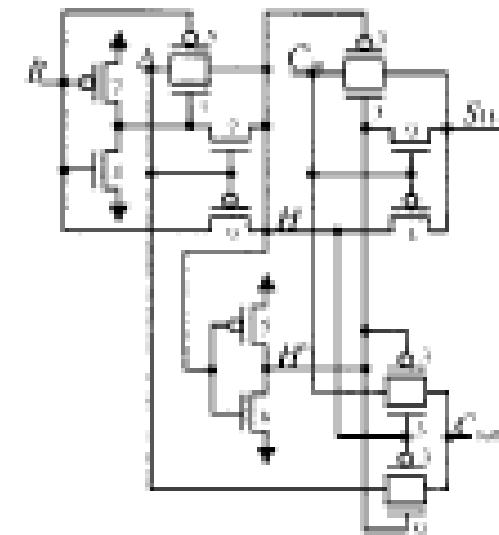


Full Adder Designs (Cont'd)



20 Transistor Adder

M. Weste et al (1991)

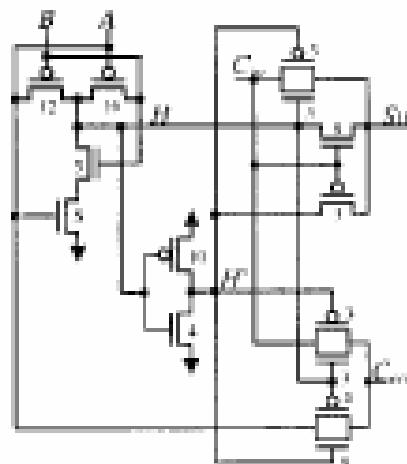


16 Transistor Adder

N. Zhuang et al (1993)

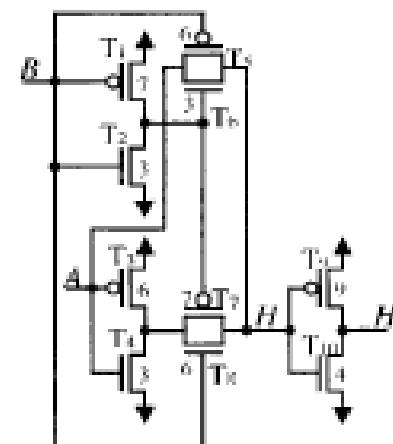


Full Adder Designs (Cont'd)



14 Transistor Adder

E. Abu Shama et al (1995)

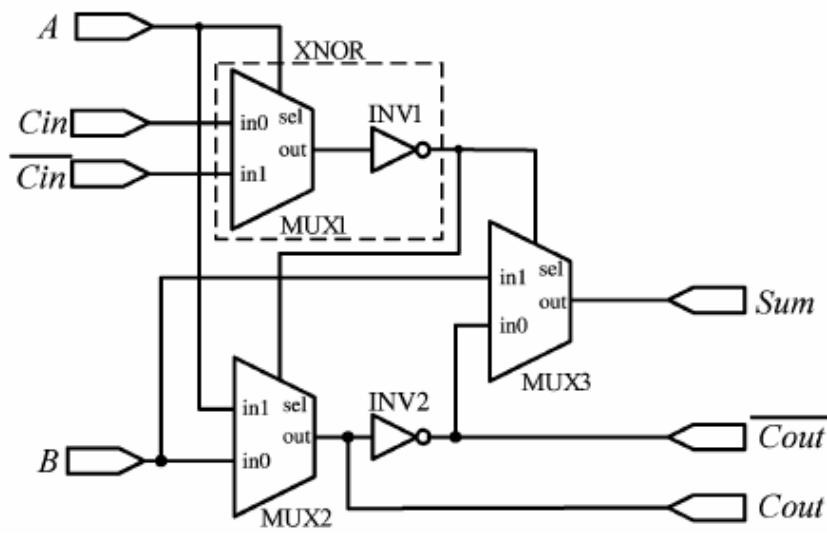


10 Transistor Adder

Ahmed M. Shams et al (1995)

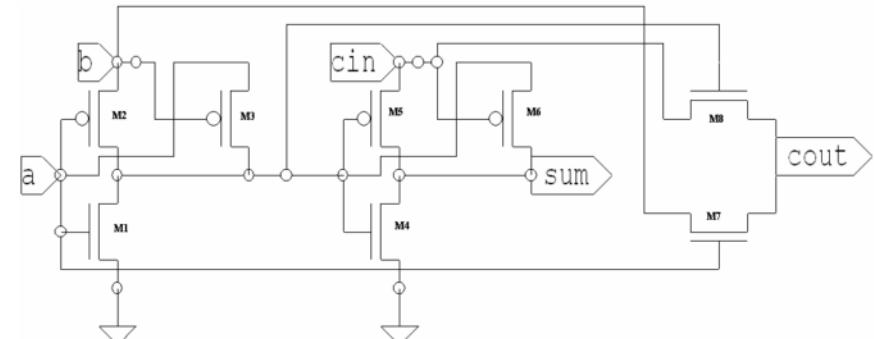


Full Adder Designs (Cont'd)



10 Transistor Adder

J.F. Lin et al (2007)



8 Transistor Adder

S. Roy Chowdhury et al (2008)



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ASIC Design by Rapid Prototyping

- Prototype:
 - The original or model on which something is based or formed
 - Something that serves as an example of its kind
- Rapid:
 - Occurring within a short time
 - Happening Speedily



Miniaturization



Honey, I have shrunk the
kids!

No problem dear. They
still do the crying.



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Towards ULSI

- Complexity $\rightarrow \infty$
- Delay $\rightarrow 0$
- Power Consumption $\rightarrow 0$
- Cost $\rightarrow 0$
- Design Time $\rightarrow 0$
- Field Failures $\rightarrow 0$



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Traditional Architectural Design Styles

- Sea of gates
- Gate Array
- Programmable Logic Devices
- Full Custom ASIC

How are the basic requirements being met?



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Systematizing Analog Designs

- Algorithm to analog circuit mapping: Is that possible?
- Mapping circuit design ideas into a array of analog circuit building blocks
- Analog counterpart of FPGA: Field Programmable Analog Array (FPAAs)



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ULSI Design: The Challenge

- Conquest over complexity
- Systems on a chip: Analog and digital functions on the same chip
- High Speed design
- Control on Power Consumption
- Test and verification



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Ways to manage Complexity

- Take a page out of software developers' book
: Hardware Description Languages
- Design reuse
- Exploit Regularity of designs



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Can we go on downscaling the transistors?

- Will Moore's Law run out of steam?
 - Can't build transistors smaller than an atom...
- Many reasons have been predicted for end of scaling
 - Dynamic power
 - Subthreshold leakage, tunneling
 - Short channel effects
 - Fabrication costs
 - Electromigration
 - Interconnect delay
- **The nano-walls have to be crumbled!!!!**



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Solution Idea

- Possible way for the microelectronics industry to maintain growth in device density is to change from the FET-based paradigm to one based on **nanostructures**
- Instead of fighting the effects that come with feature size reduction, these effects are used advantageously.



Possible Avenues

- Molecular Electronics
 - ❖ Build logic devices from conducting molecules
- Carbon Nanotubes
 - ❖ Can get switch like behavior make wires
- Quantum Computing
 - ❖ Rather than using voltages on transistors to encode information, exploits interacting electric or magnetic field polarization to effect Boolean logic functions
- Biological Computing
 - ❖ Biological reactions mimic logic gates



**Where do you want to
go tomorrow?**

THINK



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