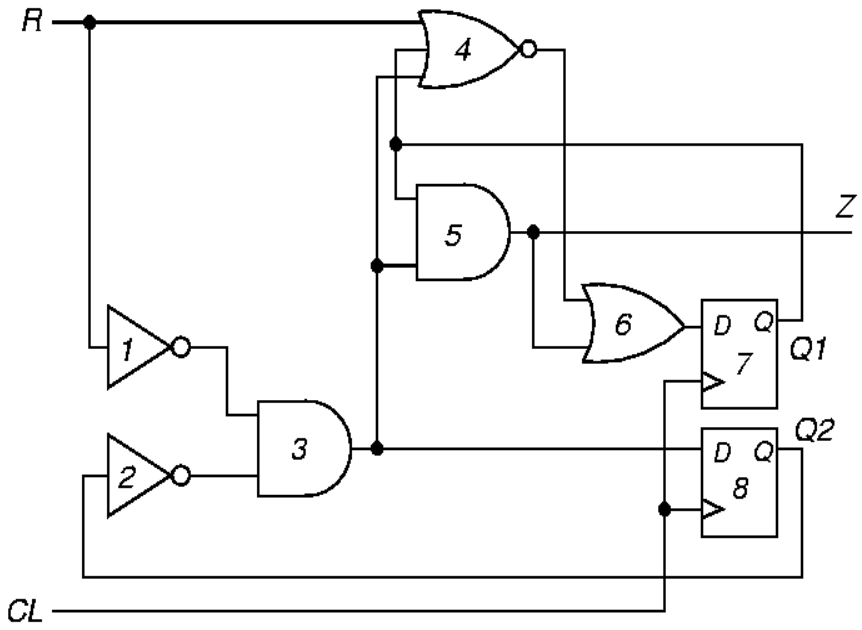
DESIGN FOR TESTABILITY

Assignment-3

1. Calculate the probability based testability measures for a three input XNOR gate and for its NAND-NOR implementation. Assume that the probability based controllability values at all primary inputs and probability based observability value at the primary output are 0.5 and 1 respectively.

2. Repeat problem no. 1 for a full adder circuit.

3. Calculate the SCOAP controllability and observability measures of all nodes in the following circuit.



4. Show a possible gate level implementation of a clocked scan cell with separate scan and data clocks.

5. In a barrel shifter circuit how will you use scan register for increasing controllability and observability of it. What is the area overhead of adding such DFT to a circuit?

6. Repeat problem no. 4 for ALU design.

7. A company ABC works on processor design which designed the ALU having three kinds of operation :
   Logical (NOT, AND, OR)
   Shift Operation (Left Shift, Right Shift)
   Arithmetic Operation (Add, Subtract)

Suppose you are employee in that company and you are given a job to re-design this ALU. The new ALU consist of 3 types of operation as given above and along with that a new operation: Comparator which will compare the two inputs and give output in three new registers namely GRT, LESS, EQ

Compare operation:

GRT=1 if A>B

LESS=1 if A<B

EQ=1 if A=B

If you model the ALU functionally then you have to make complete new ALU. But, if you use structural modeling then in the old ALU itself, you can add another block COMPARATOR (say) while the code of old ALU remains the same. That is why bigger projects in VLSI like processor design are using structural models since it is easy to verify and modify. As in this TASK you have to make RTL code of this COMPARE operation and instantiate this with the old ALU.

8. Write a program in C that will accept the truth table or state table of a 4 input digital circuit as its input and compute the controllability and observability of all the nodes of the circuit.

9. Cellular multipliers may be classified by the format in which data words are accessed, namely serial form and parallel form. The choice lies more or less in speed (or throughput) and silicon area, which are the major factors contributing to the performance and cost of the circuit. Bit-serial multipliers can further be divided into bit-sequential ones and serial-parallel ones. A bit-sequential multiplier accepts its operands bit by bit; while a serial-parallel one takes one input in serial and the other in parallel. Both types produce outputs in series. They have about the same area (hardware) and time complexities. Design a 4-bit unsigned bit-serial integer multiplier in either bit-sequential or serial-parallel form. Give the block diagram of the multiplier, which is an array of four basic cells. Give the schematic of the cell, which consists of a full adder and a few primitive gates, flip-flops, and latches. Explain how the multiplier works. Enter your design into a CAD environment, using, e.g., Verilog, VHDL, or any schematic capture tool. Verify your design by your functional patterns until you are confident that the design is correct.

10. Repeat the above experiment, but now use MUX scan approach in your design. Explain the difference.