Intro to VLSI

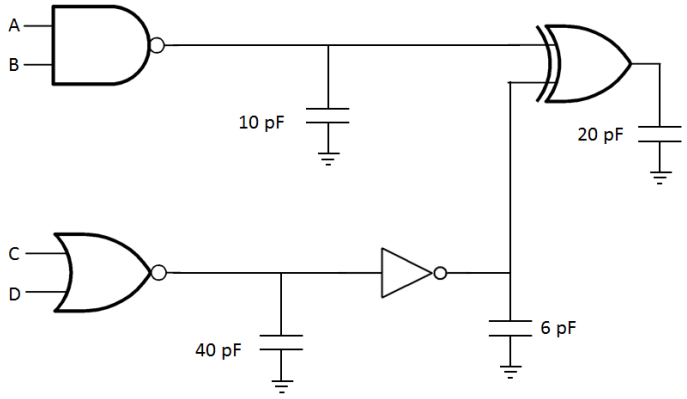
Assignment #4

Deadline: 22nd March 2012 (In Class)

Q1. Find dynamic power for the following circuit.

Assume V_{DD} = 3V, f_{clk} = 1.5 GHz and inputs have following probability values that change on +ive edge of clock.

P(A=1) = 0.5, P(B=1) = 0.3, P(C=1) = 0.2, P(D=1) = 0.1



Q2. Considering all NMOS transistors to be of same dimensions (W/L) in a 3-input XOR gate, find the dimensions of an equivalent transistor.

Q3. The path from the data cache to the register file of a microprocessor involves 500 ps of gate delay and 500 ps of wire delay along a repeated wire. The chip is scaled using constant field scaling and reduced height wires to a new generation with S=2. Estimate the gate and wire delays of the path. By how much did the overall delay improve?

Q4. Find the rising and falling propagation delays of a 2-1 AOI (And-Or-Invert) gate using the Elmore delay model.

Q5. Describe the various limitations in CMOS scaling.