ASSIGNMENT 5:

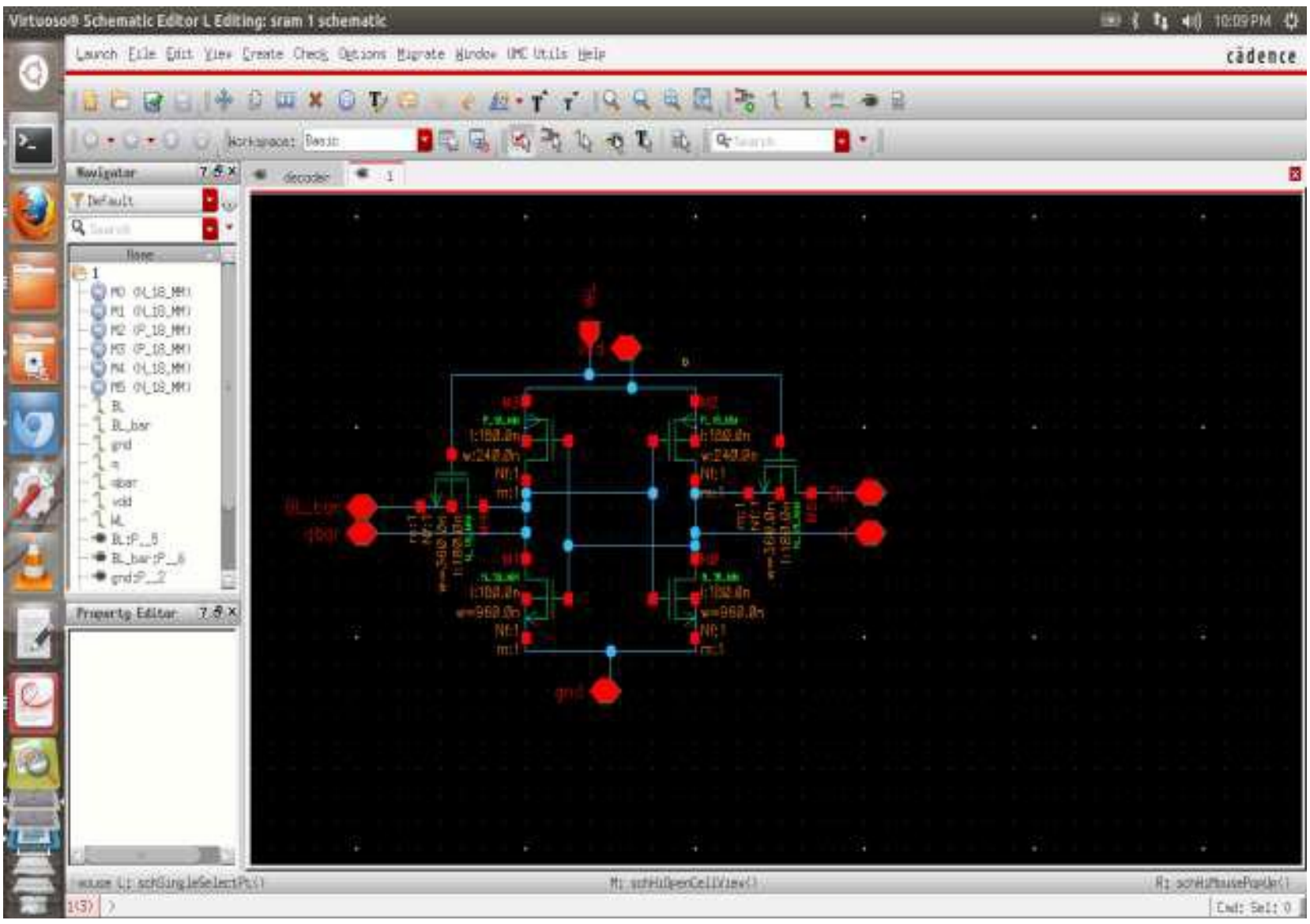
VLSI ARCHITECTURES

1. Consider a 1KX64 bit SRAM. The memory consist of1K words, each consisting of 64 bits arranged as a 256X256 array of 6T SRAM cells. A word is selected for reading by the row and column decoders. The row decoder asserts one of the 256 word-lines. Each word-line selects a row of four 64 bit words. Four selected words feed the input of the 4:1 MUX controlled by the outputs of the column decoder. Each access transistor in the memory cell is 4 in width. Each SR M cell is 40 X40 . Use TSMC 180nm CMOS process.

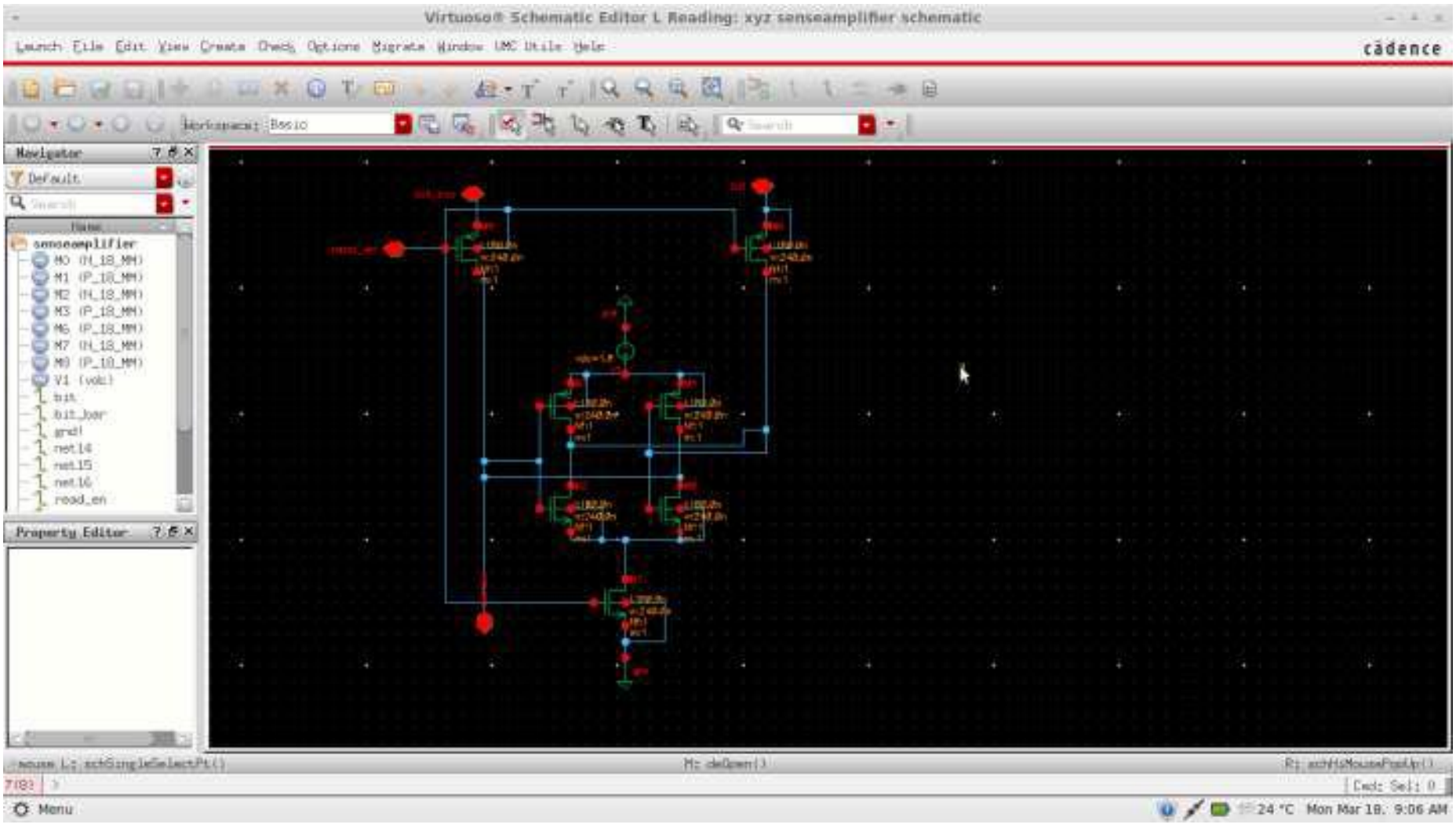
(a) Estimate the average power being dissipated and the maximum power being dissipated.

(b) Estimate the average delay to access a word from the memory.

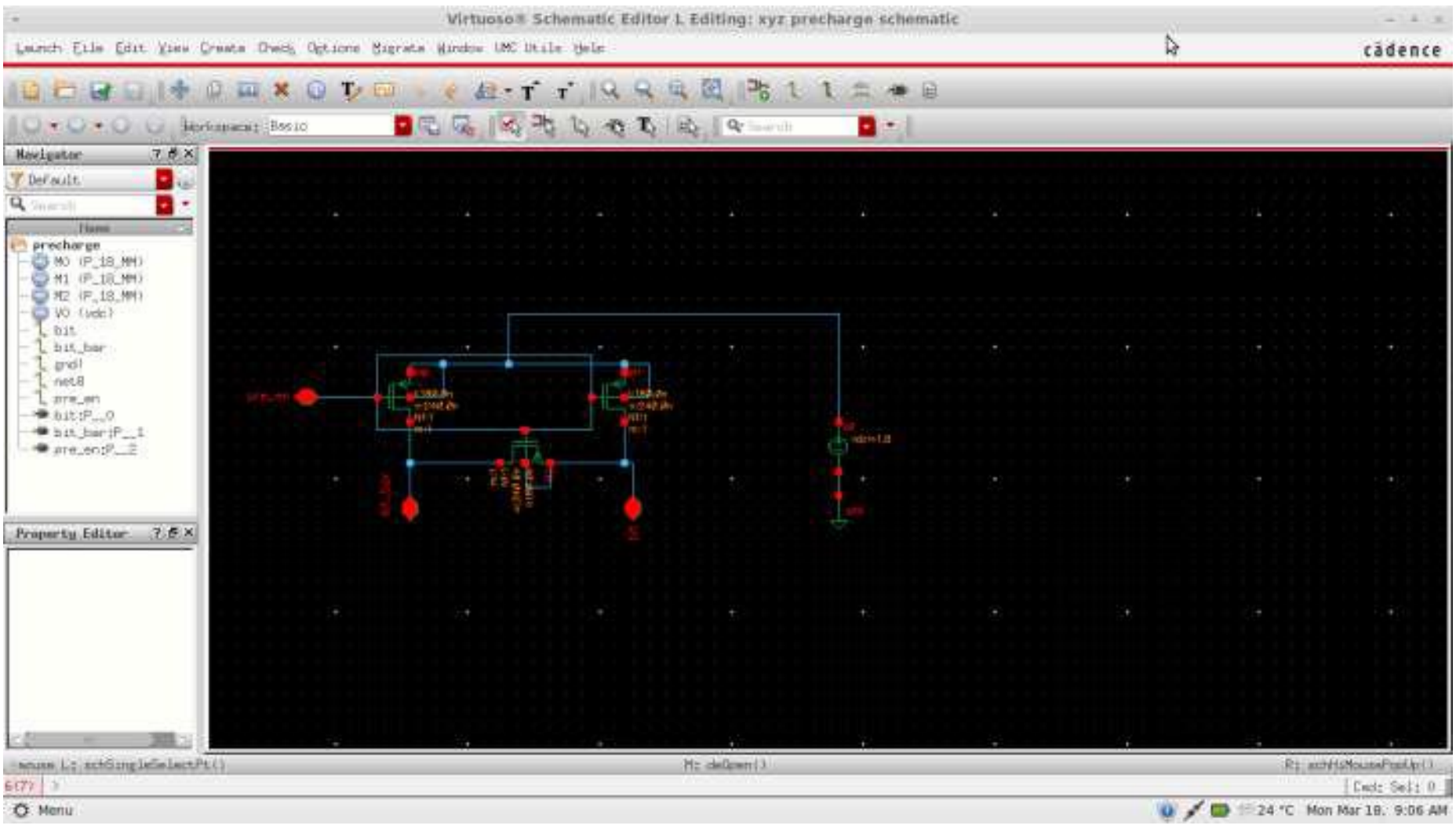
The schematic of SRAM is as below:



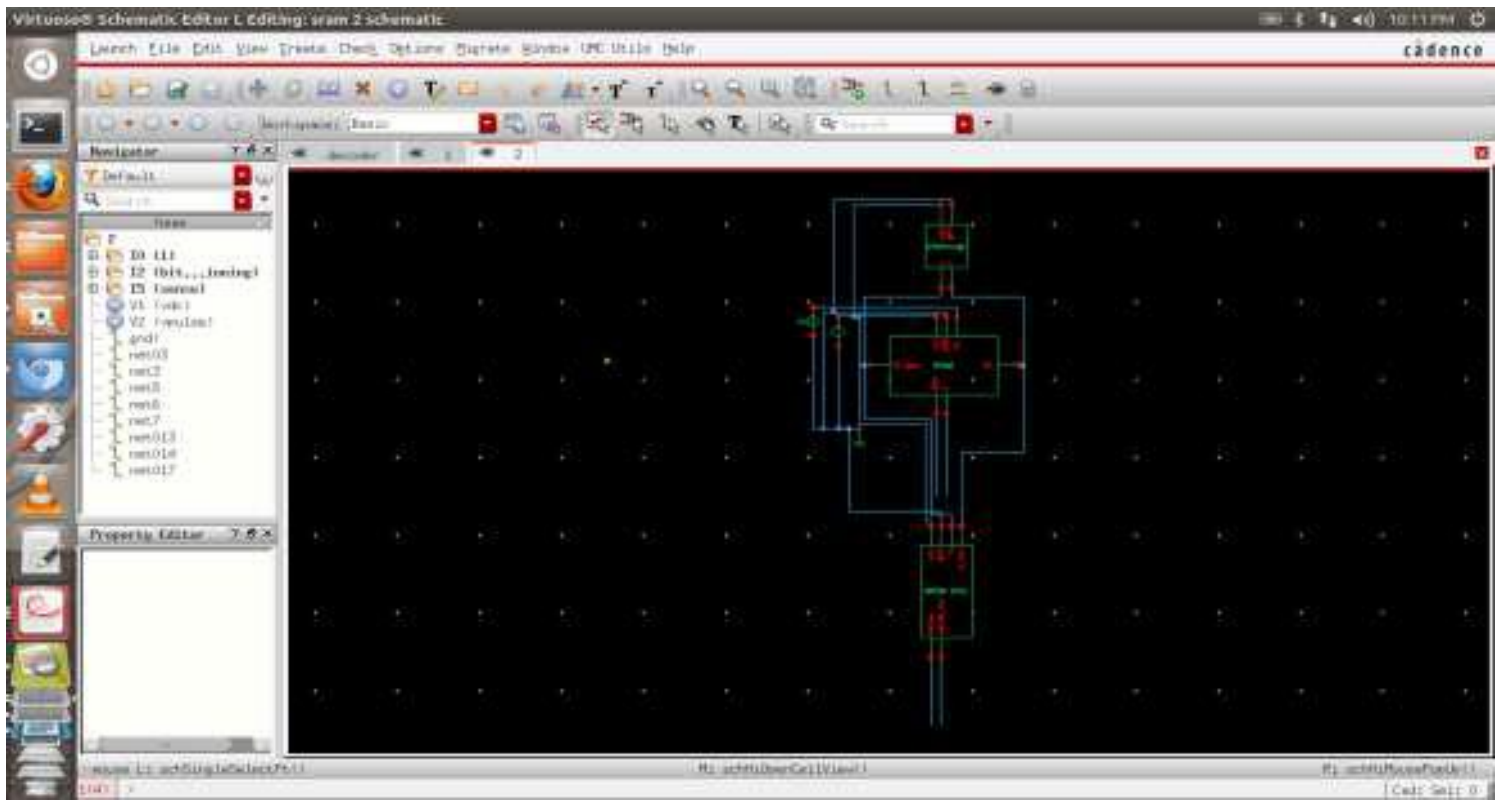
Below is the circuit schematic for the sense amplifier:



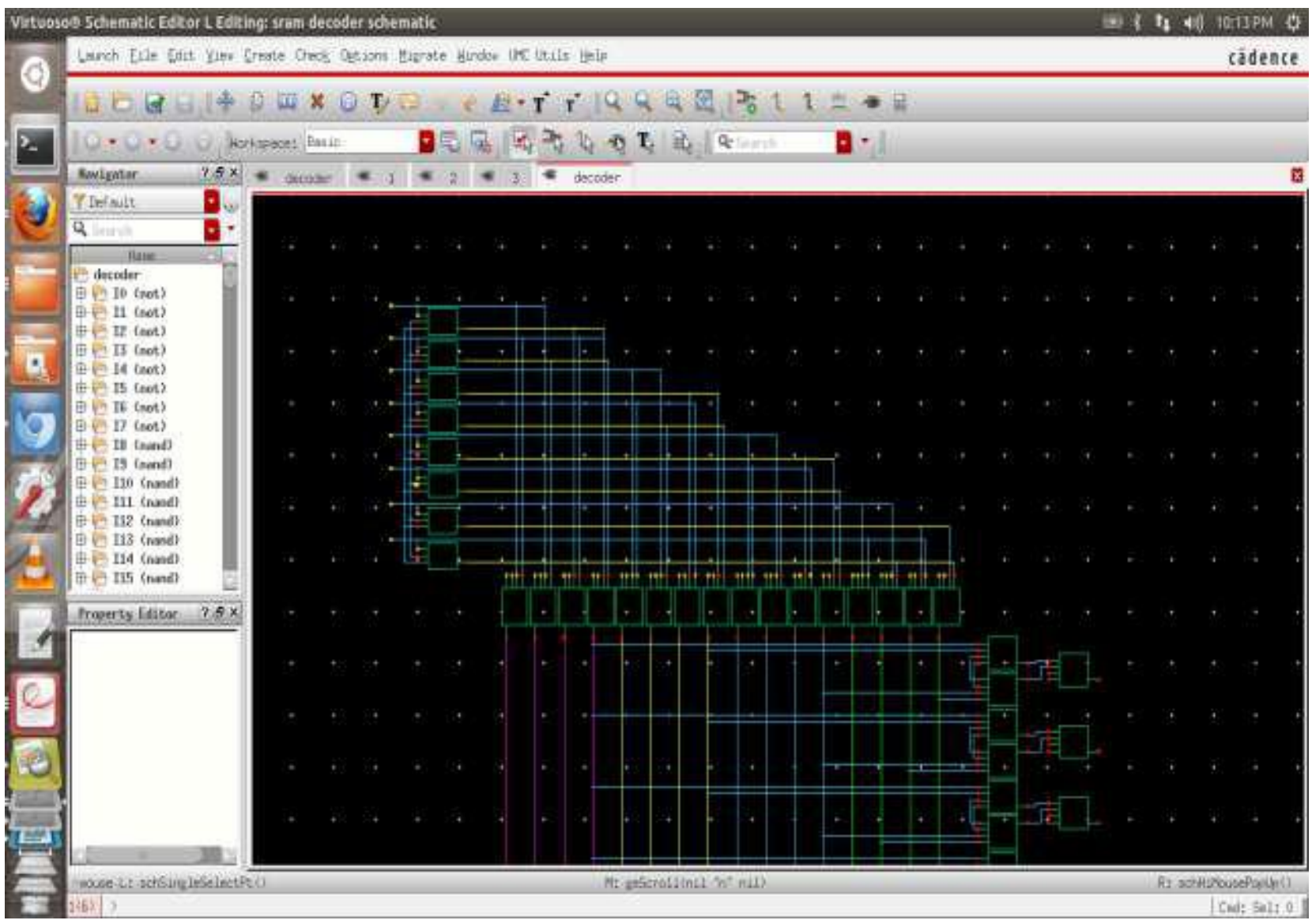
Precharge circuit:



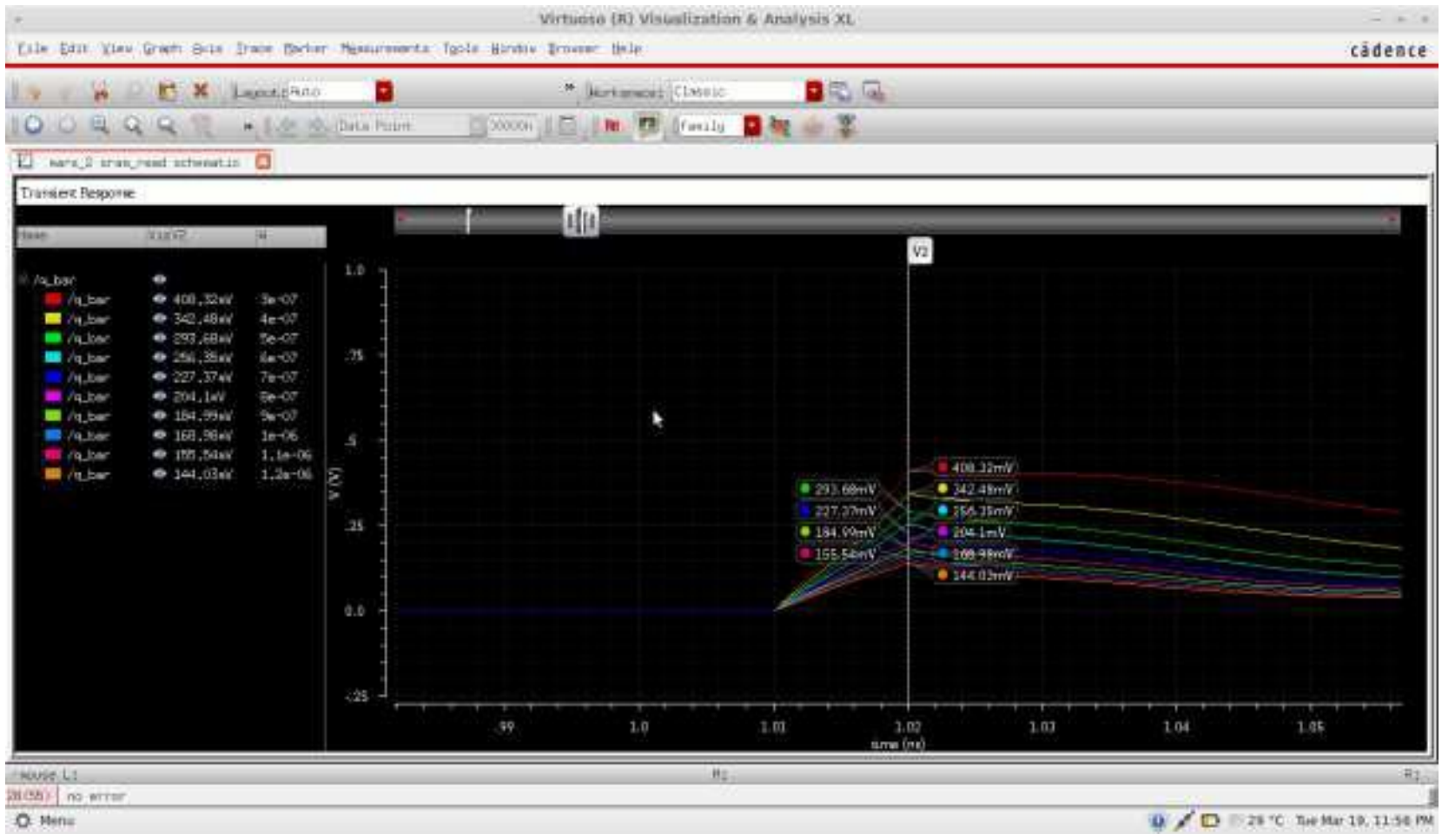
Sense amplifier, precharge and SRAM circuit circuit



Decoder circuit:



Width variation and the corresponding read variatio



Vbump voltage calculation: