Intro. To VLSI (ECE 361)

Assignment #3

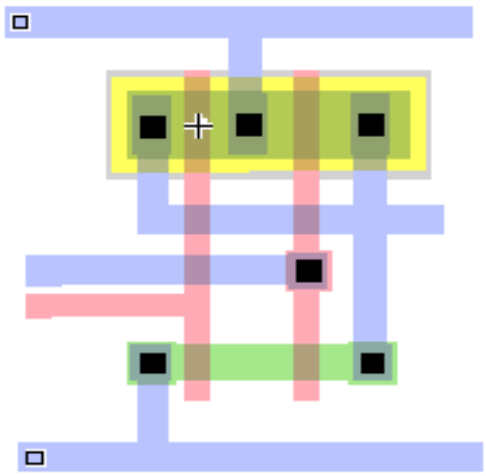
Deadline: 16th Feb

Q1. Draw the schematic of the following using 'BICMOS' logic: [6 Marks]

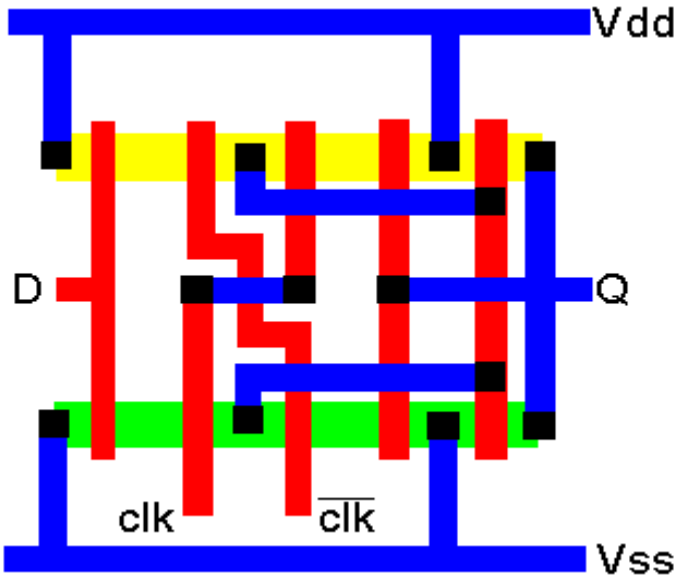
a) 2-input AND gate
b) 2-input XOR gate
c) AB+BC+AC

Q2. Estimate the area of the following layout designs: [4 Marks]

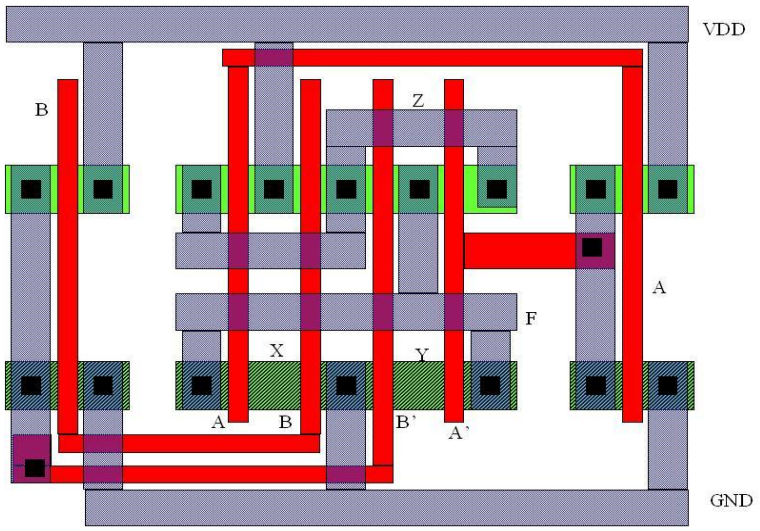
a)



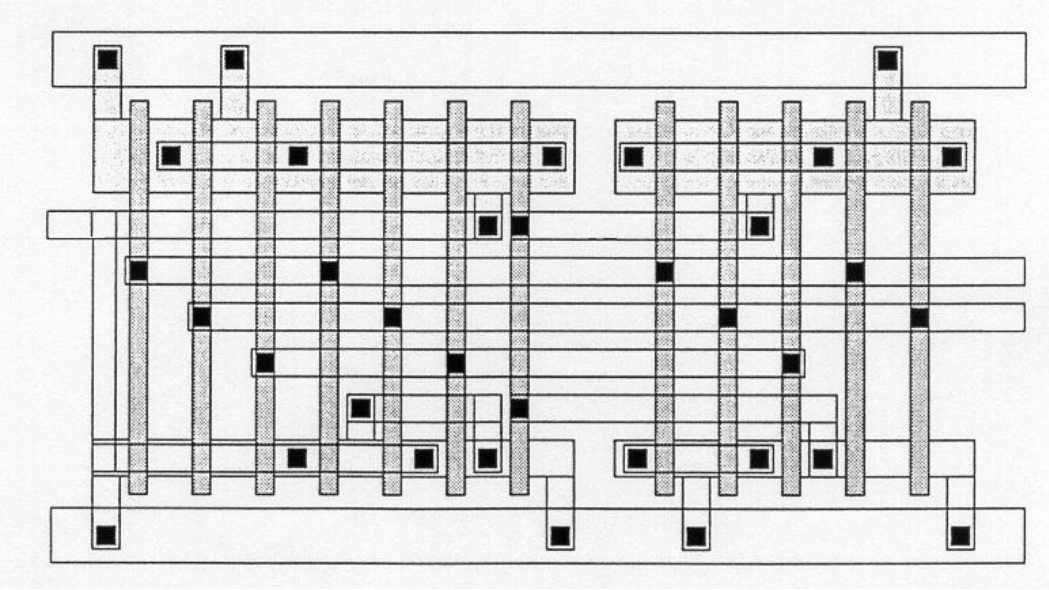
b)



c)



d)



Q3. Sketch the layout of the following gate and estimate its area in terms of λ^2. [5 Marks]

3-input XOR gate (A xor B xor C)

Q4. Write short notes on: [5 Marks]

a.) Photolithography
b.) Ion implantation
c.) Solid state diffusion

d.) Etching
e.) Photoresist

Q5. Describe the fabrication process (including all steps and diagrams) for a NOR gate. [10 Marks]