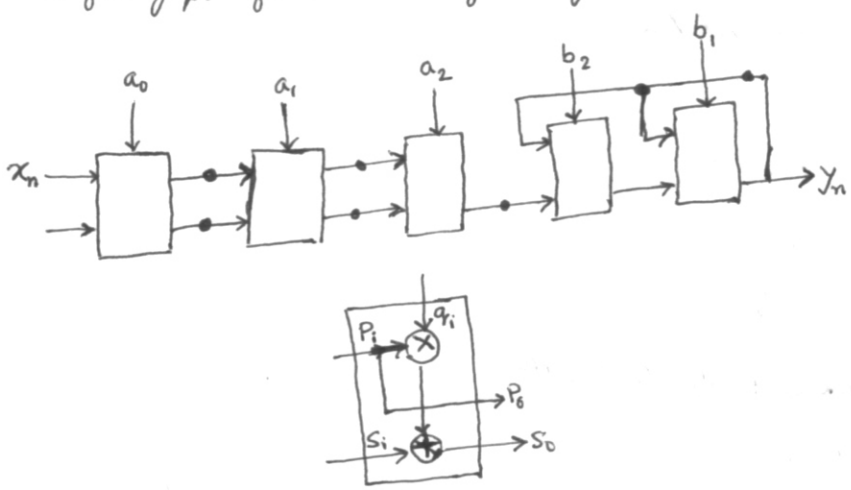
Hints and Solutions to

Mid Semester Examination I (Spring 2012)

VLSI Architectures.

1. The dataflow graph for the IIR filter is given as:-



$P_i \rightarrow$ Multiplicand ~~Previous product~~

$q_i \rightarrow$ Multiplier

$P_0 \rightarrow$ Product output

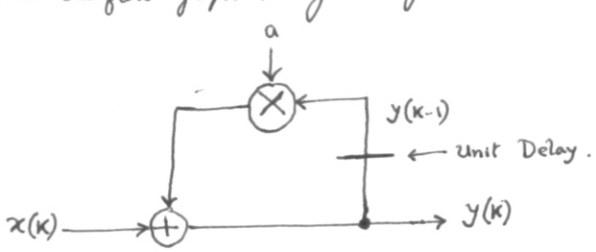
$S_i \rightarrow$ Sum input

$S_0 \rightarrow$ Sum output.

Dots on the edges of the graph represent unit delays.

Now draw the sequencing graph.

2. The dataflow graph is given by:-



Unfolding the loop by a factor of 4 we get,

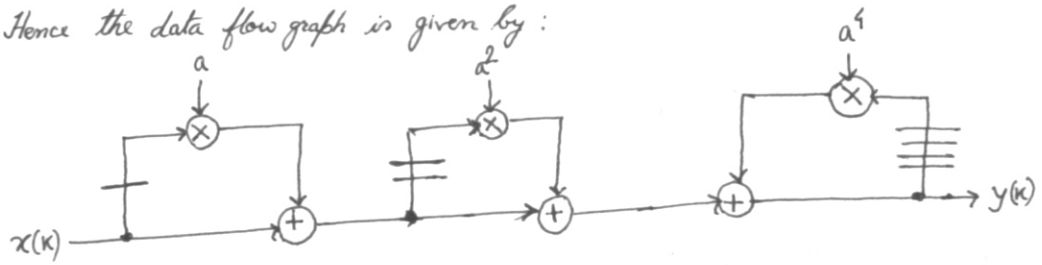
$$y(k) = a^4 y(k-4) + a^3 x(k-3) + a^2 x(k-2) + a x(k-1) + x(k).$$

Taking Z transform of both sides we get,

$$Y(z) = a^4 z^{-4} Y(z) + a^3 z^{-3} X(z) + a^2 z^{-2} X(z) + a z^{-1} X(z) + X(z)$$

$$\text{Hence, } H(z) = \frac{Y(z)}{X(z)} = \frac{1 + a z^{-1} + a^2 z^{-2} + a^3 z^{-3}}{1 - a^4 z^{-4}} = \frac{(1+az^{-1})(1+a^2 z^{-2})}{1 - a^4 z^{-4}}.$$

Hence the data flow graph is given by :



Now draw the hardware architecture.

The loop equation is given by:

$$y(k) = a(k)\, y(k-1) + x(k).$$

Substituting for $y(k-1)$ we get,

$$y(k) = a(k)\, a(k-1)\, y(k-2) + a(k)x(k-1) + x(k)$$

Substituting for $y(k-2)$ we get,

$$y(k) = a(k)\, a(k-1)\, a(k-2) y(k-3) + a(k)\, a(k-1)\, x(k-2) + a(k)x(k-1) + x(k).$$

Generalizing we get,

$$y(k) = \left(\prod_{n=0}^{p-1} a(k-n) \right) \cdot y(k-p) + \left(\sum_{n=0}^{p-1} \left(\prod_{m=0}^{n-1} a(k-m) \right) \cdot x(k-n) \right) + x(k)$$

Substitute for $p=4$ and obtain the data flow graph.