S.No.	Team Name	Project
1	Prahal Priyam Shreyam	FPGA Implementation of a Scalable Encryption Algorithm
2	Anirban Guha Abhishek Bhatia YELLAPRAGADA KIRAN KUMAR	A High-speed 32-bit Signed/Unsigned Pipelined Multiplier
3	Aashit Abhay Siddharth	FPGA Implementation of RS232 to Universal serial bus converter
4	Aakash Deepank Praveen	Performance Efficient FPGA Implementation of Parallel 2-D MRI Image Filtering Algorithms
5	Pradyumna Reddy Shivaram Reddy Ramakrishna Vedantam	Design and FPGA implementation of high-performance face-detection engine for mobile applications
6	Rahul.P.R R Dinesh Sai Varma Repuri Bhargav	Shift Invert Coding (SINV) for Low Power
7	Chetan Anshul Akhil Agrawal	VLSI Implementation of Fully Pipelined Multiplier-less 2D DCT/IDCT Architecture for JPEG
8	DHRUBAJYOTI DUTTA JAIDEEP SIHORA SACHIN KUMAR	Parallel Architecture for Hierarchical Optical Flow Estimation Based on FPGA
9	Shubham Gupta Harish reddy Govardhan	FPGA Based Power Efficient Channelizer for Software Defined Radio
10	P. Pranav Kumar Pradeep Gavvp Koora Rahul Reddy	Design and Implementation of Low Power Digital FIR Filter based on low power multipliers and adders on FPGA
11	MAMIDI RAJA Venna Sai Sindu VENU NALLA	Multiplier design based on ancient Indian Vedic Mathematics
12	Rituraj Yadav Ankit Verma Avni Jain	FPGA based robust UART Architecture Based on Recursive Running Sum Filter for Better Noise Performance
13	Aditya Kumar Kshitij Agrawal NAGA SITARAM	Implementing Gabor Filter for Fingerprint Recognition Using VHDL
14	samyak gandhi ruchin jain parveez iqbal	VLSI Implementation of Auto-correlator and CORDIC algorithm for OFDM based WLAN
15	Hiten Jayswal Ravi Kumar Saumya Suneja	VLSI Implementation of an Edge-Oriented Image Scaling Processor
16	sai krishna teja.K phani sriram P.V.D praveen kumar verma	A Symbol-Rate Timing Synchronization Method for Low Power Wireless OFDM Systems
17	K.Anudeep Hari prasad.G Naveen kumar.V	A Low-Power Multiplier With the Spurious Power Suppression Technique
18	sachin.Y karthik kumar.A Arun gowtham .S	An Effective Fast and Small-Area Parallel-Pipeline Architecture for OTM - Convolution Encoders

19	Abhimanyu singh PRADEEP N Niranjan Reddy	VLSI Architecture and Chip for Combined Invisible Robust Watermarking
20	Abhiram sai krishna Bokka Varun Sarma harshvardhan	High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics
21	NUPOOR VYAS MANSI BHARGAVA TRIVEDI RAVI MAHESHBHAI	An Efficient Architecture Design for VGA Monitor Controller
22	Ranga teja hrishikesh chillal L.V.R. PRASADA RAJU	An Implementation of a 2D FIR Filter Using the Signed-Digit Number System
23	BHUVANAN.K RASHMI SONI SHRUTI CHORMALLE	A Robust UART Architecture Based on Recursive Running Sum Filter for Better Noise Performance
24	Jasmeet Aman Siddharth	Design and FPGA Implementation of Modular Multiplication methods using Cellular Automata

Instructions for Students

1. **Reports are to be submitted in the format of one report per group.**
2. **In those topics where FPGA is mentioned in the project topic, only in those cases FPGA based implementation is requested.**