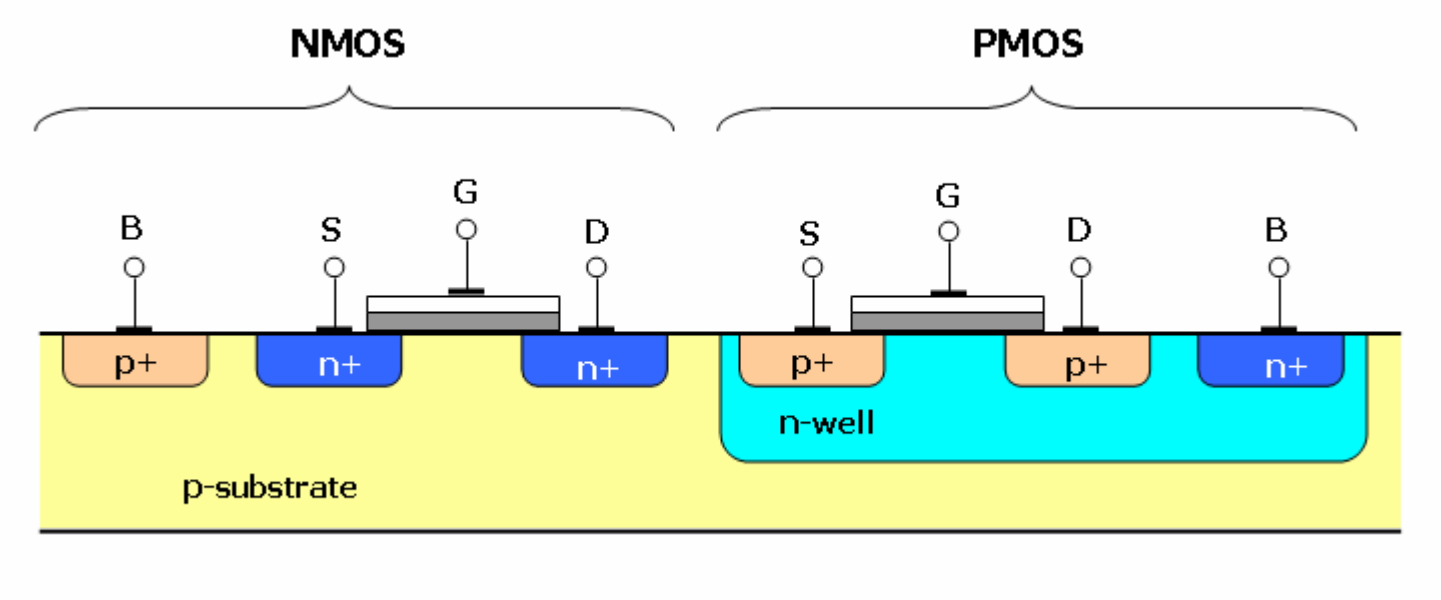
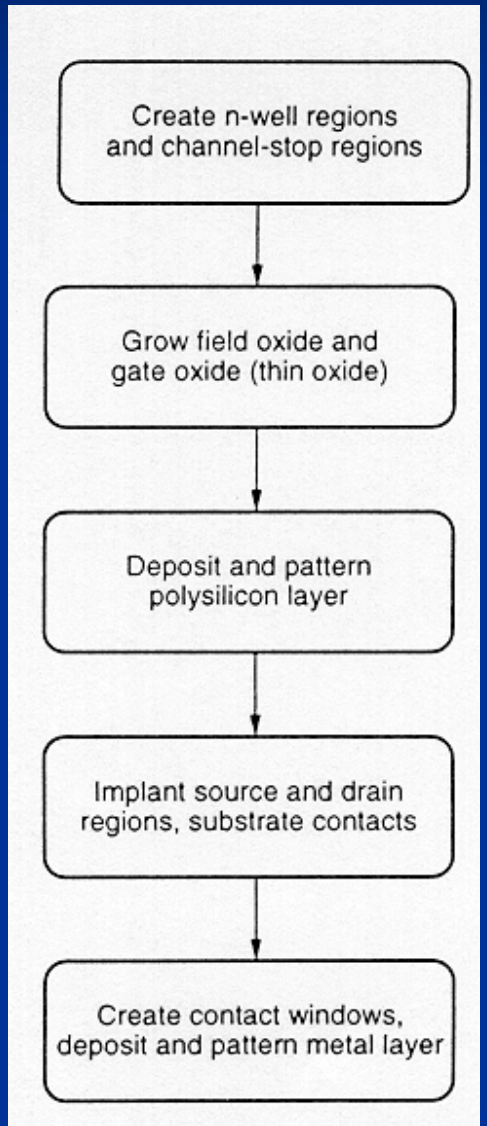
VLSI Design

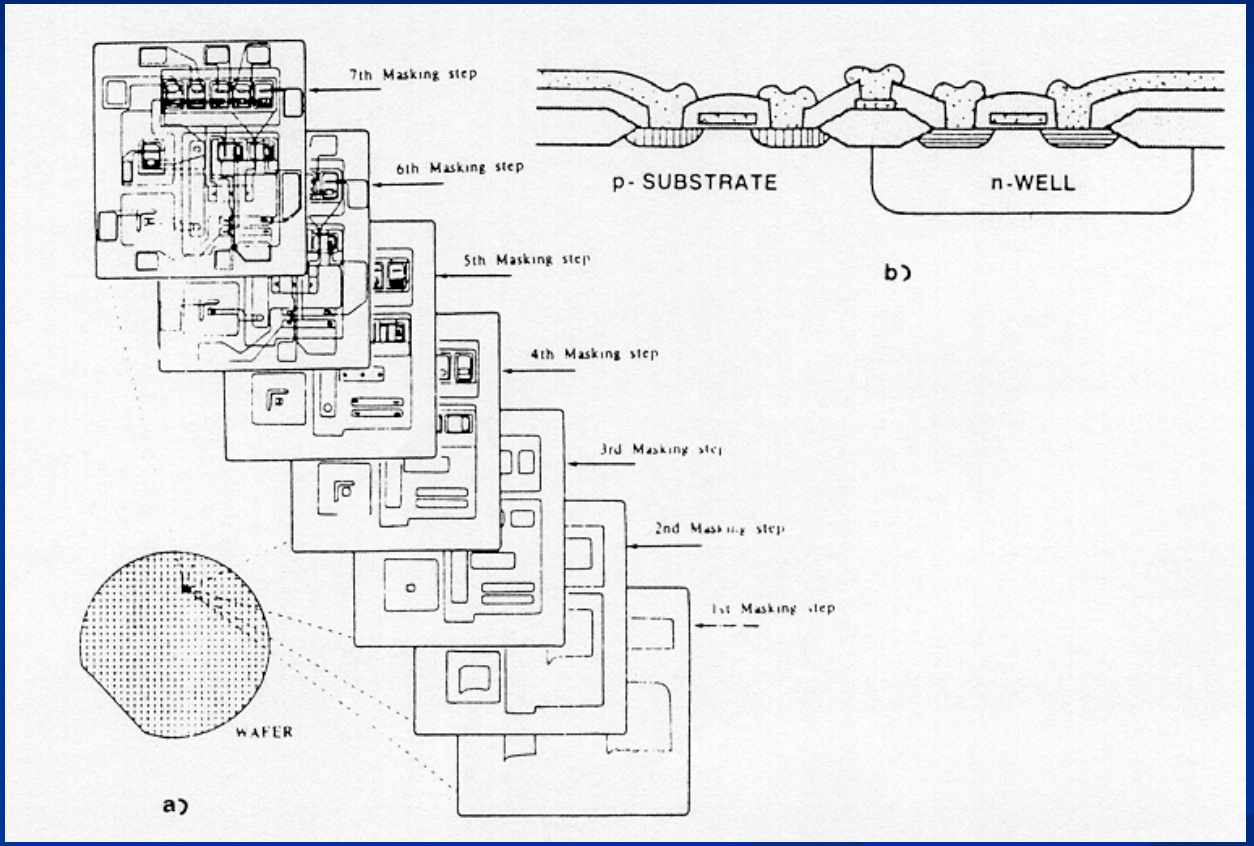
Fabrication Process

CMOS Transistors

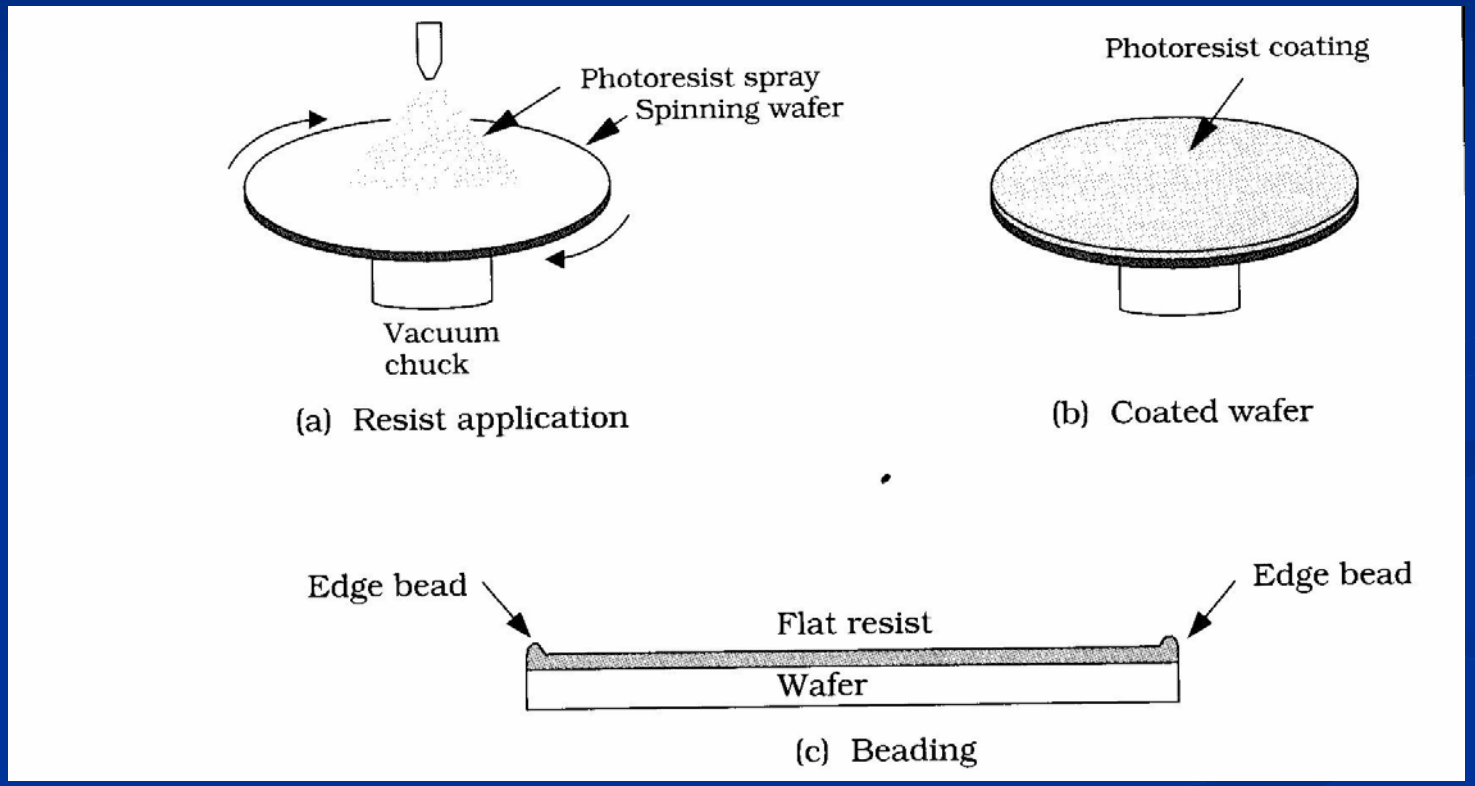


Overview

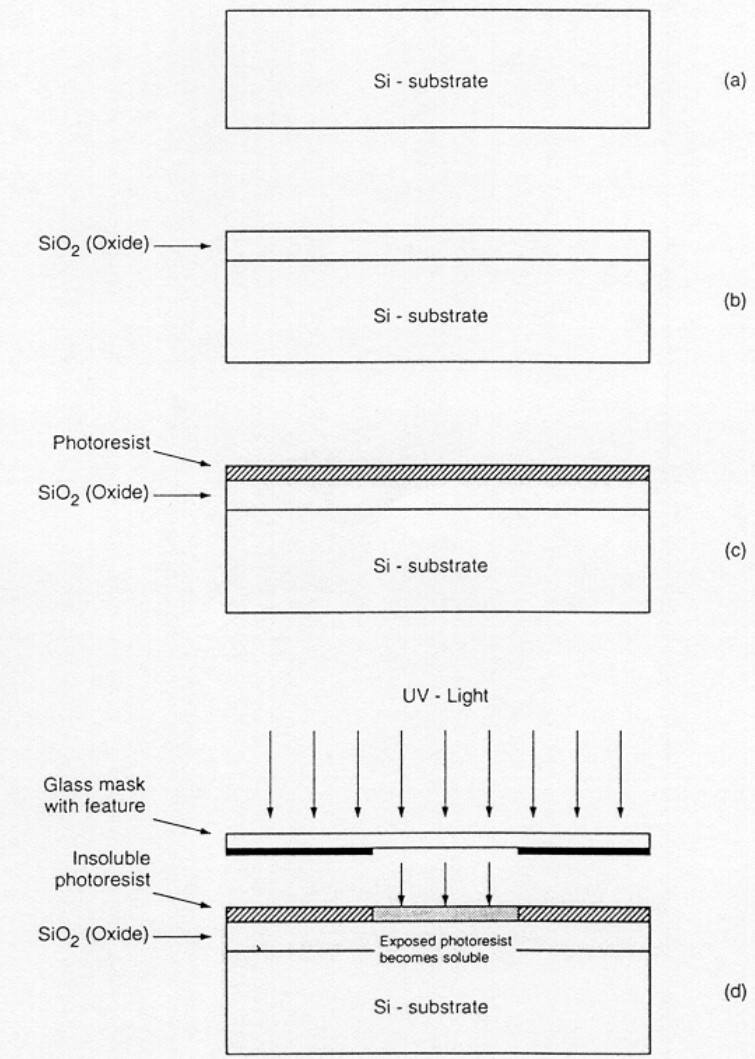

Create n-well regions and channel-stop regions
Grow field oxide and gate oxide (thin oxide)
Deposit and pattern polysilicon layer
Implant source and drain regions, substrate contacts
Create contact windows, deposit and pattern metal layer


7th Masking step
6th Masking step
5th Masking step
4th Masking step
3rd Masking step
2nd Masking step
1st Masking step
WAFER
a)
p- SUBSTRATE
n-WELL
b)

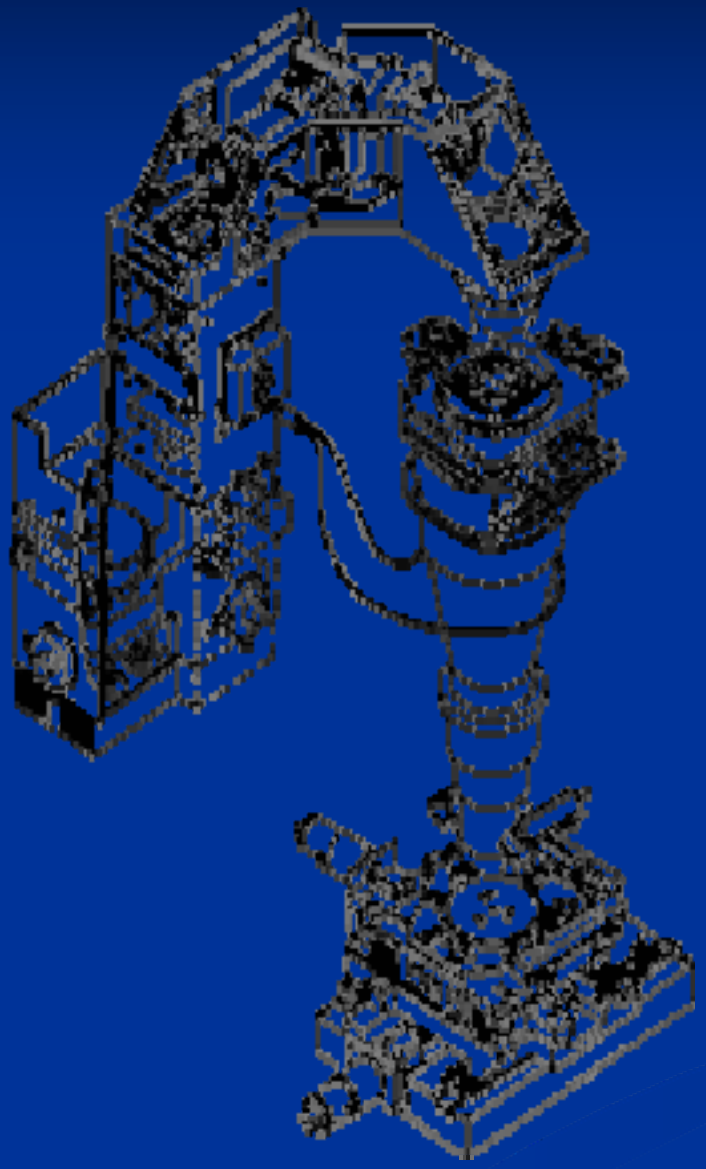
Coating

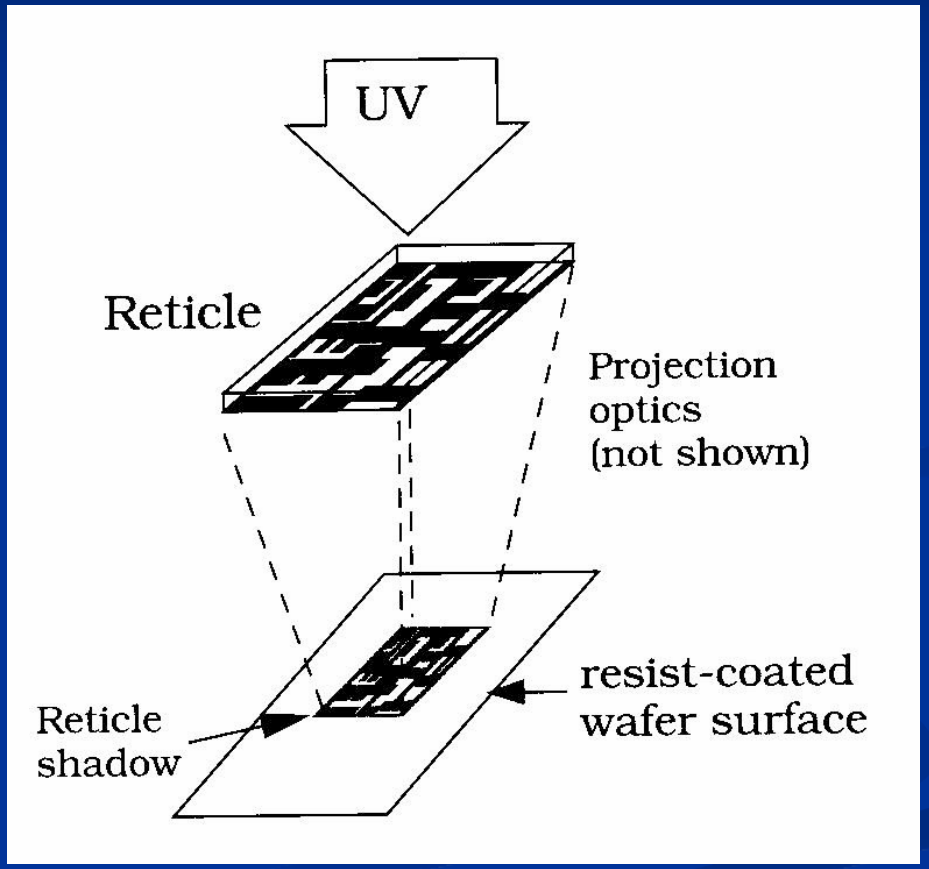

Photoresist spray
Spinning wafer
Vacuum chuck
(a) Resist application
Photoresist coating
(b) Coated wafer
Edge bead
Edge bead
Flat resist
Wafer
(c) Beading

Patterning

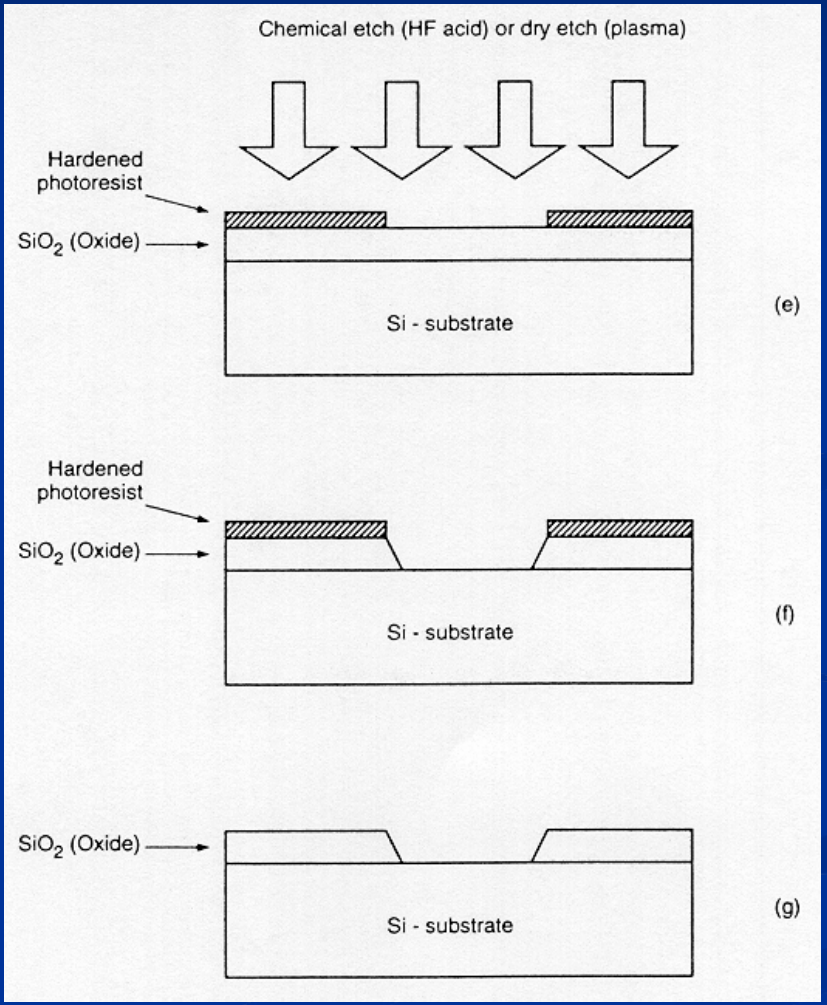

Si - substrate
(a)
SiO_2 (Oxide)
Si - substrate
(b)
Photoresist
SiO_2 (Oxide)
Si - substrate
(c)
UV - Light
Glass mask with feature
Insoluble photoresist
SiO_2 (Oxide)
Exposed photoresist becomes soluble
Si - substrate
(d)

Exposure



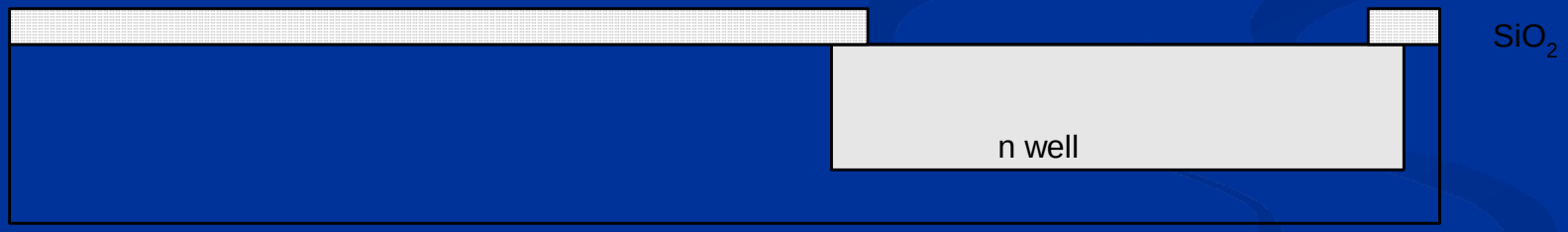

UV
Reticle
Projection
optics
(not shown)
resist-coated
wafer surface
Reticle
shadow

Etching

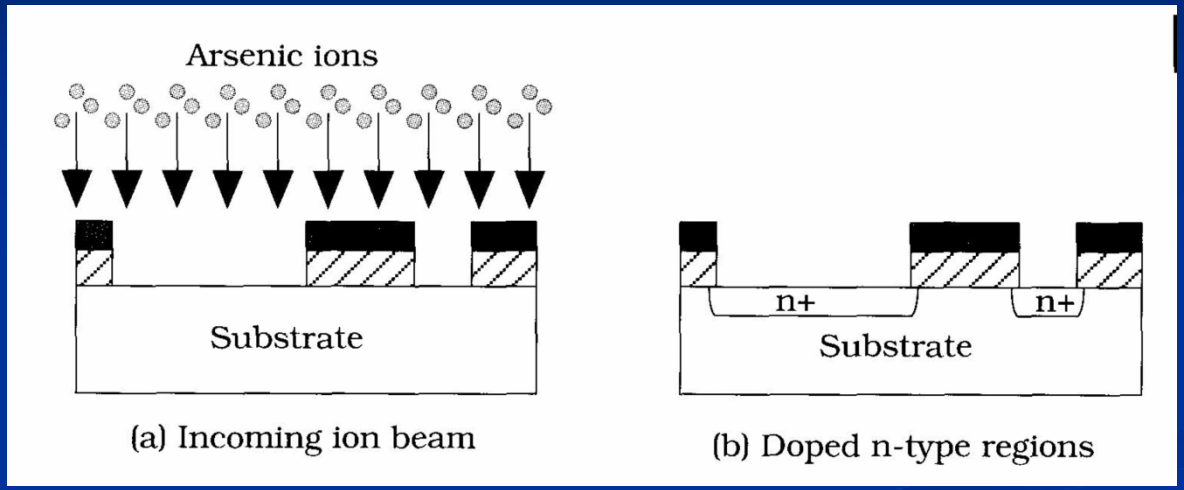

Chemical etch (HF acid) or dry etch (plasma)
Hardened photoresist
SiO_2 (Oxide)
Si - substrate
(e)
Hardened photoresist
SiO_2 (Oxide)
Si - substrate
(f)
SiO_2 (Oxide)
Si - substrate
(g)

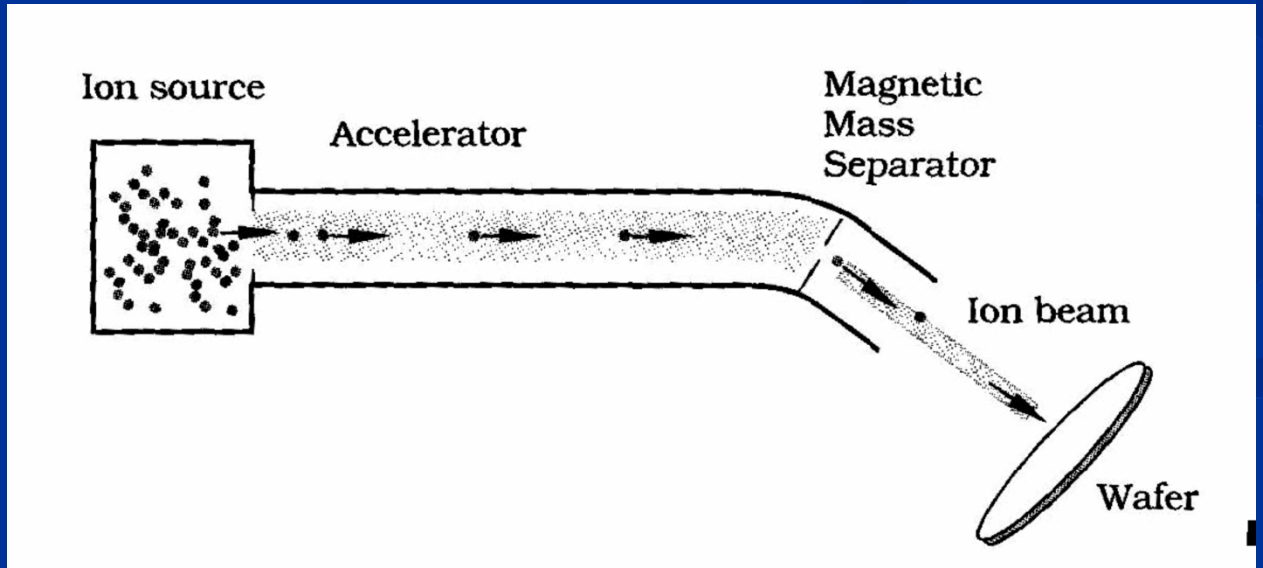
Diffusion

- To create a n well:
  - Diffusion
    - Heat wafer in gas chamber until diffusion occurs.
  - Ion Implantation
    - Arsenic or phosphorous are implanted in window.

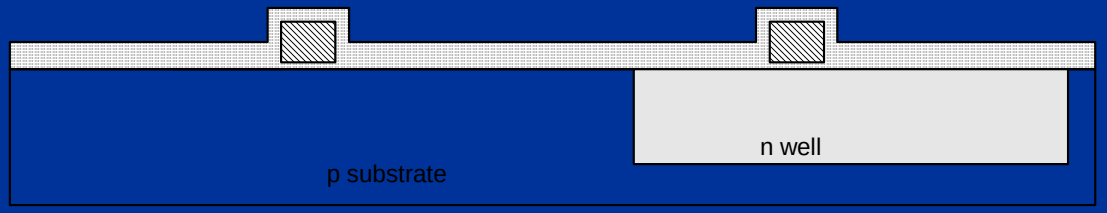


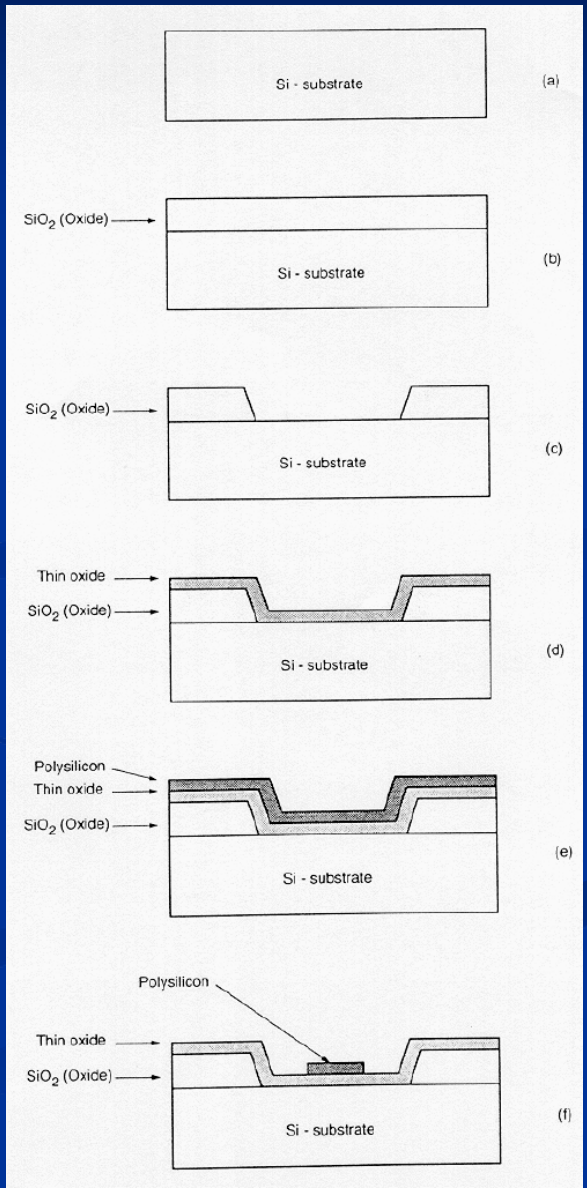
Implantation





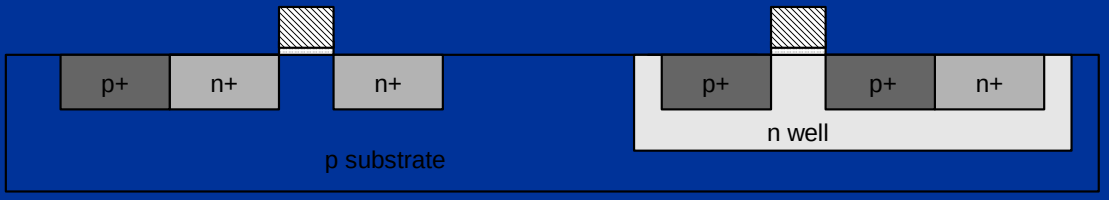
Poly Deposition

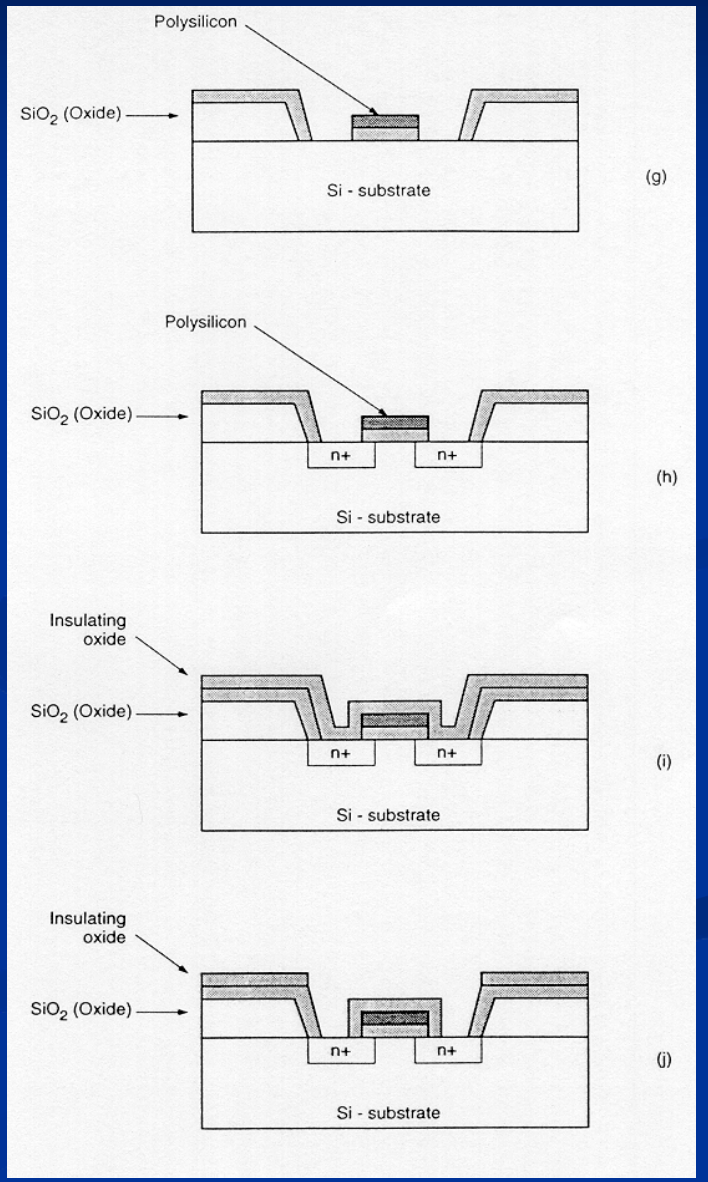




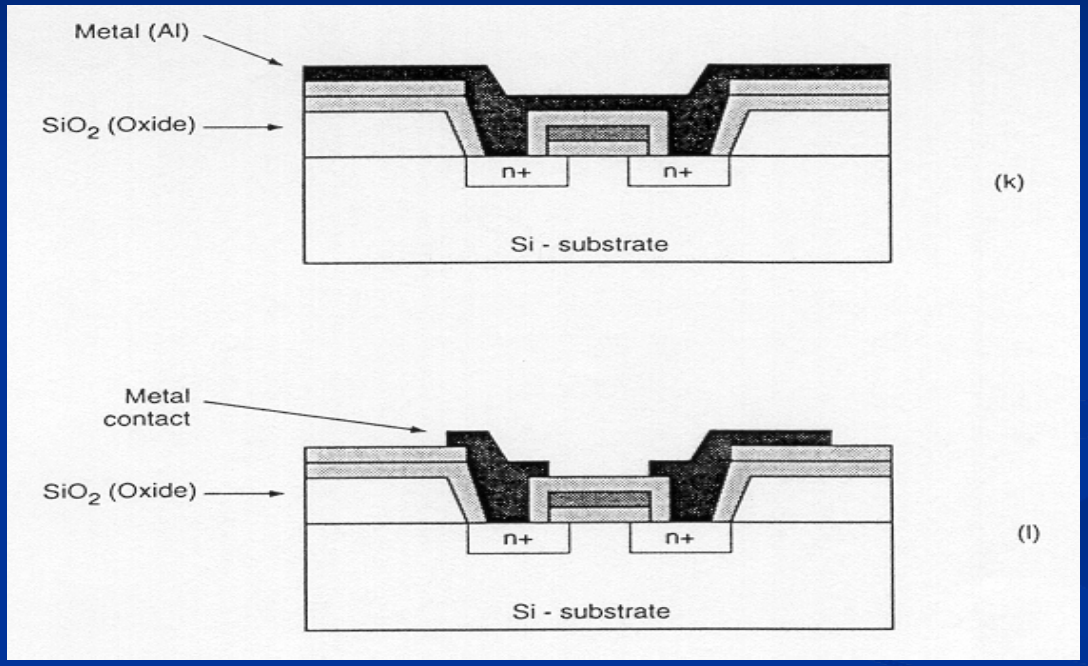
Creating D and S

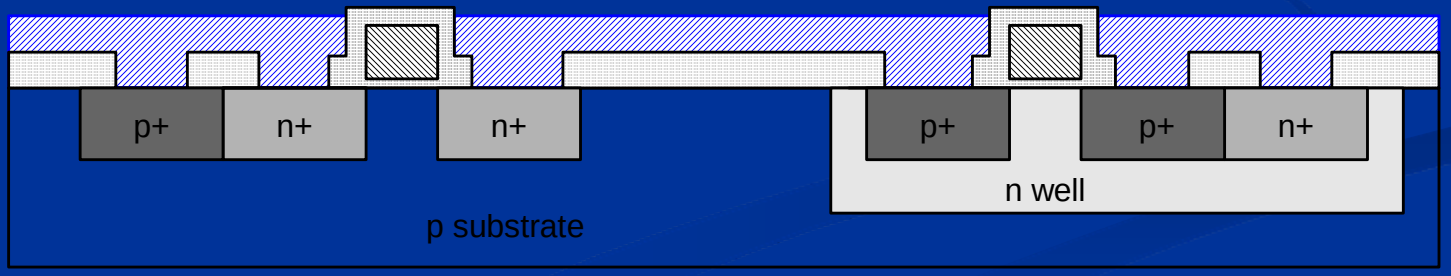
- Remove oxide layer using acid.
- Dope open area using Ion implantation or diffusion.



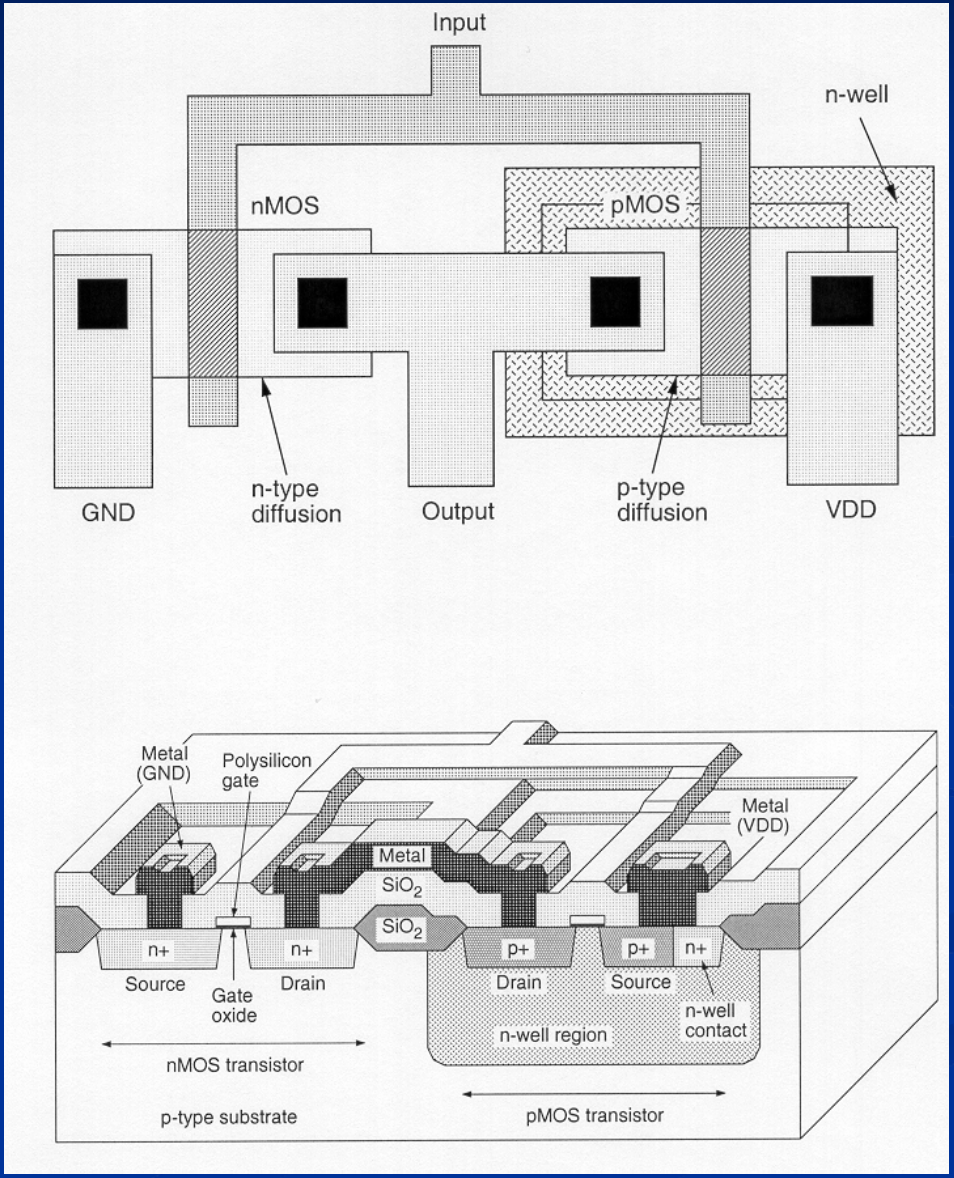


Metal Deposition

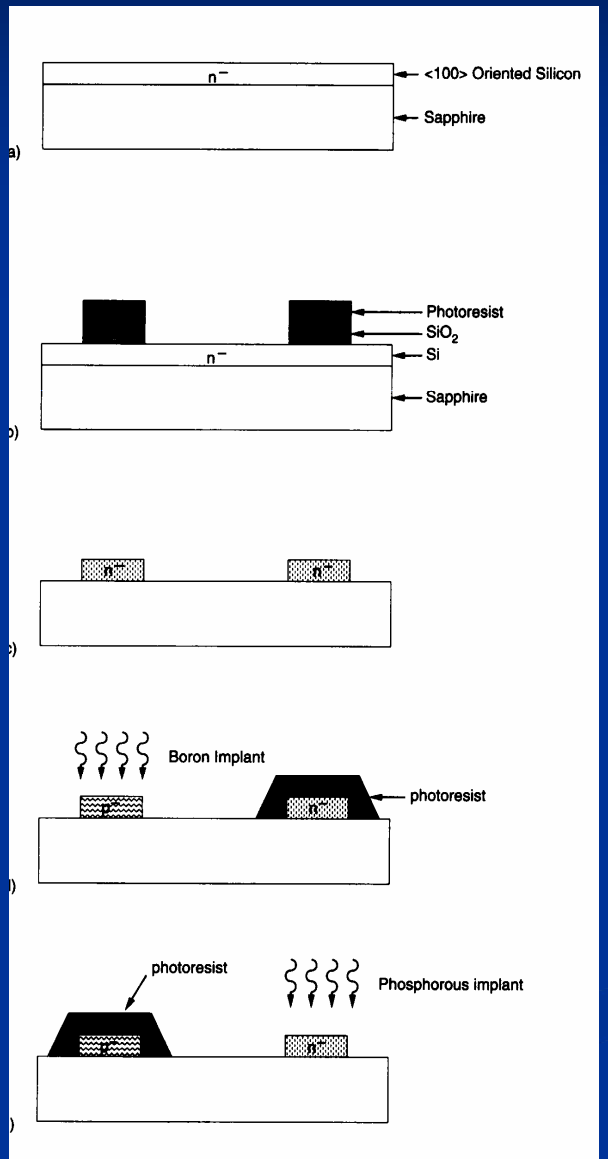


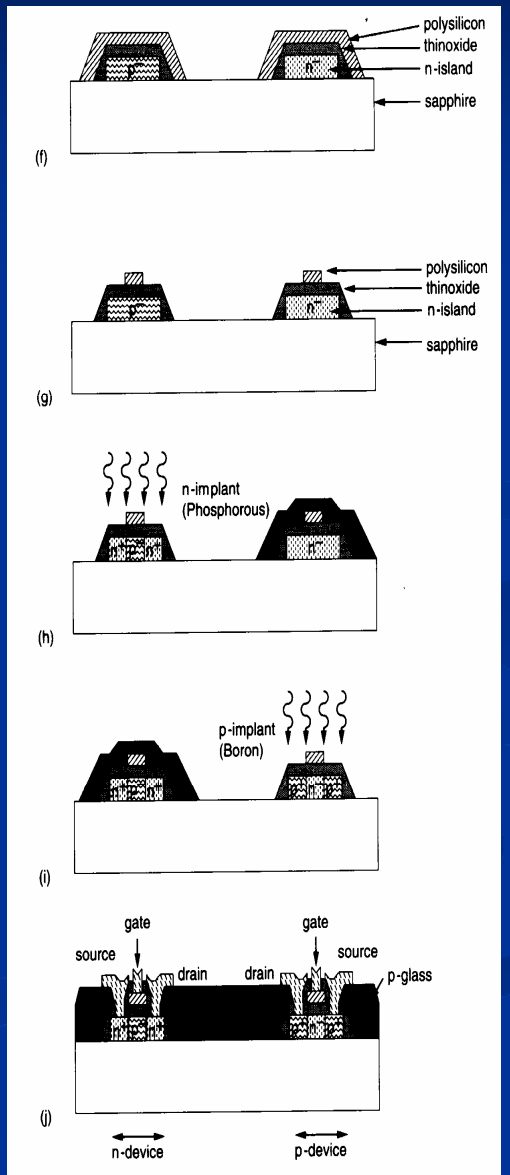


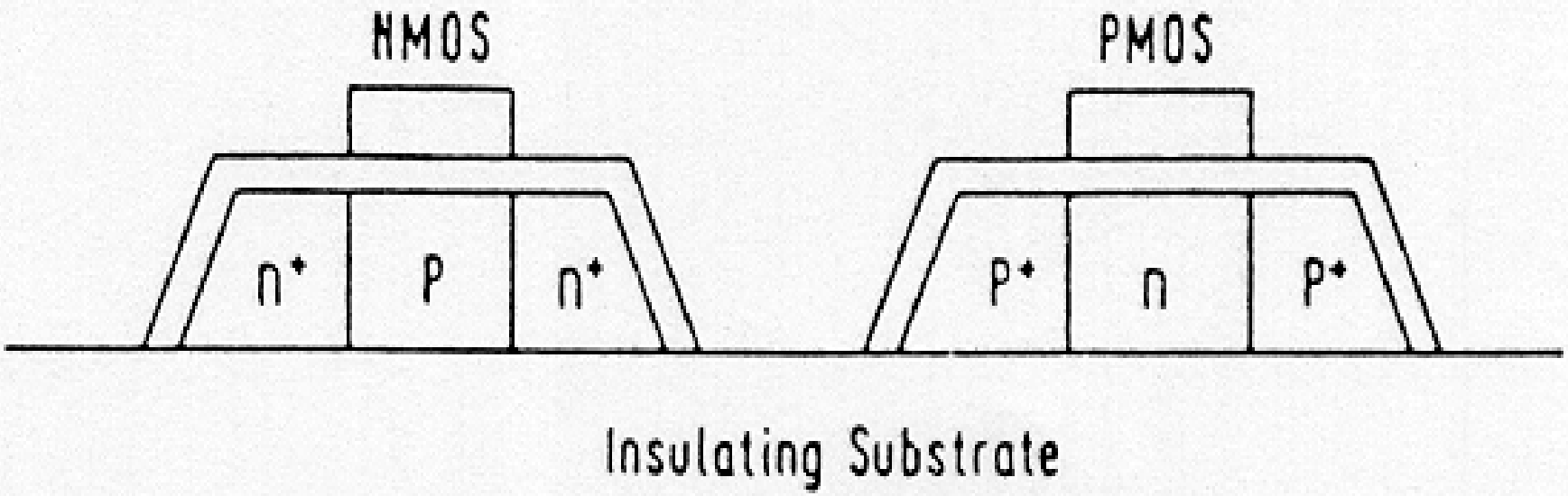
Inverter


Input
n-well
nMOS
pMOS
GND
n-type diffusion
Output
p-type diffusion
VDD
Metal (GND)
Polysilicon gate
Metal (VDD)
Metal
SiO_2
SiO_2
n+
n+
p+
p+
n+
Source
Gate oxide
Drain
Drain
Source
n-well contact
n-well region
nMOS transistor
p-type substrate
pMOS transistor

Silicon on Insulator






NMOS
PMOS
n+
P
n+
P+
n
P+
Insulating Substrate