VLSI Design

Scaling MOS

Figure of Merit

- Minimum feature size
- No. of gates on one chip
- Power dissipation
- Max. operational freq.
- Die Size
- Production cost

Improving FOM

- FOM can be improved by
  - Shrinking the dimensions of transistors
  - Interconnections
  - Separation between features
  - Doping level adjustment
  - Supply voltages

Scaling Model

- Constant dimension model
- Constant Voltage model
- Both varying – voltage and dimension
- Two scaling factors – $1/\alpha$ and $1/\beta$
- $1/\alpha$ for linear dimensions
- $1/\beta$ for supply voltage and oxide thickness

Scaling factors

- Gate Area - A = L.W = 1/α * 1/α
- C_{ox}
- Cg
- Cx
- Channel Density
- Channel Resistance
- Gate Delay

- Max operating frequency
- Eg
- Power dissipation
- Power speed product

Limitations on scaling