Temp 207 **VLSI Architectures**

Mid Semester Examination 2

Spring 2012

Maximum Marks: 50 **Time Allowed: 90 minutes**

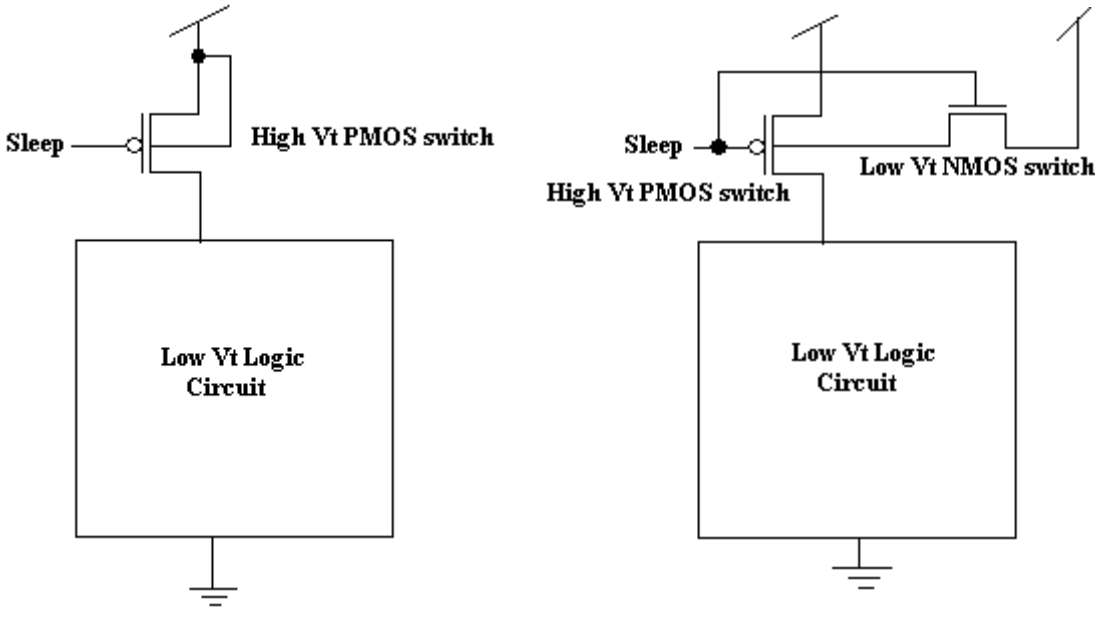
General Instructions:

a. There are **six** questions in this question paper. Attempt **ALL** questions
b. Figures in the right margin indicate marks for each question.
c. Answer in your own words as far as practicable.
d. Reasons are to be stated in support of your answers (except objective type questions). *No credit will be given to answers which are mere assertions*.
e. Use of laptops, mobile phones, pagers or any other electronic devices is strictly prohibited inside the examination hall.
f. Books may be opened at the time of the examination.
g. If any assumption is made at any step they have to be clearly stated.

::::::::BEST OF LUCK::::::::

1. Design a 2X2 CAM cell with NOR based architecture using dual threshold CMOS technology and explain how it leads to power-performance optimization of the circuit. 6+4= 10

2. Consider the circuit architectures shown in figure 1 (a) and figure 1(b).



(a) (b)

Figure 1

The two designs depict the typical architectures for power gating of digital VLSI circuits. In either of the two designs the PMOS transistor has its source connected to the supply voltage Vdd. In figure 1(b), the drain terminal of the NMOS transistor is connected to a reference voltage Vr such that $V_r > V_{dd} + V_{tn}$. Explain which one of the two designs will you prefer and why? 8

3. Consider a conventional 6T SRAM cell. The data stored in the SRAM cell is most vulnerable to external noise due to the direct access of the data storage nodes by the access transistors connected to the complementary bit lines. During a read operation, the voltage division between the access transistors and cross coupled inverters fluctuate the storage node voltage, resulting in destructive read operation. Suggest an alternate design of the SRAM that completely isolates the bit lines during the read operation and hence increases the read static noise margin. 10

4. Design an 8 bit two complement generator circuit using not more than six half adders, not more than six inverters and a NOR gate and a XOR gate. Show by intuitive reasons that the two's complement generator proposed in this problem outperforms a conventional two complement generator circuit. 8+4=12

5. A cell library based design style consists of a six transistor cell as shown in the figure 2:

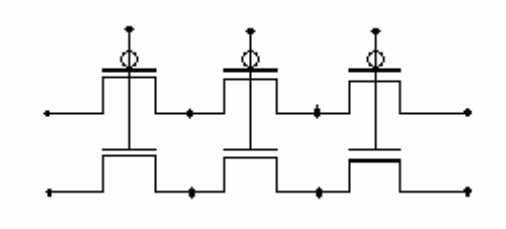


Figure 2

The black dots in the figure indicate the possible contact points. Indicate the necessary connections to transform the cell into a (i) three input CMOS NAND gate and (ii) three input CMOS NOR gate showing the points of application of VDD and the GND. 3+3=6

6. A designer is required to design an 8-bit unsigned parallel adder chip. It is also instructed to him that the sum of the 8-bit vector inputs will always be less than 255. Accordingly, the designer designed the adder with no carry output pins. A day before he is required to submit his design, his design manager instructed him that there should be a provision for carry output in the adder. Suggest a suitable methodology; he can take to finish up his design in a day's time without disturbing the original design. 4