Read Only Memory Architecture

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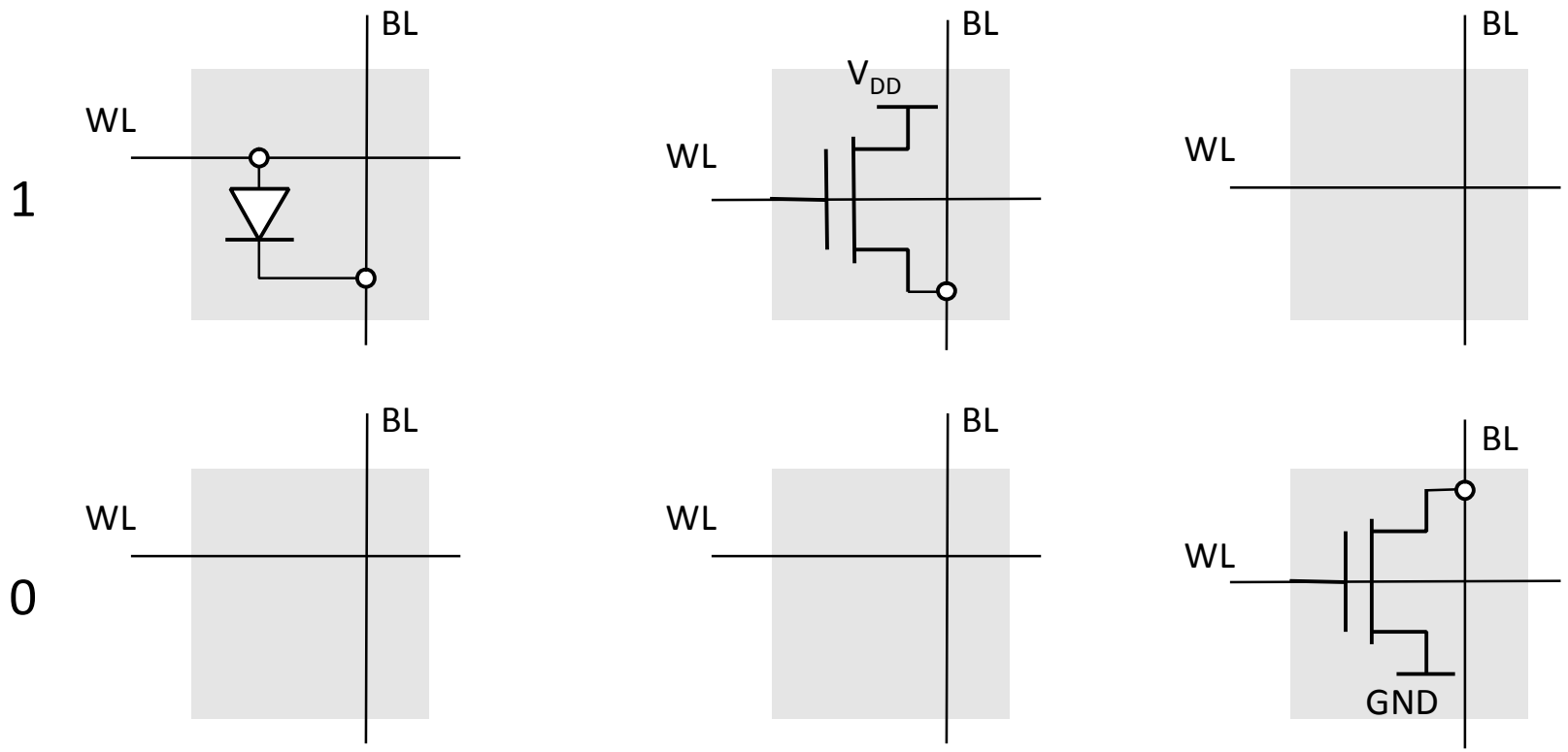
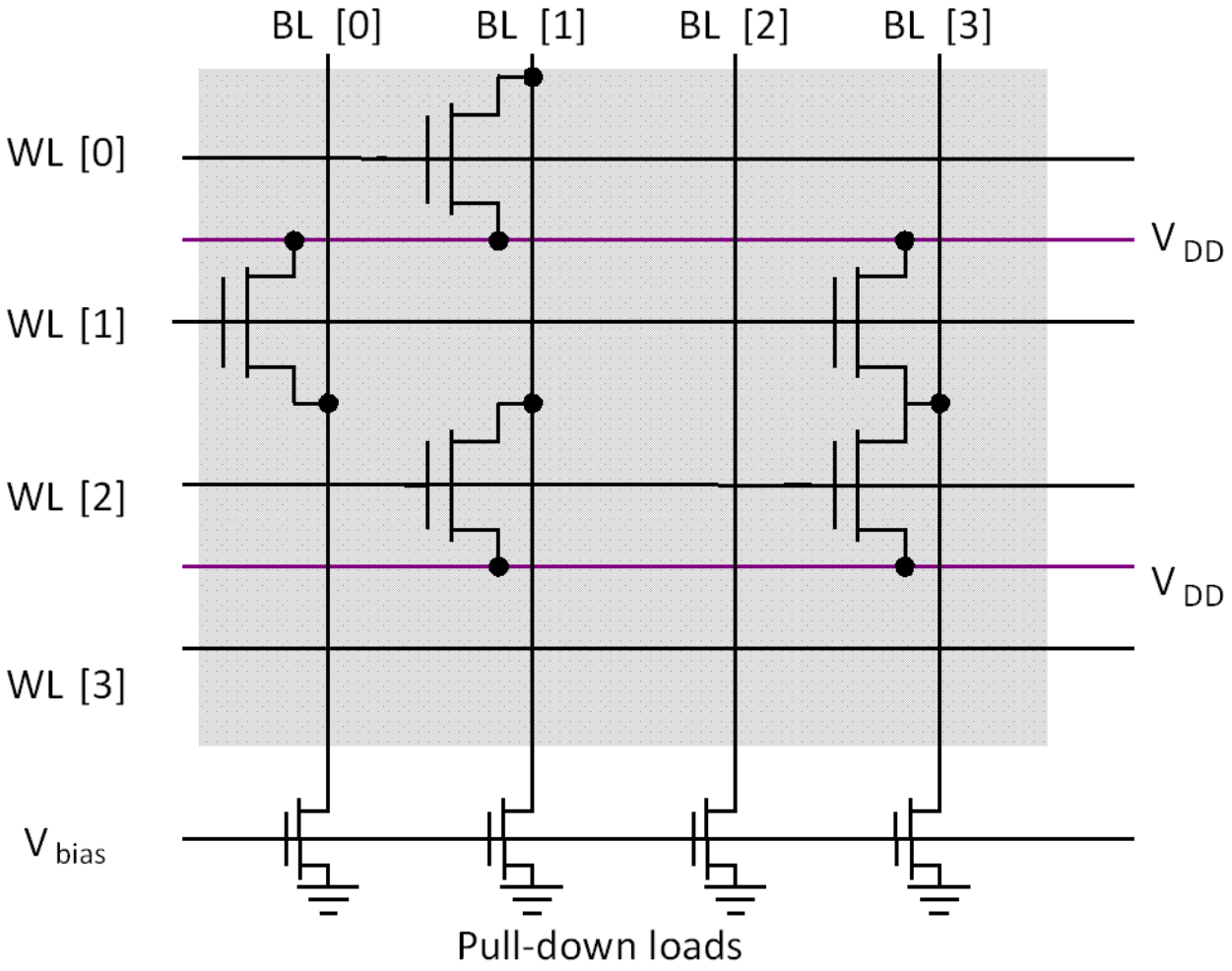
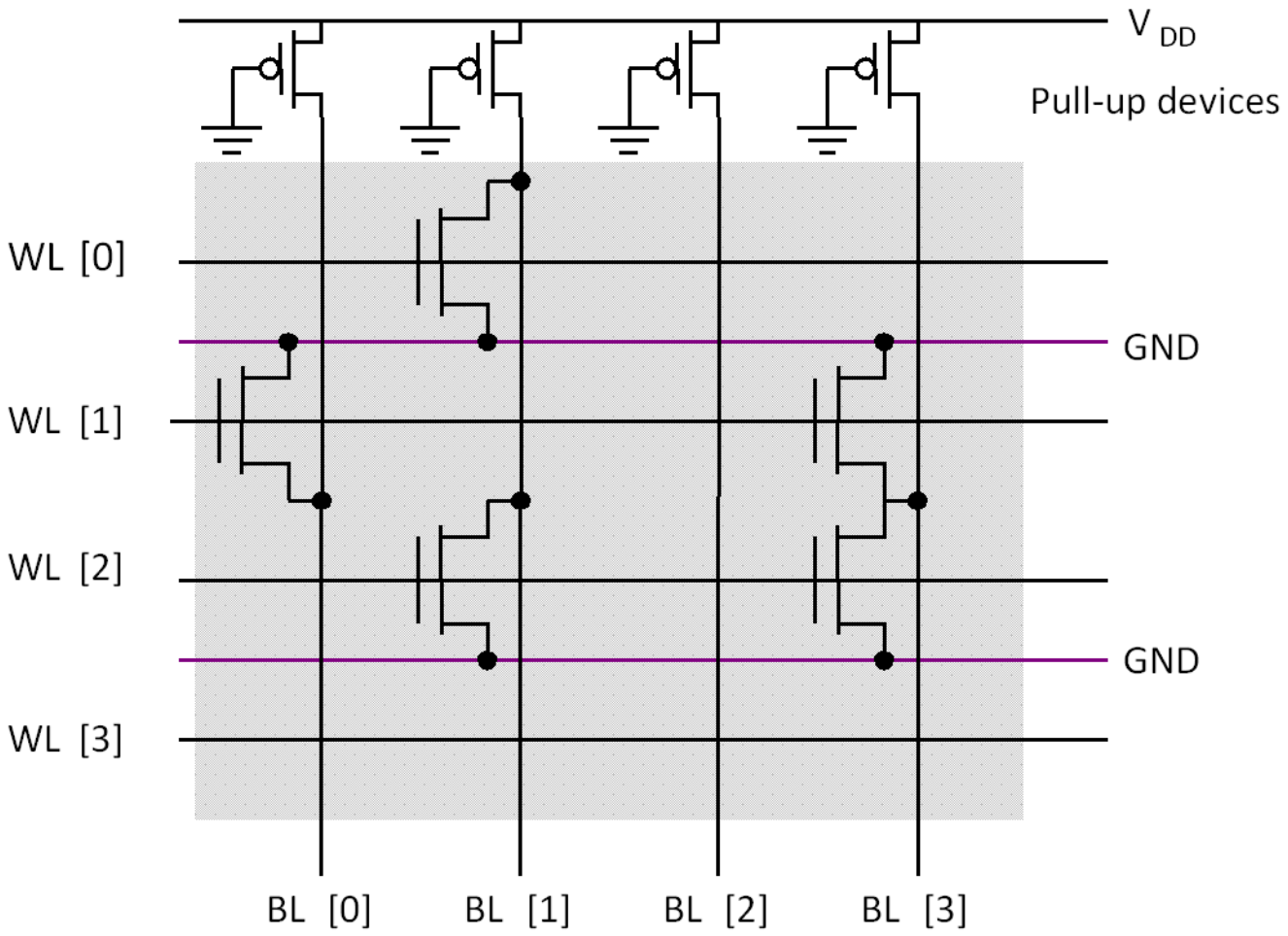
Read-Only Memory Cells



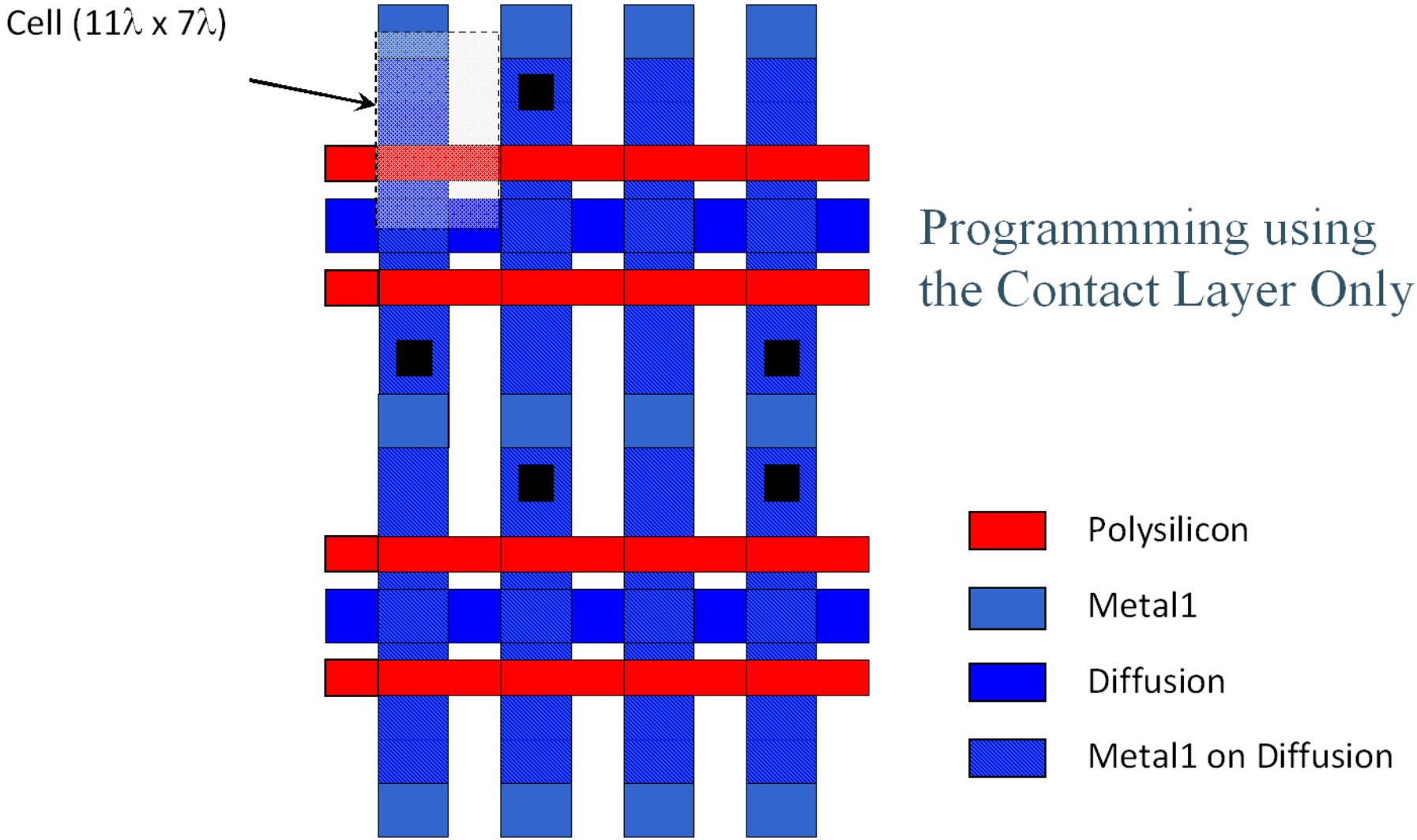
MOS OR ROM



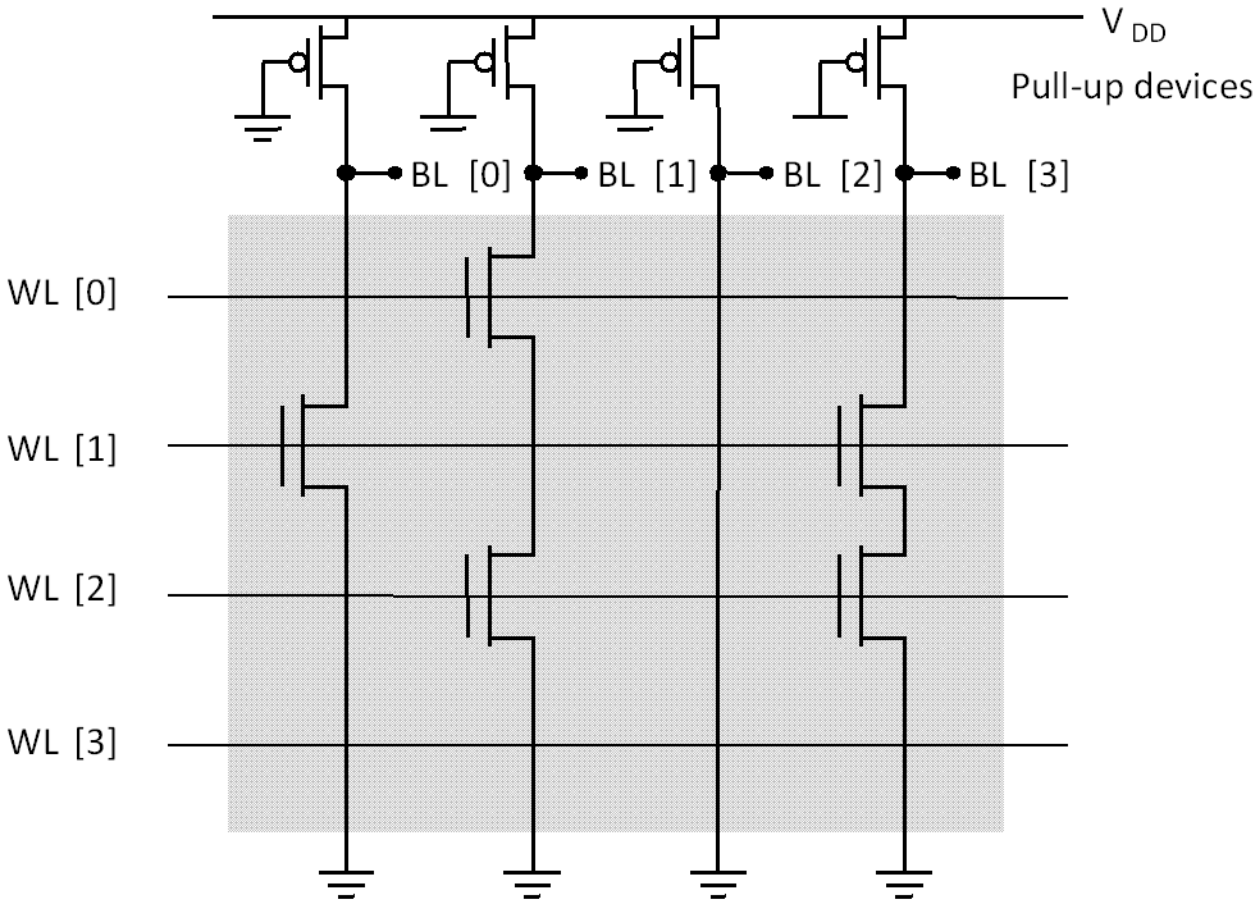
MOS NOR ROM



MOS NOR ROM Layout

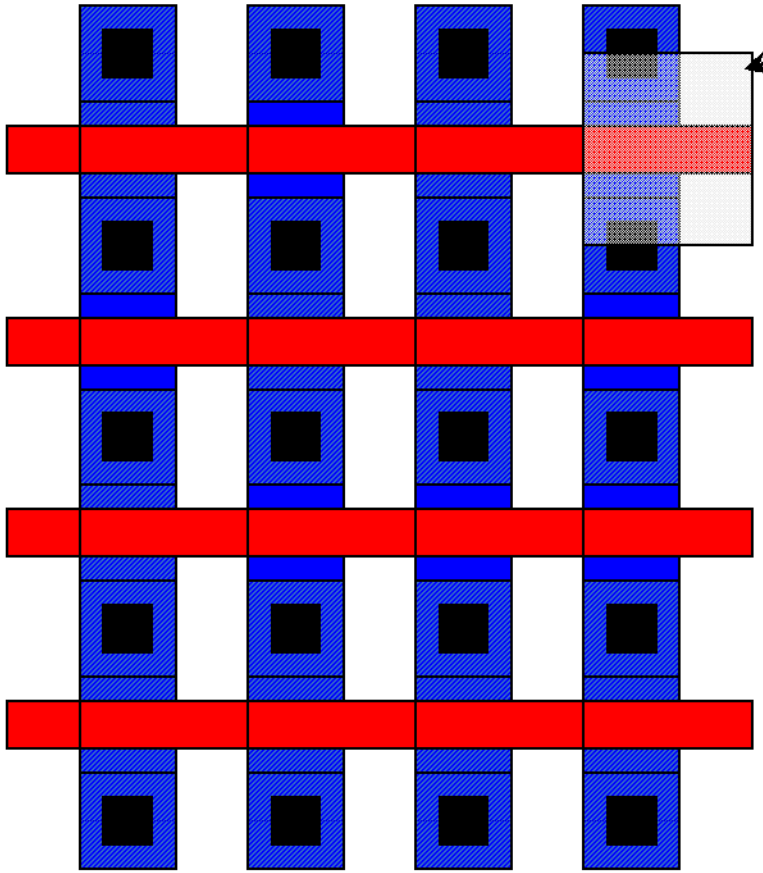


MOS NAND ROM



All word lines high by default with exception of selected row

MOS NAND ROM Layout



Programmming using
the Metal-1 Layer Only

No contact to VDD or GND necessary;
drastically reduced cell size
Loss in performance compared to NOR ROM

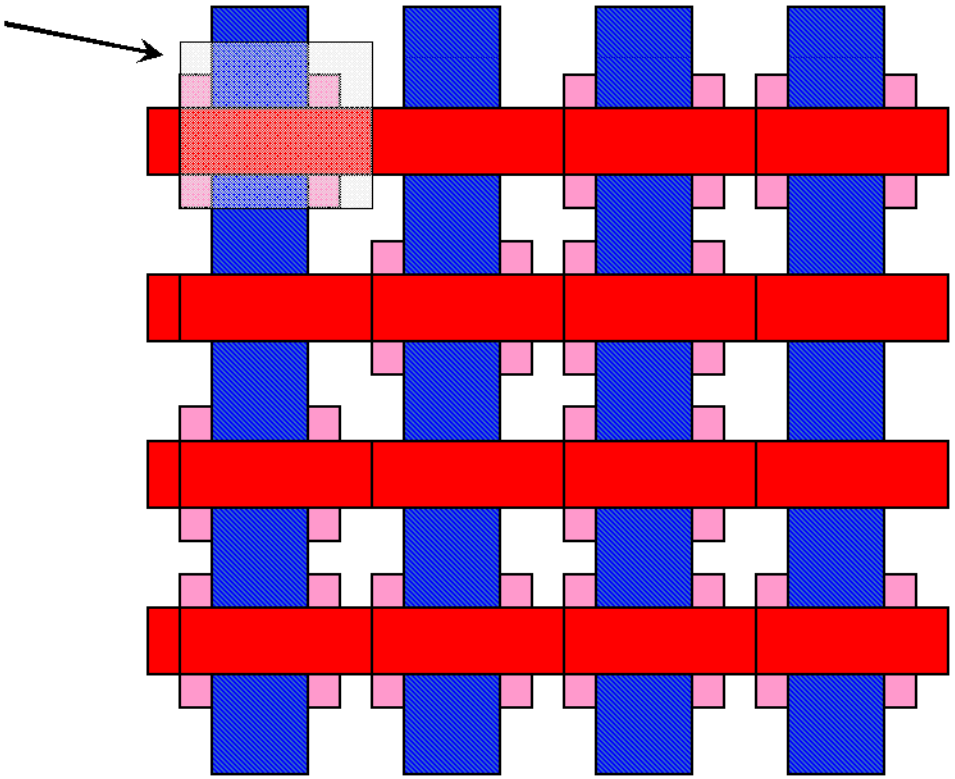
Polysilicon

Diffusion

Metal1 on Diffusion

NAND ROM Layout

Cell (5λ x 6λ)



Programmming using Implants Only

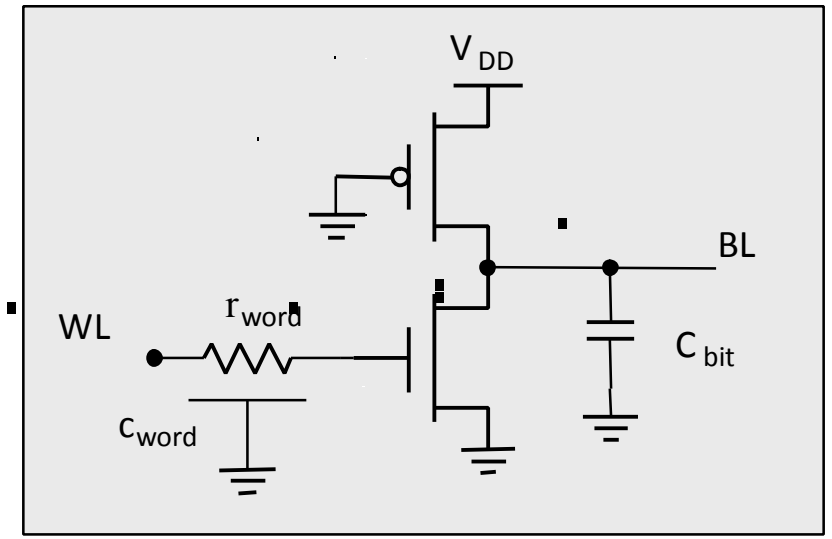
Polysilicon

Threshold-altering implant

Metal1 on Diffusion

Equivalent Transient Model for MOS NOR ROM

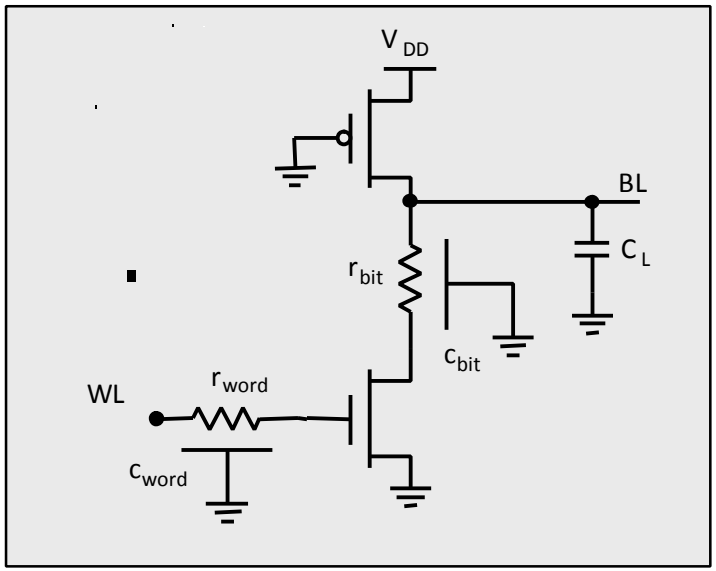
Model for NOR ROM



- Word line parasitics
  - Wire capacitance and gate capacitance
  - Wire resistance (polysilicon)
- Bit line parasitics
  - Resistance not dominant (metal)
  - Drain and Gate-Drain capacitance

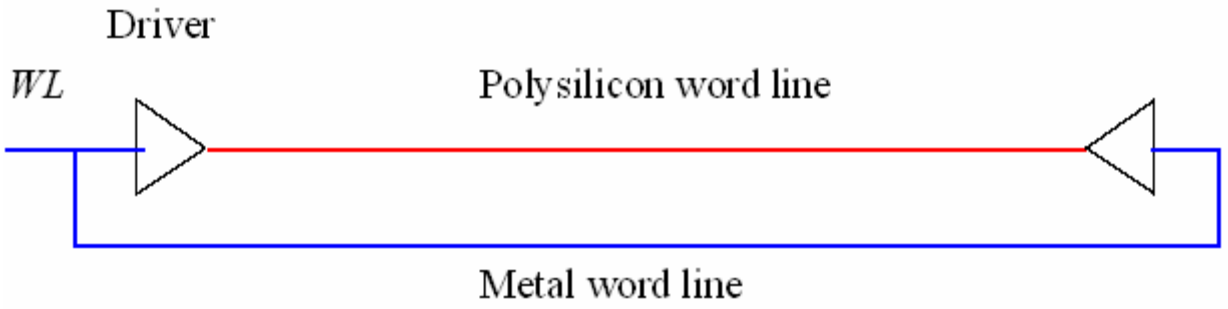
Equivalent Transient Model for MOS NAND ROM

Model for NAND ROM

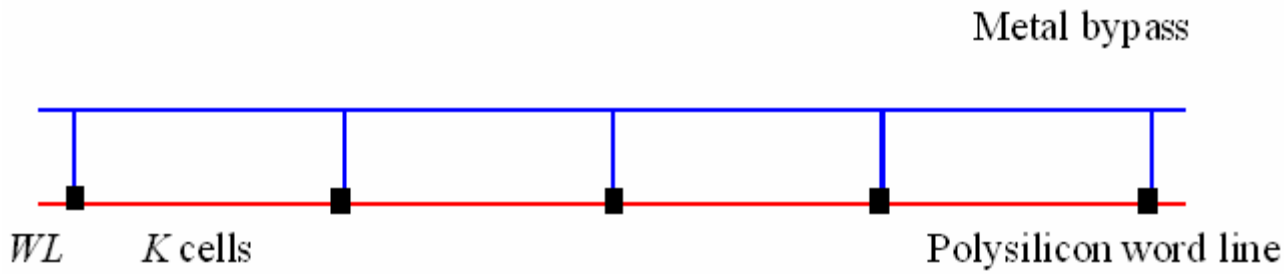


- Word line parasitics
  - Similar to NOR ROM
- Bit line parasitics
  - Resistance of cascaded transistors dominates
  - Drain/Source and complete gate capacitance

Decreasing Word Line Delay



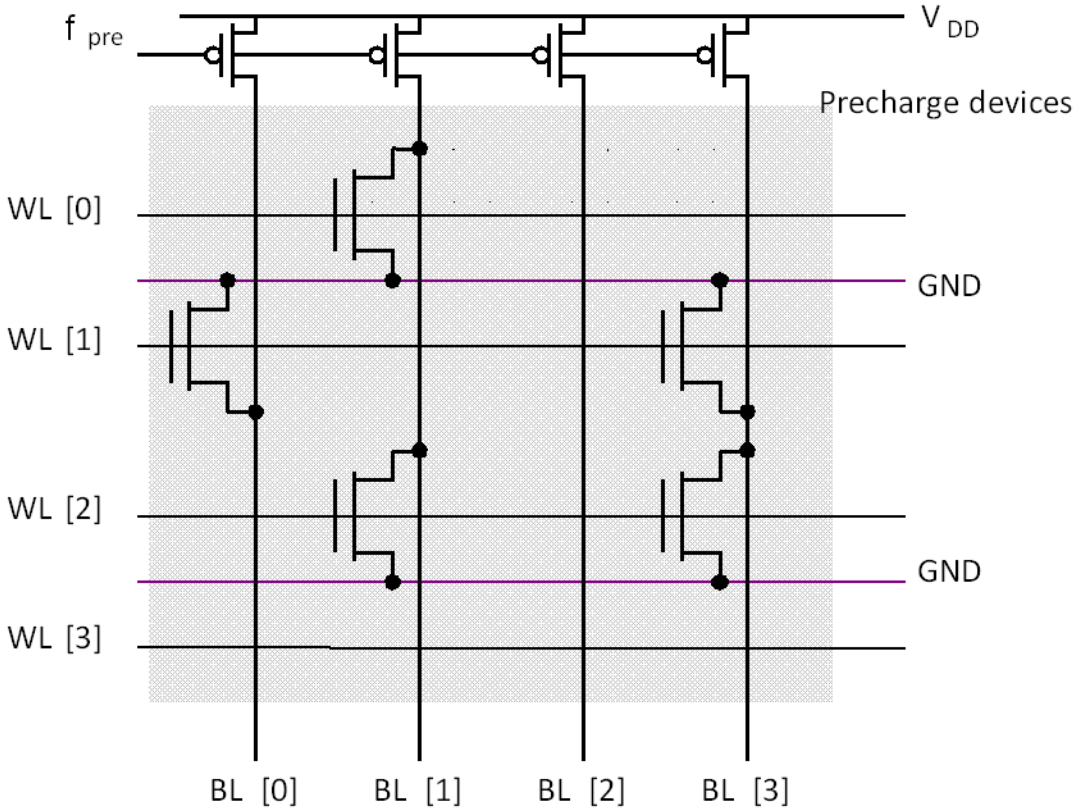
(a) Driving the word line from both sides



(b) Using a metal bypass

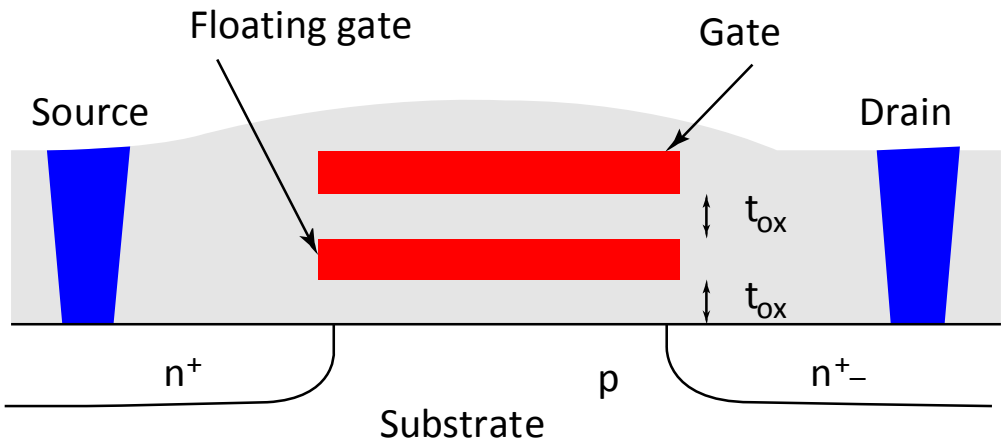
(c) Use silicides

Precharged MOS NOR ROM

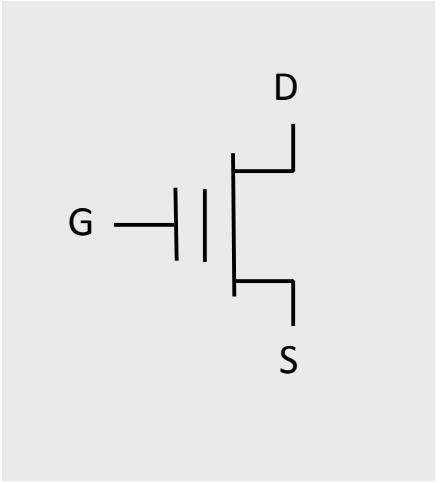


PMOS precharge device can be made as large as necessary, but clock driver becomes harder to design.

Non-Volatile Memories
The Floating-gate transistor (FAMOS)

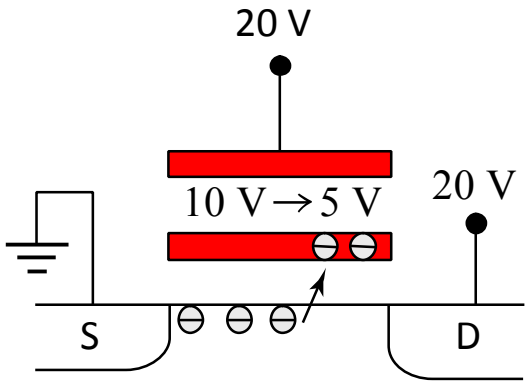


Device cross-section

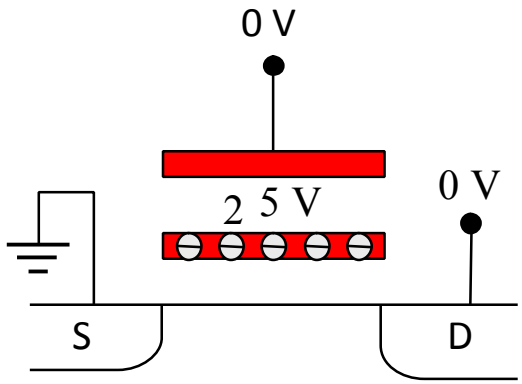


Schematic symbol

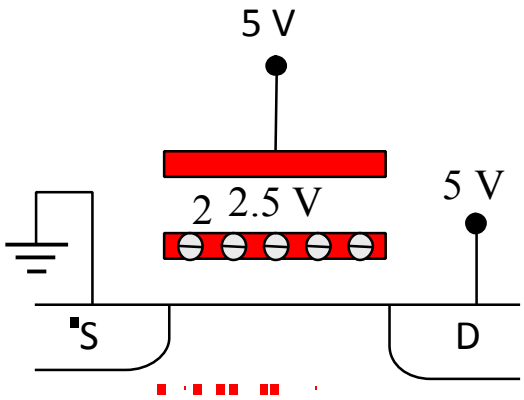
Floating-Gate Transistor Programming



Avalanche injection

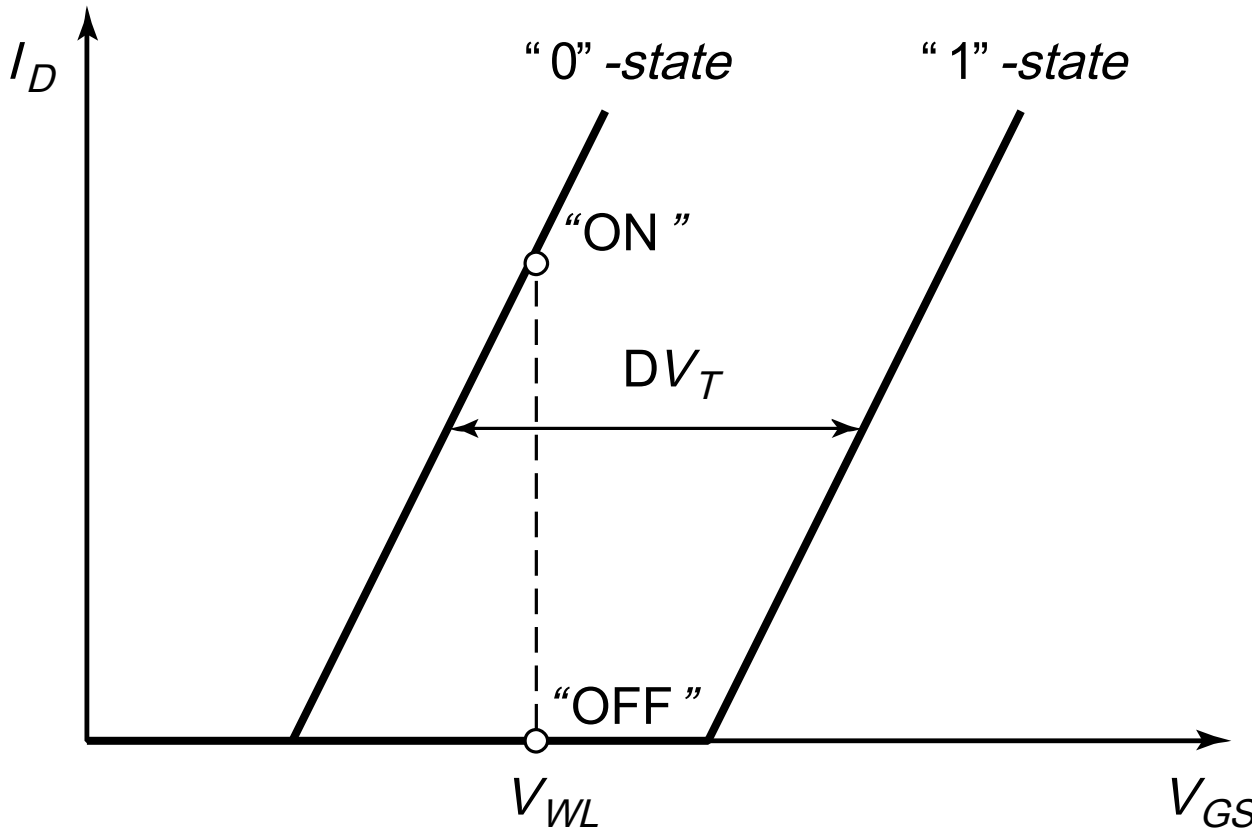


Removing programming voltage leaves charge trapped

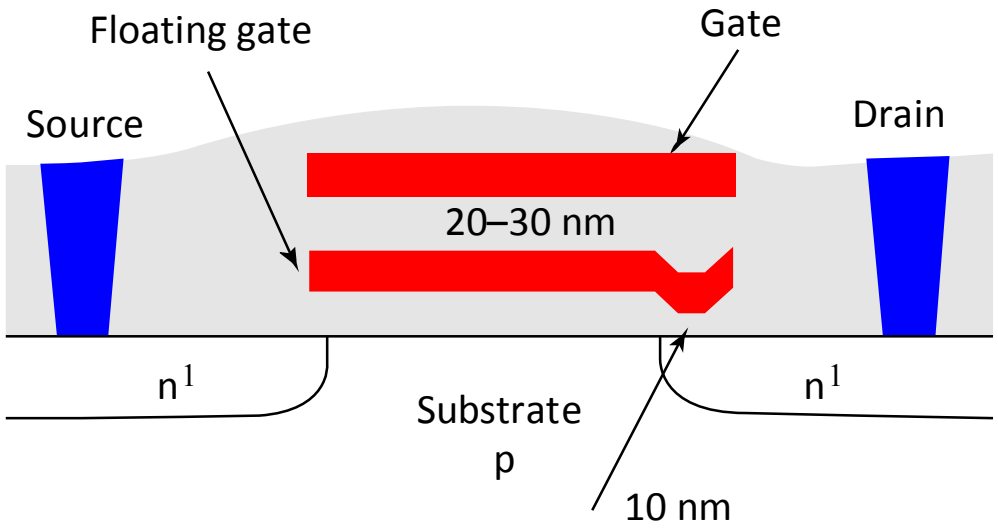


Programming results in higher V_T.

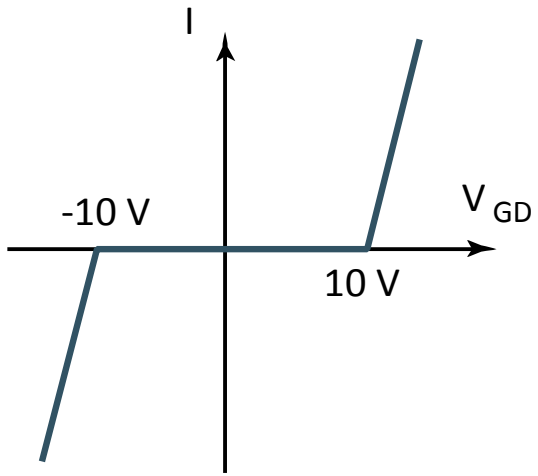
A “Programmable-Threshold” Transistor



FLOTOX EEPROM

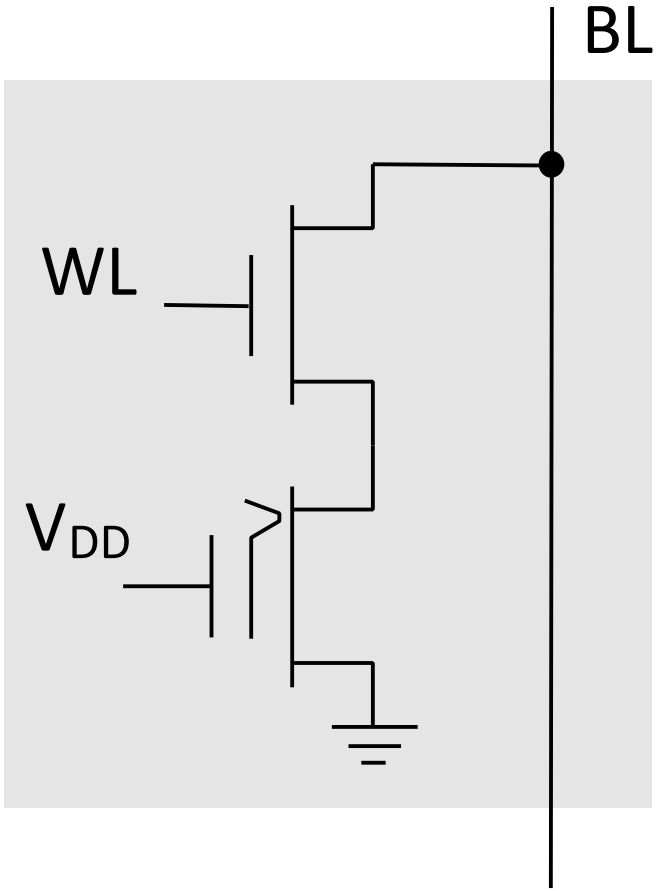


FLOTOX transistor



Fowler-Nordheim
I-V characteristic

EEPROM Cell

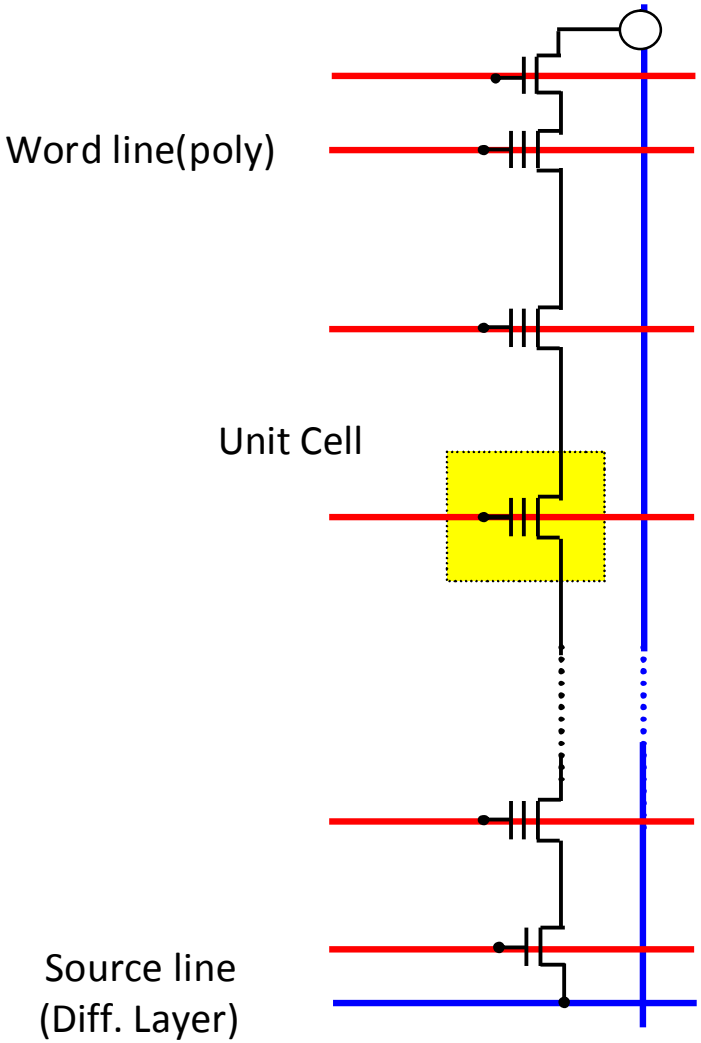


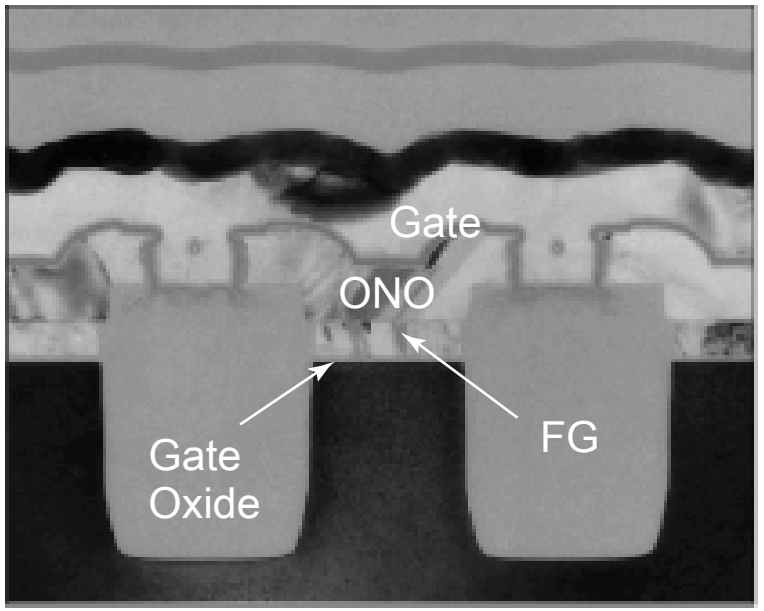
Absolute threshold control is hard

Unprogrammed transistor might be depletion

⇨ 2 transistor cell

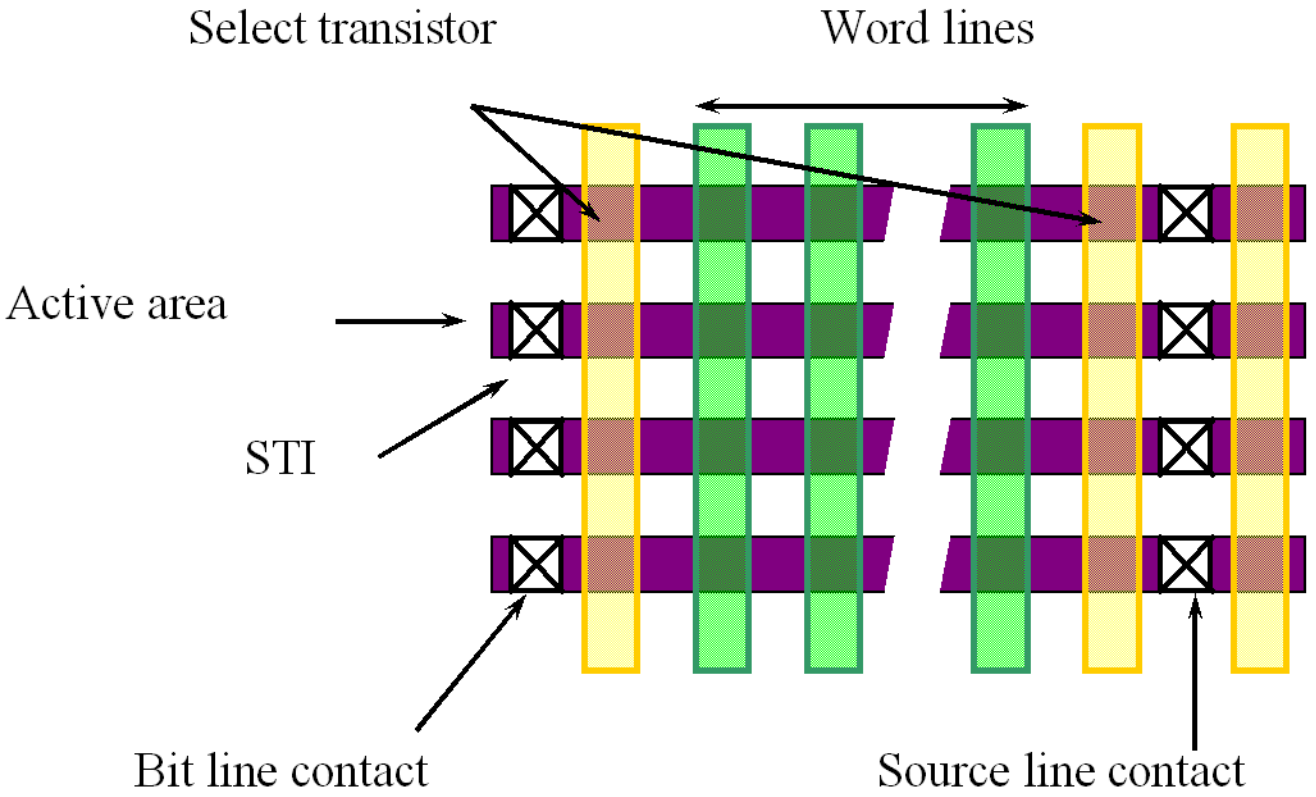
NAND Flash Memory





Courtesy Toshiba

NAND Flash Memory



Courtesy Toshiba

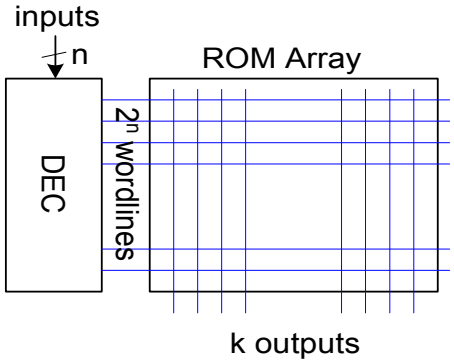
Characteristics of State-of-the-art NVM

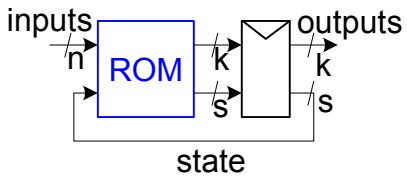
Table 12-1 Comparison between nonvolatile memories ([Itoh01]).
V_{DD} = 3.3 or 5 V; V_{PP} = 12 or 12.5 V.

	Cell—Nr. of Transistors	Cell Area (ratio wrt EPROM)	Mechanism		External Power Supply		Program/ Erase Cycles
			Erase	Write	Write	Read	
MASK ROM	1 T (NAND)	0.35–5	—	—	—	V_{DD}	0
EPROM	1 T	1	UV Exposure	Hot electrons	V_{PP}	V_{DD}	~100
EEPROM	2 T	3–5	FN Tunneling	FN Tunneling	V_{PP} (int)	V_{DD}	10^4–10^5
Flash Memory	1 T	1–2	FN Tunneling	Hot electrons	V_{PP}	V_{DD}	10^4–10^5
			FN Tunneling	FN Tunneling	V_{PP} (int)	V_{DD}	10^4–10^5

Building Logic with ROMs

- Use ROM as lookup table containing truth table
  - n inputs, k outputs requires 2^n words x k bits
  - Changing function is easy – reprogram ROM
- Finite State Machine
  - n inputs, k outputs, s bits of state
  - Build with 2^{n+s} x (k+s) bit ROM and (k+s) bit register





THANK YOU