DESIGN FOR TESTABILITY

Assignment-5

1. Consider the linear decompressor circuit in figure 1. Find the linear equations for the decompressor. Calculate the characteristic matrix A of the sequential linear decompressor such that $AX = Z$

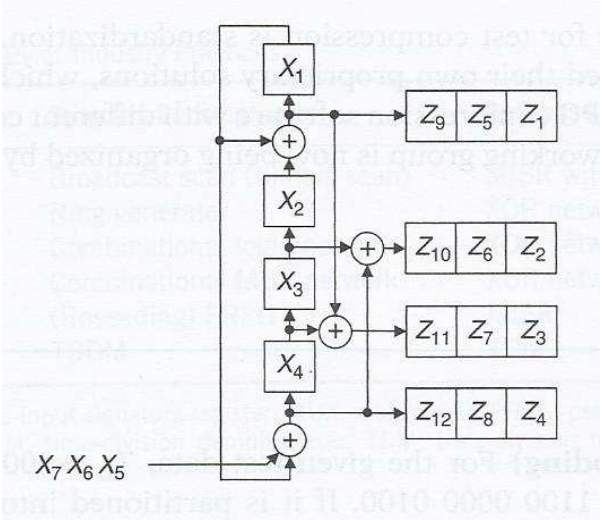

Figure 1

2. Consider the sequential decompressor circuit shown in figure 2. Evaluate the circuit and find out the set of linear equations. Find the compressed stimulus needed to encode the following test cube: $\langle Z_1, Z_2, ...Z_{12} \rangle = \langle 0---1-0--110 \rangle$

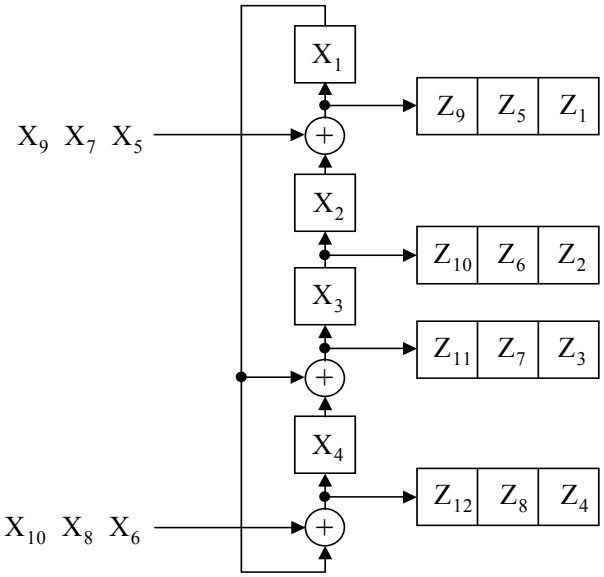

Figure 2

3. Consider the system with n cores $c_1, c_2, ...c_n$ as shown in figure 3. For each core the following are given:

$sc_i \rightarrow$ the number of scan chains

$ff_{ij} \rightarrow$ the number of flip flops in scan chain j

$wi_i \rightarrow$ the number of input wrapper cells

$wo_i \rightarrow$ the number of output wrapper cells

$nff_i = \sum_{j=1}^{sc_i} f_{ij} \rightarrow$ the total number of flip flops

$TS_i = (tS_{i1}, tS_{i2}, ..., tS_{il}) \rightarrow$ a sequence of l patterns, where tS_{ik} consists of $nff_i + wi_i$ and each bit can be 0,1 or x

$ER_i = (er_{i1}, er_{i2}, ..., er_{il}) \rightarrow$ a sequence of l patterns, where er_{ik} consists of $nff_i + wo_i$ and each bit can be 0,1 or x

$M_i = (m_{i1}, m_{i2}, ..., m_{il}) \rightarrow$ a sequence of l patterns, where m_{ik} consists of $nff_i + wo_i$ and each bit can be 0 or 1

$T_i = \{TS_i, ER_i, M_i\} \rightarrow$ initially given dedicated test consisting of TS_i, ER_i and a test mask M_i A l indicates that the corresponding bit in the PR is a care bit and should be checked with the ER otherwise it is a don't-care bit and should be masked. Also given for the system is the number of test access mechanism (TAM) wires, W_{TAM}.

For the automatic test equipment (ATE) the following is given:

$M_{ATE} \rightarrow$ the number of bits that can be stored in the ATE memory

$f_{ATE} \rightarrow$ the clock frequency of the ATE

The *share* and *compress* functions take two tests and one test respectively as input and generate a new test that is added to the list of alternative tests. This process of generating alternative tests is explained using two initially given dedicated tests $T1$ and $T2$. Table 1 shows how these two tests are used to generate new alternative tests. Column one lists the alternative tests and column two and three list which core(s) is tested by each test (marked as X in the table).

Select one test alternative for core c_i. Determine the architecture (the TAM wire usage) and the start time t_i such that the test application time (TAT) is minimized without exceeding the memory constraint M_{ATE}.

Table 1. Test alternatives per core

Alternative test	Core c_1	Core c_2	*Note*
TA_1	X		*Initially given*
TA_2		X	*Initially given*
TA_3	X		*compress(T_1)*
TA_4		X	*compress(T_2)*
TA_5	X	X	*share(T_1, T_2)*
TA_6	X	X	*compress(share(T_1, T_2))*

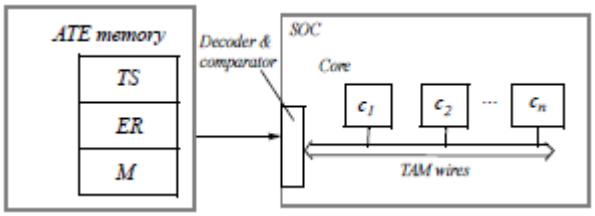

Figure 3

4. For the X-compact matrix of the compactor shown below, design the corresponding X-compactor. What errors can the X-compactor detect?

$$\begin{bmatrix} 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 \end{bmatrix}$$