Random Access Scan Design

Dr. Shubhajit Roy Chowdhury,

Centre for VLSI and Embedded Systems Technology,

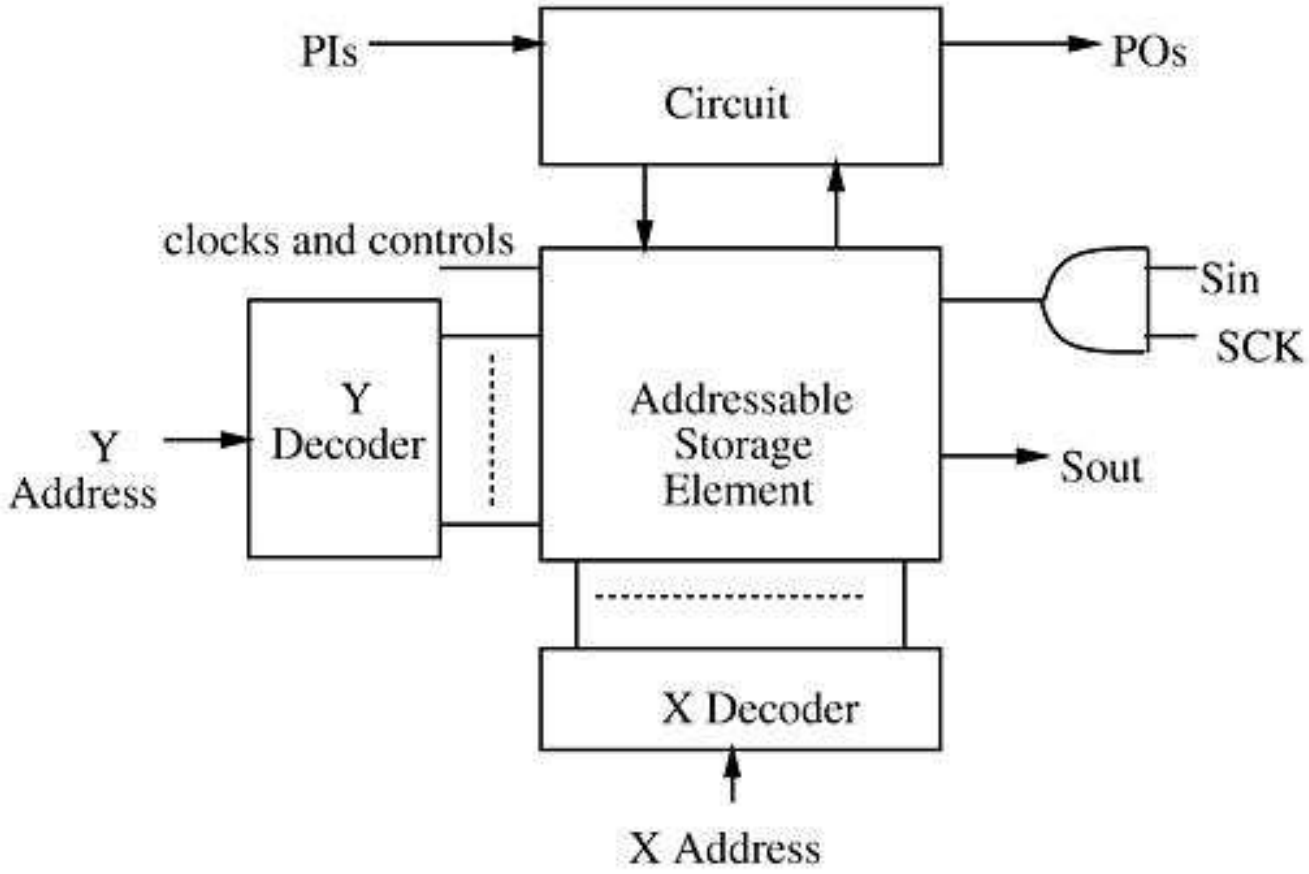
IIIT Hyderabad, India

Email: src.vlsi@iiit.ac.in

Random-Access Scan Design

- Eliminate problems in serial scan mode
  - Excessive dynamic power during capture
  - difficult fault diagnosis
- Scan cell randomly and uniquely addressable
  - Similar to storage cell in random-access memory (RAM)
- Impacts
  - Low shift power dissipation with an increase in routing overhead
  - Combinational logic diagnosis techniques for locating faults

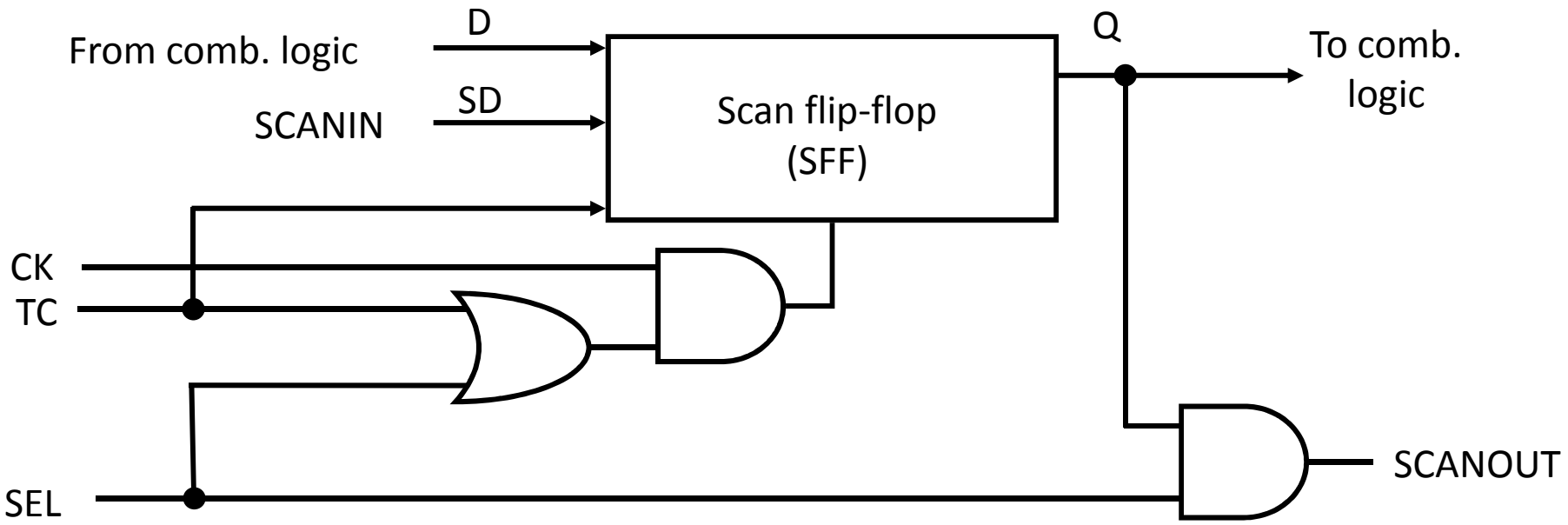
Random-Access Scan (RAS)



Random Access Scan

- Treat each one of the latch elements as a bit in memory
- Each bit in the memory has its own unique address, and it has a port which can load data into the latches so that the contents of the latch can be observed
- There is only one scan-in and one scan-out
- Addressing scheme which allows each latch to be uniquely selected, so that it can be either controlled or observed.
- Normal operation
  - Scan clock is off
- Only one latch receives the scan clock and that value is loaded into the latch.

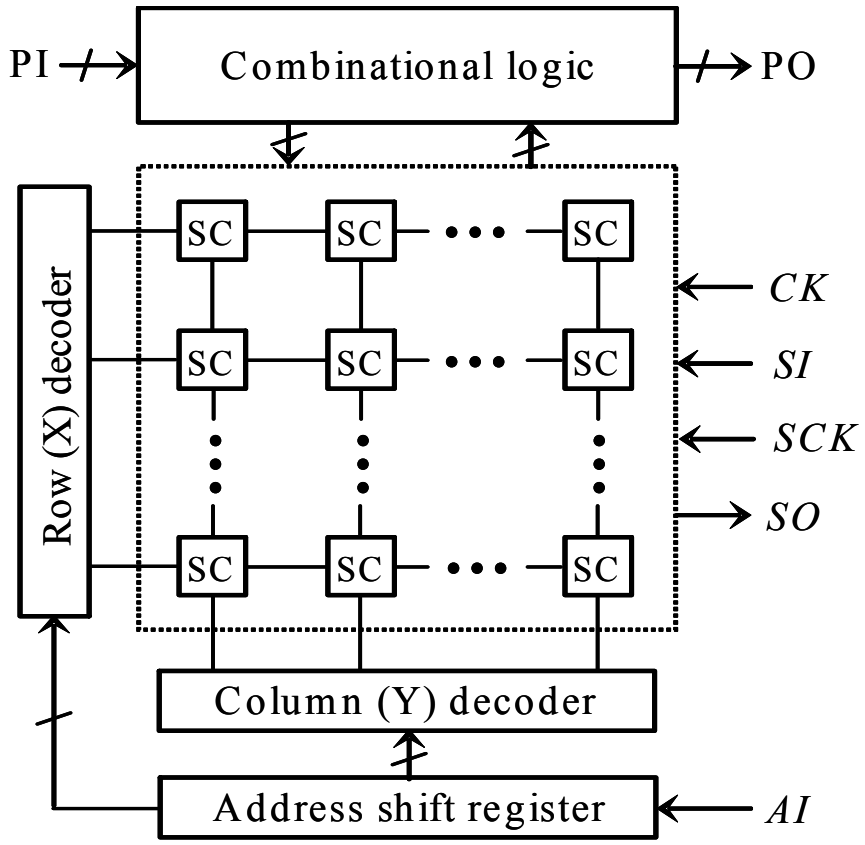
RAS Flip-Flop (RAM Cell)



Random-Access Scan Architectures

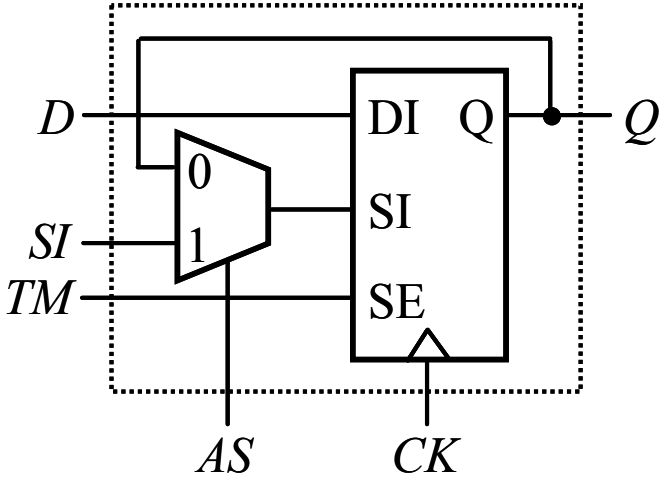
- Traditional Random-Access Scan (RAS) Architecture
  - All scan cells are organized into a two-dimensional array
  - Advantage
    - Can reduce shift power dissipation
  - Disadvantages
    - No guarantee to reduce test application time or test data volume
    - High area overhead
- Progressive Random-Access Scan Design (PRAS)
  - Use a structure similar to SRAM or a grid-addressable latch
- Shift-Addressable Random-Access Scan Design (STAR)

Traditional RAS Architecture



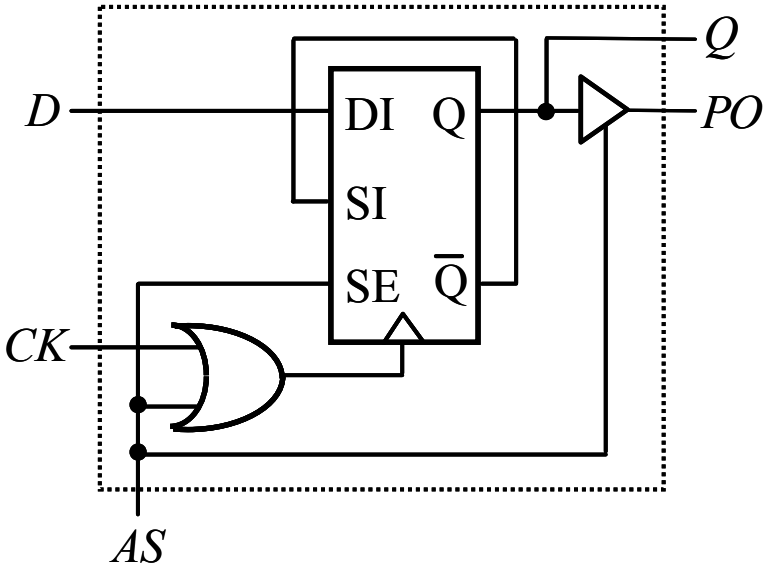
Access to a scan cell by decoding a full address with a row decoder (X) and a column decoder (Y)

Traditional RAS Scan Cell



Traditional Scan Cell Design

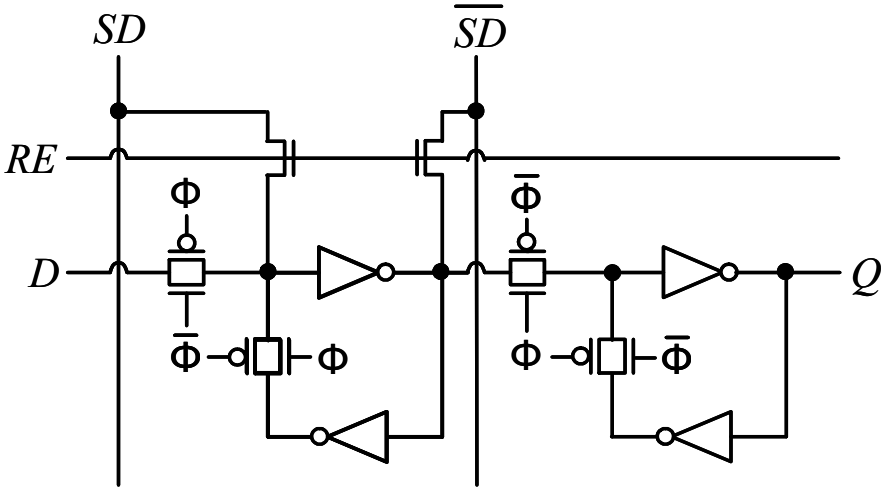
Broadcast the external SI port to all scan cells, cause routing problem



Toggle Scan Cell Design

Require a clear mechanism to reset all scan cells prior to testing

PRAS Design



PRAS Scan Cell Design

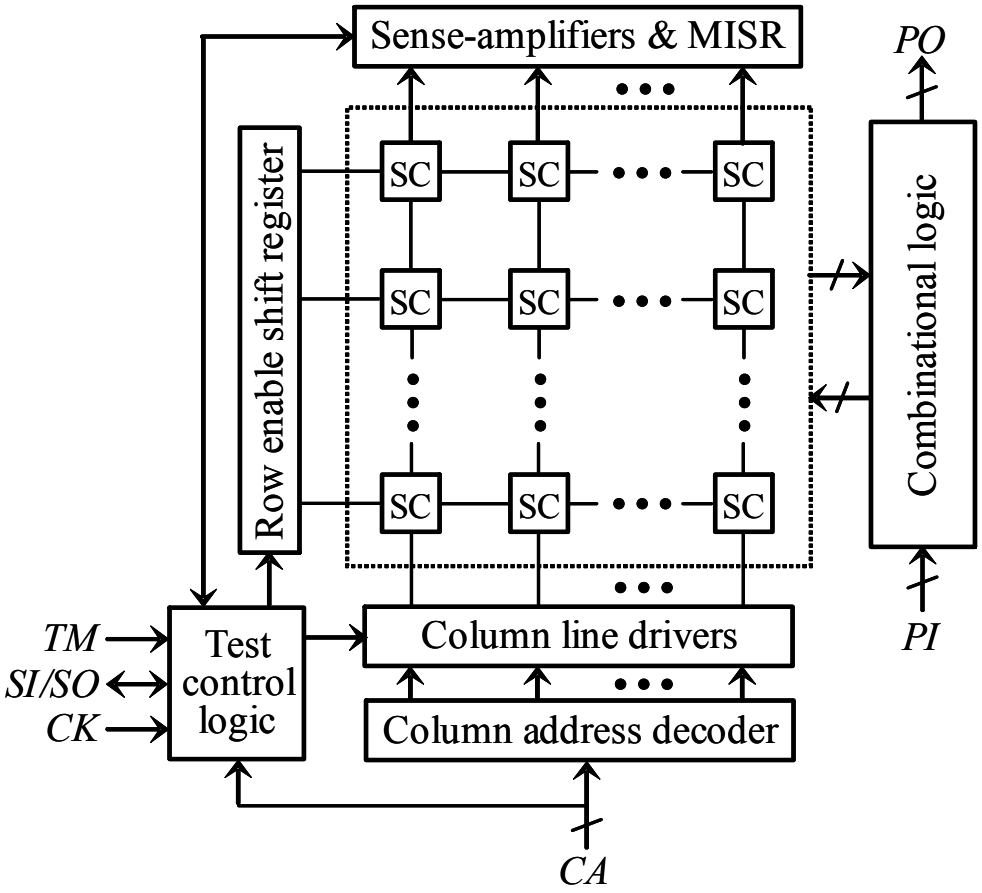
In normal mode, *RE* is set to 0, forcing each scan cell to act as a normal *D* flip-flop.

In test mode, *RE* is set to 0 and a pulse is applied on clock Φ

To read out, clock Φ is held at 1, *RE* for the selected scan cell is set to 1, and the content of the scan cell is read out through the bidirectional scan data signals *SD* and *SD_*.

To write or update a scan value into the scan cell, clock Φ is held at 1, *RE* for the selected scan cell is set to 1, and the scan value and its complement are applied on SD and SD_, respectively

PRAS Design



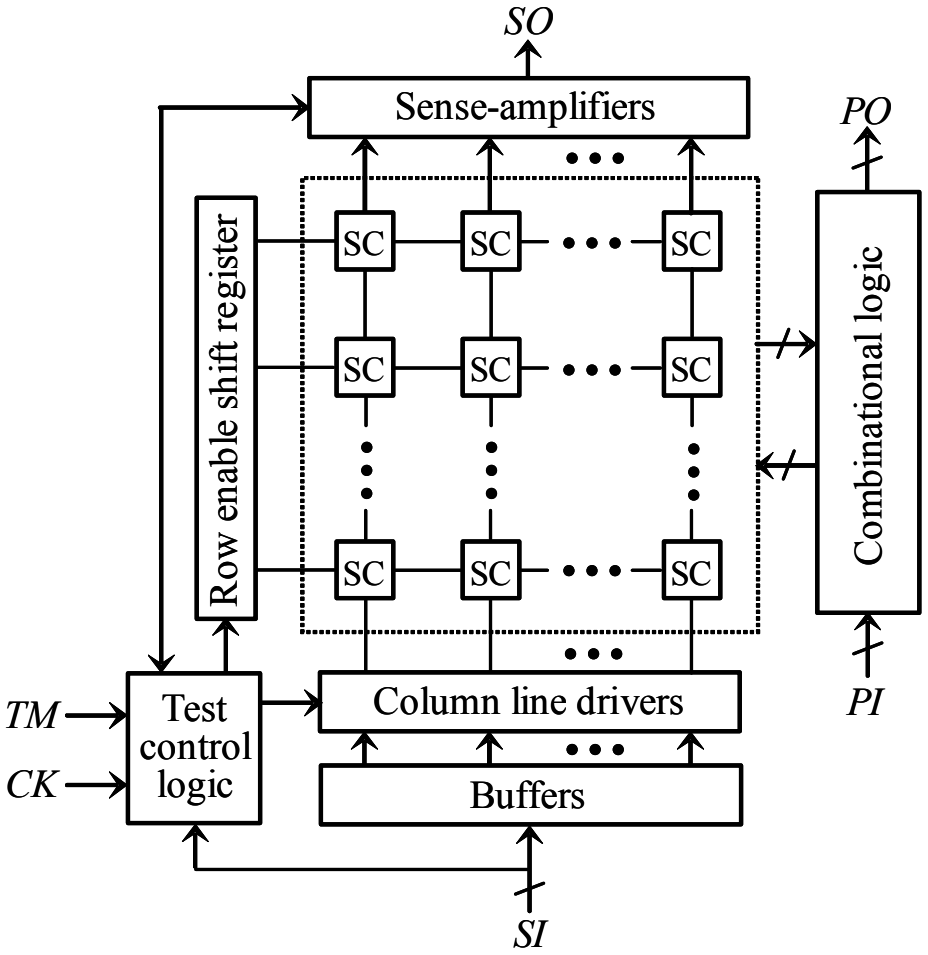
PRAS Architecture

Rows are enabled in a fixed order. It is only necessary to supply a column address to specify which scan cell in an enabled row to access.

PRAS Test Procedure

```
for each test vector v_i (i = 1, 2, …, N) {
    /* Test stimulus application */
    /* Test response compression */
    enable TM;
    for each row r_j (j = 1, 2, …, m) {
        read all scan cells in r_j / update MISR;
        for each scan cell SC in r_j
        /* v(SC): current value of SC  */
        /* v_i(SC): value of SC in v_i */
            if v(SC) ≠ v_i(SC)
                update SC;
    }
    /* Test response acquisition */
    disable TM;
    apply the normal clock;
}
scan-out MISR as the final test response;
```

STAR Design



STAR Architecture

Use only one row (*X*) decoder and support two or more *SI* and *SO* ports.

All rows are enabled (selected) in a fixed order one at a time by rotating a 1 in the row enable shift register.

When a row is enabled, all columns (or scan cells) associated with the enabled row are selected at the same time.

RAS Applications

- Logic test:
  - Reduced test length
  - Reduced scan power
- Delay test: Easy to generate *single-input-change* (SIC) delay tests.
- Advantage: RAS may be suitable for certain architecture, e.g., where memory is implemented as a RAM block.
- Disadvantages:
    - Not suitable for random logic architecture
    - High overhead – gates added to SFF, address decoder, address register, extra pins and routing

Questions?