DESIGN FOR TESTABILITY

Assignment-4

1. A scan design can contain many asynchronous set/reset signals that may require adding two or more set/reset clock points to break all ripple set/reset loops. A ripple set/reset loop is a combinational feedback loop. Assume that the design now contains two system clocks (CK1 and CK2) and two set/reset clocks (SRCK1 and SRCK2) Derive two BIST timing control diagrams including a scan enable (SE) signal, to test all data faults and set/reset faults controlled by these four clocks. Explain which timing control can detect more faults.

2. Design a one-hot decoder for testing a tri-state bus with four independent tristate drivers in BIST mode.

3. Design a four stage weighted LFSR with each output having different weight of 0.75, 0.5, 0.25 or 0.125.

4. Compare the performance of a STUMPS design and a BILBO design. Assume that both the designs operate at 200 MHz and the circuit under test has 100 scan chains each having 1000 scan cells. Compute the test time for each design when 1,00,000 test patterns are to be applied. In general, the shift (scan) speed is much slower than a circuit's operating speed. Assume that the shift speed is 20 MHz. Compute the test time for the STUMPS design again.

5. Assume that there are four synchronous clock domains each controlled by a capture clock, CK1, CK2, CK3 or CK4, and each is operated at a frequency F1=2xF2=4xF3=8xF4. Derive BIST timing control diagrams using aligned skewed load and aligned double capture to test all intra clock domain and inter clock domain delay faults. Specify by arrows the delay faults that can be detected in the diagram.