FPGA Experiment 2

Introduction: In this experiment you will be designing a decimal counter (0-255) and displaying it on the 7 segment LED display.

Procedure:

1) Design an 8-bit counter. It should have an asynchronous reset.
2) The clock to the counter is manually given through a push button. So you should come up with a method to de-bounce the push button.
3) Design a 16-bit counter from the previous 8-bit counter.
4) The clock to this counter is the 50 MHz crystal on board. So MSB will generate 50,000,000/65536 ~ 763 Hz.
5) This will be used for toggling 7 segment display.
6) Use double dabble method to generate BCD from 8-bit counter. http://en.wikipedia.org/wiki/Double_dabble

Note: If you don't want to use double dabble, in step 1 you can design a BCD counter. Then it will be 12-bit counter and you will be able to reach a count of 999.