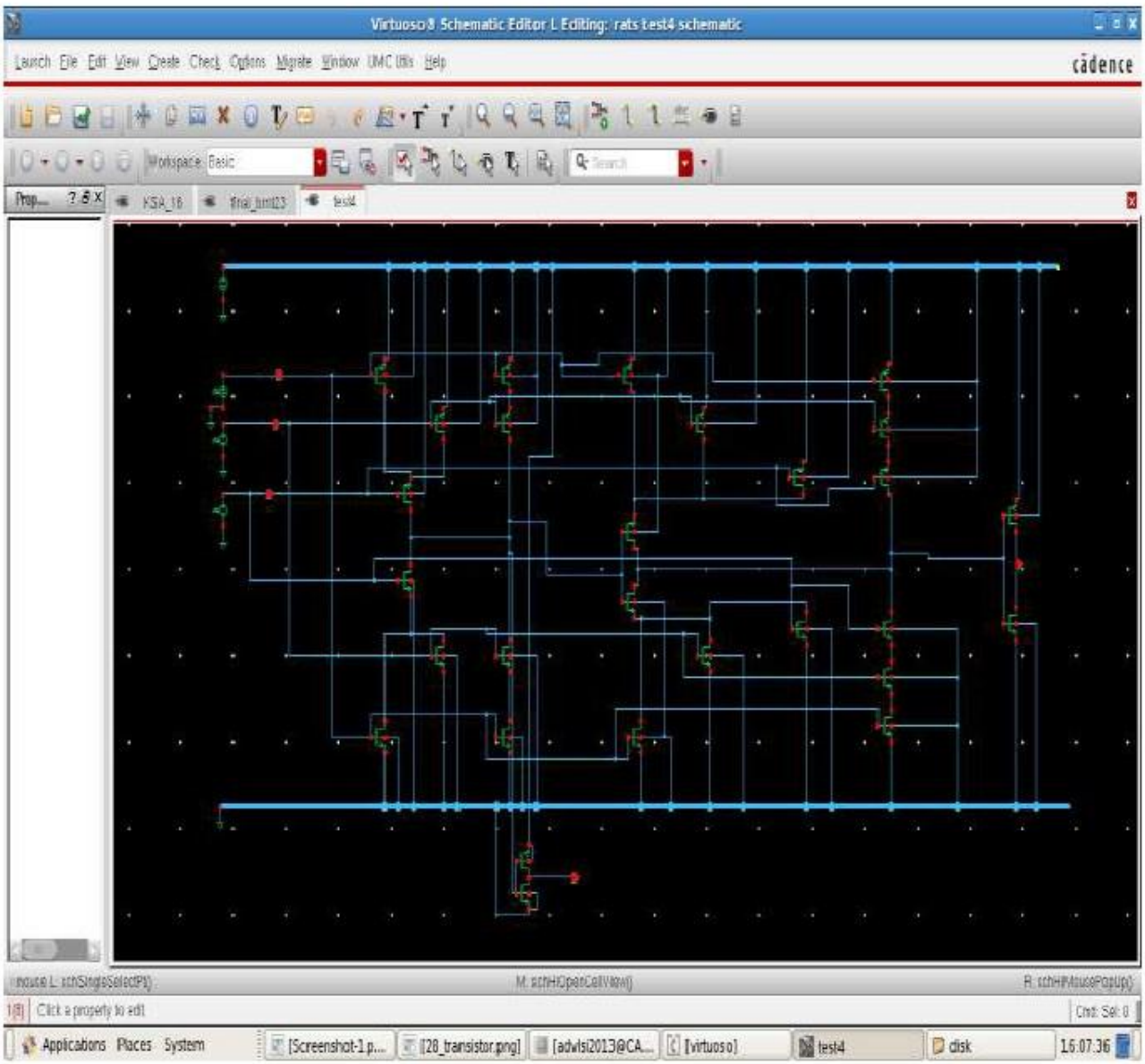
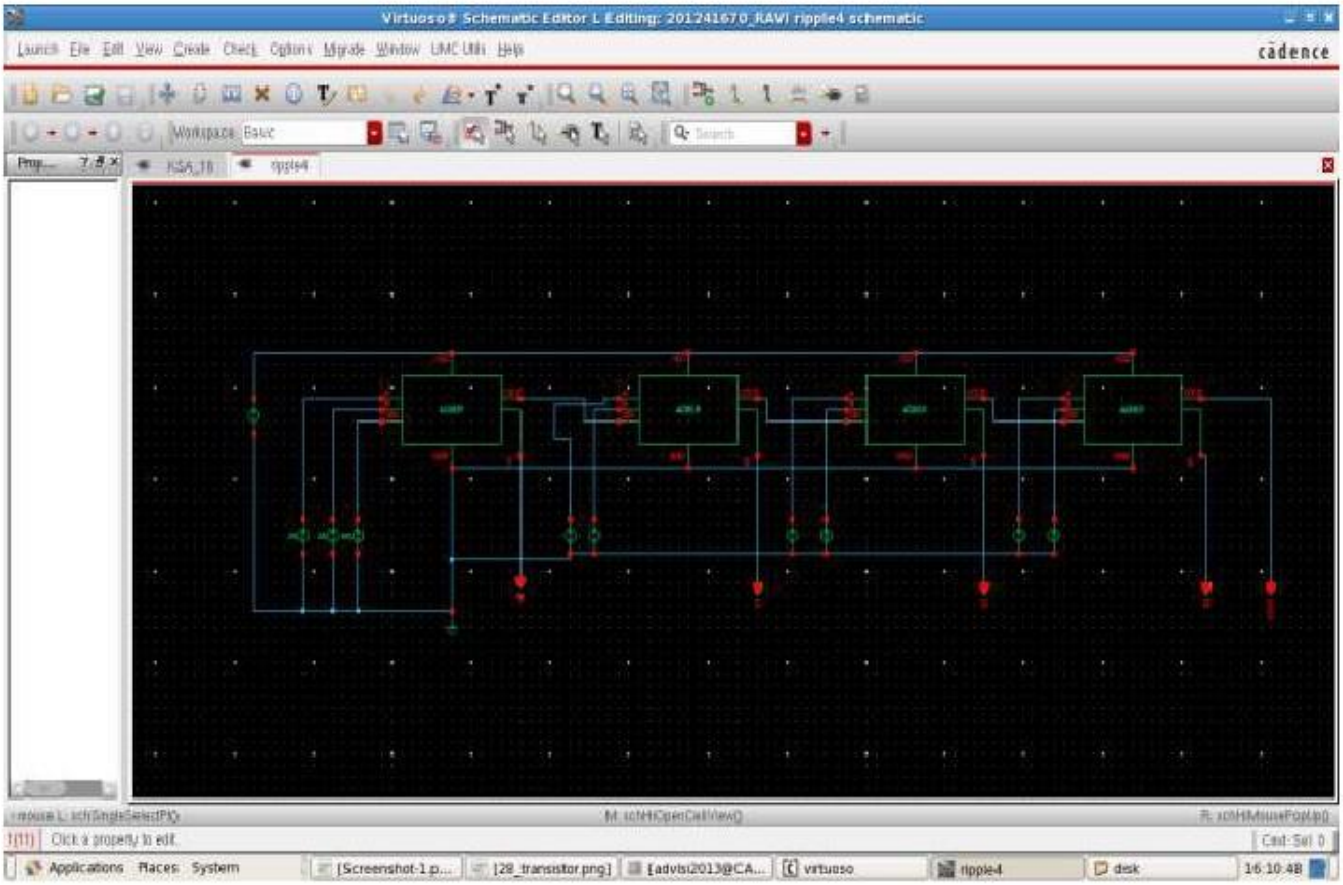
ASSIGNMENT 3:
Adder Architectures
VLSI ARCHITECTURES

Design a 4 bit ripple carry adder using CADENCE Virtuoso Schematic Editor and simulate it using Spectre simulator. Draw the layout using Virtuoso Layout Editor. Estimate the area, power dissipation and delay of the adder.

Below is the schematic diagram of the 28 transistor single bit full adder.

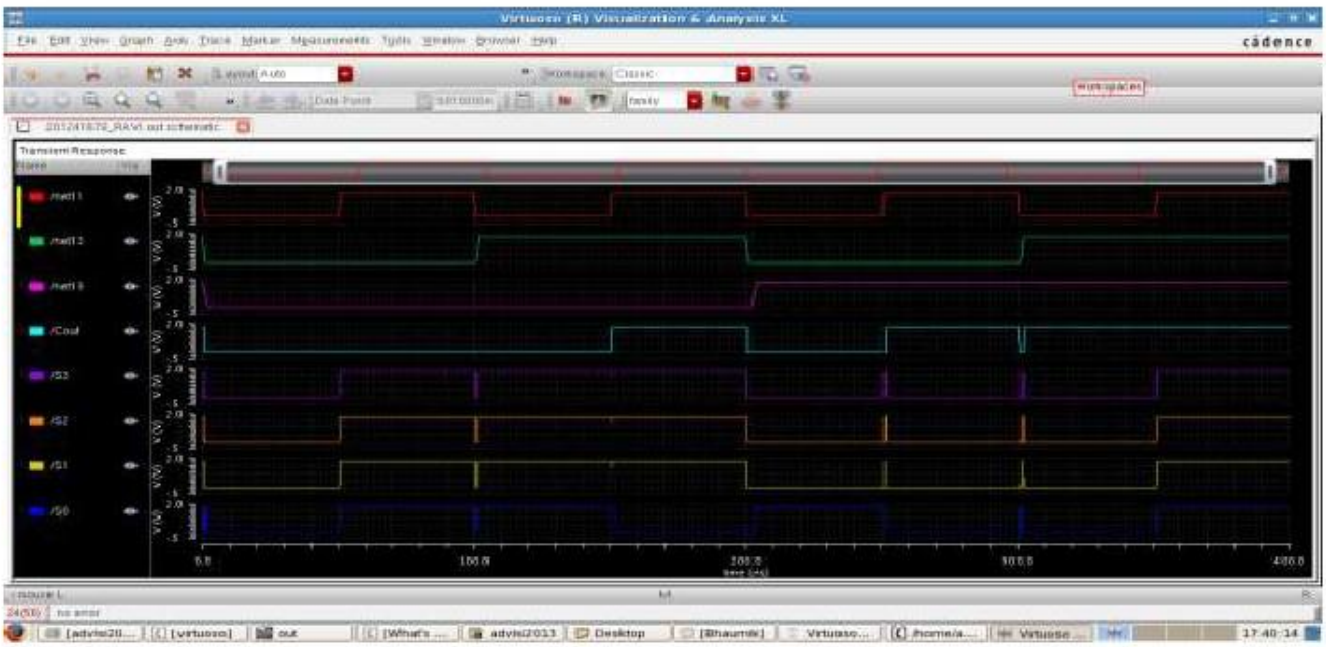


The 4 bit ripple carry adder using this as a block is shown below:

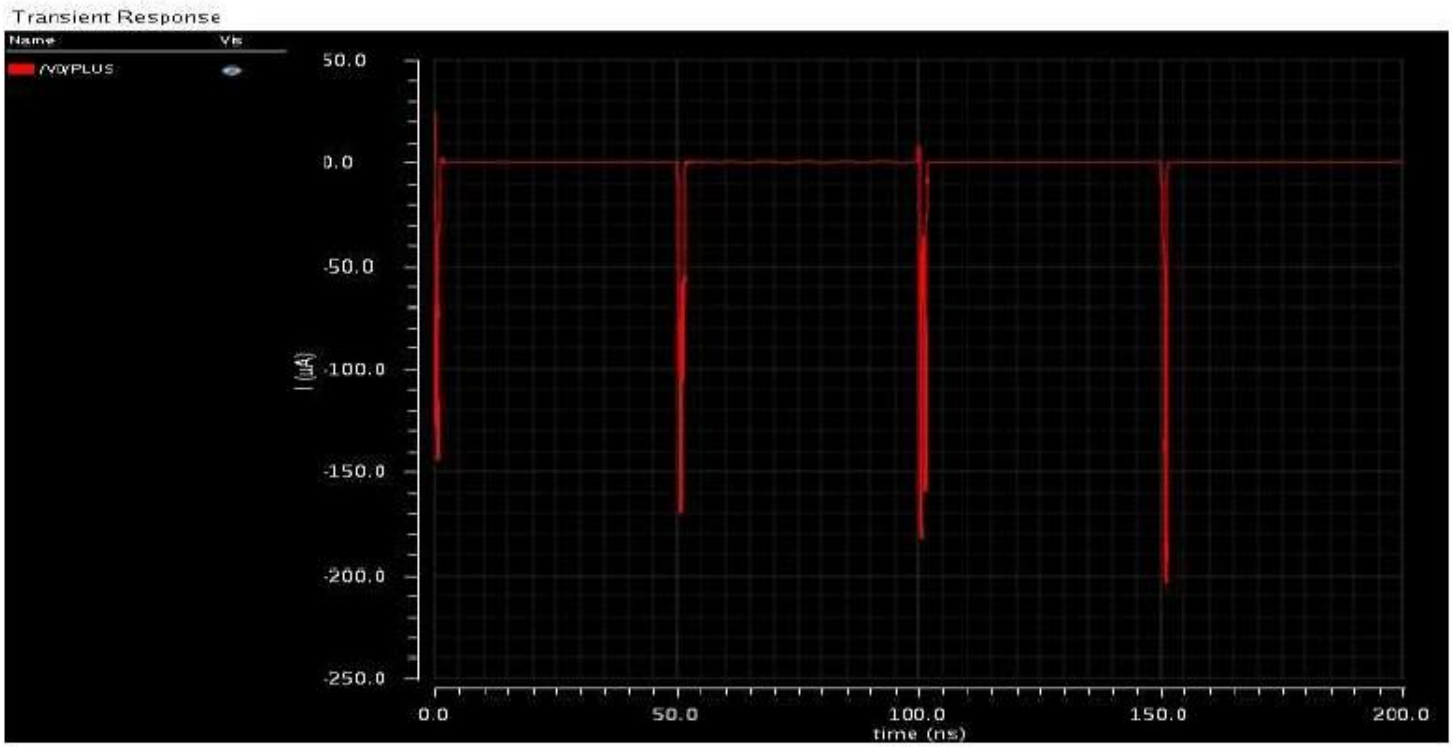


The above is the ripple carry adder 4 bit output.
Simulations of the 4 bit rpple carry adder:

Simulation results:
Power dissipation : 43 micro watts
Delay – 450ps

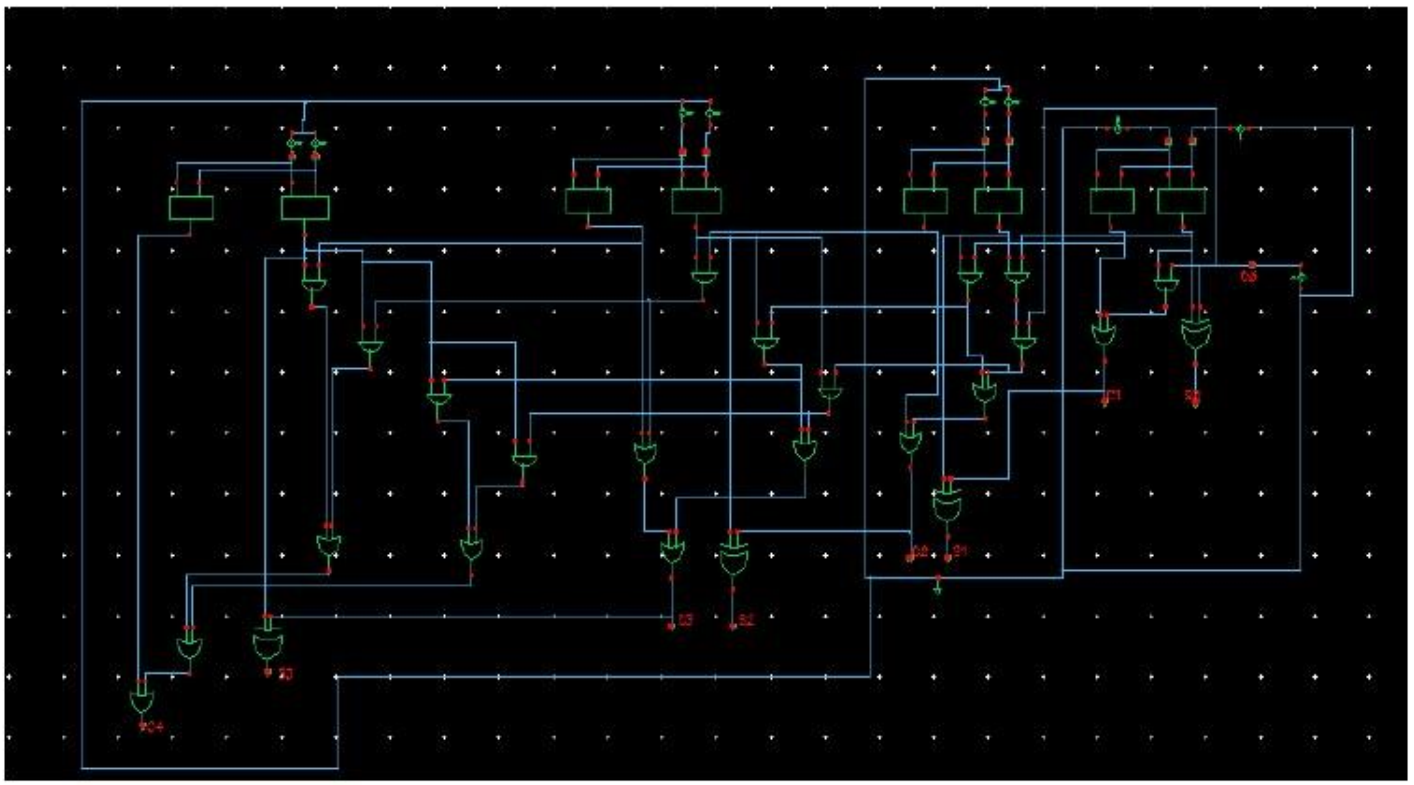


Current simulation:

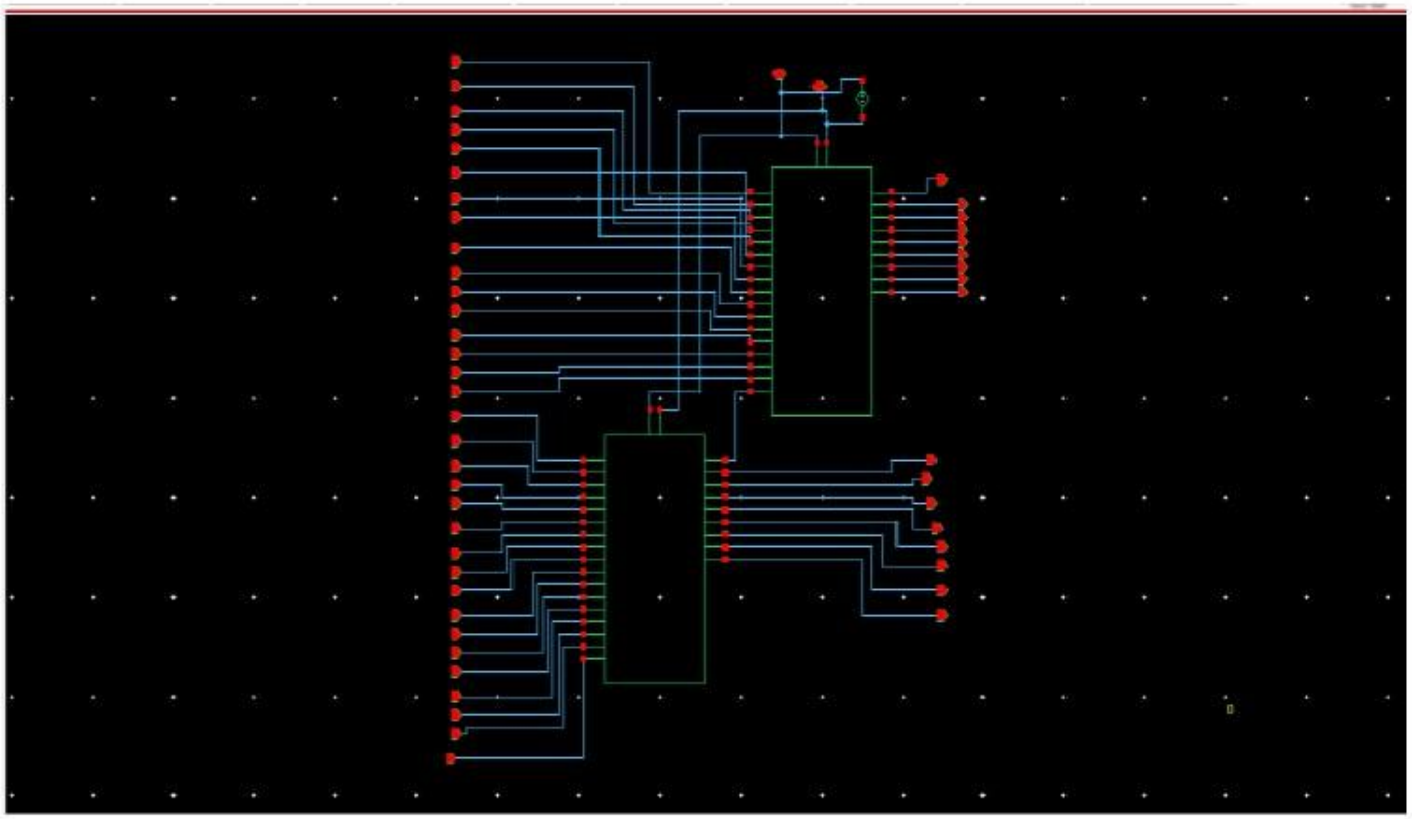


Question2: Design a 4 bit carry look ahead adder using CADENCE Virtuoso Schematic Editor and simulate it using Spectre simulator. Draw the layout using Virtuoso Layout Editor. Estimate the area, power dissipation and delay of the adder.

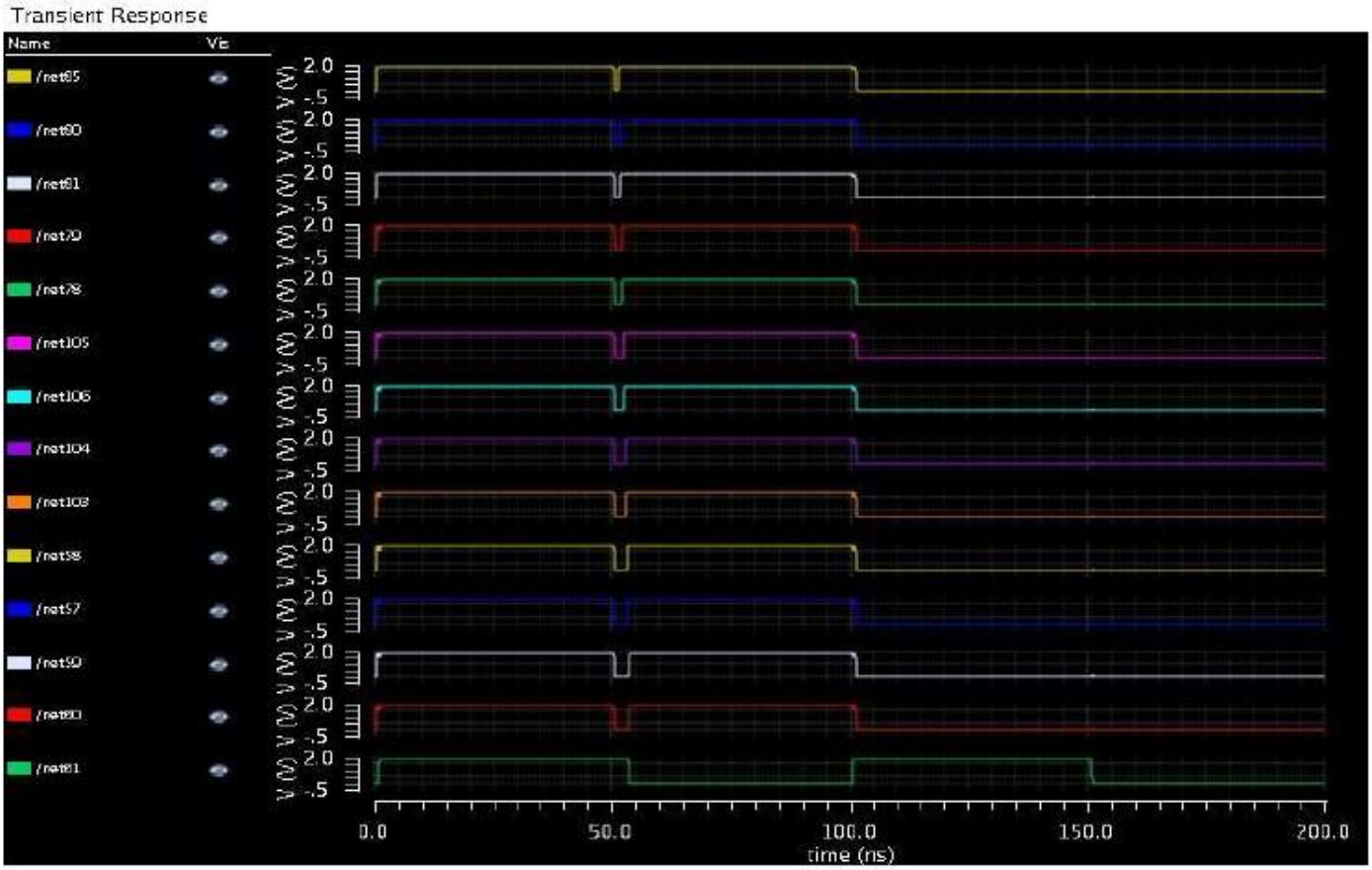
Schematic of the carry look ahead adder:



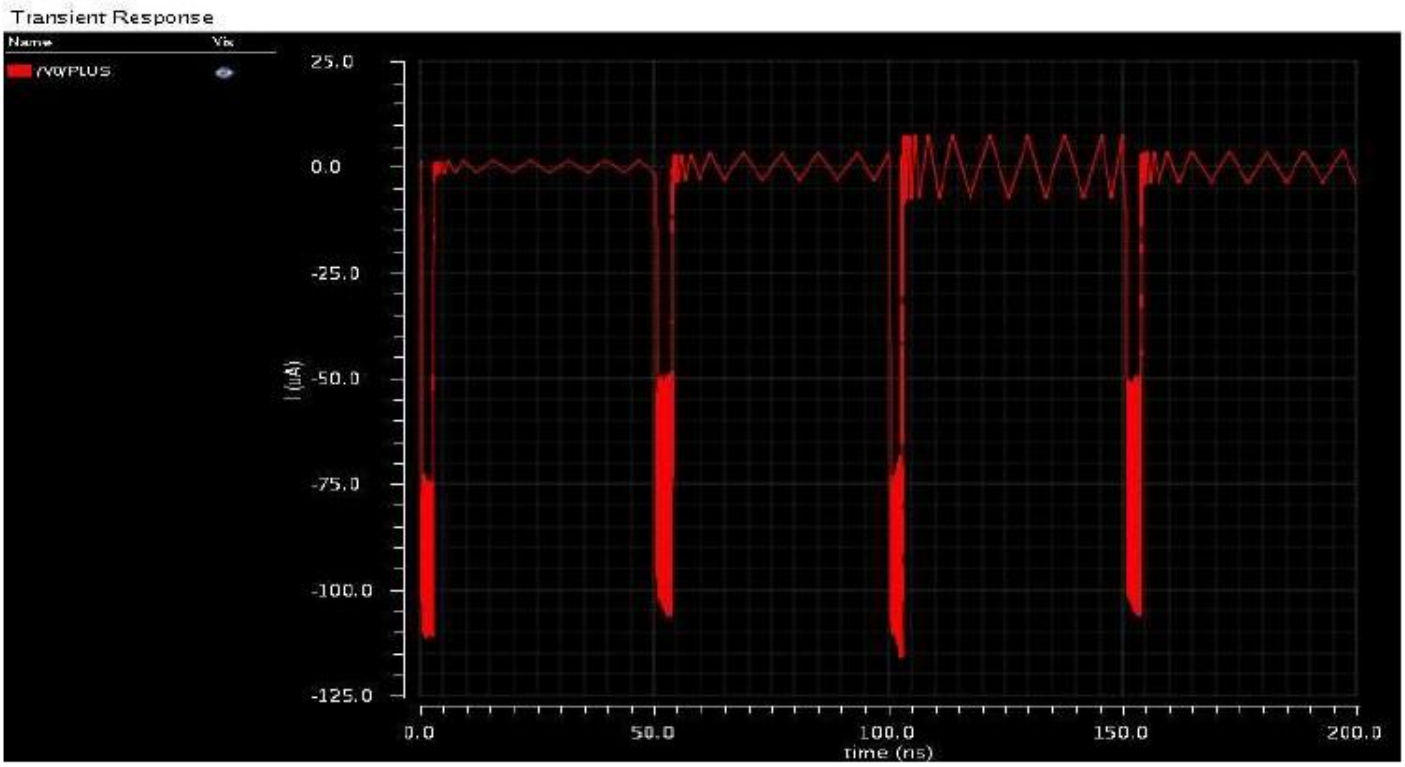
16 BIT CLA:



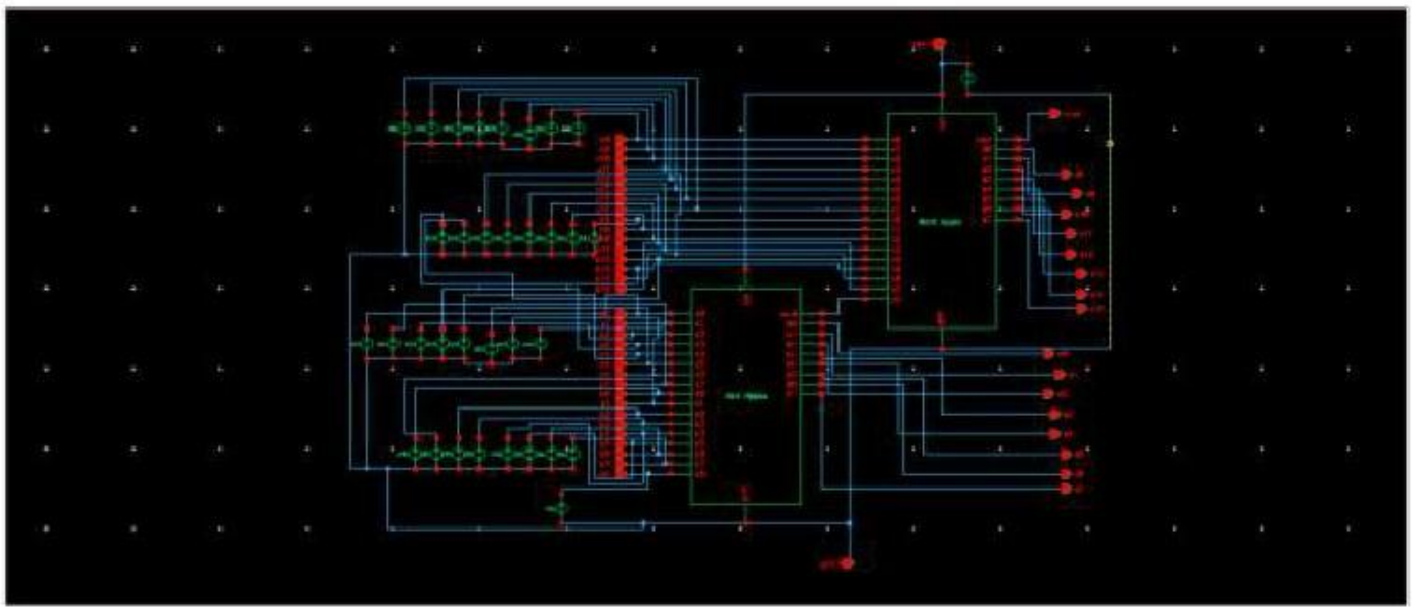
Simulation outputs:



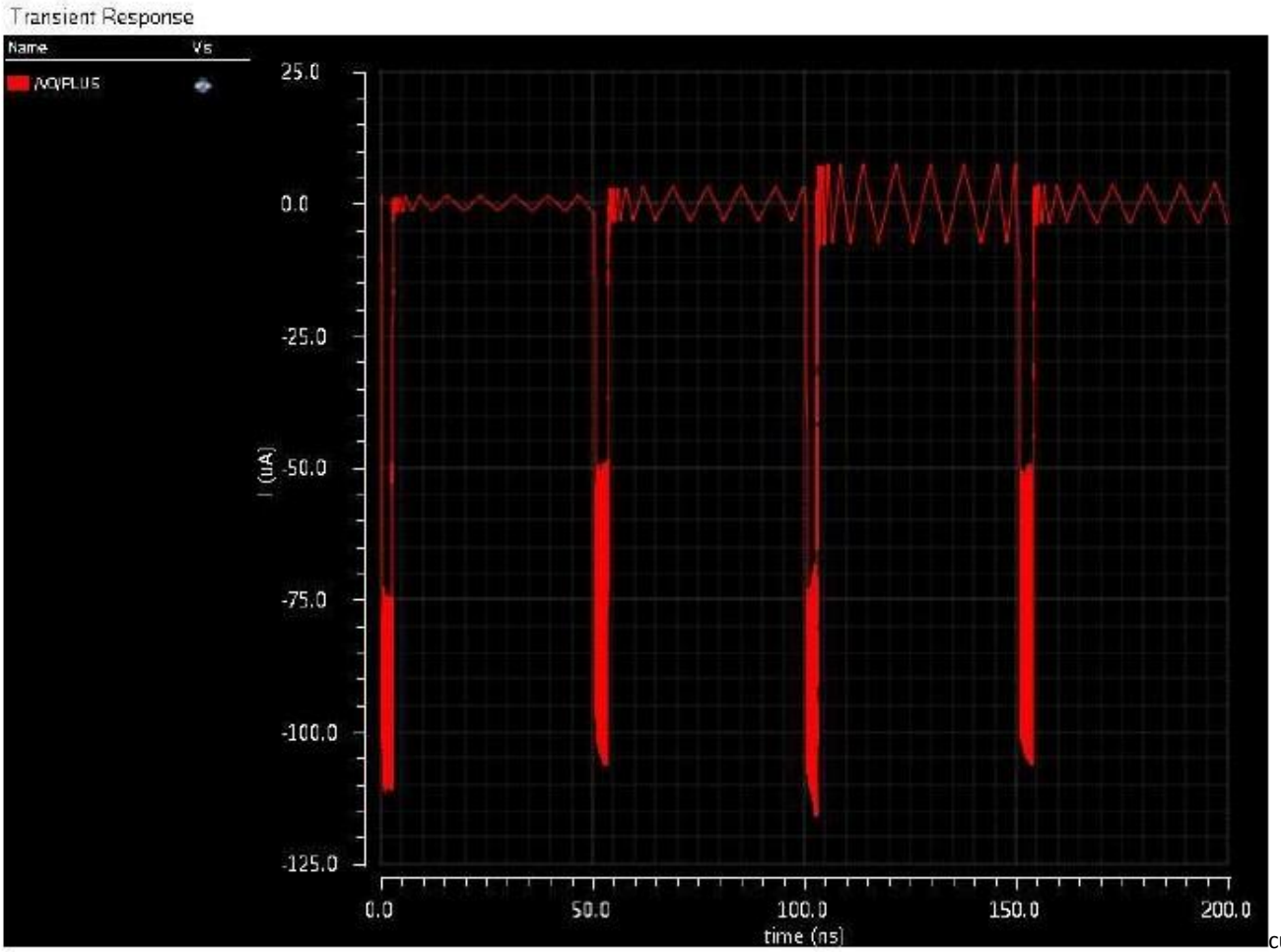
Current graph:



3. In problems 1 and 2, redesign the circuits increasing the width of the adders from 4 bits to 16 bits in steps of 1 bit. Draw the layouts of the circuits and estimate the power dissipation, delay and area of the adders. Prepare a table for your comparison. What conclusions can you draw from the table?

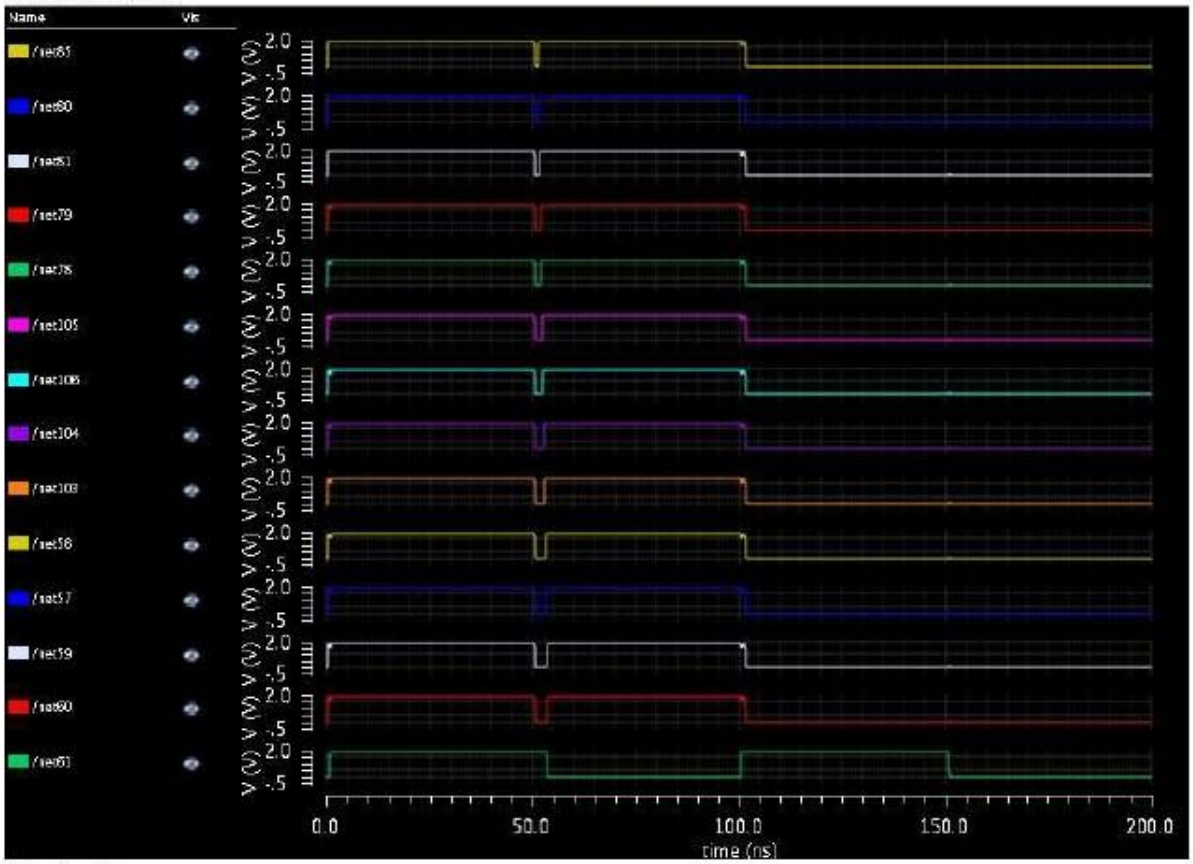


16 bit ripple adder

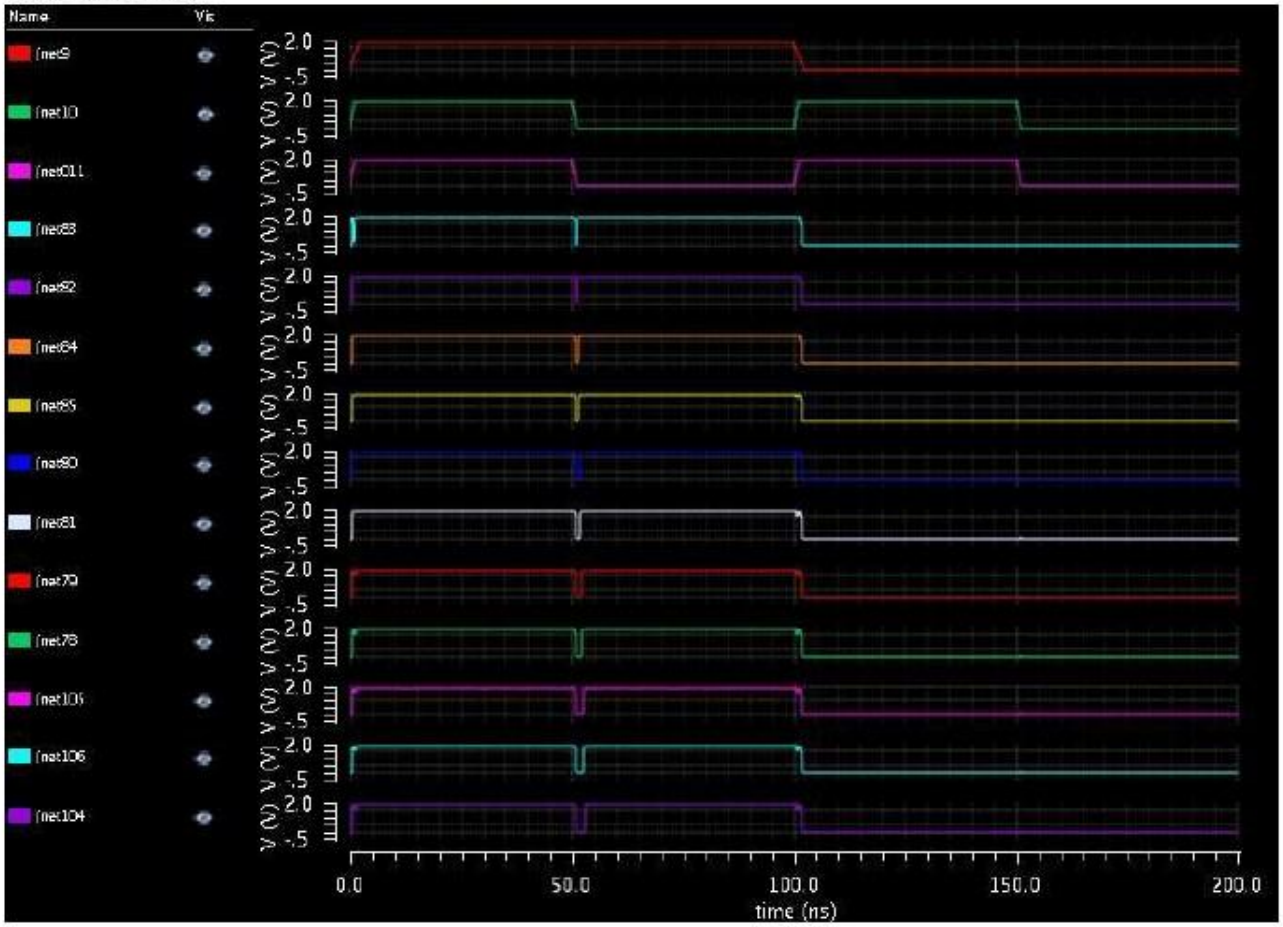


current

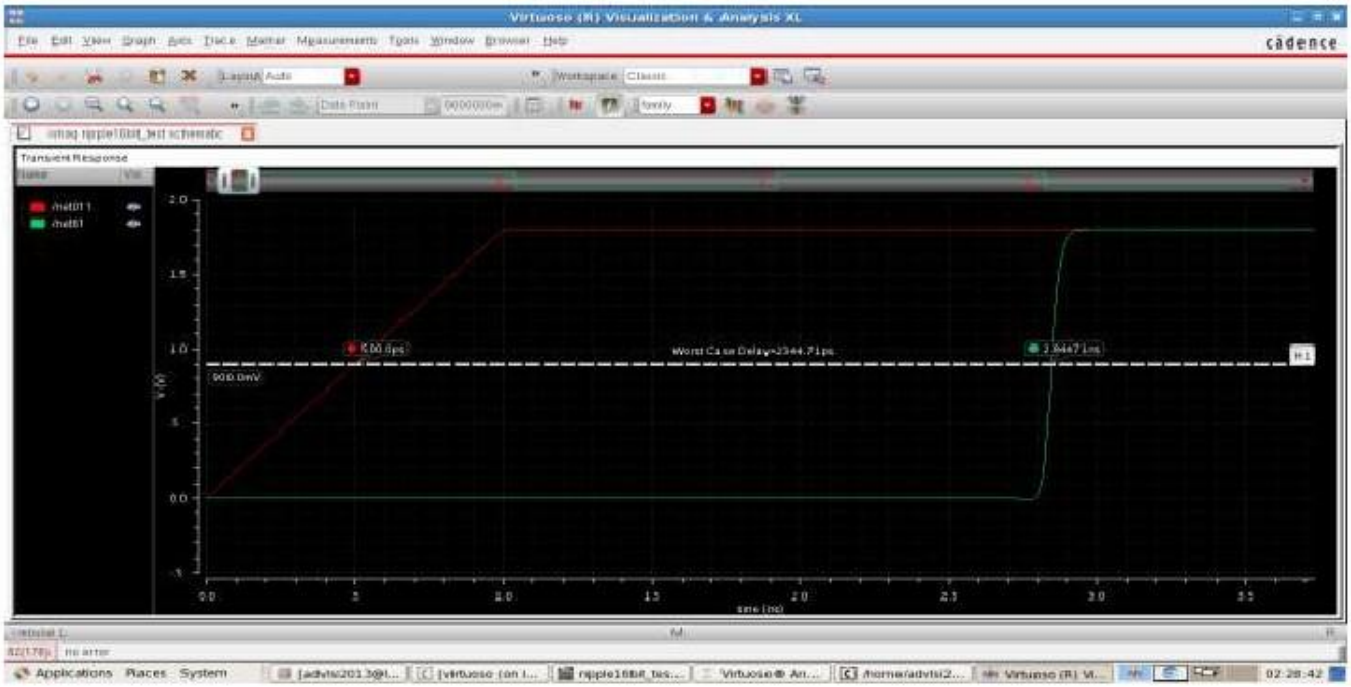
Transient Response

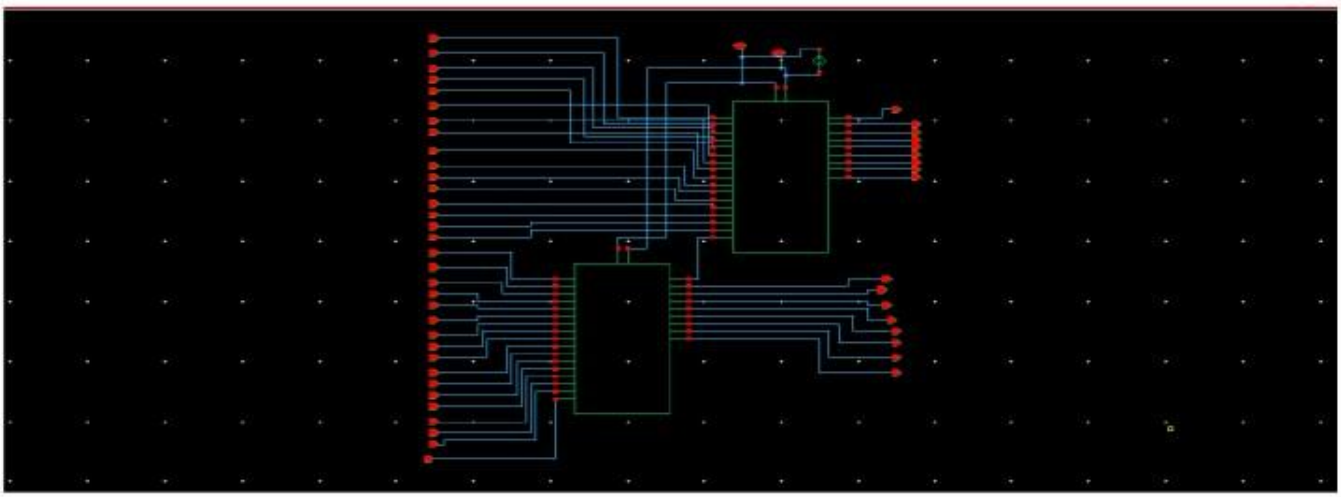


Transient Response



SIMULATION OF DELAY:

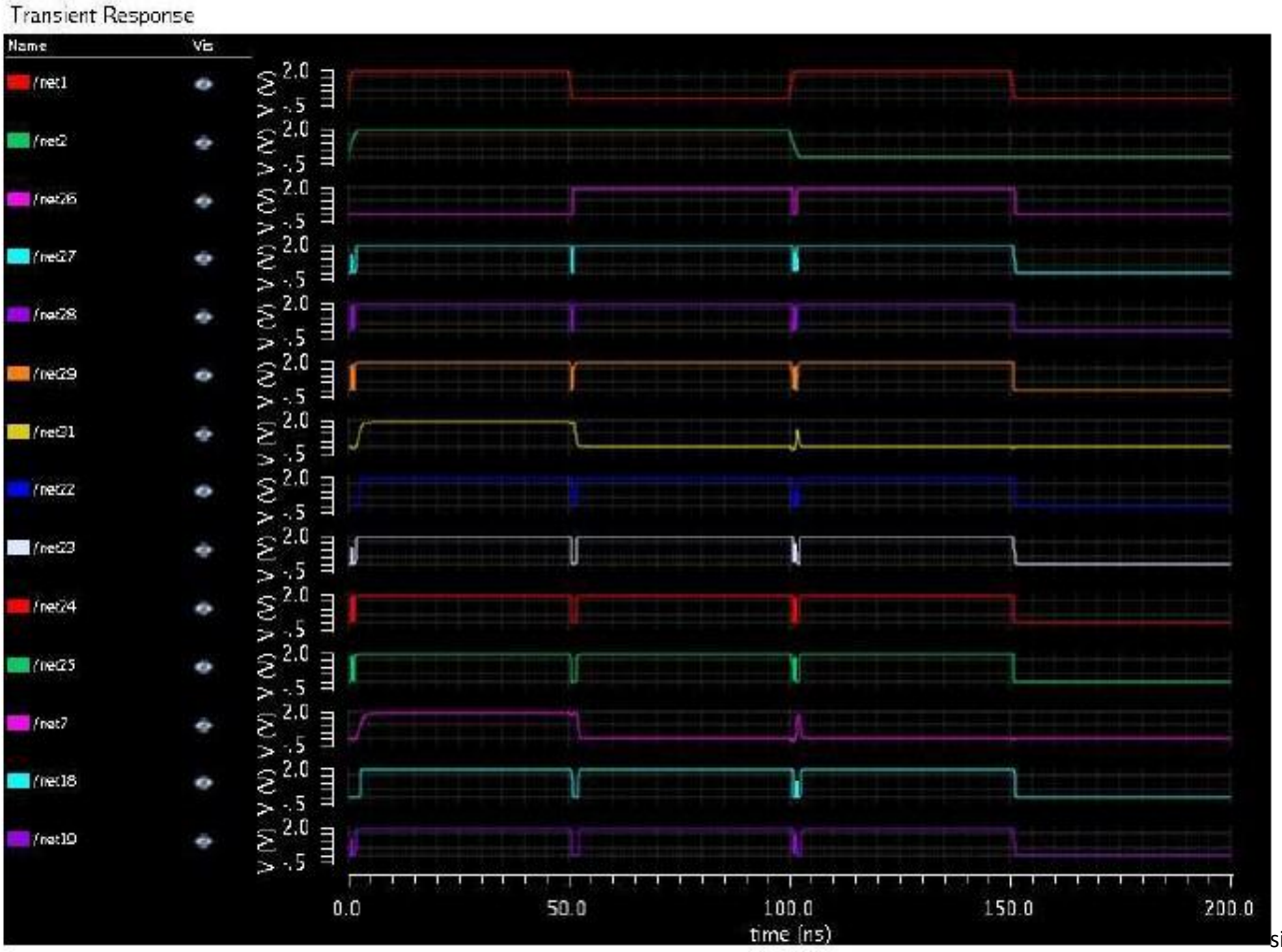




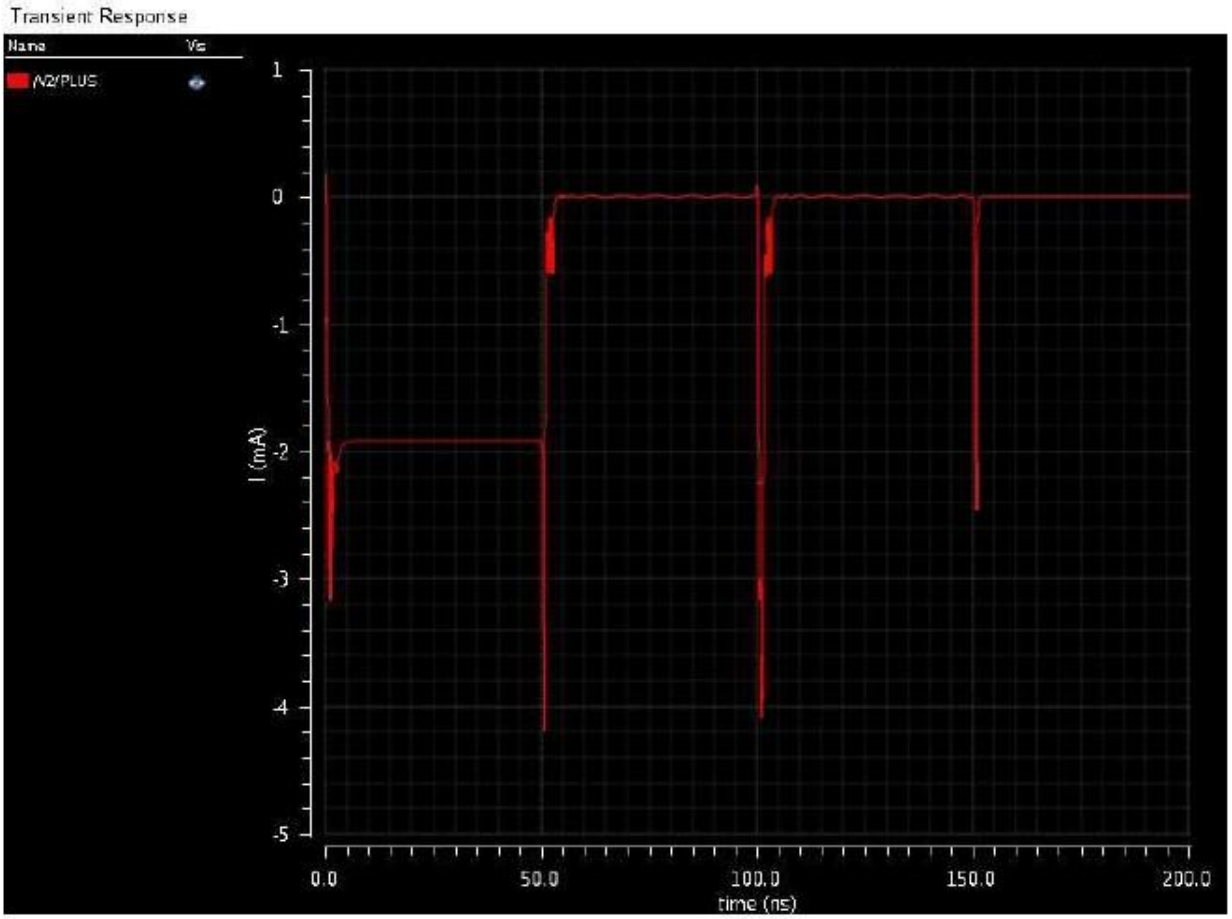
16 bit look ahead adder


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
500.0ps
Worst-Case delay=2252ps
2.752ns
300.0mV
V (V)
time (ns)
Applications Places System
02:07:47

DELAY SIMULATIONS



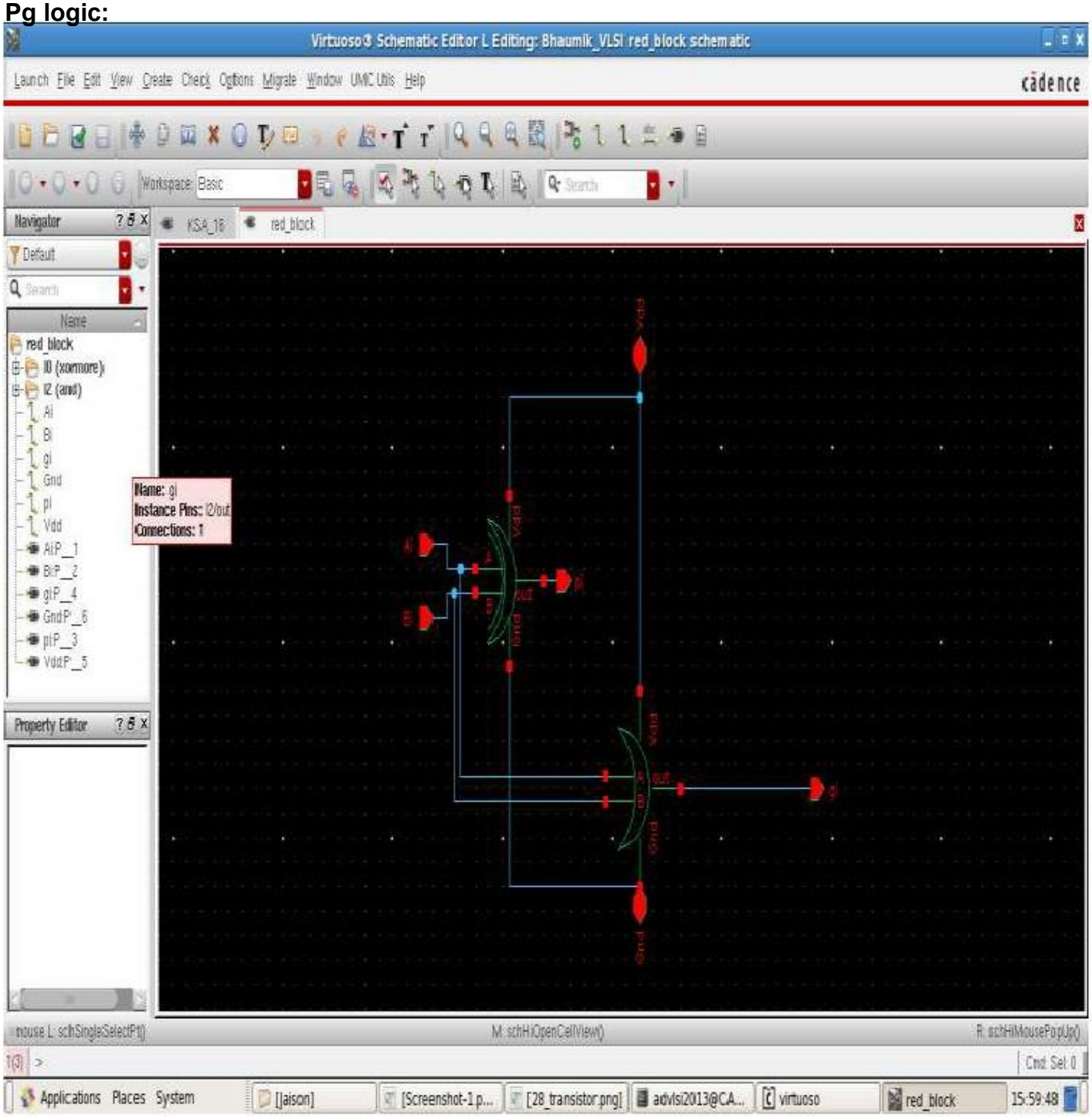
simulation



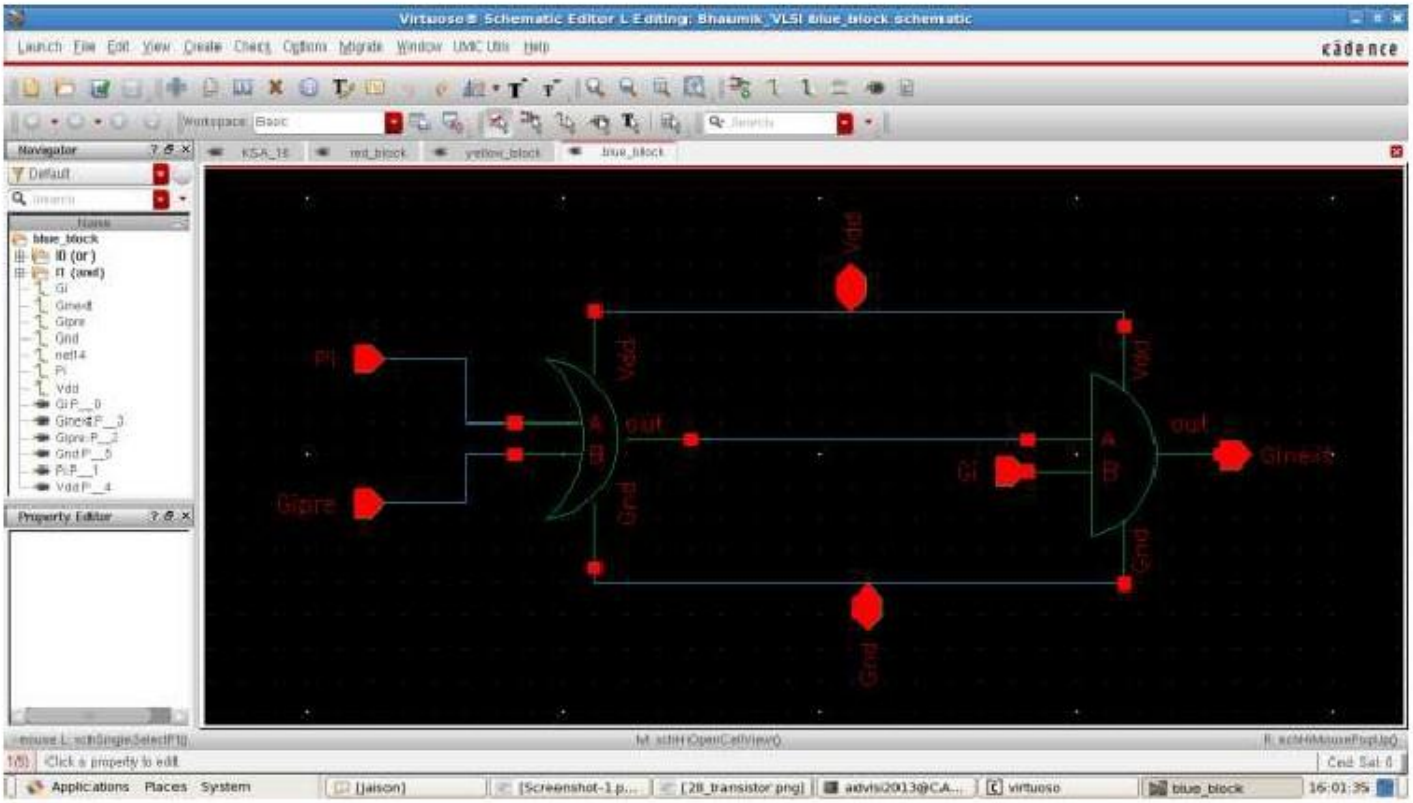
Current calc

Question 4: Design 16 bit Brent Kung and Kogge-Stone Adders. Draw the layouts of the three adders. Compare the area and performance parameters of these adders with the ripple carry and carry look ahead adders that you already designed. What conclusions can you draw from this?

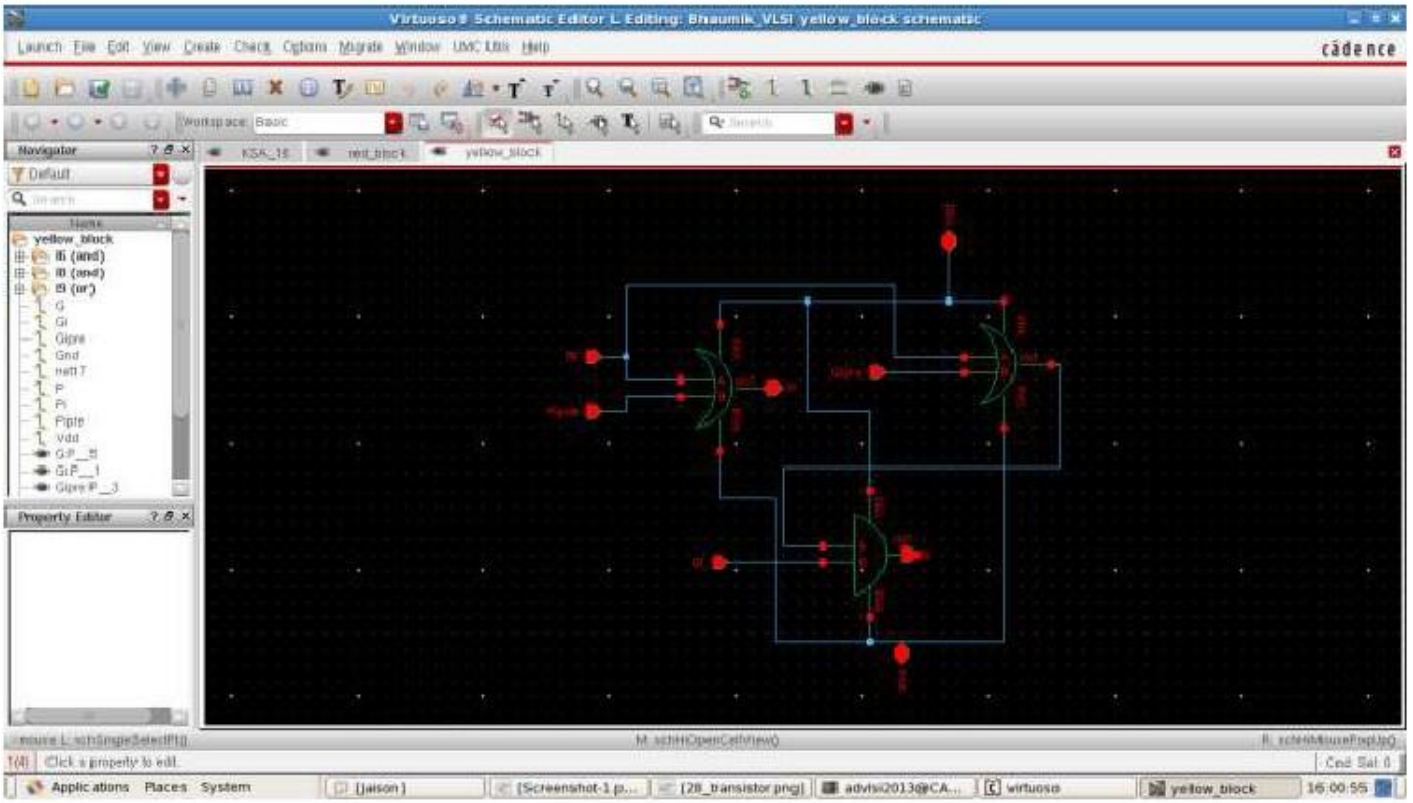
Pg logic:



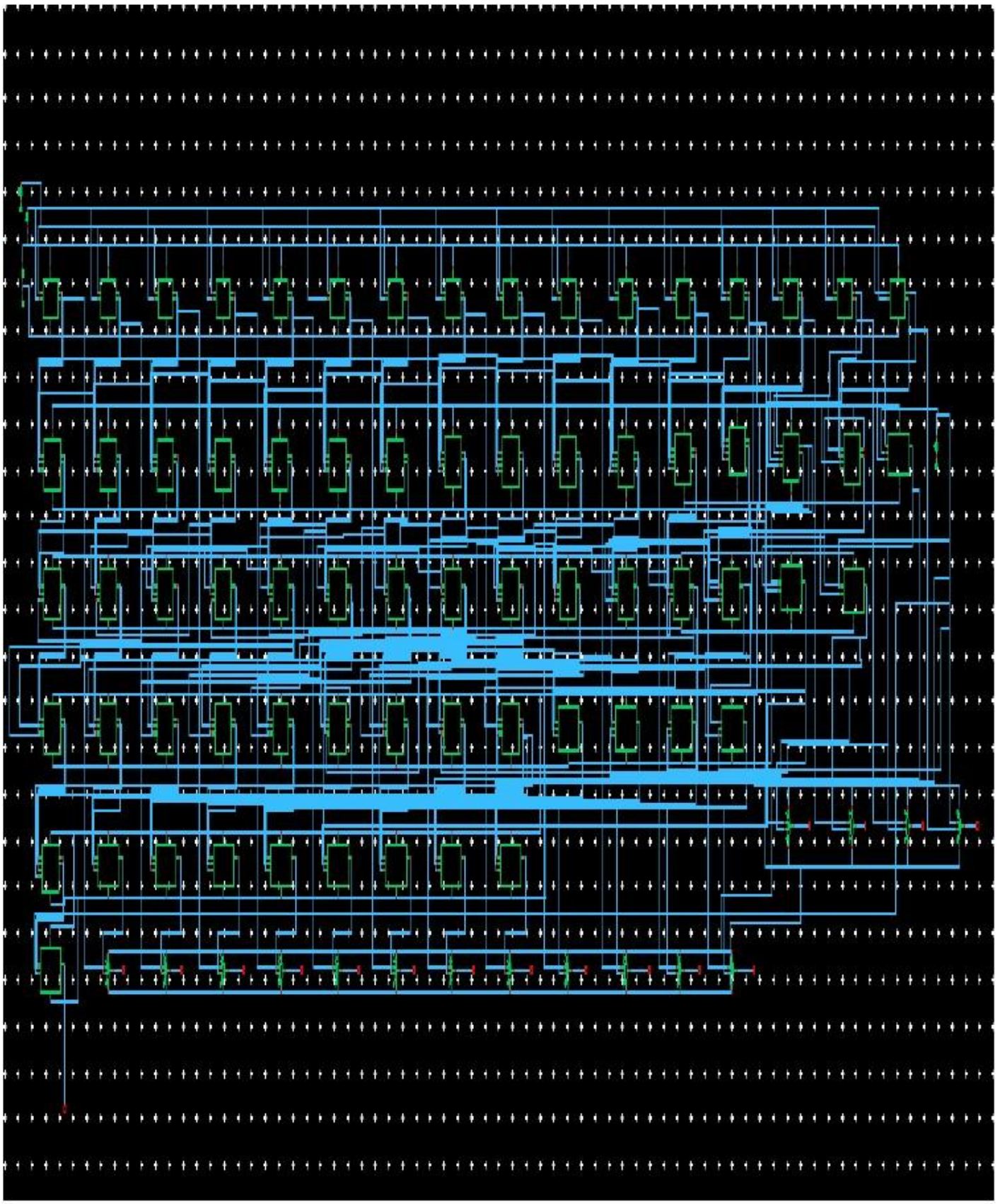
Gray cell:



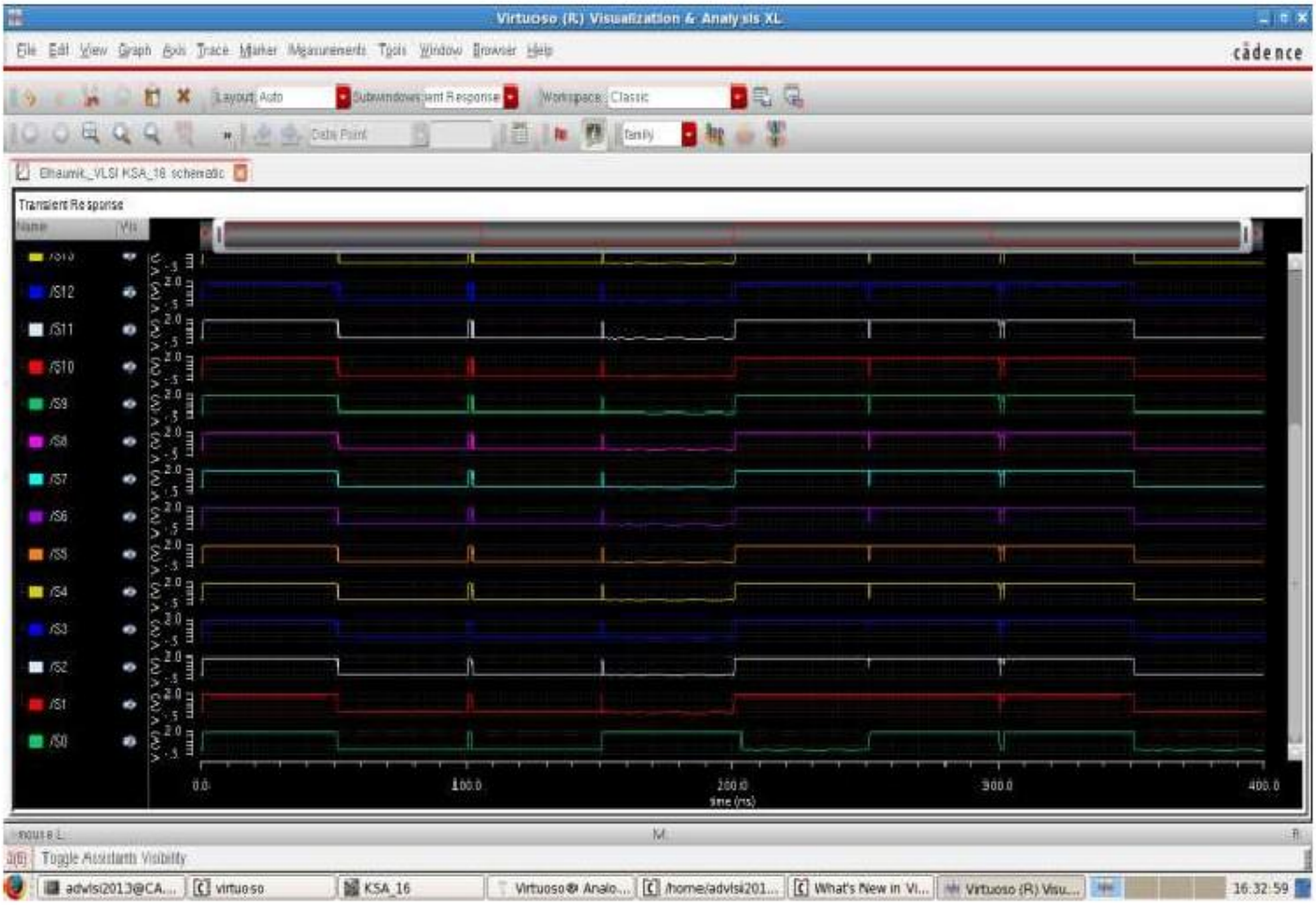
Black cell:



Kogge stone adder:

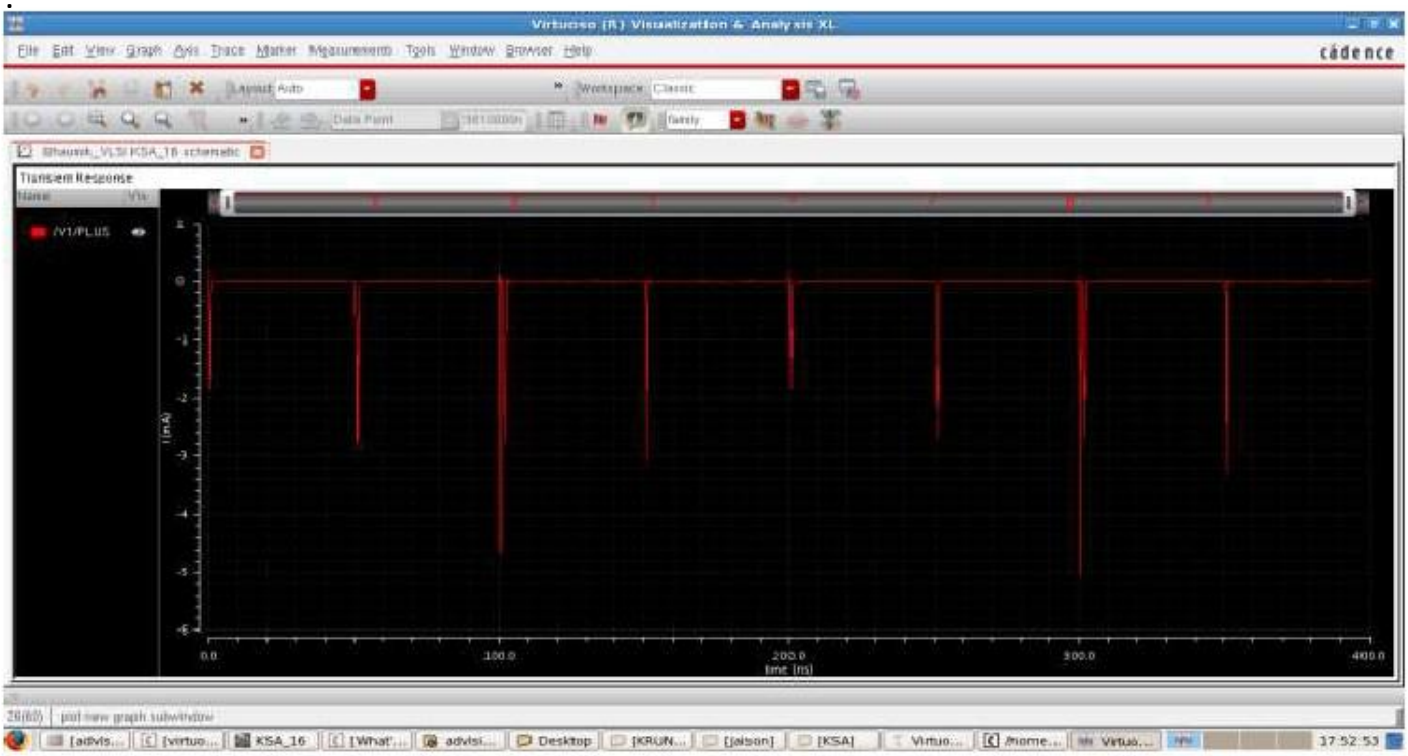


Simulation results:

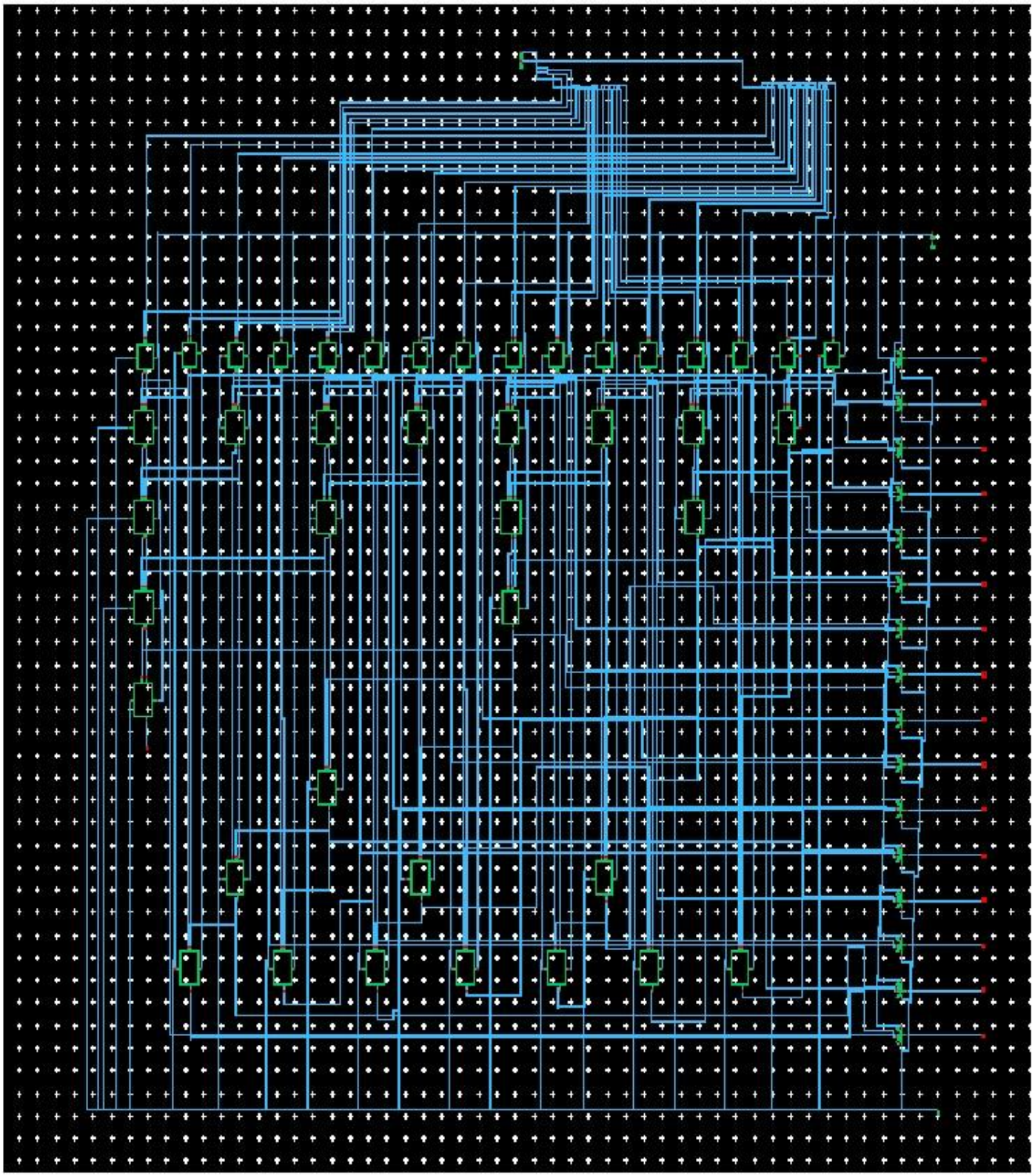


Current graph:

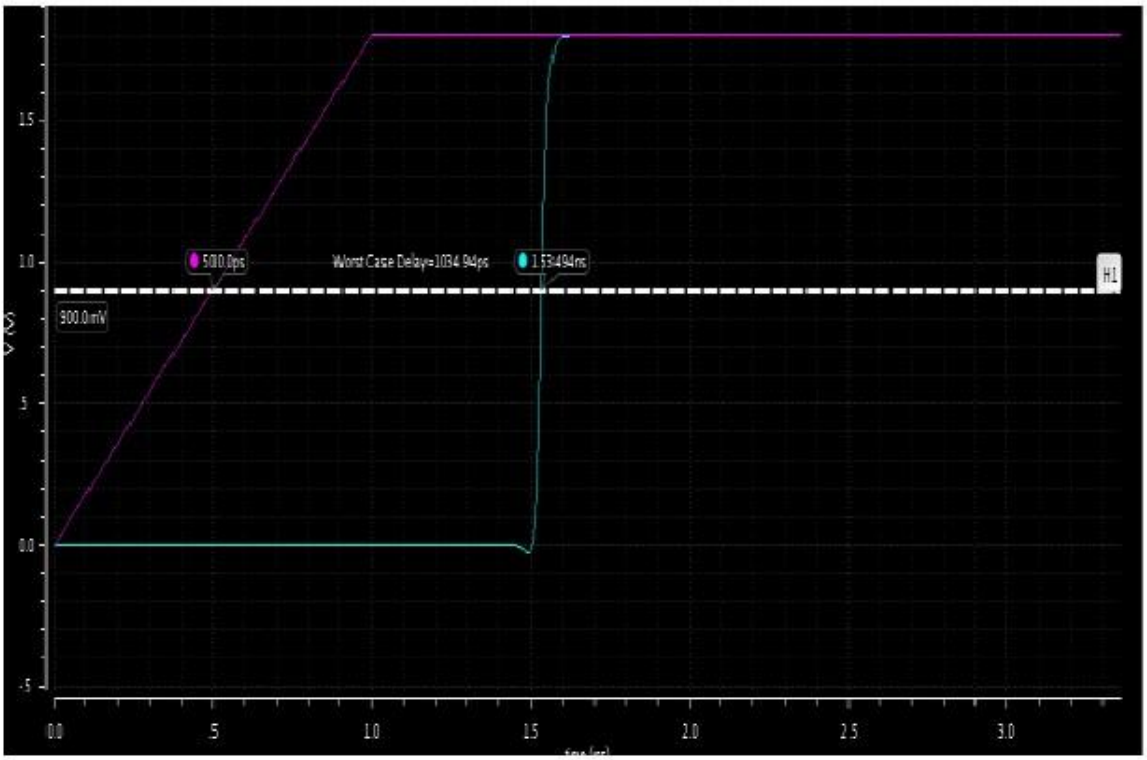
:



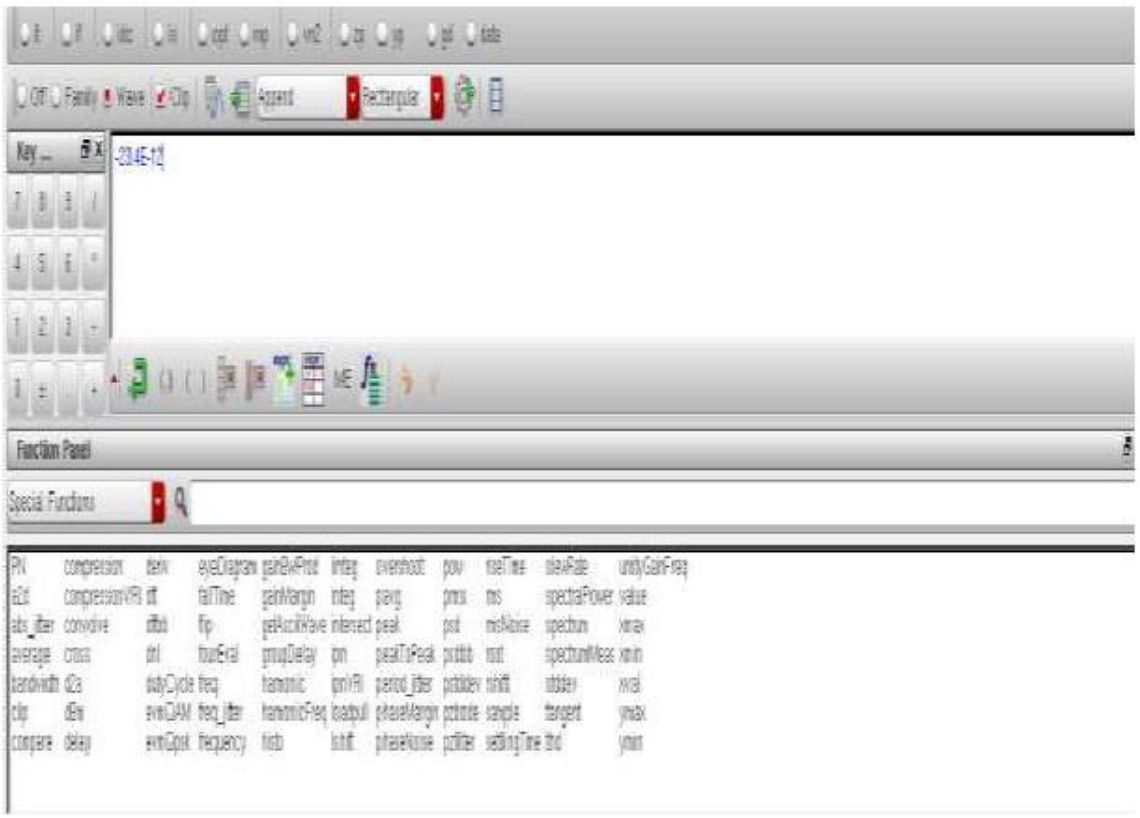
Brent kung:



SIMULATION OUTPUTS:

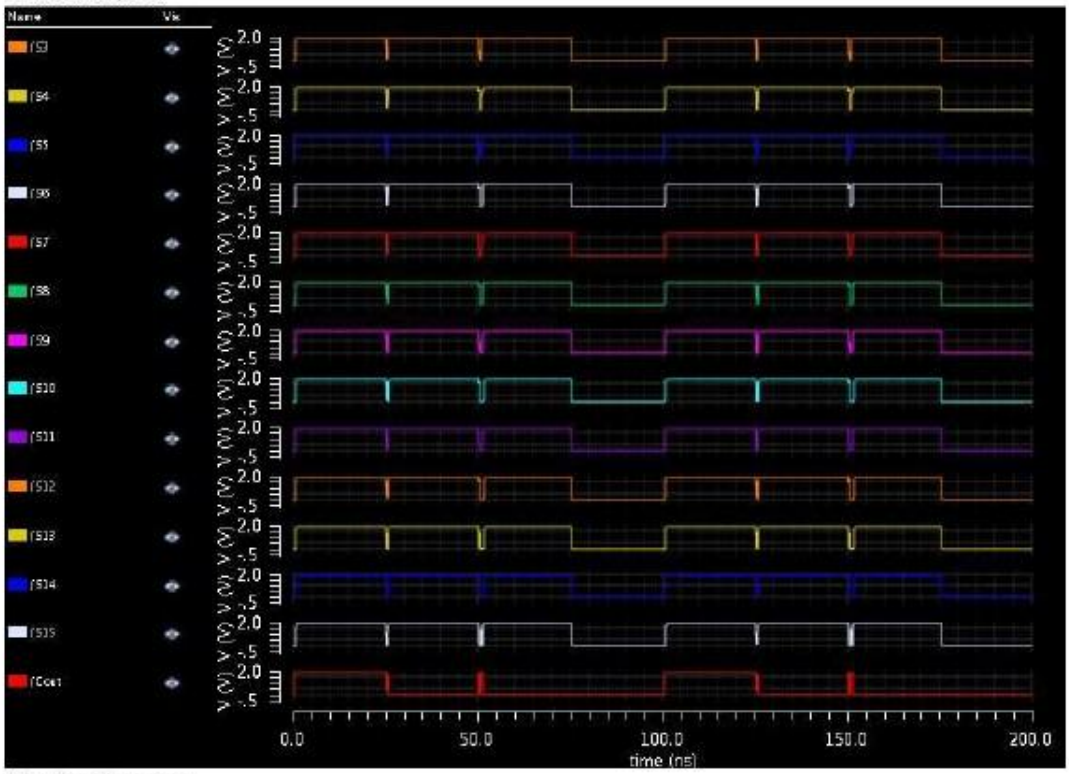


Delay calculation

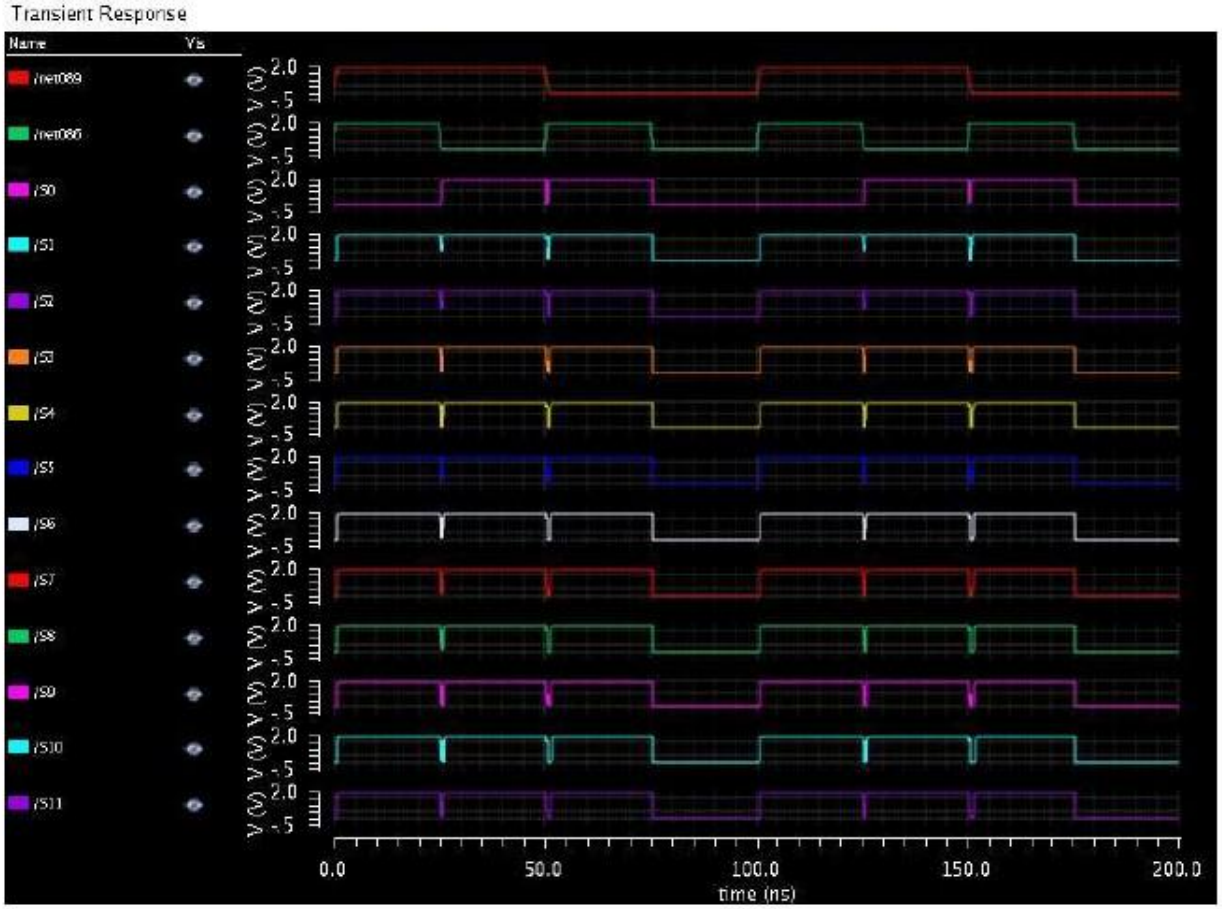


Current calculation

Transient Response



Transient Response



-	Iavg(pA)	Power(uW)	Tphl(ns)	Tplh(ns)	Tp(ns)
LA4bit	27	48.6	0.380	0.423	0.401
LA8bit	44.5	80.1	0.251	0.295	0.272
LA16bit	135.4	243.7	0.38	0.288	0.268
RA4bit	808.7	1455.6	0.624	0.627	0.626
RA8bit	34.12	61.41	0.245	0.281	0.263
RA16bit	74.61	134.29	0.291	0.582	0.436
Brent Kung	7.78	35	0.523	0.577	0.55
KoggeStone	10.22	46	0.561	0.622	0.591