IEC 103 **Basic Electronic Circuits**
Mid Semester Examination 2
Spring 2012

Maximum Marks: 50 **Time Allowed: 90 minutes**

General Instructions:

a. There are four questions in this question paper. Attempt **ALL** questions
b. Figures in the right margin indicate marks for each question.
c. Answer in your own words as far as practicable.
d. Reasons are to be stated in support of your answers (except objective type questions). *No credit will be given to answers which are mere assertions*.
e. Use of laptops, mobile phones, pagers or any other electronic communication devices is strictly prohibited inside the examination hall.
f. Use of calculators is permitted.
g. Books may be opened at the time of the examination.
h. Unless otherwise specified, *assume operational amplifier with infinite gain, infinite input impedance and zero output impedance*.
i. If any assumption is made at any step they have to be clearly stated.

::::::::BEST OF LUCK::::::::

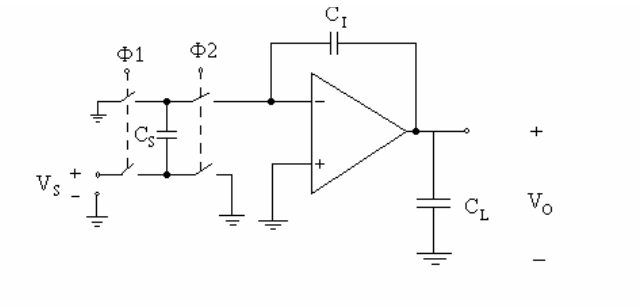
1. In a practical feedback amplifier, the feedback network causes loading at the input and output of the basic amplifier. Consider a shunt-shunt feedback amplifier. The effect of non-ideal networks may be included as input and output admittances in feed-forward and feedback paths. Finite source and load admittances Y_S and Y_L are assumed. The input current source is I_S. The input admittance of the basic amplifier is modeled by admittance Y_{11a} and its feed-forward current gain is modeled by a voltage controlled current source $Y_{21a}V_i$, where V_i is the voltage across the input terminals. The output admittance is modeled by admittance Y_{22a}. The signal fed back through the basic amplifier is modeled by a voltage controlled current source $Y_{12a}V_o$, where V_o is the output voltage. The gain of the feedback network is modeled by a voltage controlled current source $Y_{12f}V_o$ with a finite internal admittance modeled as Y_{11f}. The feedback network also provides a feed-forward gain of $Y_{21f}V_i$ with an internal admittance Y_{22f}. Develop a circuit model for this shunt-shunt feedback amplifier. Prove that the trans-conductance gain of the shunt-shunt feedback amplifier is given by:

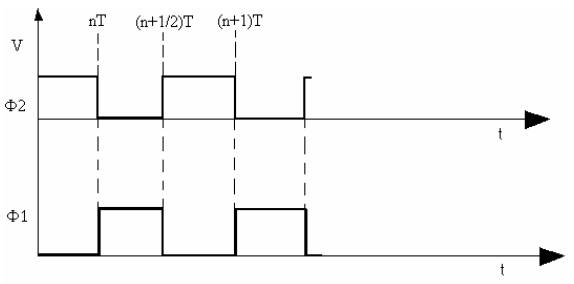
$$\frac{V_o}{I_s} = -\frac{\dfrac{\left(Y_{21a}+Y_{21f}\right)}{\left(Y_S+Y_{11a}+Y_{11f}\right)\left(Y_L+Y_{22a}+Y_{22f}\right)}}{1-\dfrac{\left(Y_{21a}+Y_{21f}\right)}{\left(Y_S+Y_{11a}+Y_{11f}\right)\left(Y_L+Y_{22a}+Y_{22f}\right)}\left(Y_{12a}+Y_{12f}\right)}$$

. Suppose, for practical analysis purposes we assume that the signal transmitted by the basic amplifier is much greater than the signal fed forward by the feedback network. Also, to a reasonable approximation, we may assume that the signal fed back by the feedback network is much greater than the signal fed through the basic amplifier. Under the conditions, prove that the trans-conductance gain of the shunt-shunt feedback amplifier is given by

$$\frac{V_o}{I_s} \approx -\frac{\dfrac{Y_{21a}}{\left(Y_S + Y_{11a} + Y_{11f}\right)\left(Y_L + Y_{22a} + Y_{22f}\right)}}{1 - \dfrac{Y_{21a}Y_{12f}}{\left(Y_S + Y_{11a} + Y_{11f}\right)\left(Y_L + Y_{22a} + Y_{22f}\right)}}$$. You must obtain this second expression as a limiting approximation of the first expression being derived. 5+7+4=16

2. Consider a switched capacitor filter as shown in figure 1 (a):





1 (a) 1(b)

Figure 1

The filter consists of a switched capacitor integrator consisting of an op-amp, a sampling capacitor C_S, an integrating capacitor C_I and four voltage controlled switches. The load capacitor C_L represents the sampling capacitor following the integrator plus any parasitic capacitances that may be present. Each switch in the schematic is controlled by one of two non overlapping clock signals $\phi 1$ and $\phi 2$, that control the operation of the circuit as well as typical input and output waveforms. The timing diagram of the clock signals are shown in figure 1 (b). Assume that the time period of each clock signal is T and its frequency is given by $f = \frac{2\pi}{\varpi}$. Also assume that each clock signal has 50% duty cycle which means the signal is on for exactly half the time period. The switches close when the control inputs to the switch are 1 (indicated by high pulse) and open when the control inputs to the switch are 0 (indicated by low pulse). Let V_S be the input signal of the integrator and V_O is the output signal of the integrator. Show that the frequency response of the circuit is given by:

$$\frac{V_O(j\varpi)}{V_S(j\varpi)} = \frac{C_S}{C_I}\left(\frac{1}{\sin\dfrac{\varpi T}{2}}\right)\left(\frac{e^{-\frac{j\varpi T}{2}}}{2j}\right).$$ 14

3. Consider the circuit shown in figure 2:

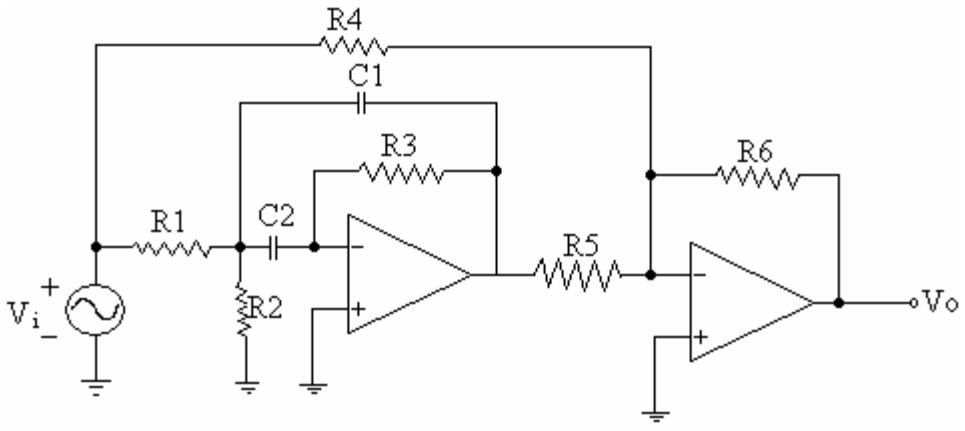


Figure 2

Show that if C1and C2 are equal, the circuit operates like a band reject filter if $\frac{R5}{R4} = \frac{R3}{2R1}$ 14

4. A 60Hz sinusoidal signal of 7.5V (rms) obtained from power outlet, is used as an input to a bridge rectifier. The average load current is expected to be 10mA. Use battery models with threshold voltage V_γ=0.7V for the diodes. Find the dc component of the output if no filter capacitor is used. Find the ripple voltage, dc component of the output voltage and the peak current through the diode, if a 47μF filtering capacitor is used in the circuit. 6