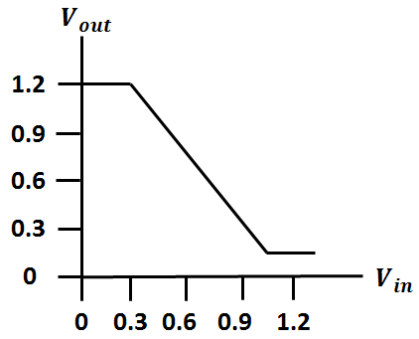
Intro. To VLSI (ECE361)

Assignment #2

Q1. Consider the nMOS transistor in a 0.6µm process with gate oxide thickness of 100Å. The doping level is $N_A = 2 \times 2^{17} cm^{-3}$ and the normal threshold voltage is 0.7V. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 4V instead of 0? [2 Marks]

Q2. Does the body effect of a process limit the no. of transistors that can be placed in series in a CMOS gate at low frequencies? Explain. [2 Marks]

Q3. A novel inverter has the transfer characteristics shown below. What are the values of V_{IL}, V_{IH}, V_{OL} and V_{OH} that give best noise margins? What are these high and low noise margins? [4 Marks]

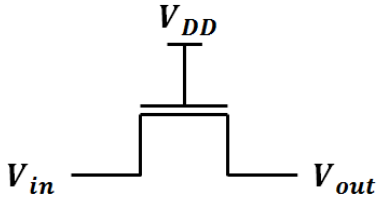


Q4. Draw the schematic of a Half Adder and a Full Adder (Max. 28 transistors) using complementary CMOS Logic. Can you think of a novel design that may reduce no. of transistors used?

[8+2 Marks]

Q5. Suppose V_{DD} = 1.2 V and V_t = 0.4 V. Neglecting body effect, determine V_{out} in the following circuit for:

i. V_{in} = 0 V
ii. V_{in} = 0.6 V
iii. V_{in} = 0.9 V
iv. V_{in} = 1.2 V



[2 Marks]