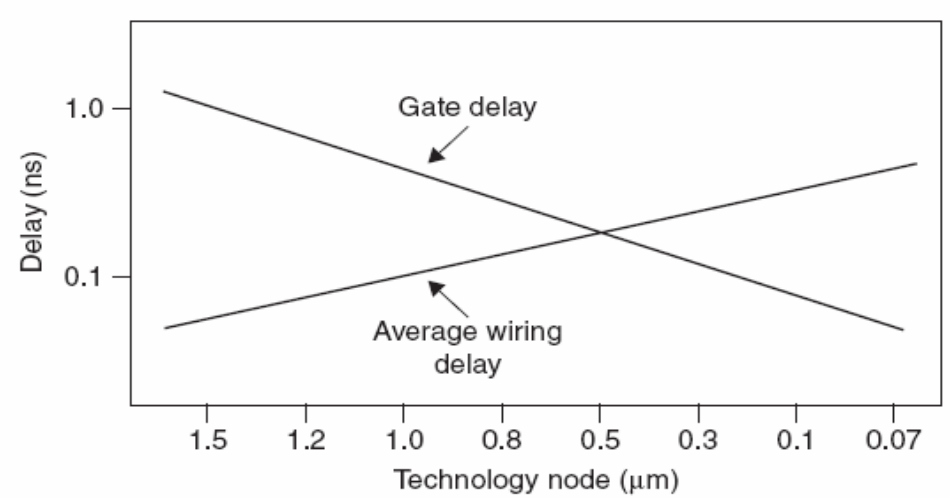
High Speed Interconnects in ICs

Dr. Shubhajit Roy Chowdhury,

Centre for VLSI and Embedded Systems Technology,
IIIT Hyderabad, India

Email: src.vlsi@iiit.ac.in

Introduction



•Local wire delay decreases with feature size due to a reduction in distance among active devices

•However overall speed of current ICs is most often limited by the long distance global interconnects

Introduction

- With shrinking feature size and larger chip die dimensions, sheer number of interconnects has increased exponentially
- Interconnect capacitance often dominates total gate load
  - therefore, a large portion of the total transient power is dissipated by these on-chip lines
  - particularly true for those long interconnects that distribute the clock signals
    - that can dissipate 40–50% of total IC power
- Gains achieved in performance with technology scaling are often accompanied by an increase in power dissipation
  - e.g., additional interconnect layers enhance circuit speed at the expense of higher power consumption due to the larger interconnect capacitance

Introduction

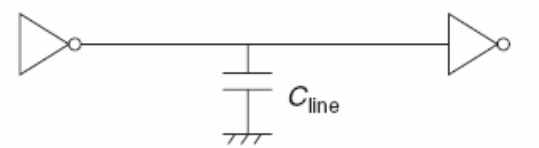
- In addition to interconnects among the various on-chip devices, the clock and power distribution networks require significant metal resources
  - both must span the entire chip
- Accurately modeling the clock, power, and signal nets is a difficult task
  - highly complex structures
- Optimally allocating metal to properly design these networks presents an even greater challenge
  - because of complexity in developing interconnect models

Deep Sub-micron Interconnect Design

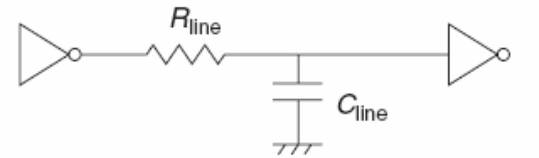
- Scaling of the lateral dimensions in planar devices, such as MOS transistors, has produced improvements in device
  - area
  - power
  - speed
- Power consumption and signal propagation delays of long (global) resistive lines have increased
- Accurate on-chip interconnect models are required
  - to determine the signal characteristics and design requirements of high speed DSM interconnect

Deep Sub-micron Interconnect Design

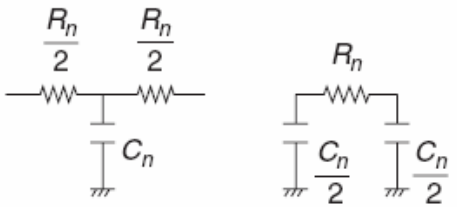
- A local line can be modeled as a single lumped capacitor
  - signal propagation delay is negligible compared to gate delay



- Longer lines must include resistive effect

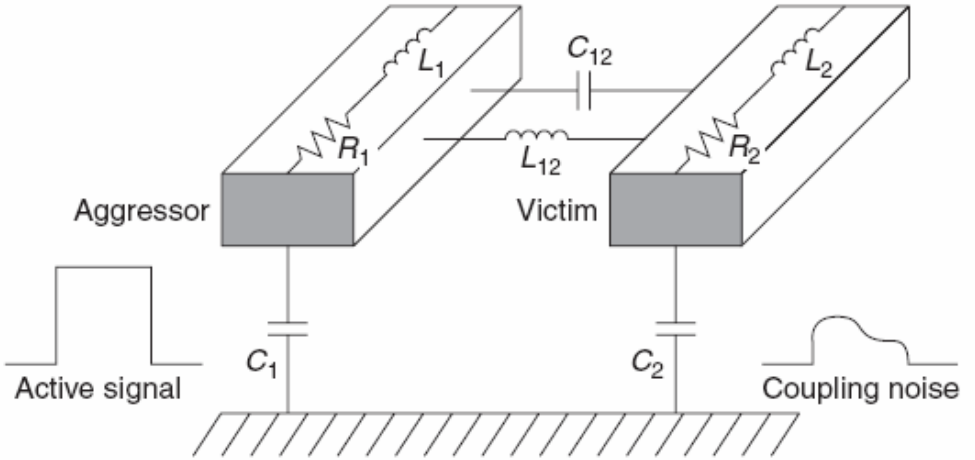


  - Long interconnect models often divide the line into sections - distributed impedance model
    - T or Π
    - accuracy depends on no. of sections



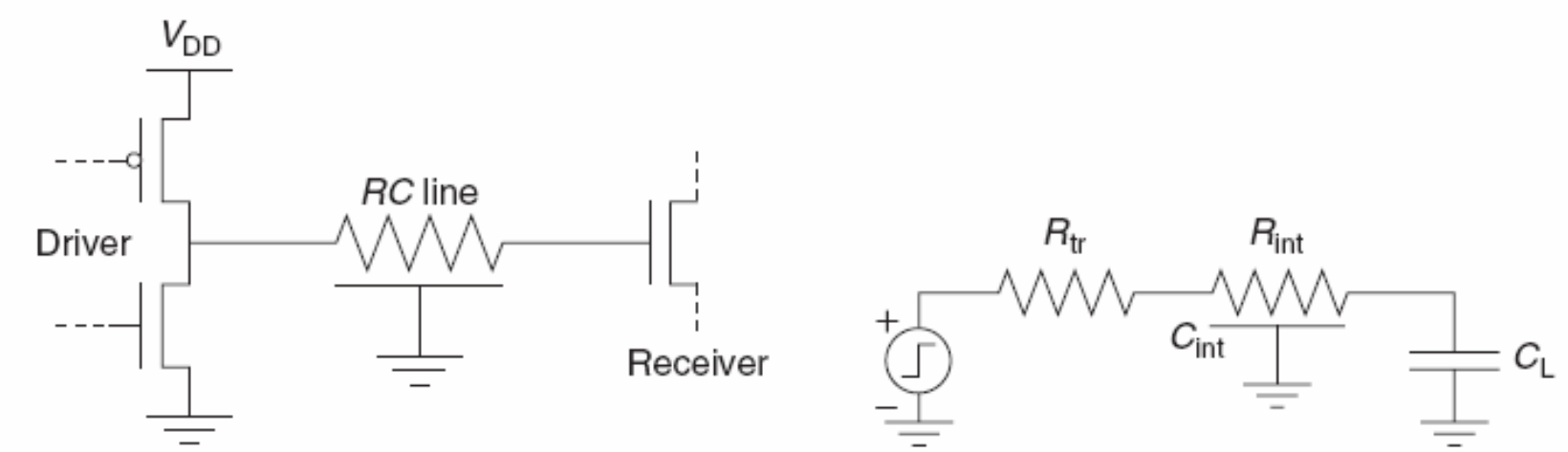
Low Power High Speed Circuit Design Techniques

- High Speed Circuit Design Goal: Improve performance
- Power and noise are important when considering design techniques to optimize circuit performance
- Noise affects delay, degrades waveform shape, and most importantly, creates the possibility of an erroneous interpretation of the digital signals



Wire Sizing

- Width of an interconnect affects the power characteristics and propagation delay
- Consider a CMOS inverter driving an *RC interconnect* line
  - Simple first order model of delay

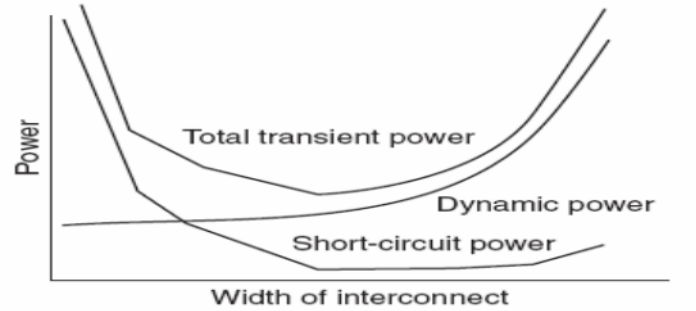


Wire Sizing

- Increasing the driver transistor width reduces R_{tr}
  - decreasing the circuit delay
  - trading off circuit power and area for higher speed
- Increasing the width of the interconnect to reduce R_{int} does not significantly reduce the delay caused by the RC interconnect impedance
  - since decrease in wire resistance is offset by increase in wire capacitance
- Many algorithms have been proposed to determine the optimum wire size that minimizes a target cost function
  - minimizing delay
  - addressing reliability issues by reducing clock skew
- Few approaches for simultaneous driver and wire sizing

Wire Sizing

- Tradeoffs exist between dynamic and short-circuit power



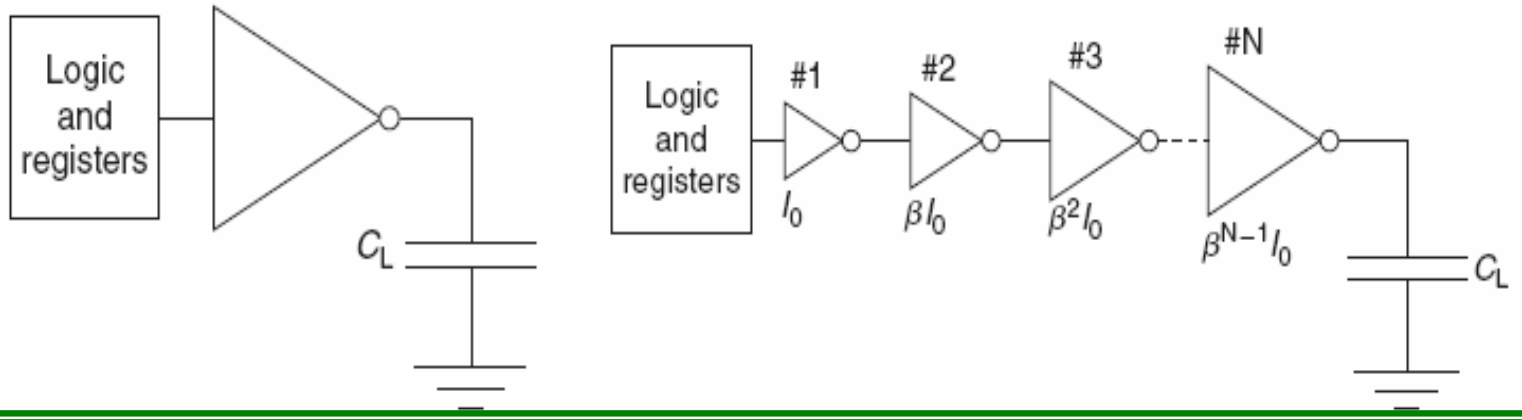
  - As line inductance-to-resistance ratio increases with wider lines, short-circuit power decreases due to reduction in signal transition time
  - For an RC line, short-circuit power remains approximately constant with increasing width
  - decrease in interconnect resistance offset by an increase in capacitance
  - If width of interconnect exceeds a specific limit, short-circuit power increases
    - change in the matching characteristics between driver and interconnect
  - Dynamic power increases with width since line capacitance is greater

Driver sizing

- Transistor sizing techniques aim to lower delay
- Wider transistors have a few advantages but also several disadvantages
  - + produce more current
  - + reduce charge time of load capacitance
  - – have greater physical area
  - – have larger gate capacitance
  - – increased circuit area and power
- A careful balance of the current drive and output load is necessary to enhance circuit performance
- Power optimal transistor size is smaller than the power-delay optimal transistor size

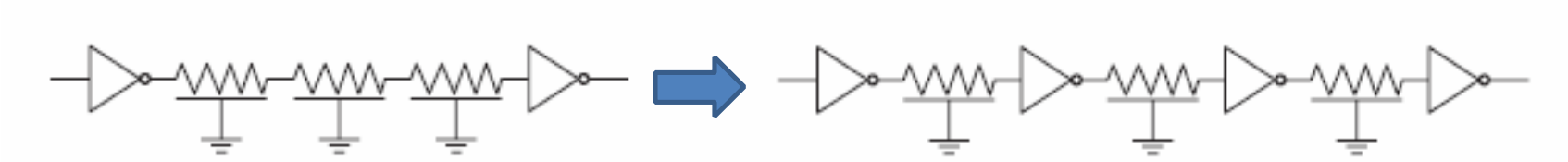
Tapered Buffers

- An important example of transistor sizing is tapered buffers
  - Used to drive large capacitive loads
- Consists of chain of inverters of gradually increasing size
- Ratio of size of an inverter to size of the preceding inverter is the tapering factor β
- Delay of tapered buffer system is less than delay of a single large inverter



Regenerative Repeaters

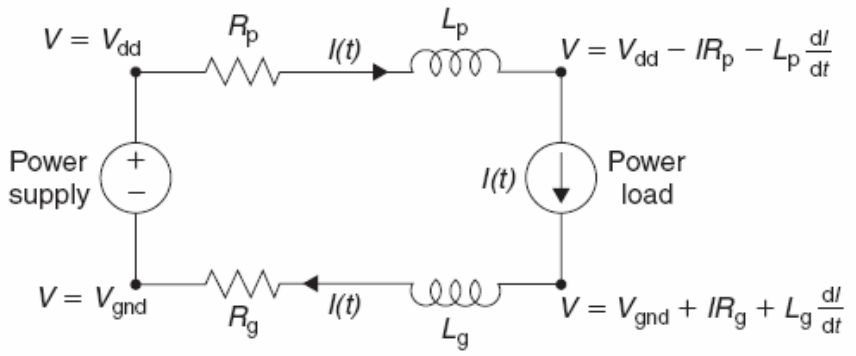
- An effective strategy for reducing delay of a long interconnect is to strategically insert buffers along a line
- Repeaters circumvent quadratic increase in interconnect delay by partitioning the line into smaller and approximately equal sections



- Sum of section delays is smaller than delay of original path since delay of each section is reduced
- Decreased interconnect delay is partially offset by the additional delay of the inserted repeaters

Power Distribution Techniques

- Power grid consists of a supply, load, and interconnect lines connecting the supply to the load



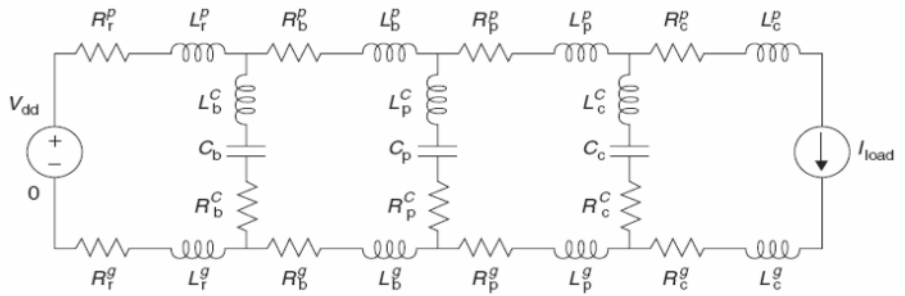
- Interconnect lines connecting the power supply to the load are non-ideal with a finite resistance and inductance,
  - R_p , L_p and R_g , L_g , for the power and ground lines, respectively
- Change in supply voltages at the load terminal is referred to as power supply noise

Power Distribution Techniques

- Power supply noise can adversely affect circuit operation
- Power supply variations reduce rail-to-rail power voltage, causing gate-to-source voltage across both NMOS and PMOS transistors to also decrease
  - lowering the output drive current of these devices
  - signal delay increases, compared to delay under nominal power supply voltage
- Power noise affects propagating clock and data signals by causing an increase in both delay and delay uncertainty within the data paths
  - severely limit the maximum operating frequency of an IC

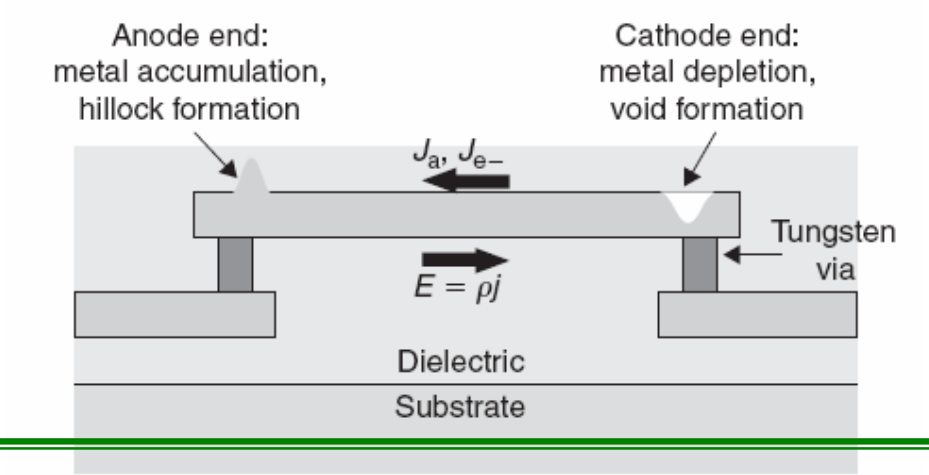
Power Distribution Techniques

- Power distribution network should exhibit a minimal impedance at terminals of the load
  - to ensure a small variation in the power supply voltage
- Decoupling capacitors ensure correct and reliable operation
  - distributed across a system, placed at board, package, and on-chip levels
  - provide charge when transient current demands on power grid are high
  - each decoupling capacitor provides transient current to the load, effectively reducing the local transient noise



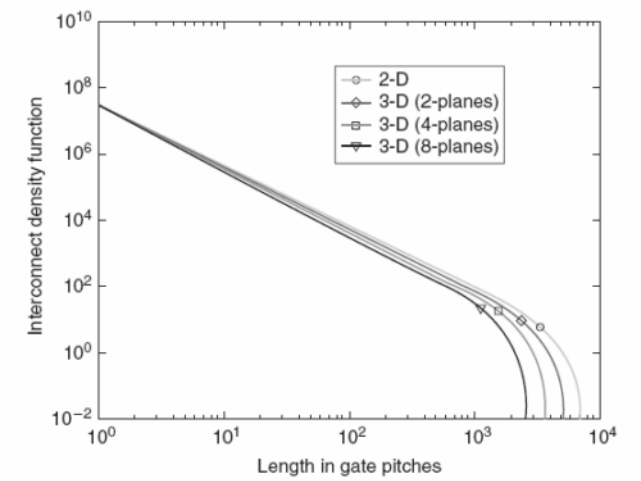
Power Distribution Techniques

- On-chip current densities can reach several hundred thousand amperes per sq. cm, leading to electromigration
- Electromigration is the transport of metal atoms under the force of an electron flux
  - depletion and accumulation of metal material resulting from atomic flow can lead to formation of extrusions and voids in metal structures
  - extrusions and voids can lead to short circuits and open circuit faults



3D interconnects

- 3-D interconnects have been proposed as a way to address increasing line delay and capacitive crosstalk
- Introduction of a third dimension significantly alters distribution of the interconnect length in ICs
  - As the number of planes is increased, the length and number of the global (local) interconnects decrease (increase)



Summary

- Complexity of properly designing interconnects in the DSM regime increases with each successive technology generation
  - Choice between RC or RLC dependant on several factors
- Low power, high speed circuit techniques are essential to expand battery lifetime and maintain ambient thermal levels
  - Wire and driver sizing, as well as repeater insertion critical
- Clock and power distribution are important applications of the general interconnect design problem
  - noise and skew must be considered during design
- Novel techniques such as 3D interconnects in interconnect design can help alleviate challenges in emerging ICs
  - e.g. longer line lengths, greater line impedances, increased signal delays

THANK YOU