Class Test

VLSI Architectures

1. A certain system consists of a data-path modeled by the following set of assignments:

$$a = i + j;$$

$$b = k + l;$$

$$c = a + b;$$

$$d = b + n;$$

$$e = c + m;$$

$$f = c + e;$$

The operations are to be implemented using single bit full adders, where the delay of the adder is 40ns. The overflow is to be indicated by means of a 1 bit carry flag. Consider the circuit as resource dominated. Draw a scheduled sequencing graph for a minimum latency schedule with 100ns clock cycle time. Show the resource binding on the sequencing graph. Suppose, now the number of resources are reduced to two. Draw the corresponding sequencing graph for a minimum latency schedule showing the necessary resource bindings. In each case draw the data-path showing the resources, registers and multiplexers. 20