## Assignment 2

## (Architectural optimization)

1. Consider the FFT problem given in assignment 1. Suppose we are given an ALU capable of performing only addition, subtraction and logic operations. Estimate with the help of sequencing graphs the approximate number of clock cycles needed to accomplish the operations.

2. Model a micro-programmed control unit for the FFT processor assuming the ALU and multiplier are available. Suppose we decentralize the controller into two discrete controllers for multiplication and addition and/or comparison. Evaluate the performance gain or loss in the whole process.

3. Suggest suitable modifications in the structural design of the FFT processor realized by you in assignment 1 to realize a power optimized implementation of the processor. Realize the model of the processor in VHDL.