VLSI Architectures

Assignment -5

Memory Design

1. Consider a 1KX64 bit SRAM. The memory consist of1K words, each consisting of 64 bits arranged as a 256X256 array of 6T SRAM cells. A word is selected for reading by the row and column decoders. The row decoder asserts one of the 256 word-lines. Each word-line selects a row of four 64 bit words. Four selected words feed the input of the 4:1 MUX controlled by the outputs of the column decoder. Each access transistor in the memory cell is 4λ in width. Each SRAM cell is 40λX40λ. Use TSMC 180nm CMOS process.
   (a) Estimate the average power being dissipated and the maximum power being dissipated.
   (b) Estimate the average delay to access a word from the memory..