Design for Testability

Solutions to Question Paper of Mid Semester Examination 2, 2013.

1. VHDL model of nibble comparator:—

```
-- VHDL model of 1bit comparator.
library ieee;
use ieee.std_logic_1164.all;
entity bit_comparator is
port (a,b, gt, eq, lt : in std_logic;
      a_gt_b, a_eq_b, a_lt_b : out std_logic);
end bit_comparator;

architecture gate_level of bit_comparator is
signal im1,im2, im3, im4, im5, im6, im7, im8, im9, im10 : std_logic;
begin
    im1 <= not a;
    im2 <= not b;
    im3 <= a nand im2;
    im4 <= a nand gt;
    im5 <= im2 nand gt;
    a_gt_b <= im3 nand im4 nand im5;
    im6 <= im1 nand im2 nand eq;
    im7 <= a nand b nand eq;
    a_eq_b <= im6 nand im7;
    im8 <= im1 nand b;
    im9 <= im1 nand lt;
    im10 <= b nand lt;
    a_lt_b <= im8 nand im9 nand im10;
end gate_level;

--VHDL model of nibble comparator
library ieee;
use ieee.std_logic_1164.all;
library work;
use work.all;
entity nibble_comparator is
port (a,b: in std_logic_vector(3 downto 0);
      gt, eq, lt : in std_logic;
      a_gt_b, a_eq_b, a_lt_b: out std_logic);
end nibble_comparator;

architecture iterative of nibble_comparator is
component bit_comparator
  port (a,b, gt, eq, lt : in std_logic;
        a_gt_b, a_eq_b, a_lt_b : out std_logic);
end component;
signal im: std_logic_vector (0 to 8);
begin
  C0: bit_comparator port map (a(0), b(0), gt, eq, lt, im(0), im(1), im(2));
  C1_2: for i in 1 to 2 generate
    C: bit_comparator port map (a(i), b(i), im(i*3-3), im(i*3-2), im(i*3-1), im(i*3+0), im(i*3+1), im(i*3+2));
  end generate;
```

```
c3: bit_comparator port map (a(3), b(3), im(6), im(7), im(8), a_gt_b, a_eq_b, a_lt_b);
end iterative;
```

Test bench of nibble comparator:-

```
library ieee;
use ieee.std_logic_1164.all;

entity nibble_comparator_test_bench is
end nibble_comparator_test_bench;

architecture input_output of nibble_comparator_test_bench is
component nibble_comparator
    port (a,b: in std_logic_vector (3 downto 0);
          gt, eq, lt          :in std_logic;
          a_gt_b, a_eq_b, a_lt_b : out std_logic);
end component;
signal a,b: std_logic_vector(3 downto 0);
signal eql, lss, gtr : std_logic;
signal vdd : std_logic := '1';
signal gnd : std_logic := '0';
begin
  a1 : nibble_comparator port map (a, b, gnd, vdd, gnd, gtr, eql, lss);
  a2: a <= "0000",
           "1111" after 500ns,
           "1110" after 1500ns,
           "1110" after 2500ns,
           "1010" after 3500ns,
           "0000" after 4000ns,
           "1111" after 4500ns,
           "0000" after 5000ns,
           "0000" after 5500ns,
           "1111" after 6000ns;
  a3 : b <= "0000",
            "1110" after 500ns,
            "1111" after 1500ns,
            "1100" after 2500ns,
            "1100" after 3500ns,
            "1111" after 4000ns,
            "1111" after 4500ns,
            "1111" after 5000ns,
            "0000" after 5500ns,
            "0000" after 6000ns;
end input_output;
```

2. Analysis of circuit given in figure 1:

a b c	Fault free	a stuck at 1	f stuck at 1	b stuck at 1
0 0 0	0	0	1	0
0 0 1	1	1	1	0
0 1 0	0	1	1	0
0 1 1	0	1	1	0
1 0 0	0	0	1	1
1 0 1	1	1	1	1
1 1 0	1	1	1	1
1 1 1	1	1	1	1
Function				
Transition count	3	3	0	1
Signature analysis	001	101	001	010
Syndrome	4	6	8	4

3.