**THE DESIGN OF A FINITE STATE VENDING MACHINE**

**INTRODUCTION TO VLSI DESIGN FINAL PROJECT**

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***Abstract*—This document contains a detailed design description of top to down level design hierarchies of a Vending Machine , which has several flexible features as well as host a lot of state of the art facilities like Change return , Cancel option .**

**I. DESIGN SPECIFICATION**

The cost of the product to be distributed is = RS 6

The possible inputs are -> RS 1,RS 2 , RS 5 , RS 10 .

* We are not limiting the amount of change in the vending machine.
* If Rs 10 coin is available it can only be give as input at the start.
* We also have not given any limit to the amount of the product.
* When the input amount crosses Rs6 the product and the change are given (no stacking of product)

**Equations for change**

C0=cp2’p1’p0+c’p2’p1p0’i2’i1i0+cp2’p1p0+ p2p1’p0’i2’i1i0c’ +c p2p1’p0’

C1=p2’p1p0’c+p2’p1p0i2’i1i0c’+p2’p1p0c

C2=p2cp1’i2i1’+p2’p1’p0c’i2’i1+c’p2p1p0’i2i0’

Expression for output:

Out=c’[s2’s1’s0’i2i1’i0’+s2s1’s0’(i2’i1)+s2s1’s0(i2’(i1’i0’+i1i0’+i1’i0))+s2’s1i2’i1i0

**Equations for state**

D0=c’[ p2’p1’p0i2’i0’ + p2’p0’i2’i0+ p2’p1p0i2’i0’+p2p1’i2’i0]

D1=c’[{p2’p0’+p2p0}p1’i2’i1i0}+p2’p1’p0i2’(i1i0’+i1’i0)+p2’p1p0i2’i1’]

D2=c’[p2’p1’p0’i2’i1i0+i2i1’i0’)+p2’p1p0’i2’i1i0’]+p2’p1p0i2’(i1i0’+i1’i0)

***II DIVISION OF FUNCTIONING OF THE VENDING MACHINE***

*THE WORKING OF THE MACHINE CAN BE SIMPLY BE MAPPED INTO THREE WAYS OF OPERATION THAT IS WITH THE*

*INPUT less than Rs 6*

*INPUT greater than or equal to Rs 6*

IN FIRST CASE OF INPUT I AM CONSIDERING ONLY TWO INPUT THAT IS

O/P WITH A CHANGE (1-5) AND NO PRODUCT IN CASE OF CANCEL

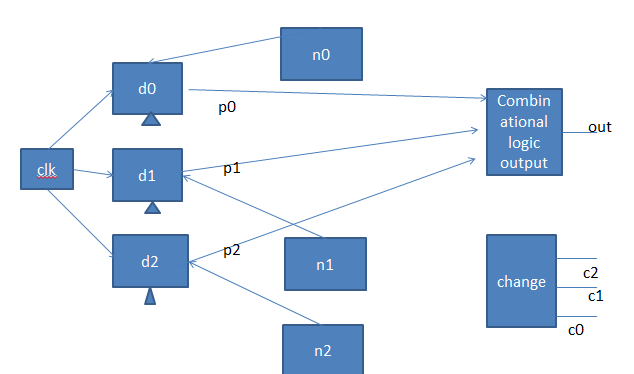
OR

*O/P WITH CHANGE AND PRODUCT IN CASE ALREADY THERE IS SOME INPUT BEFORE.*

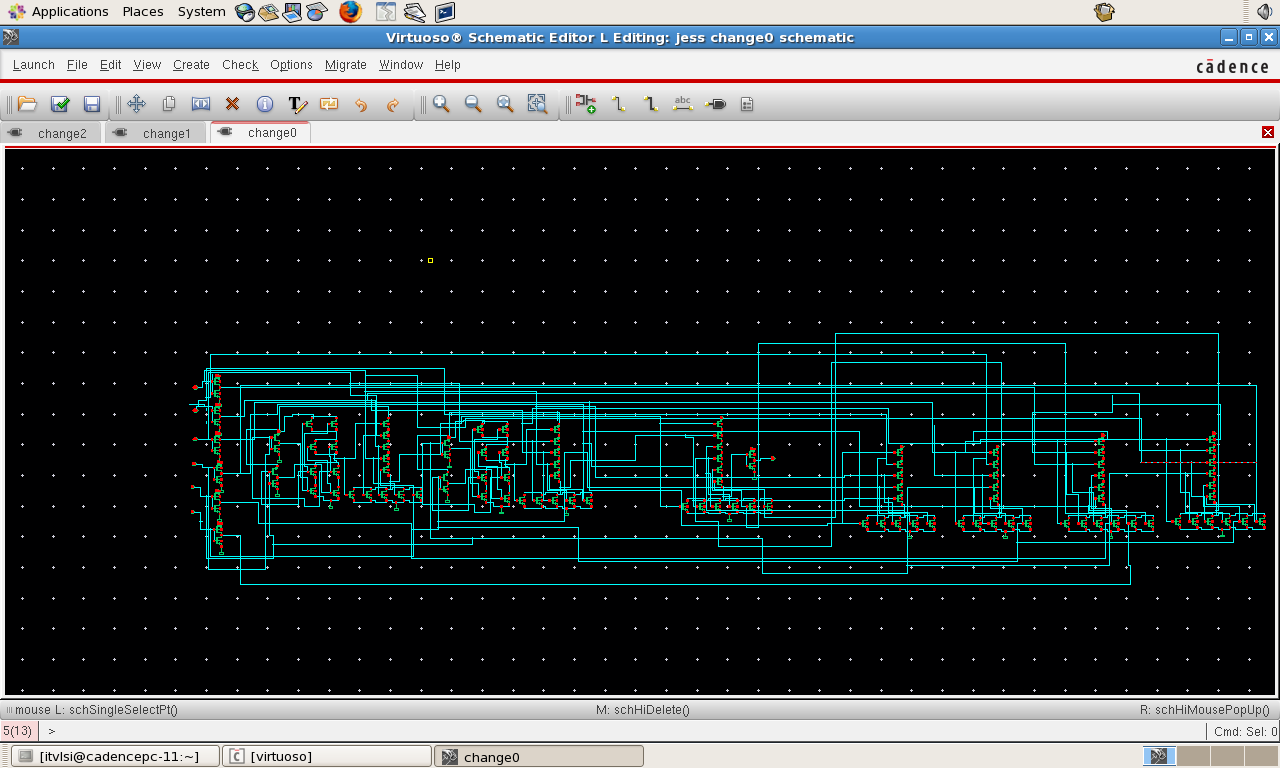
*IN SECOND CASE OF INPUT I AM CONSIDERING ONLY OUTPUT OF AGAIN ONE TYPE LIKE*

*O/P WITH A PRODUCT AND CHANGE FOR RS 7 AND MORE AND O/P WITH PRODUCT AND ZERO CHANGE FOR RS 6.*

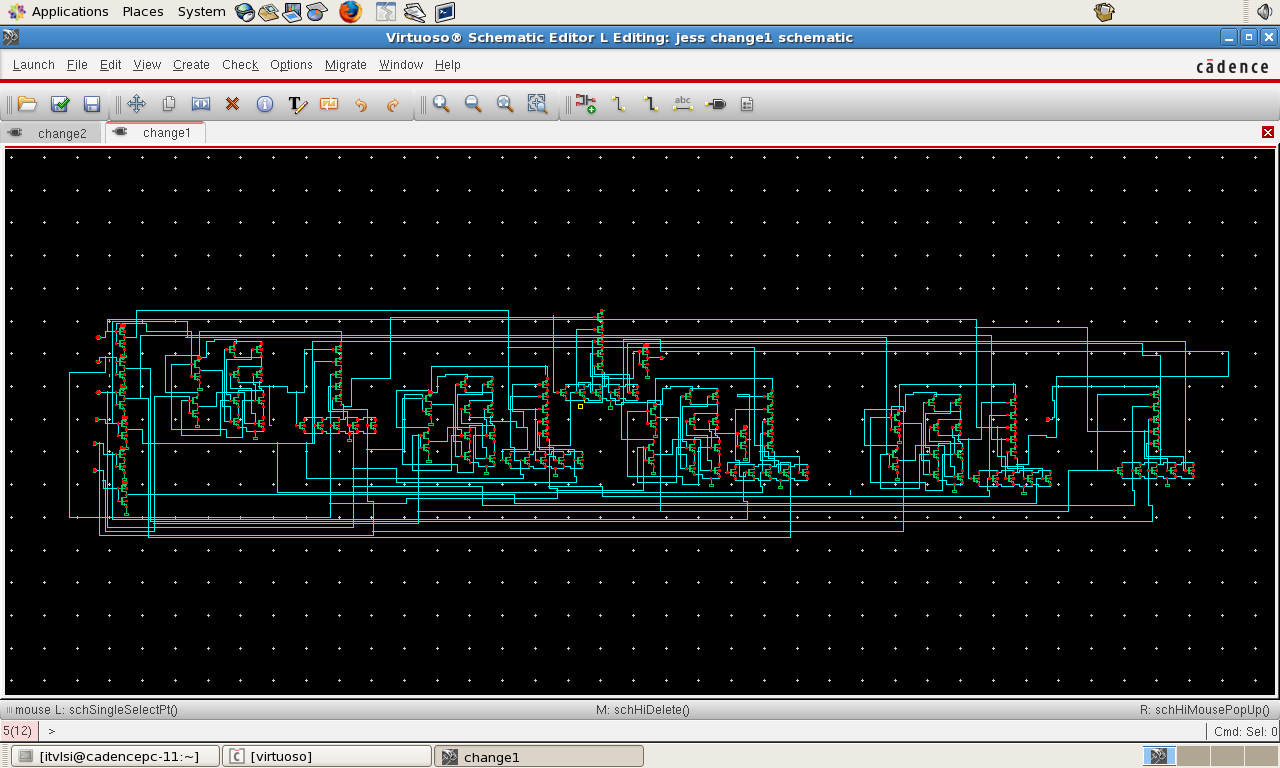
**State machine:**

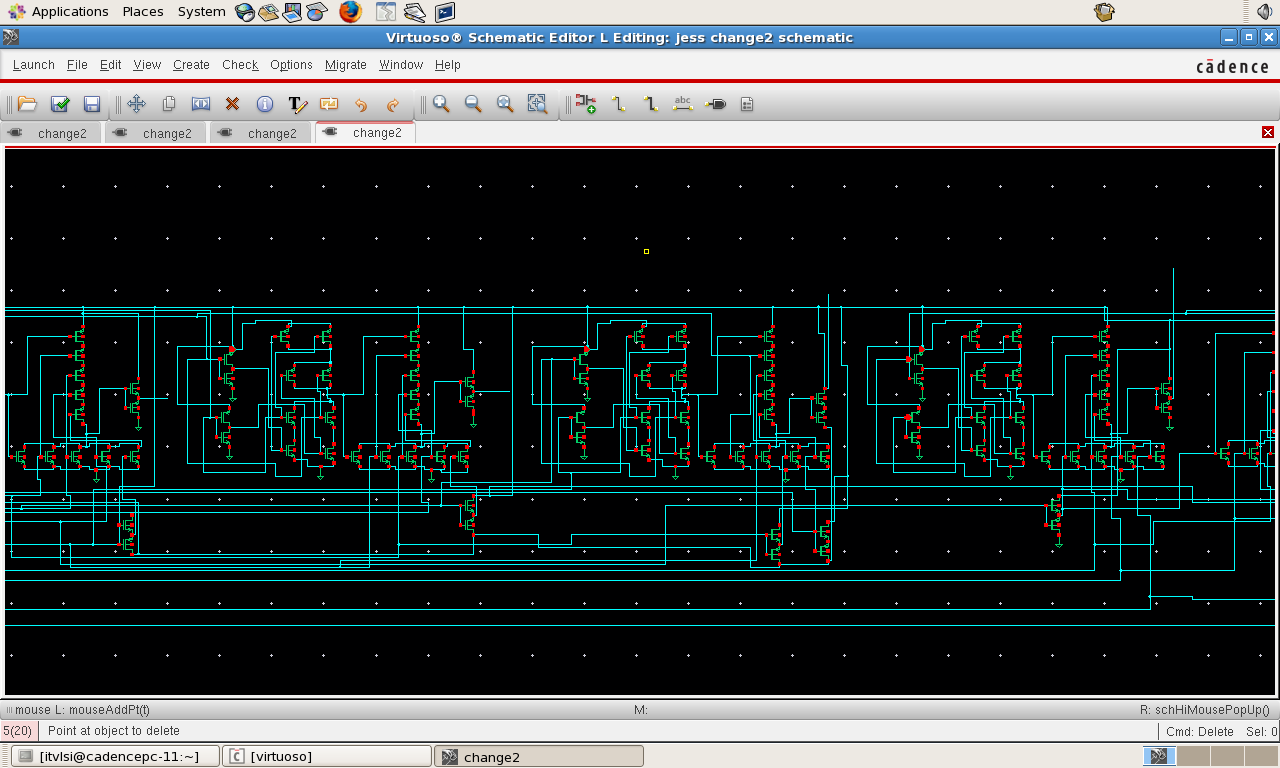


Schematics:change

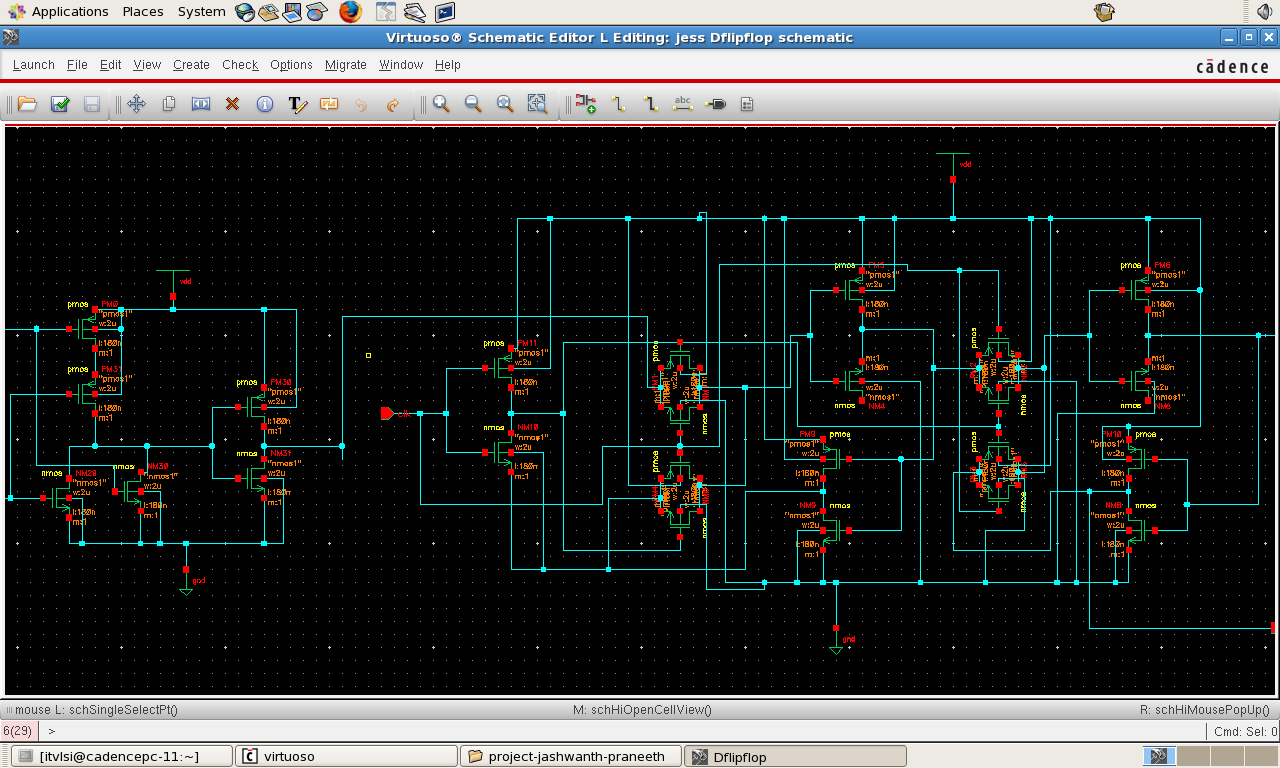


Total schematic

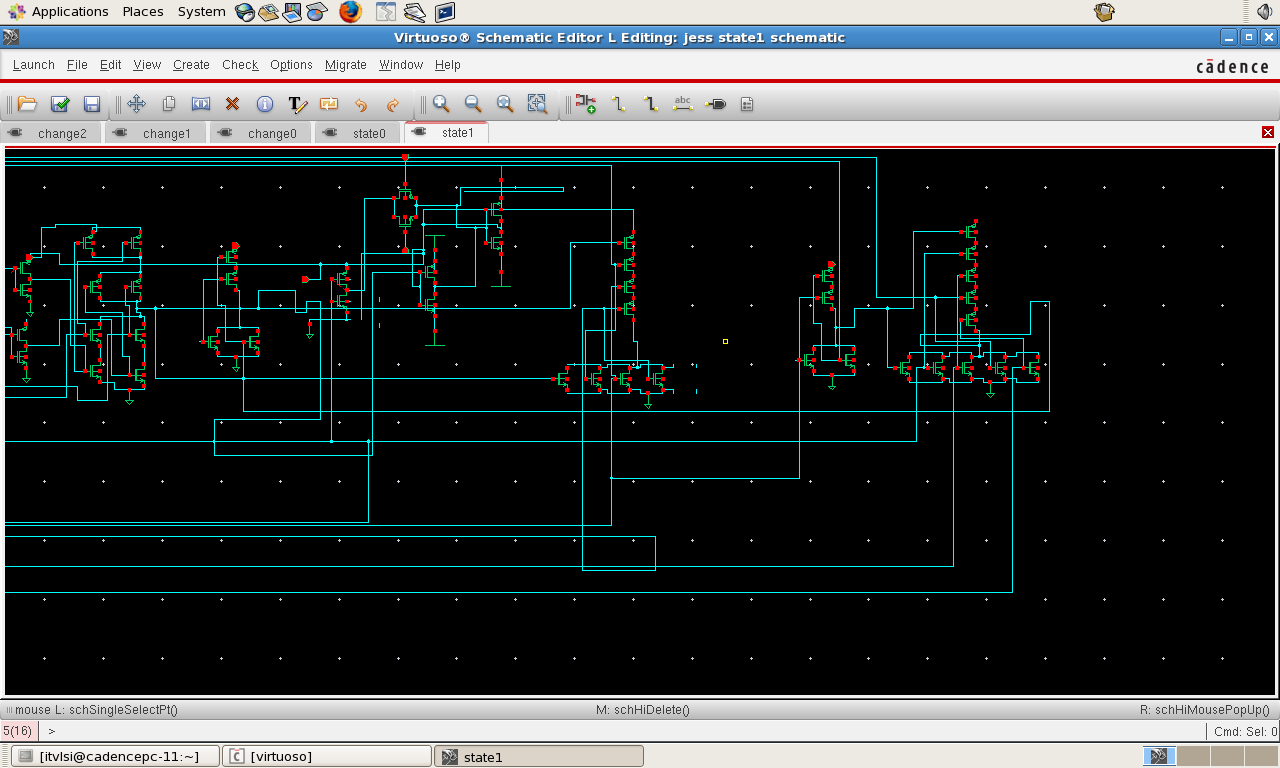


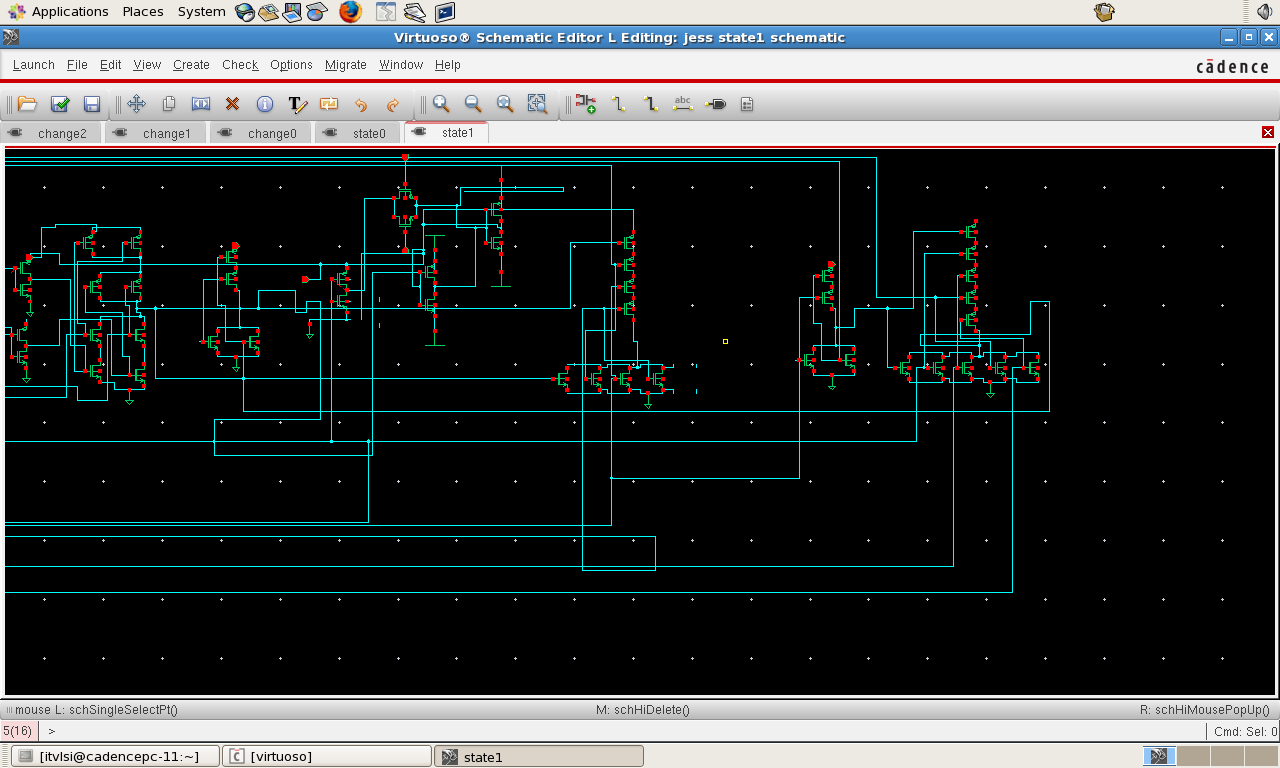


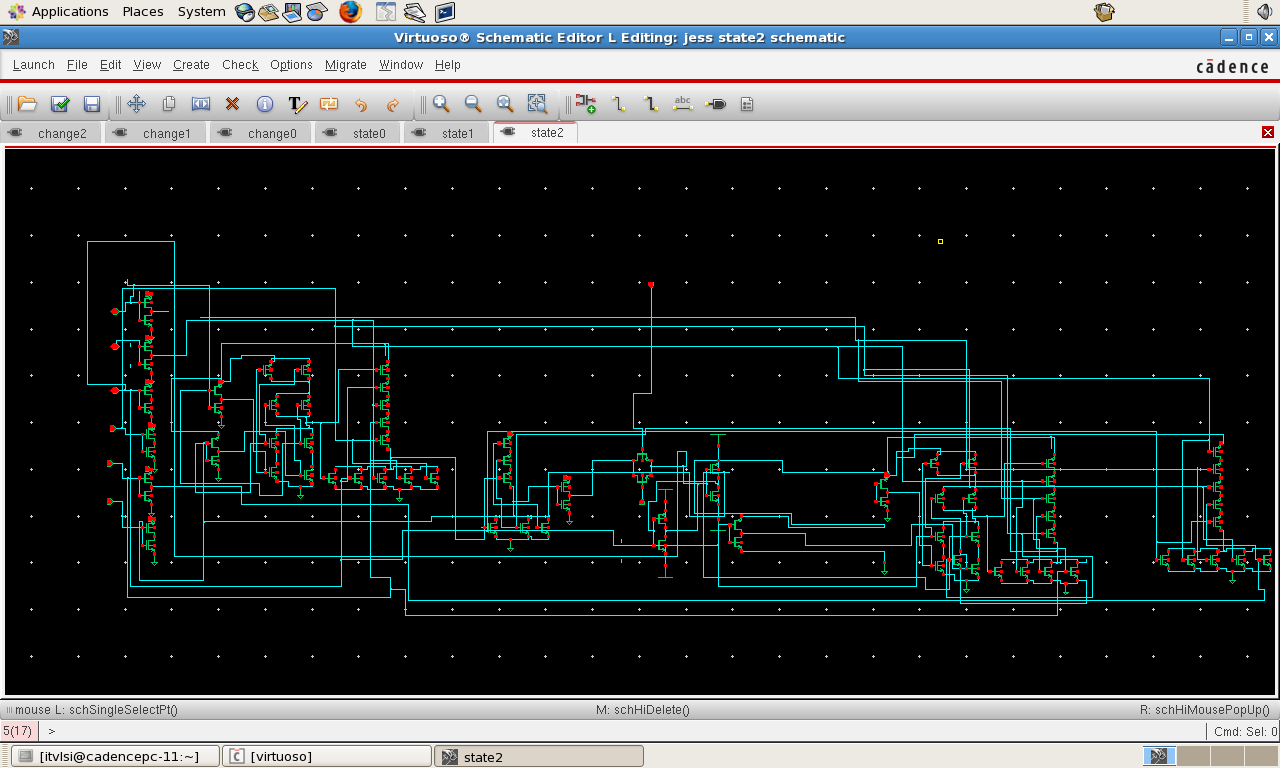
D flip flop



Schematic:states







THE POWER DISSIPATION CONSISTS OF TWO PARTS DYNAMIC POWER DISSIPATION AND STATIC POWER DISSIPATION .

FOR REDUCTION OF DYNAMIC POWER DISSIPATION WHICH IS DEPENDENT ON THE RELATION THAT THE DYNAMIC POWER = αCLV2f

 WE MADE SURE THAT AT THE OUTPUT LINE

OF ANY BLOCK OF OURS WE KEPT MINIMUM NUMBER OF TRANSISTORS EITHER IN PARALLEL OR IN SERIES TO MINIMIZE CL AS MUCH AS POSSIBLE KEEPING THE REQUIRED SIZING OF TRANSISTORS CONSTANT OR AS PLACED BY THE CADENCE VIRTUOSO TOOL .

 WE KEPT A SUPPLY OF 1.5 V INSTEAD OF THE STANDARD 5 V WHICH WE HAD EARLIER USED IN ALL OUR LAB ASSIGNMENTS .

 NOW MOST IMPORTANTLY WE NOTED WHICH STATES ARE FLIPPING MOST OFTEN AND THEN ACCORDINGLY APPLIED THEM SUCH THAT FROM OTHER STATES TO THIS STATES THIS STATE FLIPS THE MINIMUM

NUMBER OF TIMES .

**DYNAMIC POWER DISSIPATION MINIMISATION**

WE MADE A DISTRIBUTION OF WHAT STATES OCCUR WHAT NUMBER OF TIMES AND ACCORDING TO OUR DISTRIBUTION WE FOUND THAT S0 OCCURS MOST OFTEN FOLLOWED BY THE S1 STATE SWITCHING NOW TO REDUCE f THE FREQUENCY OF TRANSITIONS ULTIMATELY RESULTING IN A LOWER NUMBER OF DYNAMIC POWER DISSIPATION , WE CAME TO THE CONCLUSION THAT OUR CALCULATIONS TO THE BEST ASSIGNMENT OF THE STATES OF THE VENDING MACHINE AS IN GRAY CODING FOR 3 BITS .

Change bits are represented by c2,c1,c0 and the assignment is done as follows

Rs0=000

RS1=001

Rs2=010

Rs3=011

Rs4=100

Rs5=101

**ASSIGMENT OF INPUT STATES(MINIMIZES STATIC POWER DISSIPATION )**

* S0 – 000
* S1 – 001
* S2 – 010
* S3 – 011
* S4 – 100
* S5 – 101

**DESIGN SUMMARY**

TOTAL TRANSISTORS USED IN DESIGN OF VENDING MACHINE =167

**DESIGN OPTIMISED FOR ->**

STATIC POWER DISSIPATION DYNAMIC POWER DISSIPATION TRANSISTOR NUMBER MINIMISATION LOAD CAPACITANCE MINIMISATION

ACKNOWLEDGMENT

This Projects success can be attributed to our DIGITAL VLSI DESIGN PROFESSOR SYED AZEEMUDDIN without whome we could not have taken any serious encouragement or patience to complete our work . I would also like to acknowledge my Teaching Assistants

Rituraj Yadav Sachin Kumar Aakash Agarwal Shubham Gupta

REFERENCES

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IEEE EXPLORE

EE 470 , EE 141 repectively for various INTRICACIES IN DESIGN INVOLVED .