

Jashwant Raj Gunasekaran

407 South Corl St, Apt 7, State College, PA 16801, Ph: (814) 777-5967
Email: jashwant.raj92@gmail.com, Webpage: www.cse.psu.edu/~jqg5490

EDUCATION	<p>PhD Student in <i>Computer Science and Engineering</i> Aug '14 - Present Advisors: Dr Chita Das & Dr Mahmut Kandemir CGPA 3.6/4, Pennsylvania State University, University Park, Concentration in Cloud Computing Systems</p> <p>Bachelor of Engineering in <i>Computer Science and Engineering</i> Aug '09 - May '13 CGPA 8.24/10, Anna University, Chennai, India</p>
RESEARCH FOCUS	<p>I work on resource management in cloud with specific focus on Machine learning applications, to optimize for (i) tenant-side performance & cost and (ii) provider-side energy efficiency & utilization. Looking for potential opportunities in Distributed Cloud HPC systems research. I am also interested in exploiting heterogeneity in datacenters and characterizing overall system performance.</p>
PUBLICATIONS	<p><i>Tackling Resource Under-utilization in the Serverless Era.</i> <i>(Middleware'20).</i></p> <p><i>Multidimensional Optimization of Ensemble learning-based inference serving.</i> <i>(NSDI-revision).</i></p> <p><i>Characterizing bottlenecks in hosting microservices on Serverless Functions Chains.</i> <i>(ICDCS'20).</i></p> <p><i>Implications of Public Cloud Resource for Model Serving Applications.</i> <i>(WoSC'20).</i></p> <p><i>Dynamic VM provisioning for High Performance Computing platforms.</i> <i>(CCGrid'20).</i></p> <p><i>Energy harvesting through dynamic orchestration in GPU-based Datacenters.</i> <i>(CLUSTER'19).</i></p> <p><i>Exploiting Serverless Functions for SLO and Cost Aware Resource Procurement.</i> <i>(CLOUD'19).</i></p> <p><i>Constraint aware scheduling for Cloud Systems: Developed a trace driven scheduler for constraint aware scheduling in heterogeneous cloud architectures</i> <i>(ICDCS'17).</i></p>
INDUSTRY EXPERIENCE	<p>Intern- VMware Office of CTO, Boston MA Jun '19 - Aug '19</p> <ul style="list-style-type: none">Design a proof-of-concept integration between HPC job scheduling mechanisms and VMware virtualization software to help create a dynamic virtual machine provisioning model for virtualized HPC. The work was published in CCGRID'20. <p>Intern- Qualcomm Inc</p> <ul style="list-style-type: none">Part of wifi firmware team. Worked on adding a new software power management feature into existing MAC firmware module. Jun '16 - Aug '16Part of the Android power optimization, I developed a tool to enable log collection and process the logs to obtain critical power utilization metrics. Jun '15 - Aug '15 <p>Software Engineer- Qualcomm Inc, Chennai India Jun '13 - Jul '14</p> <ul style="list-style-type: none">Developed coded tests to validate the various Qualcomm proprietary features and also automated several wifi functionality tests. Technologies Used: SWAT automation, Networking protocols, Perl. Proposed a patent application named Processor Capacity Sharing
INTERESTED DOMAINS	<p><i>Performance Evaluation, Workload profiling and characterization, Cloud computing: Public Cloud, Serverless Computing, Docker Containers, Kubernetes, Distributed resource management</i></p> <p>Operating Systems: Virtualization, Linux Kernel Development, Device Drivers and Firmware.</p>
TECHNICAL SKILLS	<p>Cloud services: Docker containers, Mesos, Kubernetes, AWS lambda, Azure ML, Programming : C, C++, Python, JavaScript, Bash/Shell, Java, OpenMP ML frameworks: Tensorflow, Mxnet, Pytorch DataBase Technologies : MYSQL, Oracle Web Technologies: HTML, CSS, XML</p>

RELEVANT COURSE WORK	Graduate Operating Systems, Graduate Computer Architectures, Data Structures and Algorithms, Object Oriented Programming using Java and C, Multiprocessor Architecture, Public Cloud Computing,
COURSE PROJECTS	<p><i>Distributed file system:</i> Developed a parallel distributed file system (like NFS) which handles all file handling and multiple user file access.</p> <p><i>Slab Memory Allocator:</i> Developed memory allocation scheme based on buddy and slab level allocation policies used in linux kernels.</p> <p><i>Implementing Cache:</i> Developed L1 cache architecture with various cache replacement policies.</p> <p><i>Multithreaded synchronization:</i> Designed a thread-level synchronization mechanism using path expression which directs the rules for desired order of execution for multiple real application scenarios.</p> <p><i>Multilevel thread scheduler:</i> Designed a multilevel thread FCFS, SJB and MLFQ scheduler for a realtime Operating System.</p>
TEACHING EXPERIENCE	Teaching and instruction assistant for undergraduate programming practice course, undergraduate and graduate operating systems course.
PROPOSAL WRITING	<p>Re-Engineering Galaxy for Performance, Scalability and Energy Efficiency, NSF Award #1931531.</p> <p>Cross-Layer Design for Cost-Effective HPC in the Cloud, NSF Award #2028929</p>