COL215: Help session: HW assignment 2

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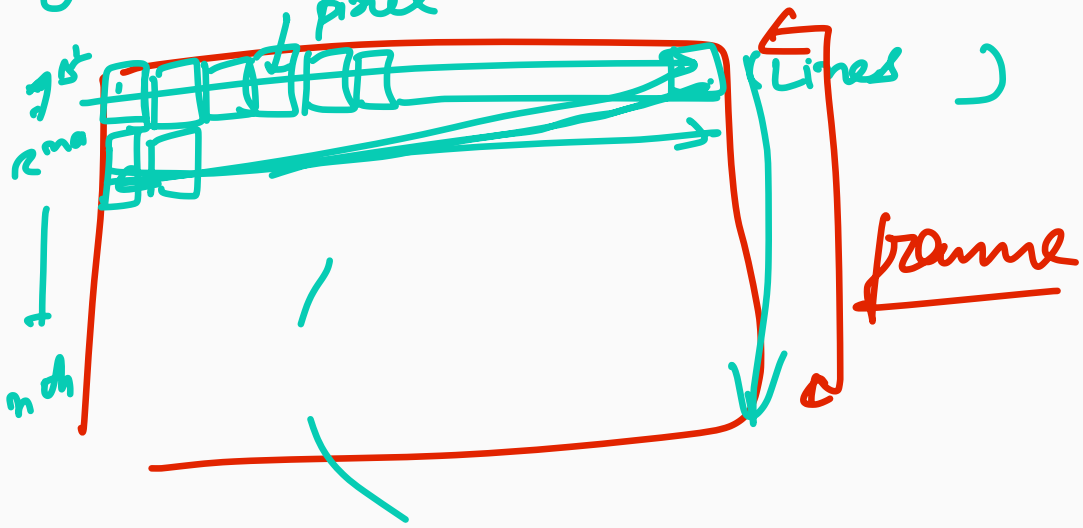
Overview

1. VGA overview
2. Timings
3. VHDL modules

VGA overview

Display timings: CRT monitors

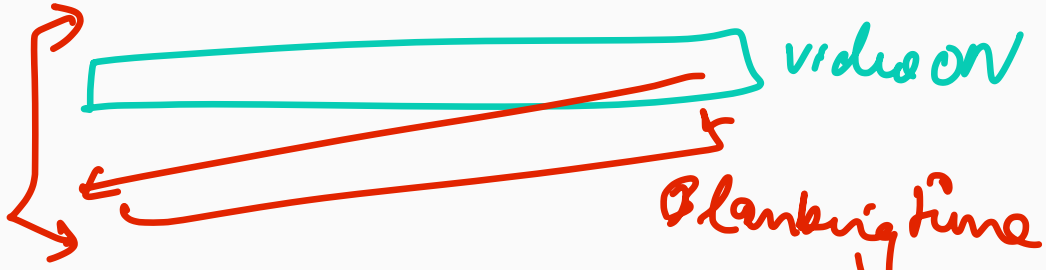
CRT Cathode Ray display



LCD LED
OLED

Display timing standard (VESA group)

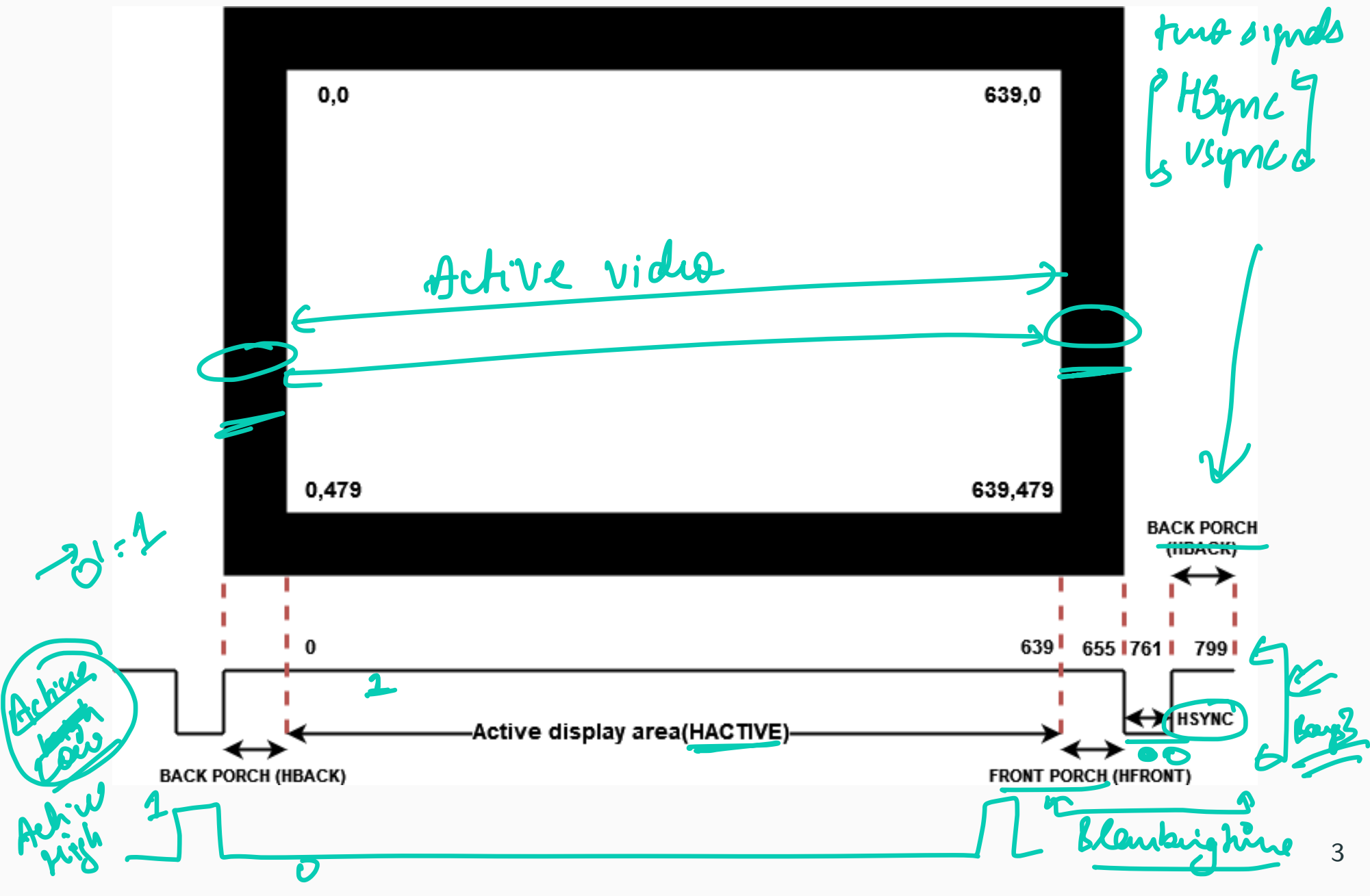
720p →
1980 FHD →



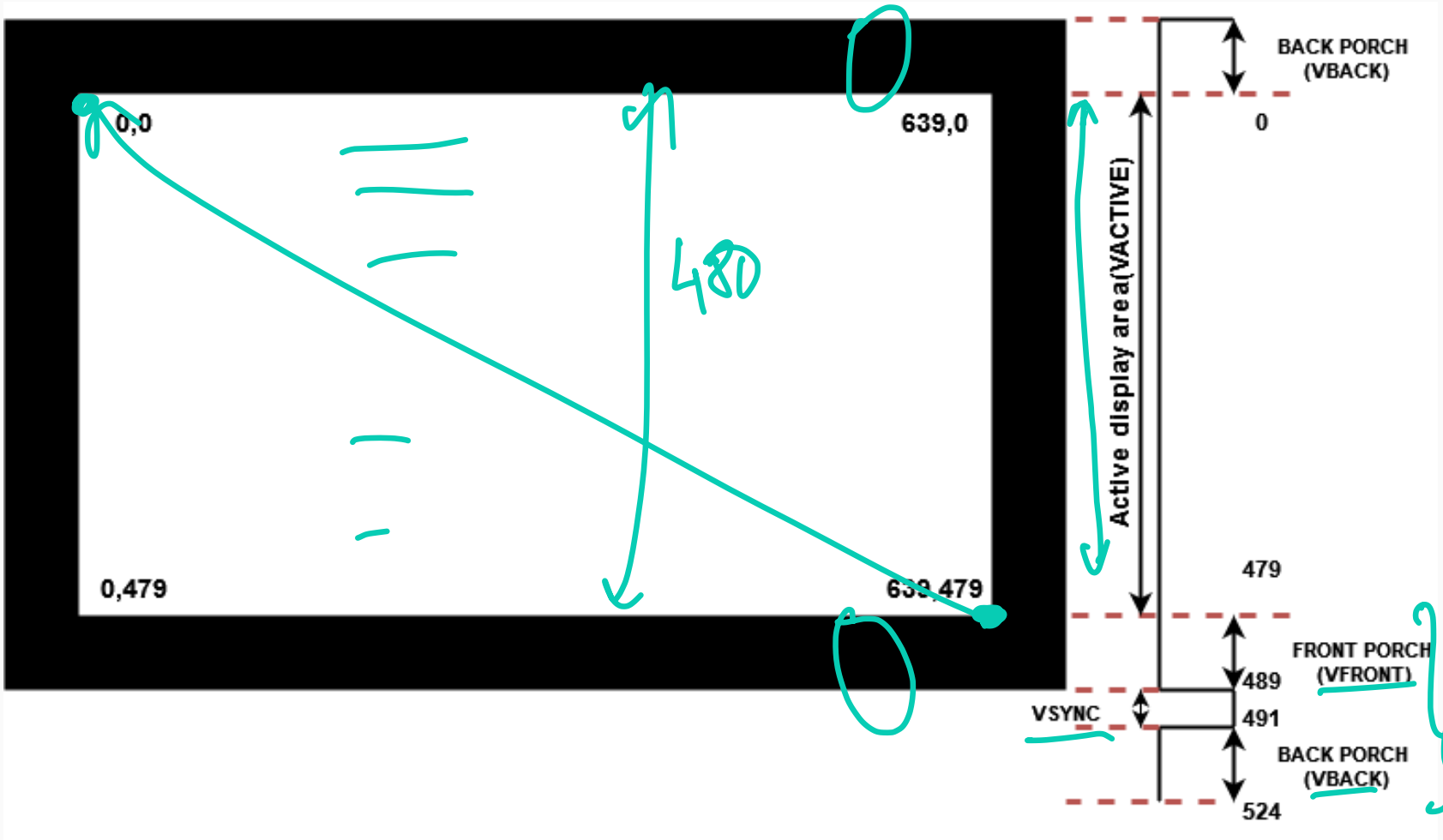
640x480@60Hz

60 frames per seconds

Display timing basics



Display timing basics



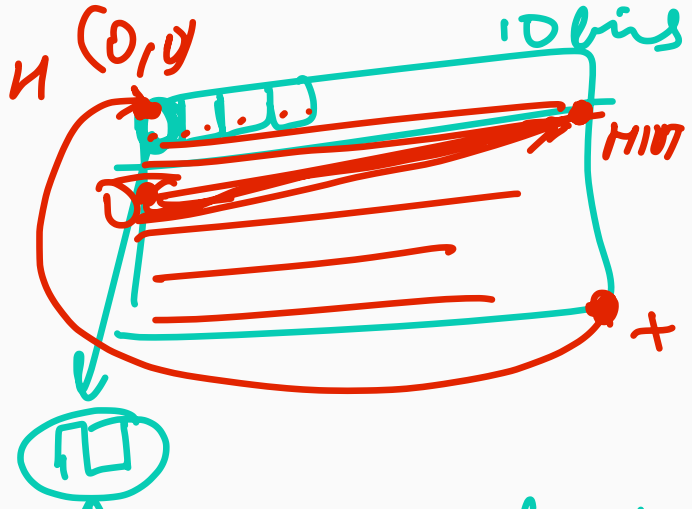
Timings

Display timings

Table 1: 640x480@60

Parameter	Value
Pixel clock	25 MHz
HSYNC	96 pixels
HBACK	48 pixels
HFRONT	16 pixels
HACTIVE	640 pixels
VSYNC	2 lines
VBACK	33 lines
VFRONT	10 lines
VACTIVE	480 lines

Display timings



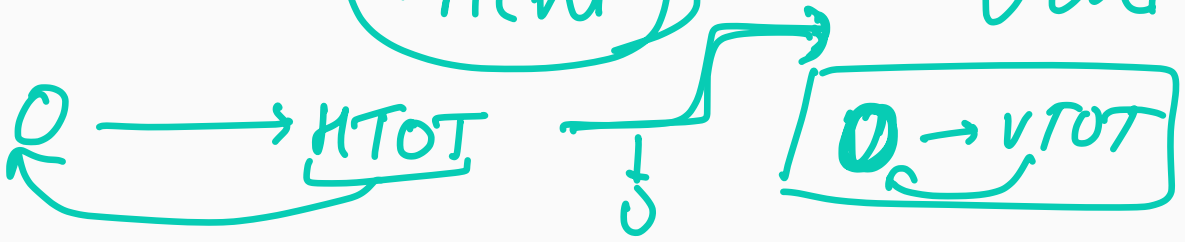
10 pixels are displayed

pclk pixel clock (twice to display one pixel)

controller → keep track of count of pixels in one line + one frame

Hcnt

Vcnt (line) count



Pixel clock calculation

Total number of pixels in one horizontal line (active+blanking) will be :

$$HTOT = HACTIVE + HBACK + HFRONT + HSYNC$$

$$800 = 640 + 48 + 16 + 96$$

Total number of lines in one frame will be :

$$VTOT = VACTIVE + VBACK + VFRONT + VSYNC$$

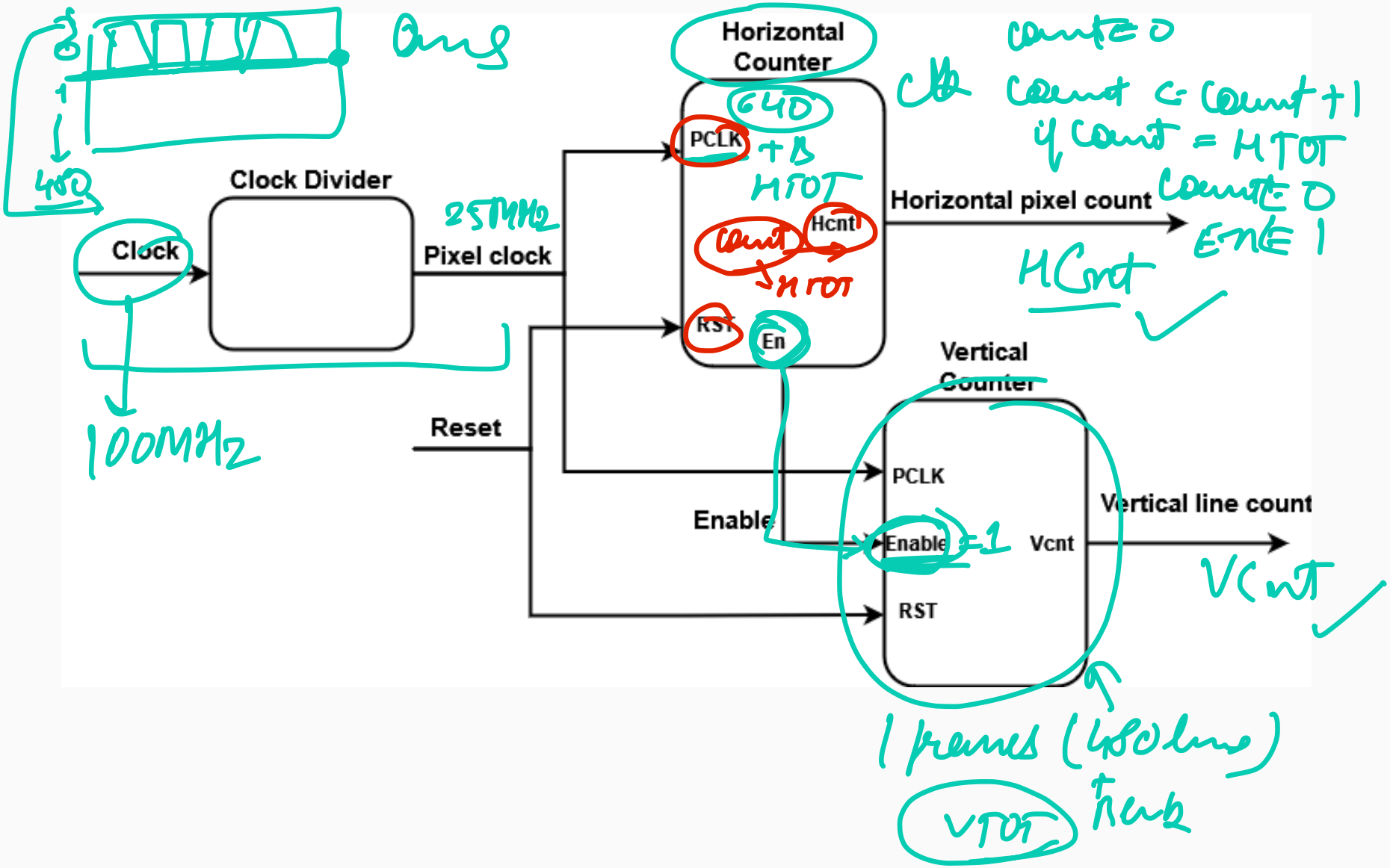
$$525 = 480 + 33 + 10 + 2$$

Total number of pixels in one frame are, **420000** to be displayed in fixed amount of time that is **16.66 ms** (60 Hz or 60 frames per seconds).
Thus, time period for the clock for one pixel will be (25.2 MHz):

$$420000 * 60 = 25200000$$

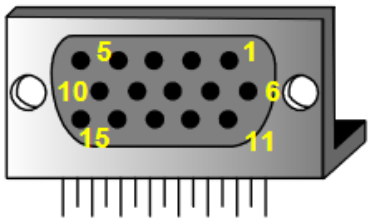
VHDL modules

Modules in VGA controller

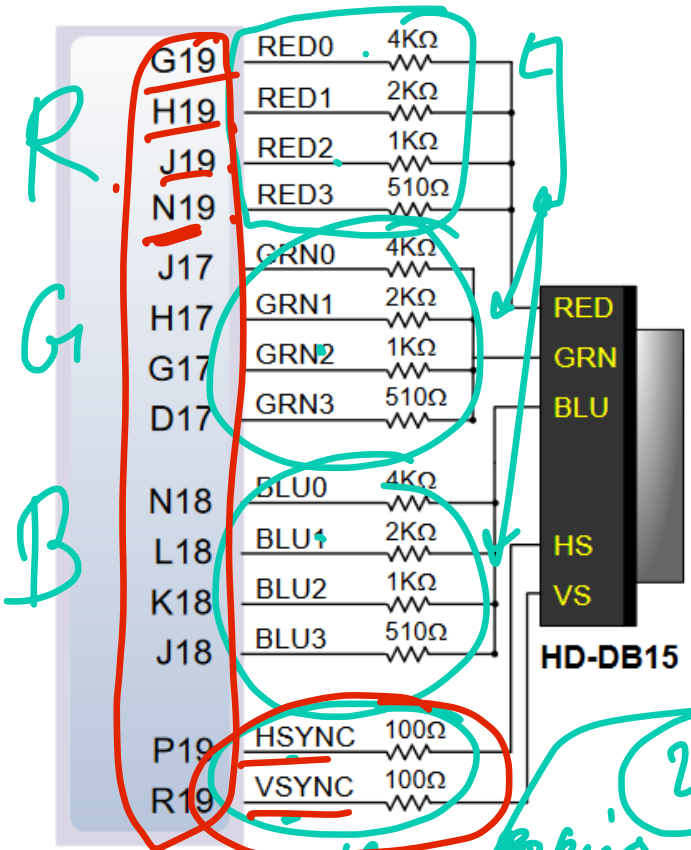


Modules in VGA controller

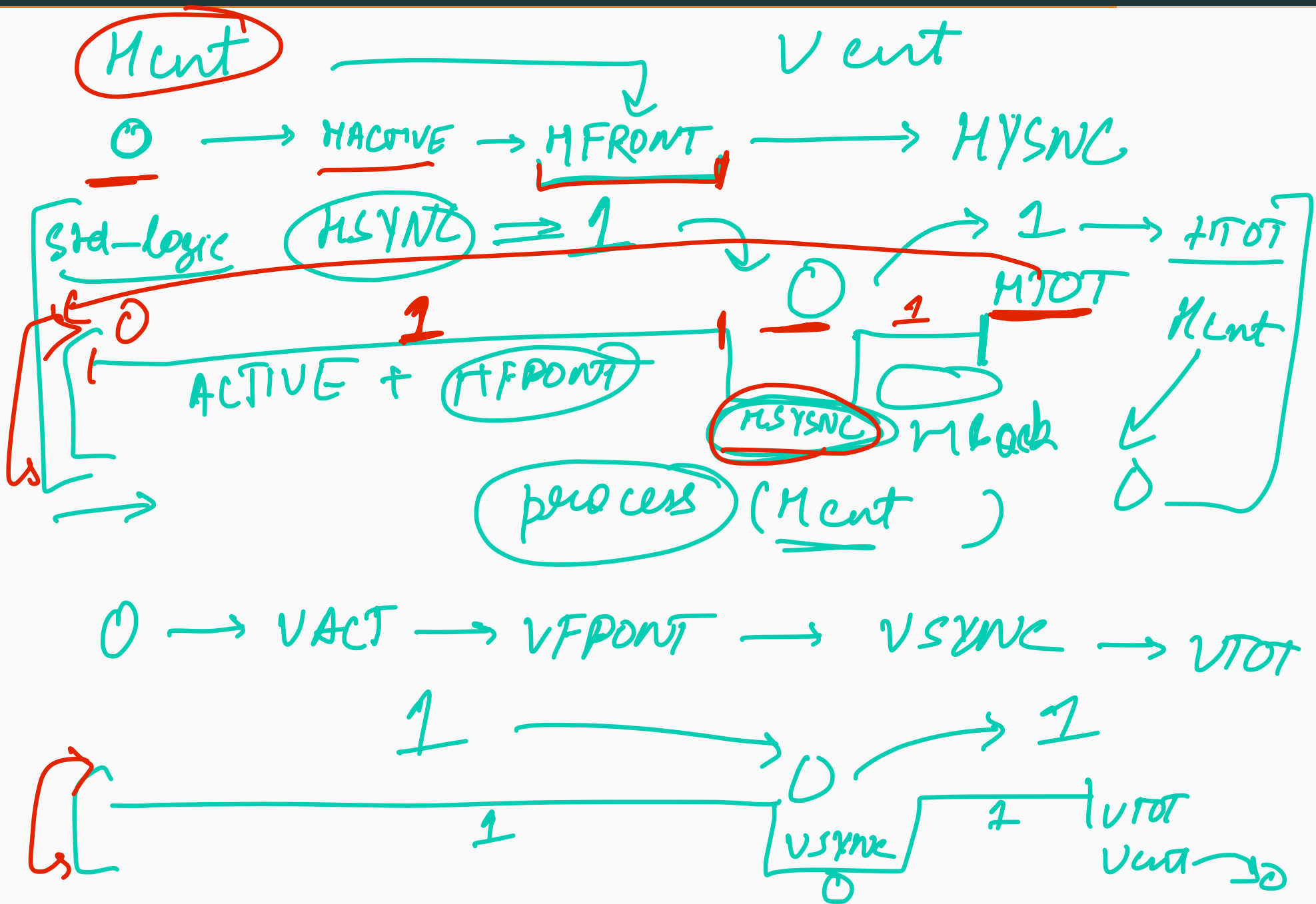
Output Signals from FPGA to Monitor



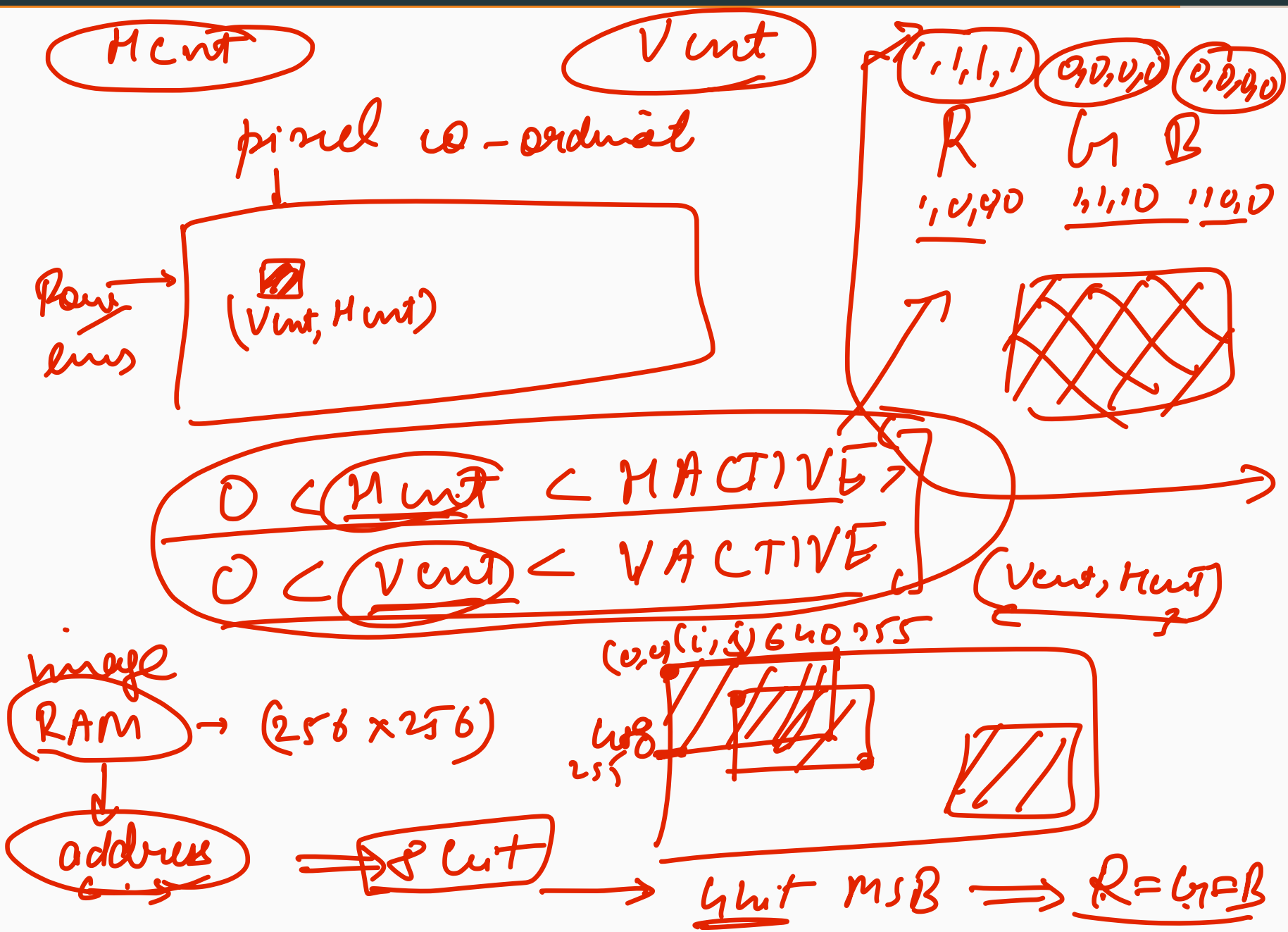
Pin 1: Red
Pin 2: Grn
Pin 3: Blue
Pin 13: HS
Pin 14: VS
Pin 5: GND
Pin 6: Red GND
Pin 7: Grn GND
Pin 8: Blu GND
Pin 10: Sync GND



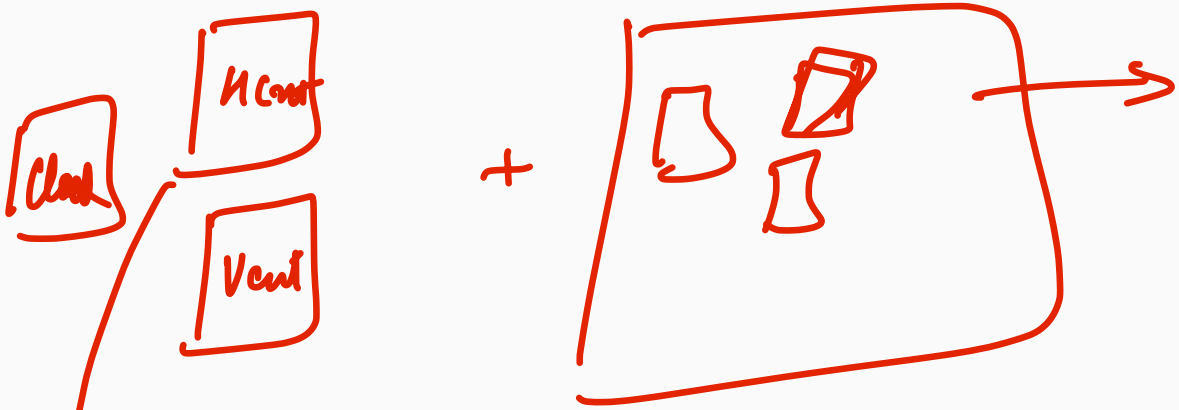
Output Signals from FPGA to Monitor



Extra


Hcnt
Vcnt
pixel co-ordinate
Pass
lines
(Vcnt, Hcnt)
1,1,1
0,0,0
0,0,0
R
G
B
1,0,0
1,1,0
1,1,0
0 < Hcnt < HACTIVE
0 < Vcnt < VACTIVE
(Vcnt, Hcnt)
image
RAM
(256 x 256)
address
Cnt
(0,0)(i,j) 640 x 255
255
MSB
4bit MSB ⟹ R=G=B

Extra



(counter) module

→

→ HSYNC
process1(Hcnt)
→ VSYNC
process2(Vcnt)

process3(clk, Hcnt, Vcnt)

0 < Hcnt & Vcnt < Active

(send image data.)