Hardware Assignment 0

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Problem

Design AND gate and create a testbench to test your implementation. Also generate synthesis and bitstream. Transfer the files to the Basys3 board and check the output.

Approach

- We set up the Vivado environment using the instructions given in the pdf.
- We created all the files and wrote the code for implementation of AND gate.
- We considered the constraints available.
- We created a test bench, considered a few test cases and ran a simulation and got the observations given below.

Implementation

Truth Table for AND gate

a	b	a AND b
0	0	0
0	1	0
1	0	0
1	1	1

Observation

Test bench Analysis

Input for a

a = 0 from 0 ns to 20 ns
a = 1 from 20 ns to 40 ns
a = from 40 ns to 60 ns
a = 1 after 60 ns

Input for b

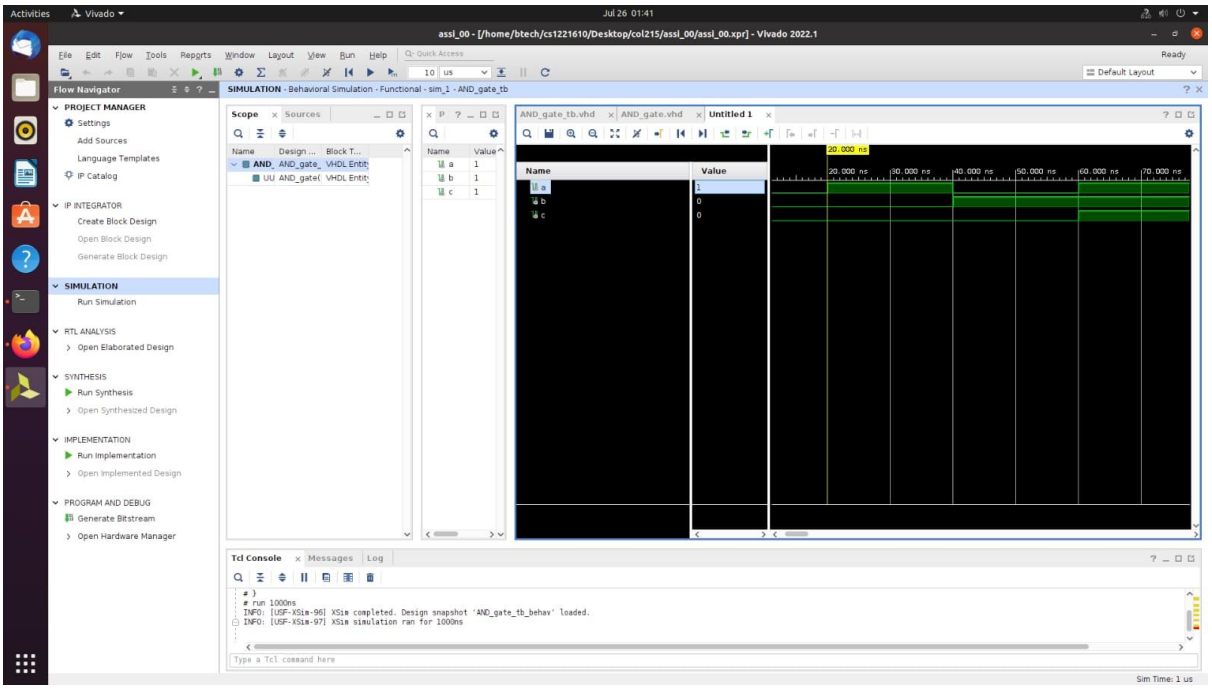
b = 0 from 0 ns to 40 ns
b = 1 after 40 ns

Output = a AND b

a AND b = 0 from 0 ns to 60 ns

a AND b = 1 from 60 ns

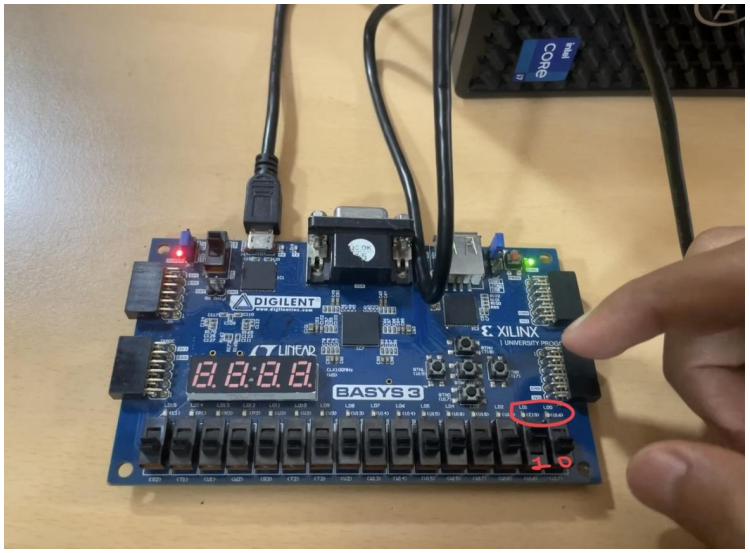
The results obtained by running a simulation using vivado are depicted in the screenshot below.



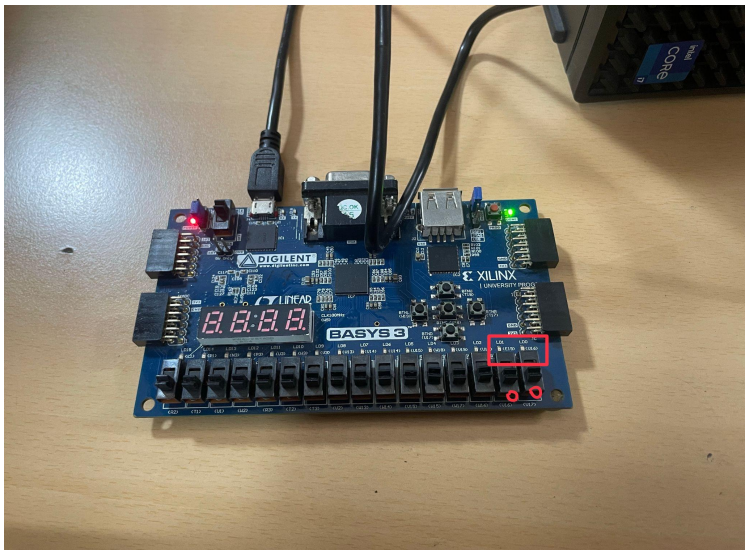
Result

The simulation matched the expected results. We transferred the code to the board and implemented the circuit in real time. Our tests using the switches and leds matched the expected implementation of the code

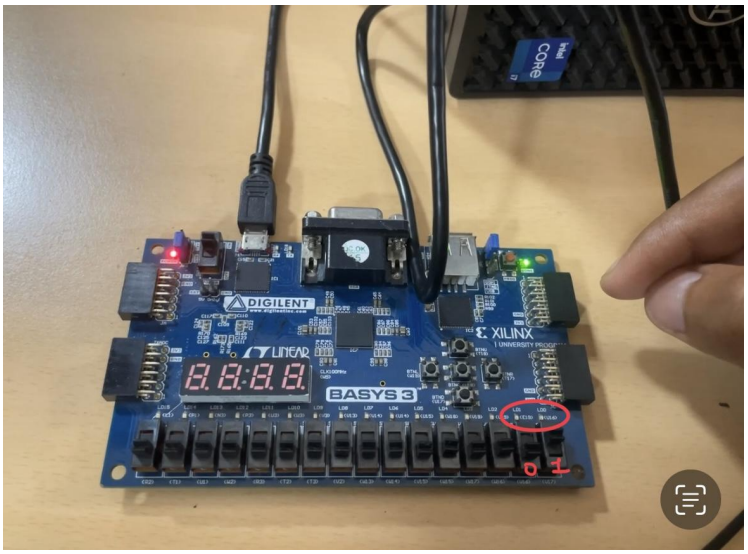
1 AND 0



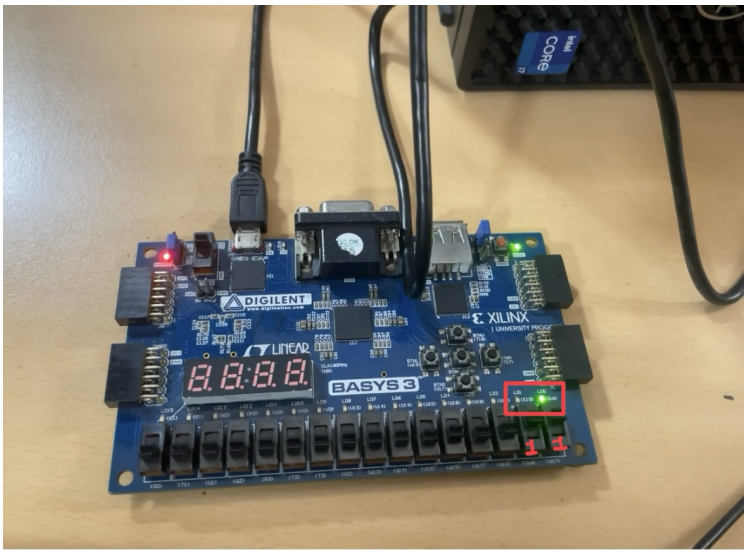
0 AND0



0 AND1



1 AND1



Concluding Remarks

We learnt and wrote the very first hardware simulation and implementation code in vivado, and learnt a little about linux. We also implemented the AND gate using the basys3 board which helped us to acquire knowledge about basic functioning of logic gates and digital circuits giving us a deeper understanding of the logic gates.