MOSFET Amplifier for ECGR3131-001

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Abstract – The purpose of this project is to construct a MOSFET amplifier with a voltage gain of at least 10V and an output swing of no less than ±5V. Each group must find an amplifier circuit to achieve the specifications while using +10V and -10V DC sources. For this project, a common-source amplifier circuit was used in conjunction with resistor values at: 15k for R_2, 13.5k for R_1, 9k for R_D, and 10.5k for R_S. The gain of the circuit was calculated to be 69.774V/V and simulated to be 68.91V/V. However, the actual gain during the live demonstration ended up at 36V/V. The most likely cause for the difference in gain between the theoretical and experimental results is that of noise produced by unoptimized potentiometer usage. Despite the differences in results, the maximum gain of the demonstration still outperformed the original specifications for the project, and maintained the appropriate output gain of ±5V.

Keywords – MOSFET, amplifier, common-emitter

I. Introduction

For this project, a MOSFET amplifier had to be constructed that achieved a voltage gain of at least 10V and an output swing of ±5V. The specifications also included the necessity of both +10 and -10 voltage sources. For these specifications, the common-source amplification circuit was chosen, as it offers the highest voltage gain out of the possible MOSFET amplification circuits.

II. DC Analysis

Before starting the DC analysis, a simulation was performed using Multisim to determine the appropriate resistance ratios and values to achieve maximum gain for the circuit. In the simulation, the circuit was constructed using 4 potentiometers seen in the figure below. This change allowed for much easier testing with the biasing conditions of the circuit, and for adjusting the resistance without having to end the simulation. In modification to the original specifications for the lab, the 2N7000 MOSFET chip was used instead, as the CD4007UBE is not included in the Multisim database and the two are functionally identical. Any differences in manufacturing specifications were noted and used during hand analysis.

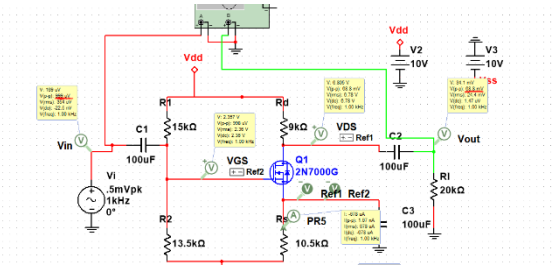

Figure 1 Simulated Common-Source Circuit

The simulation proved the following resistor values as optimal choices:

$$\frac{R_2}{R_1} = \frac{15k}{13.5k}\Omega, \frac{R_D}{R_S} = \frac{9k}{10.5k}\Omega$$

Once the resistor values were found, DC analysis was performed using standard biasing techniques for MOSFET amplifiers. As such, a 0V AC source was assumed, and so only the +10V and -10V DC sources contributed to the calculations.

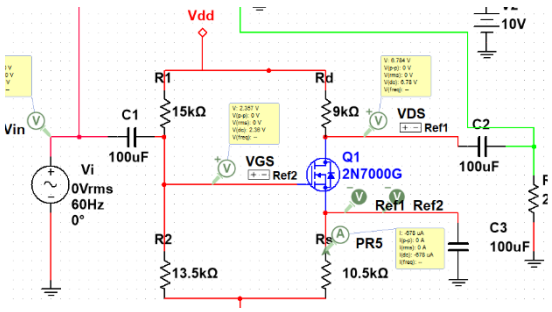

Figure 2 Common-Source Biasing Circuit

The equation for calculating the current across the drain branch I_D is:

$$I_D = \frac{1}{2}k_n V_{OV}^2 = \frac{1}{2}k_n (V_G - V_T)^2$$

To solve for the drain current, the gate voltage must be calculated first. Knowing that gate voltage V_G is equal to $V_{DD} - V_{R1}$, the equation could then be broken down as follows using voltage division:

$$V_G = V_{DD} - (V_{DD} - V_{SS}) * \left(\frac{R_1}{R_1 + R_2}\right)$$

Using this equation, the gate voltage was found to be -0.526V. Since I_S=I_D, the gate-source equation was then modified into mostly known values:

$$V_{GS} = V_G - V_S = V_G - (V_{SS} + I_D R_S)$$

This allows for a substitution in the current equation I_D so that the only unknown is the current itself. Completing the substitution for V_{GS} in the voltage overdrive of the current equation leaves:

$$I_D = \frac{1}{2} k_n (V_G - V_{SS} - I_D R_S - V_T)^2$$

The value of k_n and V_T is given by the PSPICE model for the 2N7000, which is 0.0932A/V^2 and 2.236V respectively. A substitution for V_G-V_{SS}-V_T is used with variable x to simplify the expression. The complete decomposition of the equation creates the polynomial:

$$\frac{1}{2} k_n R_S^2 I_D^2 + (-k_n x R_S - 1) I_D + \frac{1}{2} k_n x^2$$

Solving the polynomial in terms of I_D gives two possible currents for the branch: 701µA or 677.8µA. The two current values were substituted back into the gate-source equation. For I_D=701µA, the gate-source voltage is 2.113V which is not greater than the V_T value of the MOSFET used. Therefore, the only valid I_D value was 677.8µA.

To determine the drain-source voltage V_{DS}, the equation can be broken down into the sum of the voltages across the branch:

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = V_{SS}$$
$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S - V_{SS}$$

By using this equation, the drain-source voltage is found to be 6.783V.

III. AC Analysis

To perform AC analysis on the amplifier, a small signal equivalent was used equivalent. This circuit is split into two main parts: input and output characteristics. Using this model, finding the input and output impedances is much simpler.

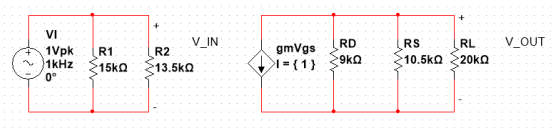

Figure 3 Small-Signal Biasing Circuit

The transconductance g_m can be calculated as $\frac{2I_D}{V_{OV}}$ which, using the values found during DC analysis, is equal to 0.0112. Since V_{GS}= V_{IN} during small-signal analysis, V_{OUT} can be characterized with the equation:

$$V_{OUT} = -g_m V_{IN} * (R_D || R_L)$$

Then by dividing the equation by V_{IN}, the gain can be calculated:

$$\frac{V_{OUT}}{V_{IN}} = -g_m * (R_D || R_L)$$

The input impedance r_{in} is equal to $R_1||R_2$, so by using the existing resistor values the input impedance is equal to 7.105kΩ. The output impedance r_{out} is similar, using the resistors $R_D||R_L$, resulting in a value of 6.207kΩ.

IV. Results

	Theoretical	Simulated	Experimental	Percent Error
V_{GS} (V)	2.357	2.357	2.423	2.8%
V_{DS} (V)	6.783	6.784	6.873	1.327%
I_D (µA)	678	678	684	0.885%

Table 1 Results of DC Analysis

The simulation and live testing performed at about the level calculated during DC analysis. The small amount of percent error between the theoretical and experimental values is likely the result of manufacturing error in the resistors, leading to an increase in maximum current during the demonstration.

	Theoretical	Simulated	Experimental	Percent Error
Gain (V/V)	69.774	68.91	36	48.405%
Rin (KOHM)	7.105	7.11	7.194	1.253%
Rout (KOHM)	6.207	6.211	6.329	1.966%

Table 2 Results of AC Analysis

The input and output impedance measured during the lab was close to that found during AC analysis and the simulation. However, the voltage gain was far from ideal during the demonstration, achieving little more than half of the simulated and calculated value. It is likely that due to the high gain and sensitivity of the amplifier, the noise generated weakened the gain potential.

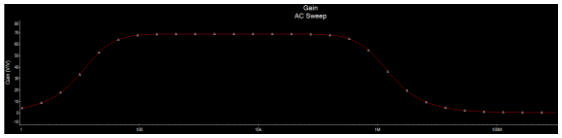

Figure 4 Simulated Gain vs. Frequency

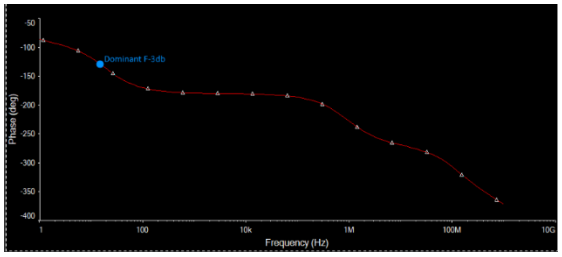

Figure 5 Simulated Phase vs. Frequency

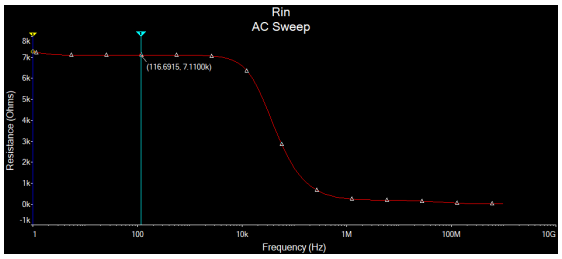

Figure 6 Simulated Input Impedance

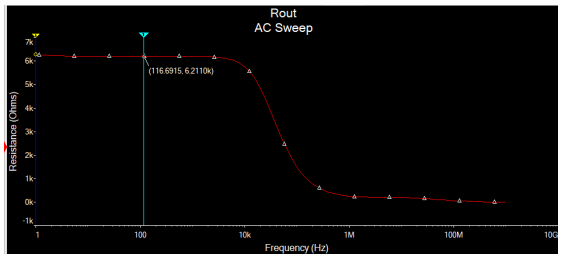

Figure 7 Simulated Output Impedance

The change in impedance is related to the capacitors in the circuit, which operate at lower frequencies. As the frequency increases, the capacitor passes less and less current through the circuit, eventually acting as an open circuit. Though the capacitors due help with noise, this means that the circuit will be less effective at higher frequencies.

For the demonstration, the amplifier was constructed based off the simulated model and performed with a peak voltage gain of 36 volts/volt at an input of 260mV at 100.39Hz.

Figure 8 Demonstration of Gain (Left) and Swing (Right) for MOSFET Amplifier

The amplifier measured at frequencies between 22Hz and 25kHz, after which the amplifier fails to achieve optimal gain. This range was less than the simulated range, only operating between 80Hz and 300kHz. This could have again been the result of increased noise due to unoptimized resistor usage. The bandwidth of the amplifier was measured at 914.978kHz, which was around the simulated bandwidth of 916.946kHz at a 0.215% error.

V. Areas for Improvement

The resistances found during the lab were not optimized appropriately. Despite using proper techniques to create our simulated result, calculating these values might have led to better gain results from the live demonstration.

VI. Conclusion

During the experiment, the best gain achieved during the simulation and through hand calculations was around 69V/V. However, the measured value was only capable of reaching 36. It is very possible the noise from unoptimized potentiometer combinations, and the use of two potentiometers for R_D and R_S instead of just one, likely contributed to an interference in the total possible gain of the amplifier.

The amplifier's output remains symmetrical up to 130mV. This is likely a result of the unoptimized resistor combinations used for the circuit, resulting in an imbalance in the resistance ratios and a loss of stability at higher voltages.

In designing the circuit, the most important aspect was determining the correct ratio of resistances to achieve the best possible gain for the amplifier. Everything else was built around these ratios and resistor combinations. As such, having an imbalance as proven by the gain and asymmetry of the output signal proves that much more could have been done in ensuring that the best possible resistors could have been found