

# Jaskirat Singh Virdi

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## Education

<i>Bachelor of Technology</i> 2016-2020	<b>Indian Institute of Technology (IIT) Roorkee</b> Electronics and Communication Engineering GPA: 8.88/10
<b>Coursework includes</b>	Analog VLSI, RF Amplifier and Transmitter Design, Power Management IC, Microwave Engineering, Semiconductor Devices, Antenna Theory, Embedded Systems, Digital VLSI, Communication Systems, Digital Communication, Computer Architecture, Automatic Control Systems, Electronic Network Theory.

## Research Interests

Power Amplifiers, RF/mm-wave Integrated Circuits, Analog/Mixed-Signal IC

## Work Experience

July 2020 - Present	<b>Texas Instruments Incorporated</b> Analog Design Engineer	<i>Bangalore, India</i>
	<ul style="list-style-type: none"><li>Analog Design Engineer in Memory IP development team.</li><li>The team is responsible for designing Non Volatile Memory IPs for TI worldwide.</li><li>Responsibilities include design of CMOS oscillators, Low Drop Out regulators, charge pumps and several other analog peripherals for internal Non Volatile Memory IPs.</li></ul>	

## Internship Experience

May 2019 - July 2019	<b>Texas Instruments Incorporated</b> Analog Design Intern	<i>Bangalore, India</i>
	<ul style="list-style-type: none"><li>Analog Design Engineering Internship in IO design team.</li><li>A bi-directional, high speed GPIO was designed and simulated in a BiCMOS 150nm technology.</li><li>Any 1.5V digital core can be interfaced with the standard 1.8V/3.3V/5V I/O voltage domains.</li><li>The GPIO was designed in accordance with various JEDEC and IEEE I/O standards and can be used across the standard automotive temperature range (<math>-40^{\circ}\text{C}</math> to <math>125^{\circ}\text{C}</math>).</li></ul>	

## Research Projects

Dec 2018 - June 2020	<b>A low power CMOS ECG sensor for early detection of CVDs</b> Prof. Bishnu Prasad Das, IIT Roorkee	<i>Undergraduate Thesis</i>
	<ul style="list-style-type: none"><li>Designed nano-watt power, custom, wearable SoC for real-time detection of heart diseases (CVDs).</li><li>Analog blocks like peak detector, BGR, comparator were designed in TSMC 0.18<math>\mu\text{m}</math> CMOS PDK.</li><li>The designed system was fabricated and post-silicon results were measured.</li><li>The test chip successfully detected ECG P, R, and T peaks which are crucial in CVD detection.</li><li>ECG P, R, T peaks were detected at a much lower power consumption than the existing designs.</li></ul>	
May 2018 - Oct 2018	<b>Design of CLB for an indigenous FPGA</b> Prof. Anand Bulusu, IIT Roorkee	
	<ul style="list-style-type: none"><li>Studied various architectures for a configurable logic block (CLB) of an FPGA.</li><li>Designed a custom CLB for an indigenous FPGA.</li><li>A master-slave D flip-flop and some LUT based memories were designed in SCL 0.18<math>\mu\text{m}</math> CMOS PDK.</li><li>Custom layouts were drawn and post layout simulations were performed on the designed CLB.</li></ul>	
July 2017 - Nov 2017	<b>Custom RISC microprocessor using Verilog</b> Prof. Vaskar Raychoudhury, IIT Roorkee	<i>Course Project</i>
	<ul style="list-style-type: none"><li>Created a custom instruction set architecture (ISA) for a 24-bit RISC processor.</li><li>The ISA included basic arithmetic and logical operations.</li><li>ISA was implemented in Verilog and functionality was verified using behavioral simulations.</li></ul>	

## Academic Service and Teaching Experience

Spring'19	<b>Digital Logic Design: Undergraduate Teaching Assistant</b> Enrolment: 40	<i>Dept. of ECE, IITR</i>
	<ul style="list-style-type: none"> <li>Conducted tutorial sessions and taught basics of digital design.</li> <li>Helped students in solving course assignments by clearing their queries.</li> </ul>	

## Awards and Achievements

April 2016	<b>Joint Entrance Examination, Mains</b> All India Rank 939 out of a pool of nearly 1.2 million nation-wide candidates.
March 2016	<b>CBSE Higher Secondary Examination (India)</b> Ranked in top 0.1 percent candidates in Physics (99% marks in Physics, 96.8% marks overall)

## Technical Skills

<b>Programming</b>	C++, Python, Shell scripting, SPICE, Verilog, Verilog-A, $\text{\LaTeX}$ , Java, Perl
<b>Tools</b>	Cadence Virtuoso, Vivado, Ansys HFSS, LTspice, MATLAB
<b>Languages</b>	English, Hindi, Punjabi

## Extra-Curriculars

July 2019 -	<b>IEEE Student Branch, Special Interest Group</b> Member	<i>IIT Roorkee</i>
June 2020	<ul style="list-style-type: none"> <li>Delivered a talk on 'Internal Architectures of FPGAs'.</li> <li>Organized meetings and discussions on topics in Electronics and Computer Science.</li> </ul>	
Jan 2017 -	<b>Mobile Development Group</b> Android front-end developer	<i>IIT Roorkee</i>
Dec 2017	<ul style="list-style-type: none"> <li>The group aims at developing applications for Android and IOS platforms.</li> <li>Collaborated in the development of various institute-level android apps.</li> </ul>	

## Community Service

Jan 2016 -	<b>National Cadet Corps</b> Cadet	<i>IIT Roorkee</i>
Apr 2017	<ul style="list-style-type: none"> <li>Participated in cleanliness drives and various other activities organised by NCC, IIT Roorkee.</li> <li>Attended weekly lectures on discipline and conduct organised by NCC, IIT Roorkee.</li> </ul>	