COEN 316: COMPUTER ARCHITECTURE & DESIGN

Section DM-X

LAB REPORT # 4

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"I certify that this submission is my original work and meets the Faculty's Expectations of Originality"

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OBJECTIVES:

The objective of this lab is composed of 2 parts to design a complete CPU datapath with 10 control signals performing the function of the control unit to produce the correct values for all control signals at the proper point in time. It will be developed in VHDL including the previous 3 lab components (ALU, register file and next-address unit) as well as designing the instruction cache, the data cache, and sign extension unit in VHDL and tested on Modelsim. The complete CPU will then be tested using Modelsim and Xilinx to implement on the FPGA board.

INTRODUCTION:

Part 1:

The datapath of a CPU is the design that the data within the CPU will take, based on the arrangement of the components of a CPU. This includes the previous 3 lab-designed components (ALU, register file and next-address unit) as well as designing additional hardware such as the instruction cache, the data cache and sign extension unit. There are many ways to have the datapath of a CPU in this. Here is the partial datapath given:

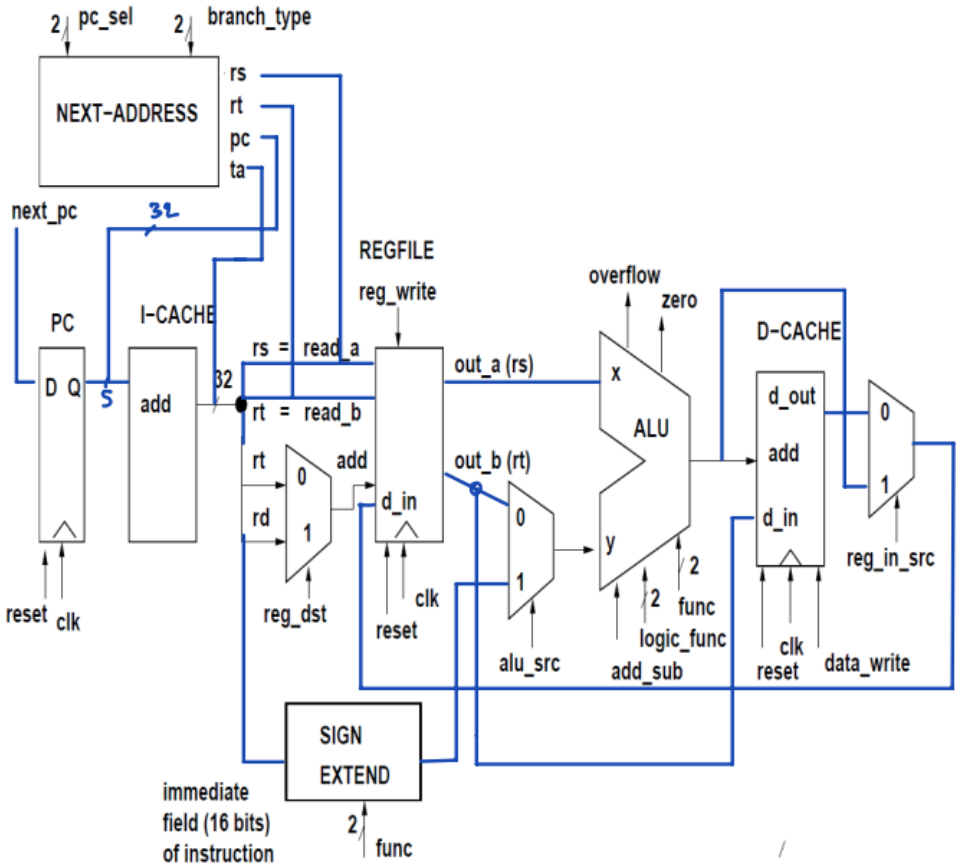

Figure 2: CPU datapath. [3]

PC register: Program counter of 32-bit register with asynchronous reset

Instruction count: Stores machine code in 32 location ROM

Register File: Designed in Lab 2

ALU: Designed in Lab 1

Sign extension: Some MIPS instructions require 16 bit immediate field (0 to 15 bits to store)

of I-format instructions sign extended to full 32-bit width

Data cache: small RAM-type of memory where ALU low order 5 bits of ALU used to address

one of 32 locations

Part 2:

The design of a complete CPU datapath with 10 control signals given table 1 and 2 performing the function of the control unit to produce the correct values for all control signals at the proper point in time. Table 3 with 20 instructions will be completed in the results section. Control unit will be designed in this section in VHDL.

Control signal	value = 0	value = 1
reg_write	do not write into register file	write into register file
reg_dst	rt is the destination register	rd is the destination register
reg_in_src	d_out of data_cache is the d_in to the register file	ALU output is the d_in to the register file
alu_src	out_b of register file (rt) is the y input of the ALU	sign extended immediate is the y input of the ALU
add_sub	ALU operation = addition	ALU operation = subtraction
data_write	do not write into data cache	write into data cache

Table 1: Single bit control signals

Control signal	value = 00	value = 01	value =10	value = 11
logic_func	AND	OR	XOR	NOR
func	load upper immediate	set less	arithmetic	logic
branch_type	no branch	beq	bne	bltz

Table 2: Two bit control signals

RESULTS:

As seen in figure 2, 3 and 4 below, the “i_cache.vhd” “d_cache.vhd” and “sign_ext” compiled well and the simulation results are accurate as the objective of part 1.

The following code files has been created to design the 32-bit datapath:

“i_cache.vhd”

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;
entity i_cache is
port(
input_addr : in std_logic_vector(4 downto 0);
instr : out std_logic_vector(31 downto 0));
end i_cache;
architecture ic_arch of i_cache is
begin
process(input_addr)
begin
case input_addr is
when "00000" =>
instr <= "00100000000000110000000000000000"; -- addi r3, r0, 0
when "00001" =>
instr <= "00100000000000010000000000000000"; -- addi r1, r0, 0
when "00010" =>
instr <= "00100000000000100000000000000101"; -- addi r2,r0,5
when "00011" =>
instr <= "00000000001000100000100000100000"; -- add r1,r1,r2
when "00100" =>
instr <= "00100000010000101111111111111111"; -- addi r2, r2, -1
when "00101" =>
instr <= "00010000010000110000000000000001"; -- beq r2,r3 (+1) THERE
when "00110" =>
instr <= "00001000000000000000000000000011"; -- jump 3 (LOOP)
when "00111" =>
instr <= "10101100000000010000000000000000"; -- sw r1, 0(r0)
when "01000" =>
instr <= "10001100000001000000000000000000"; -- lw r4, 0(r0)
when "01001" =>
instr <= "00110000100001000000000000001010"; -- andi r4,r4, 0x000A
when "01010" =>
instr <= "00110100100001000000000000000001"; -- ori r4,r4, 0x0001
when "01011" =>
instr <= "00111000100001000000000000001011"; -- xori r4,r4, 0xB
when "01100" =>
instr <= "00111000100001000000000000000000"; -- xori r4,r4, 0x0000;
when others => instr <= "00000000000000000000000000000000";
end case;
end process;
end ic_arch;
```

“i_cache.do”

```
add wave *
force input_addr "00000"
run 2;
force input_addr "00001"
run 2;
force input_addr "00010"
run 2;
force input_addr "00011"
run 2;
force input_addr "00100"
run 2;
force input_addr "00101"
run 2;
```

“d_cache.vhd”

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity d_cache is
port(   input    : in std_logic_vector(31 downto 0);
        reset    : in std_logic;
        clk      : in std_logic;
        addr     : in std_logic_vector(4 downto 0);
      data_write : in std_logic;
        output   : out std_logic_vector(31 downto 0));
end d_cache;

architecture dc_arch of d_cache is

-- declare internal signals
type Locations is array(0 to 31) of std_logic_vector(31 downto 0);
signal L: Locations;

begin
        output <= L(conv_integer(addr));

        process(input, reset, clk, data_write, addr)
        begin
                if (reset = '1') then
                        for i in L'range loop
                                L(i) <= (others => '0');
                        end loop;

                elsif( rising_edge(clk) ) then
                        if ( data_write = '1' ) then
                                L(conv_integer(addr)) <= input;
                        end if;
                end if;
        end process;
end dc_arch;
```

“d_cache.do”

```
add wave *
force reset 1
force clk 0
force input X"F00A3008"
force data_write 0
force addr 00010
run 2
force reset 0
force clk 1
force data_write 1
run 2
force clk 0
force addr 01010
run 2
force input X"00F00FAA"
force addr 00111
force clk 1
run 2
```

“sign_ext.vhd”

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity sign_ext is
port(   in16    : in std_logic_vector(15 downto 0);
        func_se : in std_logic_vector(1 downto 0);
        out32   : out std_logic_vector(31 downto 0));
end sign_ext;

architecture se_arch of sign_ext is

begin
        process(in16, func_se)
        begin
                case func_se is
                        when "00" => out32 <= in16(15 downto 0) & X"0000"; -- lui
                        when "01" | "10" => out32 <= (31 downto 16 => in16(15)) & in16(15 downto 0); -- slti, arith
                        -- when "10" => out32 <= (31 downto 16 => in16(15)) & in16(15 downto 0);
                        when "11" => out32 <= X"0000" & in16(15 downto 0); -- logical
                        when others =>
                end case;
        end process;
end se_arch;
```

“sign_ext.do”

```
# add signals to the waveform window
add wave *
#lui
force in16 X"A316"
force func_se 00
run 2;
#slt
force in16 X"0316"
force func_se 01
run 2;
#arith
force in16 X"A417"
force func_se 10
run 2;
#logical
force func_se 11
run 2;
```

“pc_comp”

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity pc_comp is
port( in_addr: in std_logic_vector(31 downto 0);
        reset   : in std_logic;
        clk     : in std_logic;
        out_q   : out std_logic_vector(31 downto 0));
end pc_comp;

architecture pc_comp_arch of pc_comp is

begin
        process(in_addr, reset, clk)
        begin
                if (reset = '1') then
                        out_q <= X"00000000";

                elsif( rising_edge(clk) ) then
                        out_q <= in_addr;
                end if;
        end process;
end pc_comp_arch;
```

“cpu.vhd”

```
library ieee;
use ieee.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity cpu is
    port ( reset        : in std_logic;
           clk  : in std_logic;

           -- output ports from register file
           rs_out, rt_out       : out std_logic_vector(3 downto 0):= (others => '0');
           pc_out               : out std_logic_vector(3 downto 0):= (others => '0');

           -- will not be constrained in Xilinx since not enough LEDs
           overflow, zero       : out std_logic);
end cpu;

architecture structural of cpu is

--  declare a PC component
component pc_comp
port( in_addr: in std_logic_vector(31 downto 0) := (others => '0');
      reset     : in std_logic;
      clk       : in std_logic;
      out_q     : out std_logic_vector(31 downto 0) := (others => '0'));
end component;

-- declare Instruction Memory component
component i_cache
port( input_addr: in std_logic_vector(4 downto 0);
        instr   : out std_logic_vector(31 downto 0));
end component;

--  declare a Next Address component
component next_address
port(
        rt,rs           : in std_logic_vector(31 downto 0);  -- two register input
        pc              : in std_logic_vector(31 downto 0);
        target_address  : in std_logic_vector(25 downto 0);
        branch_type     : in std_logic_vector(1 downto 0);
        pc_sel          : in std_logic_vector(1 downto 0);
        next_pc         : out std_logic_vector(31 downto 0));
end component;
```

```
--  declare a Register File component
component regfile
port( din        : in std_logic_vector(31 downto 0);
      reset      : in std_logic;
      clk        : in std_logic;
      write      : in std_logic;
      read_a     : in std_logic_vector(4 downto 0);
      read_b     : in std_logic_vector(4 downto 0);
      write_address : in std_logic_vector(4 downto 0);
      out_a      : out std_logic_vector(31 downto 0);
      out_b      : out std_logic_vector(31 downto 0));
end component;

-- declare Sign Extend component
component sign_ext
port(   in16     : in std_logic_vector(15 downto 0);
        func_se  : in std_logic_vector(1 downto 0);
        out32    : out std_logic_vector(31 downto 0));
end component;

--  declare an ALU component
component alu
port(
        x,y          : in std_logic_vector(31 downto 0);  -- two input operands
        add_sub      : in std_logic;                      -- 0 = add, 1 = sub
        logic_func   : in std_logic_vector(1 downto 0);   -- 00 = AND, 01 = OR, 10 = XOR, 11 = NOR
        func         : in std_logic_vector(1 downto 0);   -- 00 = lui, 01 = setless, 10 = arith, 11 = logic

        output       : out std_logic_vector(31 downto 0);
        ovrflw     : out std_logic;
        zro          : out std_logic);
end component;

-- declare Data Memory component
component d_cache
port(   input     : in std_logic_vector(31 downto 0);
        reset     : in std_logic;
        clk       : in std_logic;
        addr      : in std_logic_vector(4 downto 0);
      data_write : in std_logic;
        output    : out std_logic_vector(31 downto 0));
end component;


-- declare configuration specification
for PC : pc_comp use entity WORK.pc_comp(pc_comp_arch);
for I_C : i_cache use entity WORK.i_cache(ic_arch);
for NextAddress : next_address use entity WORK.next_address(pc_arch);
for R_F : regfile use entity WORK.regfile(reg_arch);
for SignExtend : sign_ext use entity WORK.sign_ext(se_arch);
for A : alu use entity WORK.alu(alu_arch);
for D_C : d_cache use entity WORK.d_cache(dc_arch);

-- declare internal signals used to "hook up" components
signal pc_o, next_pc_o, ic_o, dc_o, a_o, b_o, alu_o, se_o, alu_i, reg_i : std_logic_vector(31 downto 0) := X"00000000";
signal reg_addr_i : std_logic_vector(4 downto 0) := (others => '0');
signal pc_choice, branch_t, alu_f, alu_lf : std_logic_vector(1 downto 0) := "00";
signal alu_adsb, dc_write, reg_write, reg_dst, alu_src, reg_in_src : std_logic := '0';

-- opcode, func and control signal holder respectively for control unit implementation
signal mick , keith : std_logic_vector(5 downto 0) := (others => '0');
signal ctrl_sig : std_logic_vector(13 downto 0);

begin
-- control unit implementation
        process(ic_o, clk, reset, mick, keith, ctrl_sig)
        begin
                mick     <= ic_o(31 downto 26);
                keith    <= ic_o(5 downto 0);
                case mick is
                        when "000000" =>
                                 if (keith = "100000") then ctrl_sig <= "11100000100000"; -- add
                                elsif (keith = "100010") then ctrl_sig <= "11101000100000"; -- sub
                                elsif (keith = "101010") then ctrl_sig <= "11100000010000"; -- slt
                                elsif (keith = "100100") then ctrl_sig <= "11101000110000"; -- and
                                elsif (keith = "100101") then ctrl_sig <= "11100001110000"; -- or
                                elsif (keith = "100110") then ctrl_sig <= "11100010110000"; -- xor
                                elsif (keith = "100111") then ctrl_sig <= "11100011110000"; -- nor
                                elsif (keith = "001000") then ctrl_sig <= "00000000000010"; -- jr
                                else end if;
                        when "000001" => ctrl_sig <= "00000000011100"; -- bltz
                        when "000010" => ctrl_sig <= "00000000000001"; -- j
                        when "000100" => ctrl_sig <= "00000000000100"; -- beq
                        when "000101" => ctrl_sig <= "00000000001000"; -- bne
                        when "001000" => ctrl_sig <= "10110000100000"; -- addi
                        when "001010" => ctrl_sig <= "10110000010000"; -- slti
                        when "001100" => ctrl_sig <= "10110000110000"; -- andi
                        when "001101" => ctrl_sig <= "10110001110000"; -- ori
                        when "001110" => ctrl_sig <= "10110010110000"; -- xori
                        when "001111" => ctrl_sig <= "10110000000000"; -- lui
                        when "100011" => ctrl_sig <= "10010010100000"; -- lw
                        when "101011" => ctrl_sig <= "00010100100000"; -- sw
                        when others =>
                end case;
```

```
                reg_write <= ctrl_sig(13);
                reg_dst  <= ctrl_sig(12);
                reg_in_src <= ctrl_sig(11);
                alu_src <= ctrl_sig(10);
                alu_adsb <= ctrl_sig(9);
                dc_write <= ctrl_sig(8);
                alu_lf <= ctrl_sig(7 downto 6);
                alu_f <= ctrl_sig(5 downto 4);
                branch_t <= ctrl_sig(3 downto 2);
                pc_choice <= ctrl_sig(1 downto 0);
        end process;

-- component instantiation
PC: pc_comp port map(in_addr => next_pc_o, reset => reset, clk => clk, out_q => pc_o);

I_C: i_cache port map(input_addr => pc_o(4 downto 0), instr => ic_o);

NextAddress: next_address port map(rt => b_o, rs => a_o, pc => pc_o, target_address => ic_o(25 downto 0),
                                   branch_type => branch_t, pc_sel => pc_choice, next_pc => next_pc_o);

R_F: regfile port map(din => reg_i, reset => reset, clk => clk, write => reg_write,
                      read_a => ic_o(25 downto 21), read_b => ic_o(20 downto 16),
                      write_address => reg_addr_i, out_a => a_o, out_b => b_o);

SignExtend: sign_ext port map(in16 => ic_o(15 downto 0), func_se => alu_f, out32 => se_o);

A: alu port map(x => a_o, y => alu_i, add_sub => alu_adsb, logic_func => alu_lf,
                func => alu_f, output => alu_o, ovrflw => overflow, zro => zero);

D_C: d_cache port map(input => b_o, reset => reset, clk => clk,
                      addr => alu_o(4 downto 0), data_write => dc_write, output => dc_o);

-- implementation of the connections between mutiplexers
reg_addr_i <= ic_o(20 downto 16) WHEN (reg_dst = '0') ELSE
              ic_o(15 downto 11) WHEN (reg_dst = '1');

alu_i <= se_o WHEN (alu_src = '1') ELSE
         b_o WHEN (alu_src = '0');

reg_i <= alu_o WHEN (reg_in_src = '1') ELSE
         dc_o WHEN (reg_in_src = '0');

rs_out  <= a_o(3 downto 0);
rt_out  <= b_o(3 downto 0);
pc_out  <= pc_o(3 downto 0);

end structural;
```

“cpu.do”

```
# This is a comment line in a .do file
# add all signals to the Waveform window
add wave *

force reset 1
force clk 0
run 2

force clk 1

force reset 0 2 -r 4
force clk 1  2 -r 4
force clk 0  4 -r 4

# run for 9 clock periods
# 39 clock periods x 4 timesteps per period
# = 156 timesteps

run 156
```

“cpu.xdc”

```
# Vivado does not support old UCF syntax
# must use XDC syntax

set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCMOS33 } [ get_ports { reset_al }];
set_property -dict { PACKAGE_PIN L16 IOSTANDARD LVCMOS33 } [ get_ports { clk_al } ];
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk]
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 } [ get_ports { rs_out[0] }];
set_property -dict { PACKAGE_PIN K15 IOSTANDARD LVCMOS33 } [ get_ports { rs_out[1] }] ;
set_property -dict { PACKAGE_PIN J13 IOSTANDARD LVCMOS33 } [ get_ports { rs_out[2] }];
set_property -dict { PACKAGE_PIN N14 IOSTANDARD LVCMOS33 } [ get_ports { rs_out[3] }];
set_property -dict { PACKAGE_PIN R18 IOSTANDARD LVCMOS33 } [ get_ports { pc_out[0]} ];
set_property -dict { PACKAGE_PIN V17 IOSTANDARD LVCMOS33 } [ get_ports { pc_out[1]} ];
set_property -dict { PACKAGE_PIN U17 IOSTANDARD LVCMOS33 } [ get_ports { pc_out[2]} ];
set_property -dict { PACKAGE_PIN U16 IOSTANDARD LVCMOS33 } [ get_ports { pc_out[3]} ];
set_property -dict { PACKAGE_PIN V16 IOSTANDARD LVCMOS33 } [ get_ports { overflow }];
set_property -dict { PACKAGE_PIN T15 IOSTANDARD LVCMOS33 } [ get_ports { zero } ];
```

Completed 20 instructions with opcode and function fields and control signals are show in the 3 figures below:

Inst.	op	func	reg_write	reg_dst	reg_in_src	alu_src	add_sub	data_write	logic_func	func	branch_type	pc_sel
lui	001111	-	1	0	1	1	0 (don't care)	0	00 (don't care)	00	00	00
add	000000	100000	1	1	1	0	0	0	00	10	00	00
sub	000000	100010	1	1	1	0	1	0	00	10	00	00
slt	000000	101010	1	1	1	0	1	0	00	01	00	00
addi	001000	-	1	0	1	1	0	0	00	10	00	00
slti	001010	-	1	0	1	1	1	0	00	01	00	00
and	000000	100100	1	1	1	0	1	0	00	11	00	00
or	000000	100101	1	1	1	0	0	0	01	11	00	00
xor	000000	100110	1	1	1	0	0	0	10	11	00	00
nor	000000	100111	1	1	1	0	0	0	11	11	00	00
andi	001100	-	1	0	1	1	1	0	00	11	00	00

slti	001010	-	1	0	1	1	1	0	00	01	00	00
and	000000	100100	1	1	1	0	1	0	00	11	00	00
or	000000	100101	1	1	1	0	0	0	01	11	00	00
xor	000000	100110	1	1	1	0	0	0	10	11	00	00
nor	000000	100111	1	1	1	0	0	0	11	11	00	00
andi	001100	-	1	0	1	1	1	0	00	11	00	00
ori	001101	-	1	0	1	1	0	0	01	11	00	00
xori	001110	-	1	0	1	1	0	0	10	11	00	00
lw	100011	-	1	0	0	1	0	0	10 (don't care)	10	00	00

Inst.	op	func	reg_write	reg_dst	reg_in_src	alu_src	add_sub	data_write	logic_func	func	branch_type	pc_sel
sw	101011	-	0	0	0	1	0	1	00	10	00	00
j	000010	-	0	0	0	0	0	0	00	00	00	01
jr	000000	001000	0	0	0	0	0	0	00	10	00	10
bltz	000001	-	0	0	0	0	0	0	00	00	11	00
beq	000100	-	0	0	0	0	0	0	00	00	01	00
bne	000101	-	0	0	0	0	0	0	00	00	10	00

Figure 6: Complete table 3

CONCLUSION

In conclusion, the satisfactory complete datapath design was performed by creating a VHDL code, thorough simulation using ModelSim, and VHDL code for the board for synthesis and implementation using Xilinx Vivado. The simulation results, VHDL source code, and runme.log files were important procedures to follow for ensuring an error free register file design.

“synth_1 runme.log”

```
*** Running vivado
   with args -log cpu.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source cpu.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
   ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source cpu.tcl -notrace
Command: synth_design -top cpu -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 15607
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.574 ; gain = 85.805 ; free physical = 9462 ; free virtual = 21924
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'cpu' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:17]
INFO: [Synth 8-3491] module 'pc_comp' declared at
'/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/pc_comp.vhd:5' bound to instance 'PC' of component
'pc_comp' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:152]
INFO: [Synth 8-638] synthesizing module 'pc_comp'
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/pc_comp.vhd:12]
INFO: [Synth 8-256] done synthesizing module 'pc_comp' (1#1)
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/pc_comp.vhd:12]
INFO: [Synth 8-3491] module 'i_cache' declared at
'/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/i_cache.vhd:4' bound to instance 'I_C' of component 'i_cache'
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:154]
INFO: [Synth 8-638] synthesizing module 'i_cache'
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/i_cache.vhd:9]
INFO: [Synth 8-256] done synthesizing module 'i_cache' (2#1)
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/i_cache.vhd:9]
INFO: [Synth 8-3491] module 'next_address' declared at
'/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/pc_reg.vhd:5' bound to instance 'NextAddress' of component
'next_address' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:156]
INFO: [Synth 8-638] synthesizing module 'next_address'
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/pc_reg.vhd:15]
INFO: [Synth 8-226] default block is never used [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/pc_reg.vhd:30]
INFO: [Synth 8-256] done synthesizing module 'next_address' (3#1)
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/pc_reg.vhd:15]
INFO: [Synth 8-3491] module 'regfile' declared at '/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/reg_file.vhd:5'
bound to instance 'R_F' of component 'regfile' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:159]
INFO: [Synth 8-638] synthesizing module 'regfile'
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/reg_file.vhd:17]
INFO: [Synth 8-256] done synthesizing module 'regfile' (4#1)
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/reg_file.vhd:17]
INFO: [Synth 8-3491] module 'sign_ext' declared at
'/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/sign_ext.vhd:5' bound to instance 'SignExtend' of component
'sign_ext' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:163]
INFO: [Synth 8-638] synthesizing module 'sign_ext'
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/sign_ext.vhd:11]
INFO: [Synth 8-226] default block is never used
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/sign_ext.vhd:16]
INFO: [Synth 8-256] done synthesizing module 'sign_ext' (5#1)
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/sign_ext.vhd:11]
INFO: [Synth 8-3491] module 'alu' declared at '/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/alu_2.vhd:5'
bound to instance 'A' of component 'alu' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:165]
INFO: [Synth 8-638] synthesizing module 'alu' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/alu_2.vhd:17]
INFO: [Synth 8-226] default block is never used [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/alu_2.vhd:30]
INFO: [Synth 8-226] default block is never used [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/alu_2.vhd:54]
INFO: [Synth 8-226] default block is never used [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/alu_2.vhd:63]
INFO: [Synth 8-256] done synthesizing module 'alu' (6#1)
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/alu_2.vhd:17]
INFO: [Synth 8-3491] module 'd_cache' declared at
'/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/dcache.vhd:5' bound to instance 'D_C' of component 'd_cache'
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:168]
INFO: [Synth 8-638] synthesizing module 'd_cache'
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/dcache.vhd:14]
INFO: [Synth 8-256] done synthesizing module 'd_cache' (7#1)
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/dcache.vhd:14]
```

```
INFO: [Synth 8-256] done synthesizing module 'cpu' (8#1)
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:17]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.215 ; gain = 131.445 ; free physical = 9467 ; free virtual = 21929
---------------------------------------------------------------------------------

Report Check Netlist:
+------+-----------------+-------+---------+-------+------------------+
|      |Item             |Errors |Warnings |Status |Description       |
+------+-----------------+-------+---------+-------+------------------+
|1     |multi_driven_nets|      0|        0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.215 ; gain = 131.445 ; free physical = 9468 ; free virtual = 21930
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.215 ; gain = 131.445 ; free physical = 9468 ; free virtual = 21930
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/constrs_1/new/xdc.xdc]
Finished Parsing XDC File [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/constrs_1/new/xdc.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file
[/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/constrs_1/new/xdc.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/cpu_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/cpu_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1842.969 ; gain = 0.000 ; free physical = 9184 ; free virtual = 21649
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9278 ; free virtual = 21742
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9278 ; free virtual = 21742
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9280 ; free virtual = 21744
---------------------------------------------------------------------------------
INFO: [Synth 8-5546] ROM "instr" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[0]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[1]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[2]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[3]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[4]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[5]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[6]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[7]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[8]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[9]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[10]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[11]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[12]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[13]" won't be mapped to RAM because it is too sparse
```

INFO: [Synth 8-5546] ROM "R_reg[14]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[15]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[16]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[17]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[18]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[19]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[20]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[21]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[22]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[23]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[24]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[25]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[26]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[27]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[28]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[29]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[30]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "R_reg[31]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/alu_2.vhd:28]
INFO: [Synth 8-5546] ROM "L_reg[0]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[1]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[2]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[3]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[4]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[5]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[6]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[7]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[8]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[9]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[10]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[11]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[12]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[13]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[14]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[15]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[16]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[17]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[18]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[19]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[20]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[21]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[22]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[23]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[24]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[25]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[26]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[27]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[28]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[29]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[30]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "L_reg[31]" won't be mapped to RAM because it is too sparse
WARNING: [Synth 8-327] inferring latch for variable 'next_pc_reg' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/pc_reg.vhd:24]
WARNING: [Synth 8-327] inferring latch for variable 'ctrl_sig_reg' [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/sources_1/imports/code/cpu_dp.vhd:115]

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9270 ; free virtual = 21735

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start RTL Component Statistics

Detailed RTL Component Info :
+---Adders :
	2 Input 32 Bit Adders := 2
	3 Input 32 Bit Adders := 1
+---XORs :
	2 Input 32 Bit XORs := 1
+---Registers :

```
                32 Bit    Registers := 65
+---Muxes :
                2 Input    32 Bit       Muxes := 7
                4 Input    32 Bit       Muxes := 4
                3 Input    32 Bit       Muxes := 1
                8 Input    14 Bit       Muxes := 1
               14 Input    14 Bit       Muxes := 1
                2 Input     5 Bit       Muxes := 1
                4 Input     1 Bit       Muxes := 1
                2 Input     1 Bit       Muxes := 72
               14 Input     1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module cpu
Detailed RTL Component Info :
+---Muxes :
                2 Input    32 Bit       Muxes := 2
                8 Input    14 Bit       Muxes := 1
               14 Input    14 Bit       Muxes := 1
                2 Input     5 Bit       Muxes := 1
                2 Input     1 Bit       Muxes := 7
               14 Input     1 Bit       Muxes := 1
Module pc_comp
Detailed RTL Component Info :
+---Registers :
                32 Bit    Registers := 1
Module i_cache
Detailed RTL Component Info :
+---Muxes :
                2 Input    32 Bit       Muxes := 1
Module next_address
Detailed RTL Component Info :
+---Adders :
                2 Input    32 Bit      Adders := 2
+---Muxes :
                2 Input    32 Bit       Muxes := 3
                4 Input    32 Bit       Muxes := 2
                4 Input     1 Bit       Muxes := 1
Module regfile
Detailed RTL Component Info :
+---Registers :
                32 Bit    Registers := 32
+---Muxes :
                2 Input     1 Bit       Muxes := 32
Module sign_ext
Detailed RTL Component Info :
+---Muxes :
                3 Input    32 Bit       Muxes := 1
Module alu
Detailed RTL Component Info :
+---Adders :
                3 Input    32 Bit      Adders := 1
+---XORs :
                2 Input    32 Bit       XORs := 1
+---Muxes :
                4 Input    32 Bit       Muxes := 2
                2 Input    32 Bit       Muxes := 1
                2 Input     1 Bit       Muxes := 1
Module d_cache
Detailed RTL Component Info :
+---Registers :
                32 Bit    Registers := 32
+---Muxes :
                2 Input     1 Bit       Muxes := 32
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
```

DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

Finished Part Resource Summary

Start Cross Boundary and Area Optimization

Warning: Parallel synthesis criteria is not met
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][4]' (FDCE) to 'R_F/R_reg[13][4]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][4]' (FDCE) to 'R_F/R_reg[11][4]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][4])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][5]' (FDCE) to 'R_F/R_reg[13][5]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][5]' (FDCE) to 'R_F/R_reg[11][5]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][5])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][6]' (FDCE) to 'R_F/R_reg[13][6]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][6]' (FDCE) to 'R_F/R_reg[11][6]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][6])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][7]' (FDCE) to 'R_F/R_reg[13][7]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][7]' (FDCE) to 'R_F/R_reg[11][7]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][7])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][8]' (FDCE) to 'R_F/R_reg[13][8]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][8]' (FDCE) to 'R_F/R_reg[11][8]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][8])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][9]' (FDCE) to 'R_F/R_reg[13][9]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][9]' (FDCE) to 'R_F/R_reg[11][9]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][9])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][10]' (FDCE) to 'R_F/R_reg[13][10]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][10]' (FDCE) to 'R_F/R_reg[11][10]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][10])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][11]' (FDCE) to 'R_F/R_reg[13][11]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][11]' (FDCE) to 'R_F/R_reg[11][11]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][11])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][12]' (FDCE) to 'R_F/R_reg[13][12]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][12]' (FDCE) to 'R_F/R_reg[11][12]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][12])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][13]' (FDCE) to 'R_F/R_reg[13][13]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][13]' (FDCE) to 'R_F/R_reg[11][13]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][13])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][14]' (FDCE) to 'R_F/R_reg[13][14]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][14]' (FDCE) to 'R_F/R_reg[11][14]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][14])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][15]' (FDCE) to 'R_F/R_reg[13][15]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][15]' (FDCE) to 'R_F/R_reg[11][15]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][15])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][16]' (FDCE) to 'R_F/R_reg[13][16]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][16]' (FDCE) to 'R_F/R_reg[11][16]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][16])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][17]' (FDCE) to 'R_F/R_reg[13][17]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][17]' (FDCE) to 'R_F/R_reg[11][17]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][17])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][18]' (FDCE) to 'R_F/R_reg[13][18]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][18]' (FDCE) to 'R_F/R_reg[11][18]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][18])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][19]' (FDCE) to 'R_F/R_reg[13][19]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][19]' (FDCE) to 'R_F/R_reg[11][19]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][19])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][20]' (FDCE) to 'R_F/R_reg[13][20]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][20]' (FDCE) to 'R_F/R_reg[11][20]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][20])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][21]' (FDCE) to 'R_F/R_reg[13][21]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][21]' (FDCE) to 'R_F/R_reg[11][21]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][21])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][22]' (FDCE) to 'R_F/R_reg[13][22]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][22]' (FDCE) to 'R_F/R_reg[11][22]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][22])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][23]' (FDCE) to 'R_F/R_reg[13][23]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][23]' (FDCE) to 'R_F/R_reg[11][23]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][23])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][24]' (FDCE) to 'R_F/R_reg[13][24]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][24]' (FDCE) to 'R_F/R_reg[11][24]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][24])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][25]' (FDCE) to 'R_F/R_reg[13][25]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][25]' (FDCE) to 'R_F/R_reg[11][25]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][25])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][26]' (FDCE) to 'R_F/R_reg[13][26]'

INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][26]' (FDCE) to 'R_F/R_reg[11][26]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][26])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][27]' (FDCE) to 'R_F/R_reg[13][27]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][27]' (FDCE) to 'R_F/R_reg[11][27]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][27])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][28]' (FDCE) to 'R_F/R_reg[13][28]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][28]' (FDCE) to 'R_F/R_reg[11][28]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][28])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][29]' (FDCE) to 'R_F/R_reg[13][29]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][29]' (FDCE) to 'R_F/R_reg[11][29]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][29])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][30]' (FDCE) to 'R_F/R_reg[13][30]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][30]' (FDCE) to 'R_F/R_reg[11][30]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][30])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][31]' (FDCE) to 'R_F/R_reg[13][31]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][31]' (FDCE) to 'R_F/R_reg[11][31]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][31])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][0]' (FDCE) to 'R_F/R_reg[13][0]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][0]' (FDCE) to 'R_F/R_reg[11][0]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][0])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][1]' (FDCE) to 'R_F/R_reg[13][1]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][1]' (FDCE) to 'R_F/R_reg[11][1]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][1])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][2]' (FDCE) to 'R_F/R_reg[13][2]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][2]' (FDCE) to 'R_F/R_reg[11][2]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][2])
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[14][3]' (FDCE) to 'R_F/R_reg[13][3]'
INFO: [Synth 8-3886] merging instance 'R_F/R_reg[13][3]' (FDCE) to 'R_F/R_reg[11][3]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\R_F/R_reg[11][3])
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[31]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[30]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[29]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[28]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[27]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[26]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[25]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[24]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[23]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[22]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[21]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[20]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[19]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[18]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[17]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[16]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[15]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[14]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[13]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[12]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[11]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[10]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[9]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[8]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[7]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[6]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (NextAddress/next_pc_reg[5]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][31]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][30]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][29]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][28]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][27]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][26]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][25]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][24]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][23]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][22]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][21]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][20]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][19]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][18]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][17]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][16]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][15]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][14]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][13]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][12]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][11]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][10]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][9]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][8]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][7]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][6]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][5]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][4]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][3]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][2]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][1]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[8][0]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][31]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][30]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][29]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][28]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][27]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][26]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][25]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][24]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][23]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][22]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][21]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][20]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][19]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][18]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][17]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][16]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][15]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][14]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][13]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][12]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][11]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][10]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][9]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][8]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][7]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][6]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][5]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][4]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][3]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][2]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][1]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[9][0]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][31]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][30]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][29]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][28]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][27]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][26]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][25]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][24]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (R_F/R_reg[10][23]) is unused and will be removed from module cpu.
INFO: [Common 17-14] Message 'Synth 8-3332' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set_msg_config to change the current settings.

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:19 ; elapsed = 00:00:47 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9238 ; free virtual = 21706

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:23 ; elapsed = 00:00:57 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9080 ; free virtual = 21549

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:24 ; elapsed = 00:00:58 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9079 ; free virtual = 21548

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Technology Mapping

INFO: [Synth 8-3886] merging instance 'ctrl_sig_reg[3]' (LD) to 'ctrl_sig_reg[9]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\ctrl_sig_reg[9])

Finished Technology Mapping : Time (s): cpu = 00:00:25 ; elapsed = 00:00:59 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9075 ; free virtual = 21544

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:26 ; elapsed = 00:00:59 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9075 ; free virtual = 21544

Report Check Netlist:
+------+----------------+-------+---------+-------+----------------+
| |Item |Errors |Warnings |Status |Description |
+------+----------------+-------+---------+-------+----------------+
|1 |multi_driven_nets | 0| 0|Passed |Multi driven nets |
+------+----------------+-------+---------+-------+----------------+

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:26 ; elapsed = 00:00:59 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9075 ; free virtual = 21544

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:26 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9075 ; free virtual = 21544

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:26 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9075 ; free virtual = 21544

```
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:26 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9075 ; free virtual = 21544
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:26 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9075 ; free virtual = 21544
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |    14|
|3     |LUT1   |     1|
|4     |LUT2   |    14|
|5     |LUT3   |    45|
|6     |LUT4   |    26|
|7     |LUT5   |   142|
|8     |LUT6   |   466|
|9     |MUXF7  |   176|
|10    |MUXF8  |    62|
|11    |FDCE   |  1285|
|12    |LD     |    17|
|13    |IBUF   |     2|
|14    |OBUF   |    14|
+------+-------+------+

Report Instance Areas:
+------+--------------+------------+------+
|      |Instance      |Module      |Cells |
+------+--------------+------------+------+
|1     |top           |            |  2265|
|2     |  A           |alu         |    77|
|3     |  D_C         |d_cache     |  1486|
|4     |  NextAddress |next_address |    13|
|5     |  PC          |pc_comp     |    84|
|6     |  R_F         |regfile     |   576|
+------+--------------+------------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:26 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9075 ; free virtual = 21544
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 761 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:19 ; elapsed = 00:00:29 . Memory (MB): peak = 1842.969 ; gain = 131.445 ; free physical = 9133 ; free virtual = 21602
Synthesis Optimization Complete : Time (s): cpu = 00:00:26 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.969 ; gain = 527.199 ; free physical = 9143 ; free virtual = 21613
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 271 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 17 instances were transformed.
  LD => LDCE: 17 instances

INFO: [Common 17-83] Releasing license: Synthesis
205 Infos, 102 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
```

synth_design: Time (s): cpu = 00:00:27 ; elapsed = 00:01:01 . Memory (MB): peak = 1844.973 ; gain = 541.852 ; free physical = 9130 ; free virtual = 21600
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.runs/synth_1/cpu.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file cpu_utilization_synth.rpt -pb cpu_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.14 . Memory (MB): peak = 1868.992 ; gain = 0.000 ; free physical = 9128 ; free virtual = 21598
INFO: [Common 17-206] Exiting Vivado at Tue Nov 28 16:47:38 2023...

“impl_1 runme.log”

*** Running vivado
  with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source cpu.tcl -notrace

****** Vivado v2018.2 (64-bit)
 **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
 **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
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source cpu.tcl -notrace
Command: link_design -top cpu -part xc7a100tcsg324-1
Design is defaulting to srcset: sources_1
Design is defaulting to constrset: constrs_1
INFO: [Netlist 29-17] Analyzing 254 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/constrs_1/new/xdc.xdc]
Finished Parsing XDC File [/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.srcs/constrs_1/new/xdc.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
link_design completed successfully
link_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:31 . Memory (MB): peak = 1654.371 ; gain = 346.242 ; free physical = 9290 ; free virtual = 21756
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1747.398 ; gain = 93.027 ; free physical = 9279 ; free virtual = 21745

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: c1ca35ef

Time (s): cpu = 00:00:10 ; elapsed = 00:00:36 . Memory (MB): peak = 2199.895 ; gain = 452.496 ; free physical = 8871 ; free virtual = 21337

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: c1ca35ef

Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.05 . Memory (MB): peak = 2199.895 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21369
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: c1ca35ef

Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2199.895 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21369
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: 13c8d20b9

Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2199.895 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21368
INFO: [Opt 31-389] Phase Sweep created 1 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 13c8d20b9

Time (s): cpu = 00:00:00.14 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2199.895 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21368
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 12cf1502f

Time (s): cpu = 00:00:00.16 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2199.895 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21368
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 81f6e717

Time (s): cpu = 00:00:00.17 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2199.895 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21368
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2199.895 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21368
Ending Logic Optimization Task | Checksum: 81f6e717

Time (s): cpu = 00:00:00.17 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2199.895 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21368

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 81f6e717

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2199.898 ; gain = 0.004 ; free physical = 8903 ; free virtual = 21368

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 81f6e717

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2199.898 ; gain = 0.000 ; free physical = 8903 ; free virtual = 21368
INFO: [Common 17-83] Releasing license: Implementation
23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:39 . Memory (MB): peak = 2199.898 ; gain = 545.527 ; free physical = 8903 ; free virtual = 21368
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.15 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2231.914 ; gain = 0.004 ; free physical = 8899 ; free virtual = 21366
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.runs/impl_1/cpu_opt.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file cpu_drc_opted.rpt -pb cpu_drc_opted.pb -rpx cpu_drc_opted.rpx
Command: report_drc -file cpu_drc_opted.rpt -pb cpu_drc_opted.pb -rpx cpu_drc_opted.rpx
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.runs/impl_1/cpu_drc_opted.rpt.
report_drc completed successfully
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2311.953 ; gain = 0.000 ; free physical = 8858 ; free virtual = 21324

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 519a66be

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2311.953 ; gain = 0.000 ; free physical = 8858 ; free virtual = 21324
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2311.953 ; gain = 0.000 ; free physical = 8858 ; free virtual = 21324

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
WARNING: [Place 30-574] Poor placement for routing between an IO pin and BUFG. This is normally an ERROR but the CLOCK_DEDICATED_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

    clk_IBUF_inst (IBUF.O) is locked to IOB_X0Y82
    clk_IBUF_BUFG_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL_X0Y0
Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 48d2502c

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.60 . Memory (MB): peak = 2311.953 ; gain = 0.000 ; free physical = 8855 ; free virtual = 21321

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 88056526

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.64 . Memory (MB): peak = 2311.953 ; gain = 0.000 ; free physical = 8854 ; free virtual = 21321

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 88056526

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.64 . Memory (MB): peak = 2311.953 ; gain = 0.000 ; free physical = 8854 ; free virtual = 21321
Phase 1 Placer Initialization | Checksum: 88056526

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.64 . Memory (MB): peak = 2311.953 ; gain = 0.000 ; free physical = 8854 ; free virtual = 21321

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 88056526

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.66 . Memory (MB): peak = 2311.953 ; gain = 0.000 ; free physical = 8852 ; free virtual = 21319
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: 12687d7a1

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8832 ; free virtual = 21298

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 12687d7a1

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8832 ; free virtual = 21298

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 1554a98bf

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8832 ; free virtual = 21298

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 14d7e2851

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8832 ; free virtual = 21298

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 14d7e2851

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8832 ; free virtual = 21298

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8826 ; free virtual = 21292

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8826 ; free virtual = 21292

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8826 ; free virtual = 21292
Phase 3 Detail Placement | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8826 ; free virtual = 21292

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8826 ; free virtual = 21292

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8828 ; free virtual = 21294

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8828 ; free virtual = 21294

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8828 ; free virtual = 21294
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 180aac176

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8828 ; free virtual = 21294
Ending Placer Task | Checksum: cd199408

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2372.977 ; gain = 61.023 ; free physical = 8845 ; free virtual = 21311
INFO: [Common 17-83] Releasing license: Implementation
41 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.34 ; elapsed = 00:00:00.33 . Memory (MB): peak = 2372.977 ; gain = 0.000 ; free physical = 8841 ; free virtual = 21311
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.runs/impl_1/cpu_placed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_io -file cpu_io_placed.rpt
report_io: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.09 . Memory (MB): peak = 2372.977 ; gain = 0.000 ; free physical = 8838 ; free virtual = 21305
INFO: [runtcl-4] Executing : report_utilization -file cpu_utilization_placed.rpt -pb cpu_utilization_placed.pb
report_utilization: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2372.977 ; gain = 0.000 ; free physical = 8845 ; free virtual = 21312
INFO: [runtcl-4] Executing : report_control_sets -verbose -file cpu_control_sets_placed.rpt
report_control_sets: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2372.977 ; gain = 0.000 ; free physical = 8845 ; free virtual = 21312
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement for routing between an IO pin and BUFG.
Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.
This is normally an ERROR but the CLOCK_DEDICATED_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

clk_IBUF_inst (IBUF.O) is locked to IOB_X0Y82
clk_IBUF_BUFG_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL_X0Y0
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: a2daed43 ConstDB: 0 ShapeSum: 2a3ea6c5 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: eb566d1e

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2410.574 ; gain = 37.598 ; free physical = 8768 ; free virtual = 21228
Post Restoration Checksum: NetGraph: 2e8d8fc2 NumContArr: bcc8dd5c Constraints: 0 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: eb566d1e

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2415.562 ; gain = 42.586 ; free physical = 8737 ; free virtual = 21197

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: eb566d1e

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2415.562 ; gain = 42.586 ; free physical = 8737 ; free virtual = 21197
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: 19353e791

Time (s): cpu = 00:00:16 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8724 ; free virtual = 21184

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: 77b248a7

Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21188

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 171
 Number of Nodes with overlaps = 1
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: e23faa38

Time (s): cpu = 00:00:19 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21188
Phase 4 Rip-up And Reroute | Checksum: e23faa38

Time (s): cpu = 00:00:19 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21188

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: e23faa38

Time (s): cpu = 00:00:19 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21188

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: e23faa38

Time (s): cpu = 00:00:19 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21188
Phase 6 Post Hold Fix | Checksum: e23faa38

Time (s): cpu = 00:00:19 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21188

Phase 7 Route finalize

Router Utilization Summary
 Global Vertical Routing Utilization = 0.281412 %
 Global Horizontal Routing Utilization = 0.374396 %
 Routable Net Status*
 *Does not include unroutable nets such as driverless and loadless.
 Run report_route_status for detailed report.
 Number of Failed Nets = 0
 Number of Unrouted Nets = 0
 Number of Partially Routed Nets = 0
 Number of Node Overlaps = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 31.5315%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 24.3243%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 35.2941%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 30.8824%, No Congested Regions.

Reporting congestion hotspots

```
---------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: e23faa38

Time (s): cpu = 00:00:19 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21188

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: e23faa38

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21187

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 97f0816c

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8728 ; free virtual = 21187
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2443.828 ; gain = 70.852 ; free physical = 8762 ; free virtual = 21222

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
54 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2443.832 ; gain = 70.855 ; free physical = 8762 ; free virtual = 21221
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.52 ; elapsed = 00:00:00.42 . Memory (MB): peak = 2443.832 ; gain = 0.000 ; free physical = 8756 ; free virtual = 21219
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.runs/impl_1/cpu_routed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file cpu_drc_routed.rpt -pb cpu_drc_routed.pb -rpx cpu_drc_routed.rpx
Command: report_drc -file cpu_drc_routed.rpt -pb cpu_drc_routed.pb -rpx cpu_drc_routed.rpx
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.runs/impl_1/cpu_drc_routed.rpt.
report_drc completed successfully
INFO: [runtcl-4] Executing : report_methodology -file cpu_methodology_drc_routed.rpt -pb cpu_methodology_drc_routed.pb -rpx
cpu_methodology_drc_routed.rpx
Command: report_methodology -file cpu_methodology_drc_routed.rpt -pb cpu_methodology_drc_routed.pb -rpx cpu_methodology_drc_routed.rpx
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [DRC 23-133] Running Methodology with 8 threads
INFO: [Coretcl 2-1520] The results of Report Methodology are in file
/nfs/home/k/k_jask/COEN316/lab4/code/lab4coen316/lab4coen316.runs/impl_1/cpu_methodology_drc_routed.rpt.
report_methodology completed successfully
INFO: [runtcl-4] Executing : report_power -file cpu_power_routed.rpt -pb cpu_power_summary_routed.pb -rpx cpu_power_routed.rpx
Command: report_power -file cpu_power_routed.rpt -pb cpu_power_summary_routed.pb -rpx cpu_power_routed.rpx
WARNING: [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock,
otherwise the vectorless estimation might be inaccurate
INFO: [Timing 38-35] Done setting XDC timing constraints.
Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation
66 Infos, 4 Warnings, 0 Critical Warnings and 0 Errors encountered.
report_power completed successfully
INFO: [runtcl-4] Executing : report_route_status -file cpu_route_status.rpt -pb cpu_route_status.pb
```

INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file cpu_timing_summary_routed.rpt -pb cpu_timing_summary_routed.pb -rpx cpu_timing_summary_routed.rpx -warn_on_violation
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
INFO: [runtcl-4] Executing : report_incremental_reuse -file cpu_incremental_reuse_routed.rpt
INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
INFO: [runtcl-4] Executing : report_clock_utilization -file cpu_clock_utilization_routed.rpt
INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file cpu_bus_skew_routed.rpt -pb cpu_bus_skew_routed.pb -rpx cpu_bus_skew_routed.rpx
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
Command: write_bitstream -force cpu.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set_property CFGBVS value1 [current_design]
#where value1 is either VCCO or GND

set_property CONFIG_VOLTAGE value2 [current_design]
#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
WARNING: [DRC PDRC-153] Gated clock check: Net NextAddress/next_pc_reg[4]_i_2_n_0 is a gated clock net sourced by a combinational pin NextAddress/next_pc_reg[4]_i_2/O, cell NextAddress/next_pc_reg[4]_i_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.
WARNING: [DRC PDRC-153] Gated clock check: Net PC/R_reg[0][31]_0[0] is a gated clock net sourced by a combinational pin PC/ctrl_sig_reg[13]_i_2/O, cell PC/ctrl_sig_reg[13]_i_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 3 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./cpu.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
83 Infos, 8 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:10 . Memory (MB): peak = 2781.746 ; gain = 227.816 ; free physical = 8711 ; free virtual = 21181
INFO: [Common 17-206] Exiting Vivado at Tue Nov 28 16:49:46 2023...