COEN 316: COMPUTER ARCHITECTURE & DESIGN

Section DM-X

LAB REPORT # 3: NEXT-ADDRESS UNIT

INSTRUCTOR:
Dr. Fadi Alzhouri

Lab Coordinator:
Ted Obuchowicz

Submitted by:
Jaskirat Kaur
40138320

"I certify that this submission is my original work and meets the Faculty's Expectations of Originality"

Date Written: Wednesday, November 16, 2023

Objective

The main objective of the third lab is to design a Next-Address unit in VHDL that will be stored in the PC register. This unit will then be used in subsequent labs as part of component of a CPU. There is a given entity specification to be used for the design of the unit.

Introduction

The Next-Address unit is a crucial component, as it is responsible for giving the next address that is stored in the Program Counter register will work on. This data can be various things, like instructions or memory addresses. There are different ways to create the Next-Address, but in this particular lab, we're focusing on its inputs as a 32-bit value for the PC register, the contents of a rs and rt registers, a 26-bit jump target address and a 2-bit PC_sel generated by the control unit.

Theory

The inputs to the next-address unit encompass the following components:

- The 32-bit value contained within the PC register.
- The contents of both the rs and rt registers, which require comparison in the event of branch instructions.
- The 26-bit jump target address, found within a jump instruction. In cases of branch instructions, the lower 16 bits among these 26 bits constitute 16-bit immediate data, representing the signed branch offset value. This value is subject to a sign extension, resulting in a 32-bit signed offset.
- A 2-bit PC_sel signal, to be generated by the control unit. This signal is responsible for choosing one of the three inputs for a multiplexer, based on the criteria outlined in the following table:

Table 1: PC_sel functionality

PC_sel	comment
00	no *unconditional* jump (**straightline** instructions as well as the **conditional** branches will have PC_sel = 00).
01	jump
10	jump register
11	not used

As indicated in Table 1, the control signal PC_sel will be configured (by the control unit) as follows:

- For all "non-jump" instructions, such as arithmetic and logical instructions, as well as the three conditional branch instructions (beq, bne, bltz), PC_sel will be set to 00.
- In the case of a jump instruction, which represents an unconditional jump, the control unit will set the value of PC_sel to 01.
- A jump register instruction will be chosen with PC_sel set to 10 (also determined by the control unit).
- Additionally, there is a 2-bit branch_type signal, also generated by the control unit, which specifies one of four potential branch types.
- It is important to note that PC_sel will be equal to 00 for all four possible values of the branch_type signal.

Table 2: branch_type functionality

branch_type	Meaning	Value to be added to PC
00	no branch (straight-line code such as `add`, `sub`, `and`, `xor`, etcetera)	1 (as a 32 bit number)
01	`beq` (*conditional* branch equal to 0)	1 + branch offset value sign extended to 32 bits if rs = rt, otherwise 1 is to be added
10	bne (*conditional* branch not equal to 0)	1 + branch offset value sign extended to 32 bits if rs /= rt, otherwise 1 is to be added
11	`bltz` (*conditional* branch less than zero)	1 + branch offset value sign extended to 32 bits is rs <0, otherwise 1 is to be added

As outlined in Table 2, the 2-bit branch_type input plays a crucial role in determining the type of branching and, consequently, the value to be added to the PC register for the calculation of the next address.

- When the branch_type is set to 00, signifying no branching is required, a constant value of 1 is added to the PC, indicating sequential execution along the current instruction path.
- For the remaining three values that specify conditional branching instructions (branch equal, branch not equal, branch less than zero), the action taken depends on whether the condition specified by comparing the contents of the rs and rt registers is met.
- If the condition is satisfied, the value of 1 added to the sign-extended branch offset is added to the PC. Conversely, if the condition is not satisfied (false), only the value of 1 is added to the PC.
- This dynamic adjustment determines the subsequent instruction flow based on the conditional evaluation.

To design the Next-Address unit file using VHDL, processes using case statements will be used. To simulate the code using Modelsim simulator, a do file with the adequate inputs will verify all the possible operations of the register file. Finally, an xdc file will be used to implement the Next-Address unit design on a Nexys A7 FPGA board.

Conclusion

To conclude, in this third lab, the 32-bit NextAddress was coded and simulated using processes and CSA statements VHDL. It was then implemented on the Nexys board using the software Vivado. It is now to be seen how this register will be used as a component of the CPU that will be build in the subsequent lab.

Appendix

do.do

```
add wave rt
add wave rs
add wave pc
add wave target_address
add wave branch_type
add wave pc_sel
add wave next_pc_temp
add wave next_pc

force pc X"00000000"
force pc_sel "00"
force target_address "00111011001110001100010110"

force rt X"00000001"
force rs X"00000002"
force branch_type "00"
run 2

force pc X"00000001"
force branch_type "01"
run 2


force pc X"00000002"
force rt X"00000003"
force rs X"00000003"
run 2


force pc X"00000003"
force branch_type "10"
run 2


force pc X"00000004"
force rt X"00000004"
force rs X"00000005"
run 2


force pc X"00000005"
force branch_type "11"
run 2

force pc X"00000006"
force rs X"F1234567"
run 2
```

```
force target_address "00111011001110001100010111"
force pc X"00000007"
force pc_sel "01"
run 2

force pc X"00000003"
force branch_type "11"
run 2

force pc X"00000008"
force pc_sel "10"
force rs X"ABCD0000"
run 2
```

The 32-bit Next-Address code simulated correctly. And the Board-wrapper version of the register was implemented in vivado.

Next_address.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity next_address is
port(rt, rs : in std_logic_vector(31 downto 0);
-- two register inputs
pc: in std_logic_vector(31 downto 0);
target_address : in std_logic_vector(25 downto 0);
branch_type: in std_logic_vector(1 downto 0);
pc_sel: in std_logic_vector(1 downto 0);
next_pc: out std_logic_vector(31 downto 0));
end next_address ;


architecture rtl of next_address is
signal next_pc_temp : std_logic_vector(31 downto 0);
begin

process(rt, rs, pc, pc_sel, branch_type, target_address, next_pc_temp)
begin

case pc_sel is

when "00" => next_pc <= next_pc_temp;

        case branch_type is
        when "00" => next_pc_temp <= pc + X"00000001";

        when "01" =>
        if (rs = rt) then
        next_pc_temp <= pc + X"00000001" + ((31 downto 16 => target_address(15)) & target_address(15 downto 0));
        else
        next_pc_temp <= pc + X"00000001";
        end if;

        when "10" =>
        if (rs /= rt) then
        next_pc_temp <= pc + X"00000001" + ((31 downto 16 => target_address(15)) & target_address(15 downto 0));
        else
        next_pc_temp <= pc + X"00000001";
        end if;

        when "11" =>
        if (rs < 0) then
        next_pc_temp <= pc + X"00000001" + ((31 downto 16 => target_address(15)) & target_address(15 downto 0));
        else
        next_pc_temp <= pc + X"00000001";
        end if;

        when others =>
        end case;


when "01" => next_pc <= "000000" & target_address(25 downto 0);

when "10" => next_pc <= rs;

when others => next_pc <= pc + X"00000001";

end case;
end process;
end architecture;
```

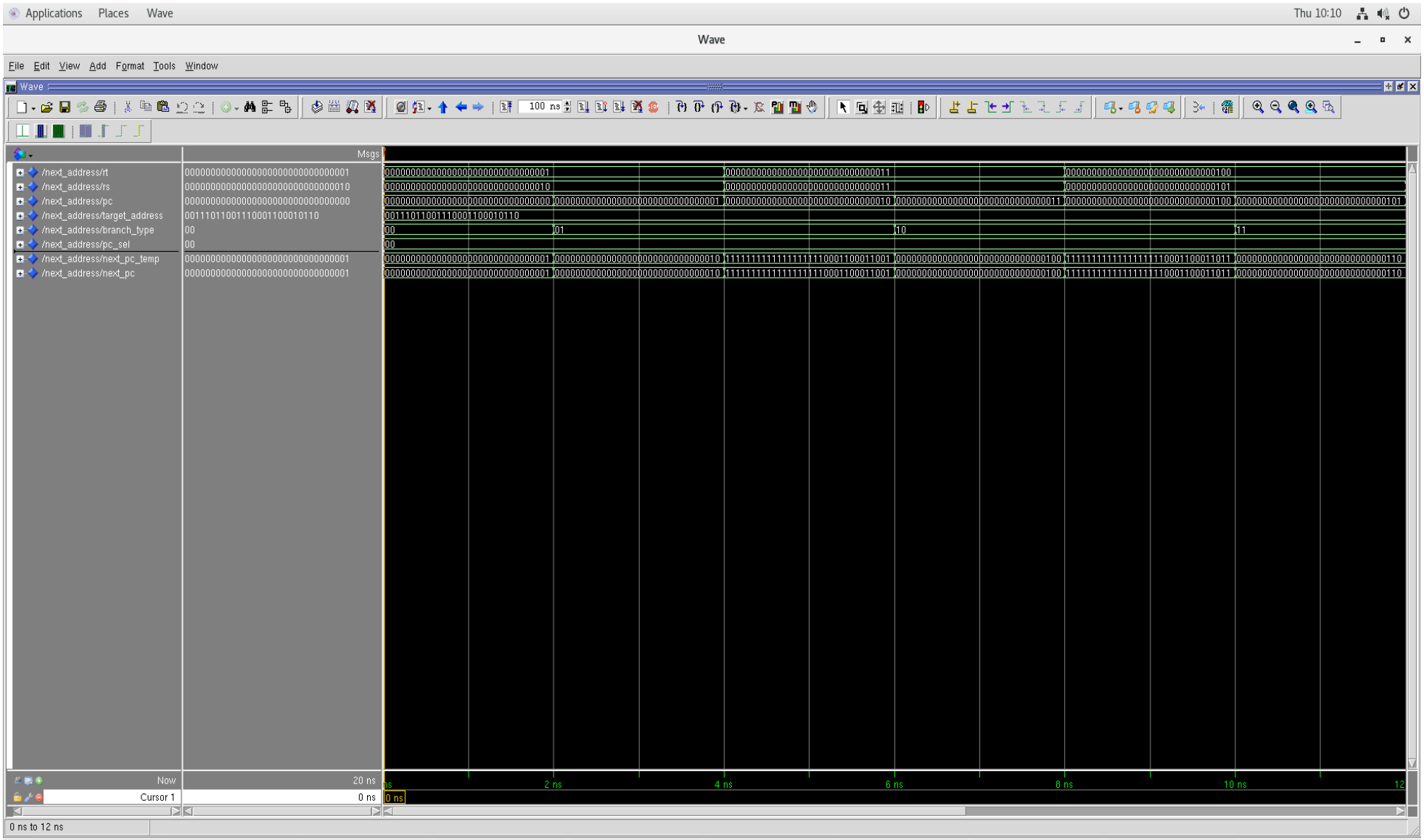
nextAddress_board.vhd

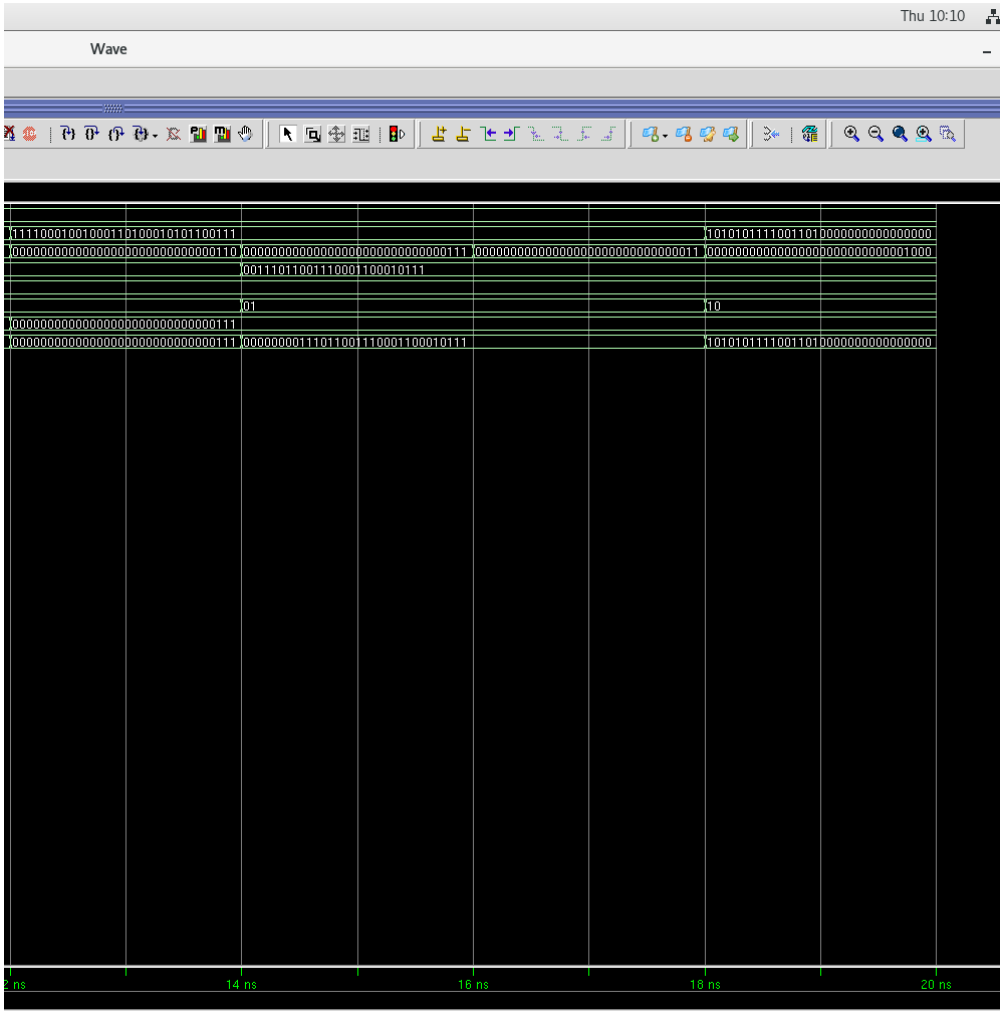
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity next_address is
port(rt_in, rs_in : in std_logic_vector(1 downto 0);
-- two register inputs
pc_in: in std_logic_vector(2 downto 0);
target_address_in : in std_logic_vector(2 downto 0);
branch_type: in std_logic_vector(1 downto 0);
pc_sel: in std_logic_vector(1 downto 0);
next_pc_out: out std_logic_vector(2 downto 0));
end next_address ;


architecture rtl of next_address is

signal next_pc_temp : std_logic_vector(31 downto 0);
signal rt, rs, pc : std_logic_vector(31 downto 0);
signal next_pc : std_logic_vector(31 downto 0);
signal target_address : std_logic_vector(25 downto 0);


begin
rt(1 downto 0 )<=rt_in(1)&rt_in(0);
rt(31 downto 2 )<=(others=>'0');
rs(1 downto 0) <= rs_in(1) & rs_in(0);
rs(31 downto 2) <= (others=>'0');
pc(2 downto 0) <= pc_in(2) & pc_in(1) & pc_in(0);
pc(31 downto 3) <= (others=>'0');
target_address(2 downto 0) <= target_address_in(2) & target_address_in(1) & target_address_in(0);
target_address(25 downto 3) <= (others=>'0');

process(rt, rs, pc, pc_sel, branch_type, target_address, next_pc_temp)
begin
```

```
case pc_sel is

when "00" => next_pc <= next_pc_temp;

        case branch_type is
        when "00" => next_pc_temp <= pc + X"00000001";

        when "01" =>
        if (rs = rt) then
        next_pc_temp <= pc + X"00000001" + ((31 downto 16 => target_address(15)) & target_address(15 downto 0));
        else
        next_pc_temp <= pc + X"00000001";
        end if;

        when "10" =>
        if (rs /= rt) then
        next_pc_temp <= pc + X"00000001" + ((31 downto 16 => target_address(15)) & target_address(15 downto 0));
        else
        next_pc_temp <= pc + X"00000001";
        end if;

        when "11" =>
        if (rs < 0) then
        next_pc_temp <= pc + X"00000001" + ((31 downto 16 => target_address(15)) & target_address(15 downto 0));
        else
        next_pc_temp <= pc + X"00000001";
        end if;

        when others =>
        end case;


when "01" => next_pc <= "000000" & target_address(25 downto 0);

when "10" => next_pc <= rs;

when others =>next_pc <=X"00000000";

end case;
end process;

next_pc_out(2 downto 0) <=next_pc(2 downto 0);
end architecture;
```

NextAddress.xdc

```
set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCMOS33 } [get_ports {rt_in[1]} ];
set_property -dict { PACKAGE_PIN L16 IOSTANDARD LVCMOS33 } [get_ports {rt_in[0]} ];
set_property -dict { PACKAGE_PIN M13 IOSTANDARD LVCMOS33 } [get_ports {rs_in[1]} ];
set_property -dict { PACKAGE_PIN R15 IOSTANDARD LVCMOS33 } [get_ports {rs_in[0]} ];
set_property -dict { PACKAGE_PIN R17 IOSTANDARD LVCMOS33 } [get_ports {pc_in[2]} ];
set_property -dict { PACKAGE_PIN T18 IOSTANDARD LVCMOS33 } [get_ports {pc_in[1]} ];
set_property -dict { PACKAGE_PIN U18 IOSTANDARD LVCMOS33 } [get_ports {pc_in[0]} ];
set_property -dict { PACKAGE_PIN R13 IOSTANDARD LVCMOS33 } [get_ports {target_address_in[2]} ];
set_property -dict { PACKAGE_PIN T8 IOSTANDARD LVCMOS33 } [get_ports {target_address_in[1]} ];
set_property -dict { PACKAGE_PIN U8 IOSTANDARD LVCMOS33 } [get_ports {target_address_in[0]} ];
set_property -dict { PACKAGE_PIN R16 IOSTANDARD LVCMOS33 } [get_ports {branch_type[1]} ];
set_property -dict { PACKAGE_PIN T13 IOSTANDARD LVCMOS33 } [get_ports {branch_type[0]} ];
set_property -dict { PACKAGE_PIN H6 IOSTANDARD LVCMOS33 } [get_ports {pc_sel[1]} ];
set_property -dict { PACKAGE_PIN U12 IOSTANDARD LVCMOS33 } [get_ports {pc_sel[0]} ];
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 } [get_ports {next_pc_out[2]} ];
set_property -dict { PACKAGE_PIN K15 IOSTANDARD LVCMOS33 } [get_ports {next_pc_out[1]} ];
set_property -dict { PACKAGE_PIN J13 IOSTANDARD LVCMOS33 } [get_ports {next_pc_out[0]} ];
```


Applications
Places
Wave
Thu 10:10
Wave
File Edit View Add Format Tools Window
Wave
100 ns
Msgs
/next_address/rt
/next_address/rs
/next_address/pc
/next_address/target_address
/next_address/branch_type
/next_address/pc_sel
/next_address/next_pc_temp
/next_address/next_pc
00000000000000000000000000000001
00000000000000000000000000000010
00000000000000000000000000000000
00111011001110001100010110
00
00
00000000000000000000000000000001
00000000000000000000000000000001
00000000000000000000000000000010
00000000000000000000000000000011
00000000000000000000000000000100
00000000000000000000000000000101
00000000000000000000000000000010
00000000000000000000000000000011
11111111111111111110001100011001
11111111111111111110001100011011
00000000000000000000000000000100
00000000000000000000000000000110
01
10
11
Now
20 ns
Cursor 1
0 ns
2 ns
4 ns
6 ns
8 ns
10 ns
0 ns to 12 ns


Thu 10:10
Wave
14 ns
16 ns
18 ns
20 ns

Synythesis Runme.log:

```
*** Running vivado
   with args -log next_address.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source next_address.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
   ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source next_address.tcl -notrace
Command: synth_design -top next_address -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 11952
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.578 ; gain = 85.805 ; free physical = 9319 ; free virtual = 21420
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'next_address'
[/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/sources_1/imports/CODE/nextAddress_board.vhd:17]
INFO: [Synth 8-226] default block is never used
[/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/sources_1/imports/CODE/nextAddress_board.vhd:42]
INFO: [Synth 8-256] done synthesizing module 'next_address' (1#1)
[/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/sources_1/imports/CODE/nextAddress_board.vhd:17]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 9331 ; free virtual = 21432
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |     0|       0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 9331 ; free
virtual = 21432
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 9331 ; free
virtual = 21432
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/constrs_1/new/XDC.xdc]
Finished Parsing XDC File [/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/constrs_1/new/XDC.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file
[/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/constrs_1/new/XDC.xdc]. These constraints will be ignored for
synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/next_address_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/next_address_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the
used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1791.973 ; gain = 0.000 ; free physical = 9029 ; free virtual =
21132
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9148 ; free virtual =
21250
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9148
; free virtual = 21250
---------------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical =
9149 ; free virtual = 21251
---------------------------------------------------------------------------------
WARNING: [Synth 8-3936] Found unconnected internal register 'next_pc_temp_reg' and it is trimmed from '32' to '3' bits.
[/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/sources_1/imports/CODE/nextAddress_board.vhd:40]
WARNING: [Synth 8-327] inferring latch for variable 'next_pc_temp_reg'
[/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/sources_1/imports/CODE/nextAddress_board.vhd:40]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9140 ; free
virtual = 21243
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
                2 Input     3 Bit      Adders := 1
                3 Input     3 Bit      Adders := 1
+---Muxes :
                4 Input     3 Bit       Muxes := 2
                2 Input     3 Bit       Muxes := 3
                4 Input     1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module next_address
Detailed RTL Component Info :
+---Adders :
                2 Input     3 Bit      Adders := 1
                3 Input     3 Bit      Adders := 1
+---Muxes :
                4 Input     3 Bit       Muxes := 2
                2 Input     3 Bit       Muxes := 3
                4 Input     1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical =
9129 ; free virtual = 21233
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ;
free virtual = 21108
```

```
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free virtual =
21108
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free virtual =
21108
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free virtual = 21108
---------------------------------------------------------------------------------

Report Check Netlist:
+------+-----------------+-------+---------+-------+-----------------+
|      |Item             |Errors |Warnings |Status |Description      |
+------+-----------------+-------+---------+-------+-----------------+
|1     |multi_driven_nets|      0|        0|Passed |Multi driven nets|
+------+-----------------+-------+---------+-------+-----------------+
---------------------------------------------------------------------------------
Start Renaming Generated Instances
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free
virtual = 21108
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free
virtual = 21108
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Ports
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free
virtual = 21108
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
```

```
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free virtual = 21108
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free virtual = 21108
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |LUT3 |     1|
|3     |LUT4 |     1|
|4     |LUT5 |     4|
|5     |LUT6 |     2|
|6     |LD   |     3|
|7     |IBUF |    14|
|8     |OBUF |     3|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    29|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9004 ; free virtual = 21108
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 2 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:18 . Memory (MB): peak = 1791.973 ; gain = 130.445 ; free physical = 9058 ; free virtual = 21162
Synthesis Optimization Complete : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1791.973 ; gain = 476.199 ; free physical = 9069 ; free virtual = 21173
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 17 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 3 instances were transformed.
  LD => LDCE: 3 instances

INFO: [Common 17-83] Releasing license: Synthesis
15 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:17 ; elapsed = 00:00:50 . Memory (MB): peak = 1822.973 ; gain = 519.848 ; free physical = 9055 ; free virtual = 21159
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint
'/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.runs/synth_1/next_address.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file next_address_utilization_synth.rpt -pb next_address_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.09 . Memory (MB): peak = 1846.996 ; gain = 0.000 ; free physical = 9056 ; free virtual = 21160
INFO: [Common 17-206] Exiting Vivado at Thu Nov 16 11:56:02 2023...
```

Implementation Runme.log:

```
*** Running vivado
   with args -log next_address.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source next_address.tcl -notrace


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
   ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source next_address.tcl -notrace
Command: link_design -top next_address -part xc7a100tcsg324-1
Design is defaulting to srcset: sources_1
Design is defaulting to constrset: constrs_1
INFO: [Netlist 29-17] Analyzing 14 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/constrs_1/new/XDC.xdc]
Finished Parsing XDC File [/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.srcs/constrs_1/new/XDC.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
link_design completed successfully
link_design: Time (s): cpu = 00:00:06 ; elapsed = 00:00:31 . Memory (MB): peak = 1652.375 ; gain = 344.242 ; free physical = 9150 ; free virtual = 21254
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1741.402 ; gain = 89.027 ; free physical = 9140 ; free virtual = 21244

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 230495e9a

Time (s): cpu = 00:00:09 ; elapsed = 00:00:36 . Memory (MB): peak = 2166.902 ; gain = 425.500 ; free physical = 8727 ; free virtual = 20861

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 230495e9a

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 230495e9a

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: 230495e9a

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 230495e9a

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 230495e9a

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883
```

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 230495e9a

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883
Ending Logic Optimization Task | Checksum: 230495e9a

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 230495e9a

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 230495e9a

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 8749 ; free virtual = 20883
INFO: [Common 17-83] Releasing license: Implementation
23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:39 . Memory (MB): peak = 2166.902 ; gain = 514.527 ; free physical = 8749 ; free virtual = 20883
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2198.918 ; gain = 0.004 ; free physical = 8744 ; free virtual = 20879
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.runs/impl_1/next_address_opt.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file next_address_drc_opted.rpt -pb next_address_drc_opted.pb -rpx next_address_drc_opted.rpx
Command: report_drc -file next_address_drc_opted.rpt -pb next_address_drc_opted.pb -rpx next_address_drc_opted.rpx
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.runs/impl_1/next_address_drc_opted.rpt.
report_drc completed successfully
report_drc: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 2278.957 ; gain = 80.031 ; free physical = 8685 ; free virtual = 20819
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2278.957 ; gain = 0.000 ; free physical = 8683 ; free virtual = 20817
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 1a412c21e

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2278.957 ; gain = 0.000 ; free physical = 8683 ; free virtual = 20817
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2278.957 ; gain = 0.000 ; free physical = 8683 ; free virtual = 20817

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 1a412c21e

Time (s): cpu = 00:00:00.55 ; elapsed = 00:00:00.37 . Memory (MB): peak = 2278.957 ; gain = 0.000 ; free physical = 8675 ; free virtual = 20809

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 2589bd43c

Time (s): cpu = 00:00:00.60 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2278.957 ; gain = 0.000 ; free physical = 8677 ; free virtual = 20811

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 2589bd43c

Time (s): cpu = 00:00:00.61 ; elapsed = 00:00:00.40 . Memory (MB): peak = 2278.957 ; gain = 0.000 ; free physical = 8677 ; free virtual = 20811
Phase 1 Placer Initialization | Checksum: 2589bd43c

Time (s): cpu = 00:00:00.61 ; elapsed = 00:00:00.40 . Memory (MB): peak = 2278.957 ; gain = 0.000 ; free physical = 8677 ; free virtual = 20811

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 2589bd43c

Time (s): cpu = 00:00:00.64 ; elapsed = 00:00:00.41 . Memory (MB): peak = 2278.957 ; gain = 0.000 ; free physical = 8675 ; free virtual = 20809
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: 20c6a2204

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.55 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8656 ; free virtual = 20790

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 20c6a2204

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.55 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8656 ; free virtual = 20790

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 28a16d0bb

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8656 ; free virtual = 20790

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 1a51b9b0f

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8656 ; free virtual = 20790

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 1a51b9b0f

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8656 ; free virtual = 20790

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8655 ; free virtual = 20789

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8655 ; free virtual = 20789

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8655 ; free virtual = 20789
Phase 3 Detail Placement | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8655 ; free virtual = 20789

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8655 ; free virtual = 20789

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8657 ; free virtual = 20791

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8657 ; free virtual = 20791

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8657 ; free virtual = 20791
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 22caa656b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8657 ; free virtual = 20791
Ending Placer Task | Checksum: 19f9ced9e

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2343.977 ; gain = 65.020 ; free physical = 8674 ; free virtual = 20808
INFO: [Common 17-83] Releasing license: Implementation
41 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2343.977 ; gain = 0.000 ; free physical = 8671 ; free virtual = 20806
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.runs/impl_1/next_address_placed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_io -file next_address_io_placed.rpt
report_io: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2343.977 ; gain = 0.000 ; free physical = 8666 ; free virtual = 20800
INFO: [runtcl-4] Executing : report_utilization -file next_address_utilization_placed.rpt -pb next_address_utilization_placed.pb
report_utilization: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2343.977 ; gain = 0.000 ; free physical = 8672 ; free virtual = 20806
INFO: [runtcl-4] Executing : report_control_sets -verbose -file next_address_control_sets_placed.rpt
report_control_sets: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2343.977 ; gain = 0.000 ; free physical = 8673 ; free virtual = 20807
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: e48e05aa ConstDB: 0 ShapeSum: bb0ee7f4 RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: 11ee75b9d

Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak = 2393.578 ; gain = 49.602 ; free physical = 8520 ; free virtual = 20655
Post Restoration Checksum: NetGraph: 3c5461d0 NumContArr: e292f9cd Constraints: 0 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 11ee75b9d

Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak = 2399.566 ; gain = 55.590 ; free physical = 8488 ; free virtual = 20623

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 11ee75b9d

Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak = 2399.566 ; gain = 55.590 ; free physical = 8488 ; free virtual = 20623
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: 1cc99e491

Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak = 2406.832 ; gain = 62.855 ; free physical = 8487 ; free virtual = 20622

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: af9456cd

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2406.832 ; gain = 62.855 ; free physical = 8485 ; free virtual = 20620

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 2
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: 185c9da05

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2406.832 ; gain = 62.855 ; free physical = 8485 ; free virtual = 20620
Phase 4 Rip-up And Reroute | Checksum: 185c9da05

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2406.832 ; gain = 62.855 ; free physical = 8485 ; free virtual = 20620

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: 185c9da05

```
Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2406.832 ; gain = 62.855 ; free physical = 8485 ; free virtual = 20620

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: 185c9da05

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2406.832 ; gain = 62.855 ; free physical = 8485 ; free virtual = 20620
Phase 6 Post Hold Fix | Checksum: 185c9da05

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2406.832 ; gain = 62.855 ; free physical = 8485 ; free virtual = 20620

Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization    = 0.0148409 %
  Global Horizontal Routing Utilization  = 0.013214 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets               = 0
  Number of Unrouted Nets             = 0
  Number of Partially Routed Nets     = 0
  Number of Node Overlaps             = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 21.6216%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 7.35294%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

---------------------------------
Reporting congestion hotspots
---------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 185c9da05

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2406.832 ; gain = 62.855 ; free physical = 8484 ; free virtual = 20619

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: 185c9da05

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2409.832 ; gain = 65.855 ; free physical = 8483 ; free virtual = 20618

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 11ac54031

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2409.832 ; gain = 65.855 ; free physical = 8483 ; free virtual = 20618
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2409.832 ; gain = 65.855 ; free physical = 8518 ; free virtual = 20653

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
54 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:20 ; elapsed = 00:00:17 . Memory (MB): peak = 2409.836 ; gain = 65.859 ; free physical = 8518 ; free virtual = 20653
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
```

```
Write XDEF Complete: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2409.836 ; gain = 0.000 ; free physical = 8514 ; free virtual = 20649
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.runs/impl_1/next_address_routed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file next_address_drc_routed.rpt -pb next_address_drc_routed.pb -rpx next_address_drc_routed.rpx
Command: report_drc -file next_address_drc_routed.rpt -pb next_address_drc_routed.pb -rpx next_address_drc_routed.rpx
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.runs/impl_1/next_address_drc_routed.rpt.
report_drc completed successfully
INFO: [runtcl-4] Executing : report_methodology -file next_address_methodology_drc_routed.rpt -pb next_address_methodology_drc_routed.pb -rpx next_address_methodology_drc_routed.rpx
Command: report_methodology -file next_address_methodology_drc_routed.rpt -pb next_address_methodology_drc_routed.pb -rpx next_address_methodology_drc_routed.rpx
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [DRC 23-133] Running Methodology with 8 threads
INFO: [Coretcl 2-1520] The results of Report Methodology are in file /nfs/home/k/k_jask/COEN316/LAB3/CODE/COEN316_LAB3_FINAL/COEN316_LAB3_FINAL.runs/impl_1/next_address_methodology_drc_routed.rpt.
report_methodology completed successfully
INFO: [runtcl-4] Executing : report_power -file next_address_power_routed.rpt -pb next_address_power_summary_routed.pb -rpx next_address_power_routed.rpx
Command: report_power -file next_address_power_routed.rpt -pb next_address_power_summary_routed.pb -rpx next_address_power_routed.rpx
WARNING: [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate
INFO: [Timing 38-35] Done setting XDC timing constraints.
Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation
66 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
report_power completed successfully
INFO: [runtcl-4] Executing : report_route_status -file next_address_route_status.rpt -pb next_address_route_status.pb
INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file next_address_timing_summary_routed.rpt -pb next_address_timing_summary_routed.pb -rpx next_address_timing_summary_routed.rpx -warn_on_violation
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
INFO: [runtcl-4] Executing : report_incremental_reuse -file next_address_incremental_reuse_routed.rpt
INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
INFO: [runtcl-4] Executing : report_clock_utilization -file next_address_clock_utilization_routed.rpt
INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file next_address_bus_skew_routed.rpt -pb next_address_bus_skew_routed.pb -rpx next_address_bus_skew_routed.rpx
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
INFO: [Common 17-206] Exiting Vivado at Thu Nov 16 11:58:12 2023...

*** Running vivado
   with args -log next_address.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source next_address.tcl -notrace


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
   ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source next_address.tcl -notrace
Command: open_checkpoint next_address_routed.dcp

Starting open_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1277.121 ; gain = 0.000 ; free physical = 9420 ; free virtual = 21555
INFO: [Netlist 29-17] Analyzing 14 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Timing 38-478] Restoring timing data from binary archive.
INFO: [Timing 38-479] Binary timing data restore complete.
INFO: [Project 1-856] Restoring constraints from binary archive.
INFO: [Project 1-853] Binary constraint restore complete.
Reading XDEF placement.
Reading placer database...
Reading XDEF routing.
Read XDEF File: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.21 . Memory (MB): peak = 2079.070 ; gain = 0.004 ; free physical = 8684 ; free virtual = 20825
Restored from archive | CPU: 0.210000 secs | Memory: 0.955551 MB |
Finished XDEF File Restore: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.21 . Memory (MB): peak = 2079.070 ; gain = 0.004 ; free physical = 8684 ; free virtual = 20825
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
```

open_checkpoint: Time (s): cpu = 00:00:17 ; elapsed = 00:01:09 . Memory (MB): peak = 2079.070 ; gain = 801.953 ; free physical = 8684 ; free virtual = 20825
Command: write_bitstream -force next_address.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set_property CFGBVS value1 [current_design]
#where value1 is either VCCO or GND

set_property CONFIG_VOLTAGE value2 [current_design]
#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
WARNING: [DRC PDRC-153] Gated clock check: Net next_pc_temp_reg[2]_i_2_n_0 is a gated clock net sourced by a combinational pin next_pc_temp_reg[2]_i_2/O, cell next_pc_temp_reg[2]_i_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 2 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./next_address.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
21 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:11 . Memory (MB): peak = 2551.910 ; gain = 472.840 ; free physical = 8616 ; free virtual = 20761
INFO: [Common 17-206] Exiting Vivado at Thu Nov 16 11:59:54 2023...