COEN 316: COMPUTER ARCHITECTURE & DESIGN

Section DM-X

LAB REPORT # 1: ARITHMETIC & LOGIC UNIT

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"I certify that this submission is my original work and meets the Faculty's Expectations of Originality"

Date Written: Wednesday, October 18, 2023

INTRODUCTION:

In this laboratory, we design and implement a 32-bit Arithmetic Logic Unit (ALU) using VHDL. ALU is responsible for performing various arithmetic and logical operations on two 32-bit input operands and producing a 32-bit output. This ALU will be used as a VHDL component in future labs.

THEORY:

An ALU is composed of the following:

- The 3 control lines “add_sub”, “logic_func” and “func” to control the operation of “adder_subtract”, “logic_func” and determine the output respectively.

- 2 input signals x, y each has 32 bits.

- 4 functions to determine the output:
  - func = 00 → output = y
  - func = 01 → output = most significant bit of the result of from adder_subtract.
  - func = 10 → output = result of adder_subtract
  - func = 11 → output = answer of logic unit

- For the adder_subtract:
  - “add_sub” = ‘0’ →output of adder_subtract = x + y
  - “add_sub” = ‘1’ → output of adder_subtract = x – y

- For the logic unit:
  - “logic_func” = “00” → output of logic_func = x AND y
  - “logic_func” = “01” → output of logic_func = x OR y
  - “logic_func” = “10” → output of logic_func = x XOR y
  - “logic_func” = “11” → output of logic_func = x NOR y

- An “overflow” output which is set to “1” whenever the answer of “adder_subtract” is overflowed. This can be determined by the sign bit of x, y, and the output of “adder_subtract”.

RESULTS:

This experiment was conducted successfully and in a professional manner. ALU was successfully simulated and demonstrated its operation on the Nexys A7 FPGA board. The objective of the lab was met and verified by the lab tutor. The “adder_subtract” reacts as expected since it can detect overflow for any given case. The logic unit and output are also verified during the simulation.

IMPORTANCE OF MESSAGES IN runme.log:

The runme.log files generated during the synthesis and implementation runs in Xilinx Vivado are essential for ensuring the correct functionality and performance of the FPGA-based project. They guide you in debugging issues, optimizing performance, and ensuring that the FPGA implementation meets your project's requirements. It's crucial to carefully review and address any errors, critical warnings, and

constraint violations to ensure a successful FPGA implementation. In this lab, for both runme.log files, there are no critical warnings or errors that were encountered.

Appendix 1: Code used for the simulation of a 32-bit ALU

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity alu is
port(x, y : in std_logic_vector(31 downto 0);
add_sub : in std_logic ;
logic_func : in std_logic_vector(1 downto 0 ) ;
func: in std_logic_vector(1 downto 0 ) ;
output: out std_logic_vector(31 downto 0) ;
overflow: out std_logic ;
zero: out std_logic);
end alu ;

architecture behaviour of alu is

signal result, logic_unit: std_logic_vector(31 downto 0);
signal overflow_check: std_logic_vector(2 downto 0);

begin

process(x,y,func,logic_func, add_sub, result, logic_unit, overflow_check)
begin

 overflow_check <= x(x'high) & y(y'high) & result(result'high);

 case add_sub is
   when'0' => result <= x+y;
        if((overflow_check="001") or (overflow_check ="001")) then
        overflow <= '1';
        else
        overflow <='0';
        end if;
   when '1' => result <= x-y;
        if((overflow_check="100") or (overflow_check ="011")) then
        overflow <= '1';
        else
        overflow <='0';
        end if;
   when others =>
 end case;


if (result=(result'range =>'0'))then
 zero<='1';
else
 zero<='0';
end if;


case logic_func is
  when"00" => logic_unit <=x and y;
  when"01" => logic_unit <=x or y;
  when"10" => logic_unit <=x xor y;
  when"11" => logic_unit <=x nor y;
  when others =>
end case;

case func is
  when"00" => output <= y;
  when"01" => output <="00000000000000000000000000000000" & result(31)
  when"10" => output <=result;
  when"11" => output <=logic_unit;
  when others =>
end case;

end process;

end behaviour;
```

Appendix 2: The "board_wrapper" code used for synthesis of the 4-bit ALU

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity alu_board is

port(x_in, y_in :in std_logic_vector(31 downto 0);
add_sub : in std_logic ;
logic_func : in std_logic_vector(1 downto 0 ) ;
func: in std_logic_vector(1 downto 0 ) ;
output_out: out std_logic_vector(31 downto 0) ;
overflow: out std_logic ;
zero: out std_logic);
end alu_board ;

architecture behaviour of alu_board is

signal result, logic_unit: std_logic_vector(31 downto 0);
signal overflow_check: std_logic_vector(2 downto 0);
signal x,y, output : std_logic_vector(31 downto 0);

begin

x(3 downto 0) <=x_in(3) &x_in(2) & x_in(1) & x_in(0);
y(3 downto 0) <=y_in(3) &y_in(2) & y_in(1) & y_in(0);
x(31 downto 4) <= (others =>'0');
y(31 downto 4) <= (others =>'0');

output_out(3 downto 0) <= output(3 downto 0);

process(x,y,func,logic_func, add_sub, result, logic_unit, overflow_check)
begin

overflow_check <= x(x'high) & y(y'high) & result(result'high);

 case add_sub is
   when'0' => result <= x+y;
        if((overflow_check="001") or (overflow_check ="001")) then
        overflow <= '1';
        else
        overflow <='0';
        end if;
   when '1' => result <= x-y;
        if((overflow_check="100") or (overflow_check ="011")) then
        overflow <= '1';
        else
        overflow <='0';
        end if;
   when others =>
 end case;

if (result=(result'range =>'0'))then
 zero<='1';
else
 zero<='0';
end if;


case logic_func is
  when"00" => logic_unit <=x and y;
  when"01" => logic_unit <=x or y;
  when"10" => logic_unit <=x xor y;
  when"11" => logic_unit <=x nor y;
  when others =>
end case;


case func is
  when"00" => output <= y;
  when"01" => output <="00000000000000000000000000000000" & result(31);
  when"10" => output <=result;
  when"11" => output <=logic_unit;
  when others =>
end case;

end process;

end behaviour;
```

Appendix 3: DO file.

```
add wave x
add wave y
add wave add_sub
add wave result
add wave logic_func
add wave logic_unit
add wave func
add wave output
add wave overflow
add wave zero
add wave overflow_check

force x "01111111111111111111111111111111"
force y "01111111111111111111111111111100"
force add_sub '0'
force logic_func "00"
force func "00"
run 2

force logic_func "01"
force func "10"
run 2

force add_sub '1'
force logic_func "10"
force func "11"
run 2

force logic_func "11"
run 2


force x "10000000010000000000000000000000"
force y "01110000000000000000000000000000"
force add_sub '0'
force logic_func "00"
force func "00"
run 2

force logic_func "01"
force func "10"
run 2

force add_sub '1'
force logic_func "10"
force func "11"
run 2

force logic_func "11"
run 2
```

```
force func "10"
run 2

force add_sub '1'
force logic_func "10"
force func "11"
run 2

force logic_func "11"
run 2

force x "10000000000000000000000000000001"
force y "10000000000000000000000000000001"
force add_sub '0'
force logic_func "00"
force func "00"
run 2

force logic_func "01"
force func "10"
run 2

force add_sub '1'
force logic_func "10"
force func "11"
run 2

force logic_func "11"
run 2

force x "00000000000011111111000000000001"
force y "10000000000000000000000000000001"
force add_sub '0'
force logic_func "00"
force func "00"
run 2

force logic_func "01"
force func "10"
run 2

force add_sub '1'
force logic_func "10"
force func "11"
run 2

force logic_func "11"
run 2
```

Appendix 4: Synthesis runme.log.

```
*** Running vivado
   with args -log alu.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source alu.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
   ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source alu.tcl -notrace
Command: synth_design -top alu -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 23544
---------------------------------------------------------------------------------
```

```
Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.574 ; gain = 85.805 ; free physical = 9740 ;
free virtual = 22006
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'alu'
[/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/sources_1/imports/CODE/alu_board.vhd:19]
INFO: [Synth 8-226] default block is never used
[/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/sources_1/imports/CODE/alu_board.vhd:38]
INFO: [Synth 8-226] default block is never used
[/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/sources_1/imports/CODE/alu_board.vhd:62]
INFO: [Synth 8-226] default block is never used
[/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/sources_1/imports/CODE/alu_board.vhd:70]
WARNING: [Synth 8-3936] Found unconnected internal register 'output_reg' and it is trimmed from '32' to '4' bits.
[/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/sources_1/imports/CODE/alu_board.vhd:31]
WARNING: [Synth 8-3936] Found unconnected internal register 'logic_unit_reg' and it is trimmed from '32' to '4' bits.
[/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/sources_1/imports/CODE/alu_board.vhd:63]
INFO: [Synth 8-256] done synthesizing module 'alu' (1#1)
[/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/sources_1/imports/CODE/alu_board.vhd:19]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1446.215 ; gain = 130.445 ; free physical = 9752 ;
free virtual = 22017
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |     0|       0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.215 ; gain = 130.445 ; free
physical = 9751 ; free virtual = 22017
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.215 ; gain = 130.445 ; free
physical = 9751 ; free virtual = 22017
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/constrs_1/new/lab1.xdc]
Finished Parsing XDC File [/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/constrs_1/new/lab1.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file
[/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/constrs_1/new/lab1.xdc]. These constraints will be ignored for
synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/alu_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/alu_propImpl.xdc] to another XDC file and exclude this new file from synthesis
with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1774.484 ; gain = 0.000 ; free physical =
9471 ; free virtual = 21743
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical =
9554 ; free virtual = 21826
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
```

```
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9554 ; free virtual = 21826
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9554 ; free virtual = 21826
---------------------------------------------------------------------------------
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/sources_1/imports/CODE/alu_board.vhd:36]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9546 ; free virtual = 21818
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
               3 Input    32 Bit      Adders := 1
+---XORs :
               2 Input     4 Bit       XORs := 1
+---Muxes :
               2 Input    32 Bit       Muxes := 1
               4 Input     4 Bit       Muxes := 2
               2 Input     1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module alu
Detailed RTL Component Info :
+---Adders :
               3 Input    32 Bit      Adders := 1
+---XORs :
               2 Input     4 Bit       XORs := 1
+---Muxes :
               2 Input    32 Bit       Muxes := 1
               4 Input     4 Bit       Muxes := 2
               2 Input     1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
```

Warning: Parallel synthesis criteria is not met

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:11 ; elapsed = 00:00:38 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9534 ; free virtual = 21808

Report RTL Partitions:
+-+-------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+-------------+-----------+----------+
+-+-------------+-----------+----------+

Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Report RTL Partitions:
+-+-------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+-------------+-----------+----------+
+-+-------------+-----------+----------+

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Report RTL Partitions:
+-+-------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+-------------+-----------+----------+
+-+-------------+-----------+----------+

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Report Check Netlist:

+------+-----------------+-------+---------+-------+-----------------+
| |Item |Errors |Warnings |Status |Description |
+------+-----------------+-------+---------+-------+-----------------+
|1 |multi_driven_nets| 0| 0|Passed |Multi driven nets|
+------+-----------------+-------+---------+-------+-----------------+

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Report RTL Partitions:

+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Start Writing Synthesis Report

Report BlackBoxes:

+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:

+------+-----+------+
| |Cell |Count |
+------+-----+------+
1	LUT4	3
2	LUT5	6
3	LUT6	7
4	IBUF	13
5	OBUF	6
+------+-----+------+

Report Instance Areas:

	Instance	Module	Cells
1	top		35

Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9414 ; free virtual = 21688

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:18 . Memory (MB): peak = 1774.484 ; gain = 130.445 ; free physical = 9467 ; free virtual = 21741
Synthesis Optimization Complete : Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1774.484 ; gain = 458.715 ; free physical = 9478 ; free virtual = 21751
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
18 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:17 ; elapsed = 00:00:50 . Memory (MB): peak = 1822.488 ; gain = 519.367 ; free physical = 9464 ; free virtual = 21738
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.runs/synth_1/alu.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file alu_utilization_synth.rpt -pb alu_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.09 . Memory (MB): peak = 1846.508 ; gain = 0.000 ; free physical = 9463 ; free virtual = 21736
INFO: [Common 17-206] Exiting Vivado at Thu Sep 28 17:55:23 2023...

Appendix 5: Implementation runme.log.

**** Running vivado*
with args -log alu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source alu.tcl -notrace

******* Vivado v2018.2 (64-bit)*
***** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018*
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018*
*** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.*

source alu.tcl -notrace
Command: link_design -top alu -part xc7a100tcsg324-1
Design is defaulting to srcset: sources_1
Design is defaulting to constrset: constrs_1
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/constrs_1/new/lab1.xdc]
Finished Parsing XDC File [/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.srcs/constrs_1/new/lab1.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
link_design completed successfully
link_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:31 . Memory (MB): peak = 1652.375 ; gain = 344.242 ; free physical = 9567 ; free virtual = 21839
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1741.402 ; gain = 89.027 ; free physical = 9557 ; free virtual = 21829

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 210631cbc

Time (s): cpu = 00:00:10 ; elapsed = 00:00:36 . Memory (MB): peak = 2166.898 ; gain = 425.496 ; free physical = 9152 ; free virtual = 21424

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 210631cbc

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 210631cbc

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: 210631cbc

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 210631cbc

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 210631cbc

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 210631cbc

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450
Ending Logic Optimization Task | Checksum: 210631cbc

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 210631cbc

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2166.902 ; gain = 0.004 ; free physical = 9178 ; free virtual = 21450

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 210631cbc

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 9178 ; free virtual = 21450
INFO: [Common 17-83] Releasing license: Implementation
23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:39 . Memory (MB): peak = 2166.902 ; gain = 514.527 ; free physical = 9178 ; free virtual = 21450
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2198.918 ; gain = 0.004 ; free physical = 9175 ; free virtual = 21447
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.runs/impl_1/alu_opt.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file alu_drc_opted.rpt -pb alu_drc_opted.pb -rpx alu_drc_opted.rpx
Command: report_drc -file alu_drc_opted.rpt -pb alu_drc_opted.pb -rpx alu_drc_opted.rpx
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.runs/impl_1/alu_drc_opted.rpt.
report_drc completed successfully
report_drc: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 2286.961 ; gain = 88.035 ; free physical = 9140 ; free virtual = 21412
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2286.961 ; gain = 0.000 ; free physical = 9136 ; free virtual = 21408
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 180b5de08

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2286.961 ; gain = 0.000 ; free physical = 9136 ; free virtual = 21408
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2286.961 ; gain = 0.000 ; free physical = 9136 ; free virtual = 21408

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 180b5de08

Time (s): cpu = 00:00:00.56 ; elapsed = 00:00:00.37 . Memory (MB): peak = 2286.961 ; gain = 0.000 ; free physical = 9127 ; free virtual = 21399

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 266cf9927

Time (s): cpu = 00:00:00.62 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2286.961 ; gain = 0.000 ; free physical = 9127 ; free virtual = 21399

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 266cf9927

Time (s): cpu = 00:00:00.62 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2286.961 ; gain = 0.000 ; free physical = 9127 ; free virtual = 21399
Phase 1 Placer Initialization | Checksum: 266cf9927

Time (s): cpu = 00:00:00.62 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2286.961 ; gain = 0.000 ; free physical = 9127 ; free virtual = 21399

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 266cf9927

Time (s): cpu = 00:00:00.65 ; elapsed = 00:00:00.40 . Memory (MB): peak = 2286.961 ; gain = 0.000 ; free physical = 9125 ; free virtual = 21397
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: 1b7f261c7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.55 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9111 ; free virtual = 21383

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 1b7f261c7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.55 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9111 ; free virtual = 21383

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 25142bb6b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9110 ; free virtual = 21382

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 25e0d0b13

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9110 ; free virtual = 21382

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 25e0d0b13

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9110 ; free virtual = 21382

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9105 ; free virtual = 21377

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9105 ; free virtual = 21377

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9105 ; free virtual = 21377

Phase 3 Detail Placement | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9105 ; free virtual = 21377

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9105 ; free virtual = 21377

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9108 ; free virtual = 21380

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9108 ; free virtual = 21380

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9108 ; free virtual = 21380
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 13ff430e0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9108 ; free virtual = 21380
Ending Placer Task | Checksum: 136ad4936

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2344.973 ; gain = 58.012 ; free physical = 9125 ; free virtual = 21397
INFO: [Common 17-83] Releasing license: Implementation
41 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2344.973 ; gain = 0.000 ; free physical = 9124 ; free virtual = 21397
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.runs/impl_1/alu_placed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_io -file alu_io_placed.rpt
report_io: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2344.973 ; gain = 0.000 ; free physical = 9116 ; free virtual = 21388
INFO: [runtcl-4] Executing : report_utilization -file alu_utilization_placed.rpt -pb alu_utilization_placed.pb
report_utilization: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2344.973 ; gain = 0.000 ; free physical = 9122 ; free virtual = 21394
INFO: [runtcl-4] Executing : report_control_sets -verbose -file alu_control_sets_placed.rpt
report_control_sets: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2344.973 ; gain = 0.000 ; free physical = 9123 ; free virtual = 21395
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: 74465693 ConstDB: 0 ShapeSum: c266f2a3 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 152ab0b86

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2392.977 ; gain = 48.004 ; free physical = 8969 ; free virtual = 21241
Post Restoration Checksum: NetGraph: ec7bd6c4 NumContArr: 662f34c2 Constraints: 0 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 152ab0b86

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2398.965 ; gain = 53.992 ; free physical = 8937 ; free virtual = 21210

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 152ab0b86

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2398.965 ; gain = 53.992 ; free physical = 8937 ; free virtual = 21210
Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: 5f5b74c4

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.230 ; gain = 61.258 ; free physical = 8934 ; free virtual = 21206

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: c0991395

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.230 ; gain = 61.258 ; free physical = 8933 ; free virtual = 21206

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
Number of Nodes with overlaps = 3
Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: 1b9384e94

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.230 ; gain = 61.258 ; free physical = 8933 ; free virtual = 21206
Phase 4 Rip-up And Reroute | Checksum: 1b9384e94

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.230 ; gain = 61.258 ; free physical = 8933 ; free virtual = 21206

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: 1b9384e94

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.230 ; gain = 61.258 ; free physical = 8933 ; free virtual = 21206

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: 1b9384e94

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.230 ; gain = 61.258 ; free physical = 8933 ; free virtual = 21206
Phase 6 Post Hold Fix | Checksum: 1b9384e94

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.230 ; gain = 61.258 ; free physical = 8933 ; free virtual = 21206

Phase 7 Route finalize

Router Utilization Summary
Global Vertical Routing Utilization = 0.0148409 %
Global Horizontal Routing Utilization = 0.0138534 %
*Routable Net Status**
**Does not include unroutable nets such as driverless and loadless.*
Run report_route_status for detailed report.
Number of Failed Nets = 0
Number of Unrouted Nets = 0
Number of Partially Routed Nets = 0
Number of Node Overlaps = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 8.10811%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 10.8108%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 4.41176%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

Reporting congestion hotspots

Direction: North

Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South

Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East

Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West

Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 1b9384e94

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.230 ; gain = 62.258 ; free physical = 8933 ; free virtual = 21206

Phase 8 Verifying routed nets

Verification completed successfully
Phase 8 Verifying routed nets | Checksum: 1b9384e94

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2410.230 ; gain = 65.258 ; free physical = 8933 ; free virtual = 21205

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 1b5b25c96

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2410.230 ; gain = 65.258 ; free physical = 8933 ; free virtual = 21205
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2410.230 ; gain = 65.258 ; free physical = 8966 ; free virtual = 21239

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
54 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:18 ; elapsed = 00:00:16 . Memory (MB): peak = 2410.234 ; gain = 65.262 ; free physical = 8966 ; free virtual = 21239
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2410.234 ; gain = 0.000 ; free physical = 8965 ; free virtual = 21238
INFO: [Common 17-1381] The checkpoint '/nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.runs/impl_1/alu_routed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file alu_drc_routed.rpt -pb alu_drc_routed.pb -rpx alu_drc_routed.rpx
Command: report_drc -file alu_drc_routed.rpt -pb alu_drc_routed.pb -rpx alu_drc_routed.rpx
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.runs/impl_1/alu_drc_routed.rpt.

report_drc completed successfully
INFO: [runtcl-4] Executing : report_methodology -file alu_methodology_drc_routed.rpt -pb alu_methodology_drc_routed.pb -rpx alu_methodology_drc_routed.rpx
Command: report_methodology -file alu_methodology_drc_routed.rpt -pb alu_methodology_drc_routed.pb -rpx alu_methodology_drc_routed.rpx
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [DRC 23-133] Running Methodology with 8 threads
INFO: [Coretcl 2-1520] The results of Report Methodology are in file /nfs/home/k/k_jask/COEN316/LAB1/lab1_coen316/lab1_coen316.runs/impl_1/alu_methodology_drc_routed.rpt.
report_methodology completed successfully
INFO: [runtcl-4] Executing : report_power -file alu_power_routed.rpt -pb alu_power_summary_routed.pb -rpx alu_power_routed.rpx
Command: report_power -file alu_power_routed.rpt -pb alu_power_summary_routed.pb -rpx alu_power_routed.rpx
WARNING: [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate
INFO: [Timing 38-35] Done setting XDC timing constraints.
Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation
66 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
report_power completed successfully
INFO: [runtcl-4] Executing : report_route_status -file alu_route_status.rpt -pb alu_route_status.pb
INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file alu_timing_summary_routed.rpt -pb alu_timing_summary_routed.pb -rpx alu_timing_summary_routed.rpx -warn_on_violation
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
INFO: [runtcl-4] Executing : report_incremental_reuse -file alu_incremental_reuse_routed.rpt
INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
INFO: [runtcl-4] Executing : report_clock_utilization -file alu_clock_utilization_routed.rpt
INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file alu_bus_skew_routed.rpt -pb alu_bus_skew_routed.pb -rpx alu_bus_skew_routed.rpx
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
INFO: [Common 17-206] Exiting Vivado at Thu Sep 28 17:57:25 2023...

**** Running vivado*
with args -log alu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source alu.tcl -notrace

******* Vivado v2018.2 (64-bit)*
***** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018*
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018*
*** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.*

source alu.tcl -notrace
Command: open_checkpoint alu_routed.dcp

Starting open_checkpoint Task

Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1277.113 ; gain = 0.000 ; free physical = 9889 ; free virtual = 22161
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Timing 38-478] Restoring timing data from binary archive.
INFO: [Timing 38-479] Binary timing data restore complete.
INFO: [Project 1-856] Restoring constraints from binary archive.
INFO: [Project 1-853] Binary constraint restore complete.
Reading XDEF placement.
Reading placer database...
Reading XDEF routing.
Read XDEF File: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2079.062 ; gain = 0.004 ; free physical = 9163 ; free virtual = 21436

Restored from archive | CPU: 0.210000 secs | Memory: 0.963921 MB |
Finished XDEF File Restore: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2079.062 ; gain = 0.004 ; free physical = 9163 ; free virtual = 21436
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
open_checkpoint: Time (s): cpu = 00:00:17 ; elapsed = 00:01:09 . Memory (MB): peak = 2079.062 ; gain = 801.953 ; free physical = 9164 ; free virtual = 21437
Command: write_bitstream -force alu.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set_property CFGBVS value1 [current_design]
#where value1 is either VCCO or GND

set_property CONFIG_VOLTAGE value2 [current_design]
#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./alu.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
21 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:12 . Memory (MB): peak = 2550.902 ; gain = 471.840 ; free physical = 9092 ; free virtual = 21372
INFO: [Common 17-206] Exiting Vivado at Thu Sep 28 17:59:05 2023...