



**Queen Mary**  
University of London

Science and Engineering

School of Electronic Engineering and Computer Science  
QMUL-BUPT Joint Programme

# **EBU6475 Microprocessor System Design**

## **EBU5476 Microprocessors for Embedded Computing**

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The ARM Cortex-M4 Processor Architecture

**arm**

Last updated: 5 March, 2022

University Program Education Kits

# Outline

- ARM Architectures and Processors
  - What is ARM Architecture
  - ARM Processor Families
  - ARM Cortex-M Series
  - Cortex-M4 Processor
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- ARM Cortex-M4 Processor
  - Cortex-M4 Processor Overview
  - Cortex-M4 Block Diagram
  - Cortex-M4 Registers

# ARM Architectures and Processors

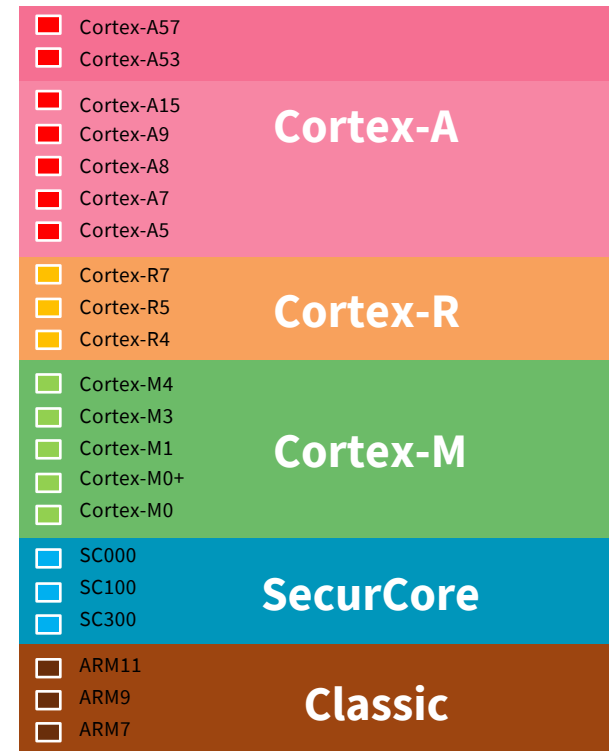
# What is ARM Architecture?

- ARM architecture is a family of RISC-based processor architectures
  - Advanced RISC Machine    **Reduced Instruction Set Computer (RISC)**
  - Well-known for its power efficiency;
  - Hence widely used in mobile devices, such as smartphones and tablets
  - Designed and licensed to a wide eco-system by ARM
- ARM Holdings
  - The company designs ARM-based processors;
  - Does not manufacture, but licenses designs to semiconductor partners who add their own Intellectual Property (IP) on top of ARM's IP, fabricate and sell to customers;
  - Also offer other IP apart from processors, such as physical IPs, interconnect IPs, graphics cores, and development tools.



# ARM Processor Families

- Cortex-A series (Application)
  - High performance processors capable of full Operating System (OS) support;
  - Applications include smartphones, digital TV, smart books, home gateways etc.
- Cortex-R series (Real-time)
  - High performance for real-time applications;
  - High reliability
  - Applications include automotive braking system, powertrains etc.
- Cortex-M series (Microcontroller)
  - Cost-sensitive solutions for deterministic microcontroller applications;
  - Applications include microcontrollers, mixed signal devices, smart sensors, automotive body electronics and airbags;
- SecurCore series
  - High security applications.
- Previous classic processors
  - Include ARM7, ARM9, ARM11 families

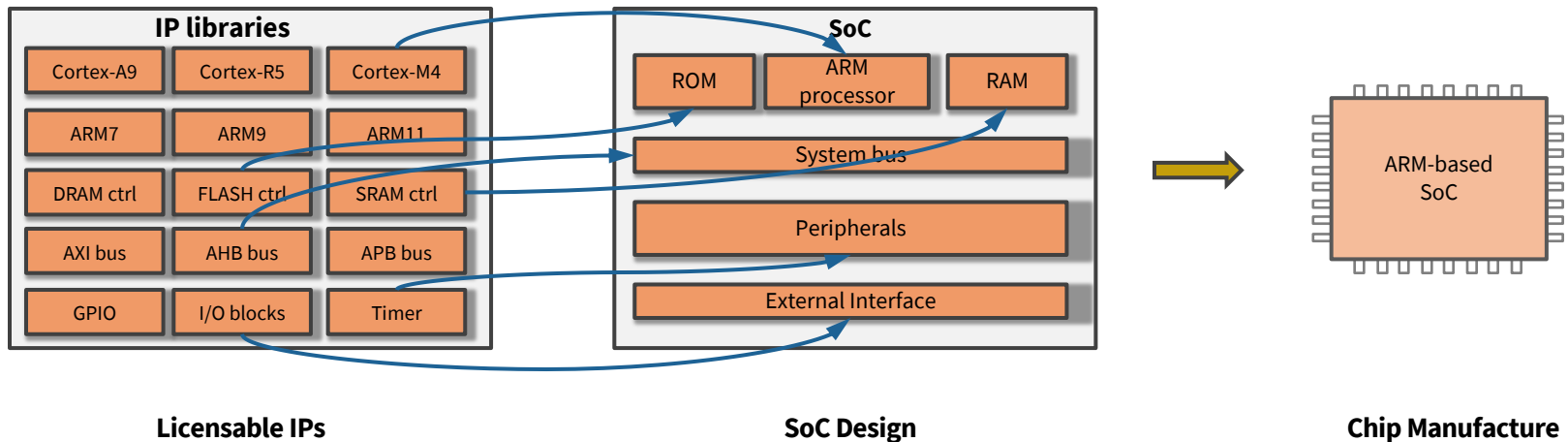


**Cortex**  
Low-Power Leadership from ARM

As of Dec 2013

# Design an ARM-based SoC (system on chip)

- Select a set of IP cores from ARM and/or other third-party IP vendors
- Integrate IP cores into a single chip design
- Give design to semiconductor foundries for chip fabrication



# ARM Cortex-M Series

Microcontroller

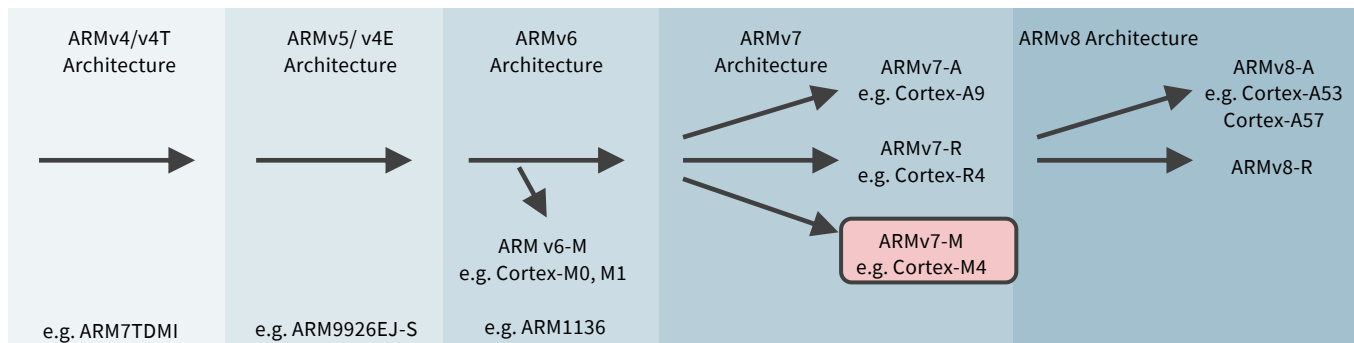
- Cortex-M series: Cortex-M0, M0+, M1, M3, M4.
- Energy-efficiency
  - Lower energy cost, longer battery life
- Smaller code
  - Lower silicon costs
- Ease of use
  - Faster software development and reuse
- Embedded applications
  - Smart metering, human interface devices, automotive and industrial control systems, white goods, consumer products and medical instrumentation



As of Dec 2013

# ARM Processors vs. ARM Architectures

- ARM architecture "design"
  - Describes the details of instruction set, programmer's model, exception model, and memory map
  - Documented in the Architecture Reference Manual
- ARM processor actual "chip" 不同processor可能用同一个architecture
  - Developed using one of the ARM architectures
  - More implementation details, such as timing information
  - Documented in processor's Technical Reference Manual

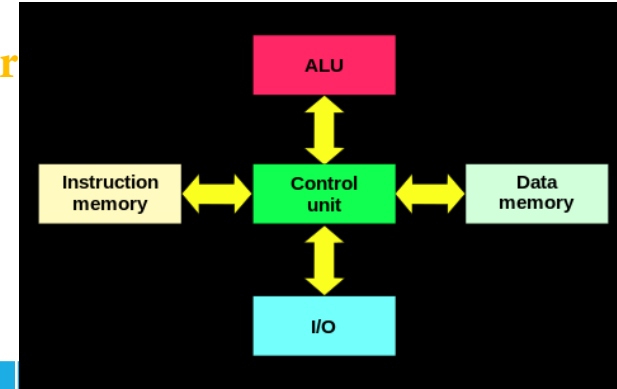


As of Dec 2013



# ARM Cortex-M Series Family

Harvard architecture



Processor	ARM Architecture	Core Architecture	Thumb®	Thumb®-2	Hardware Multiply	Hardware Divide	Saturated Math	DSP Extensions	Floating Point
Cortex-M0	ARMv6-M	Von Neumann	Most	Subset	1 or 32 cycle	No	No	Software	No
Cortex-M0+	ARMv6-M	Von Neumann	Most	Subset	1 or 32 cycle	No	No	Software	No
Cortex-M1	ARMv6-M	Von Neumann	Most	Subset	3 or 33 cycle	No	No	Software	No
Cortex-M3	ARMv7-M	Harvard	Entire	Entire	1 cycle	Yes	Yes	Software	No
Cortex-M4	ARMv7E-M	Harvard	Entire	Entire	1 cycle	Yes	Yes	Hardware	Optional

# ARM Cortex-M4 Processor Overview

# Cortex-M4 Processor Overview

- Cortex-M4 Processor
  - Introduced in 2010
  - Designed with a large variety of highly efficient signal processing features
  - Features extended single-cycle multiply accumulate instructions, optimized SIMD arithmetic, saturating arithmetic and an optional Floating Point Unit.
- High Performance Efficiency
  - 1.25 DMIPS/MHz (Dhrystone Million Instructions Per Second / MHz) at the order of  $\mu$ Watts / MHz
- Low Power Consumption
  - Longer battery life – especially critical in mobile products
- Enhanced Determinism
  - The critical tasks and interrupt routines can be served quickly in a known number of cycles

# Cortex-M4 Processor Features

word size

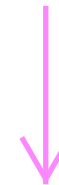
- 32-bit Reduced Instruction Set Computing (RISC) processor
- Harvard architecture
  - Separated data bus and instruction bus
- Instruction set
  - Include the entire Thumb<sup>®</sup>-1 (16-bit) and Thumb<sup>®</sup>-2 (16/ 32-bit) instruction sets
- 3-stage + branch speculation pipeline guess and save time
- Performance efficiency
  - 1.25 – 1.95 DMIPS/MHz (Dhrystone Million Instructions Per Second / MHz)
- Supported Interrupts
  - Non-maskable Interrupt (NMI) + 1 to 240 physical interrupts
  - 8 to 256 interrupt priority levels

# Cortex-M4 Processor Features

- Supports Sleep Modes
  - Up to 240 Wake-up Interrupts **to save power**
  - Integrated WFI (Wait For Interrupt) and WFE (Wait For Event) Instructions and Sleep On Exit capability (to be covered in more detail later)
  - Sleep & Deep Sleep Signals
- Enhanced Instructions
  - Hardware Divide (2-12 Cycles)
  - Single-Cycle 16/32-bit MAC, Single-cycle dual 16-bit MAC
  - 8/16-bit SIMD arithmetic
- Debug
  - Optional JTAG & Serial-Wire Debug (SWD) Ports
  - Up to 8 Breakpoints and 4 Watchpoints
- Memory Protection Unit (MPU)
  - Optional 8 region MPU with sub regions and background region

# Cortex-M4 Processor Features

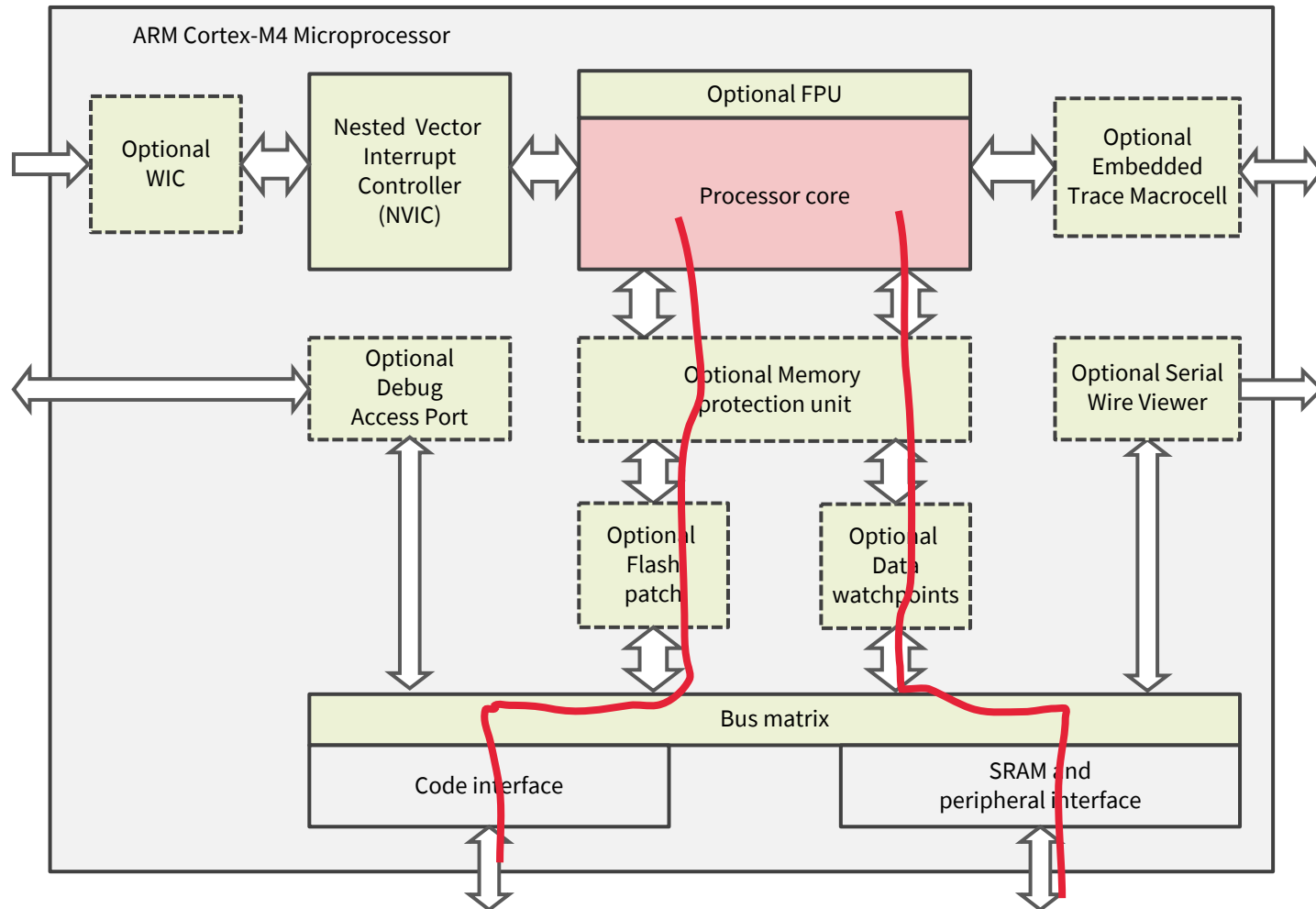
- Cortex-M4 processor is designed to meet the challenges of low dynamic power constraints while retaining light footprints
  - 180 nm ultra low power process: 151  $\mu\text{W}/\text{MHz}$
  - 90 nm low power process: 32.82  $\mu\text{W}/\text{MHz}$
  - 40 nm low power process: 12.26  $\mu\text{W}/\text{MHz}$



smaller the number is, the smaller the feature, smaller the technology, lower power.

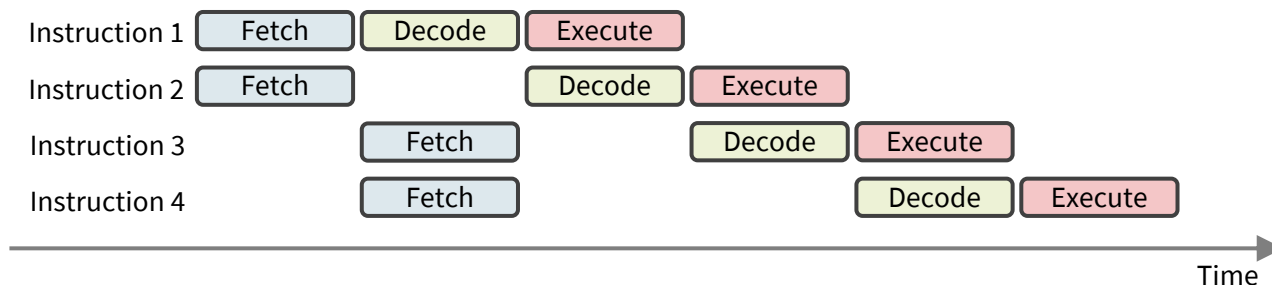
ARM Cortex-M4 Implementation Data			
Process	180ULL (7-track, typical 1.8v, 25 <sup>0</sup> C)	90LP (7-track, typical 1.2v, 25 <sup>0</sup> C)	40LP 9-track, typical 1.1v, 85 <sup>0</sup> C)
Dynamic Power	151 $\mu\text{W}/\text{MHz}$	32.82 $\mu\text{W}/\text{MHz}$	12.26 $\mu\text{W}/\text{MHz}$
Floorplanned Area	0.44 mm <sup>2</sup>	0.119 mm <sup>2</sup>	0.028 mm <sup>2</sup>

# Cortex-M4 Block Diagram



# Cortex-M4 Block Diagram

- Processor core
  - Contains internal registers, the ALU, data path, and some control logic
  - Registers include sixteen 32-bit registers for both general and special usage
- Processor pipeline stages
  - Three-stage pipeline: **fetch**, **decode**, and **execute**
  - Some instructions may take multiple cycles to execute, in which case the pipeline will be stalled
  - The pipeline will be flushed if a branch instruction is executed
  - Up to two instructions can be fetched in one transfer (16-bit instructions)





# Cortex-M4 Block Diagram

- Nested Vectored Interrupt Controller (NVIC)
  - Up to 240 interrupt request signals and a non-maskable interrupt (NMI)
  - Automatically handles nested interrupts, such as comparing priorities between interrupt requests and the current priority level
- Wakeup Interrupt Controller (WIC)
  - For low-power applications, the microcontroller can enter sleep mode by shutting down most of the components.
  - When an interrupt request is detected, the WIC can inform the power management unit to power up the system.
- Memory Protection Unit (optional)
  - Used to protect memory content, e.g. make some memory regions read-only or preventing user applications from accessing privileged application data

# Cortex-M4 Block Diagram

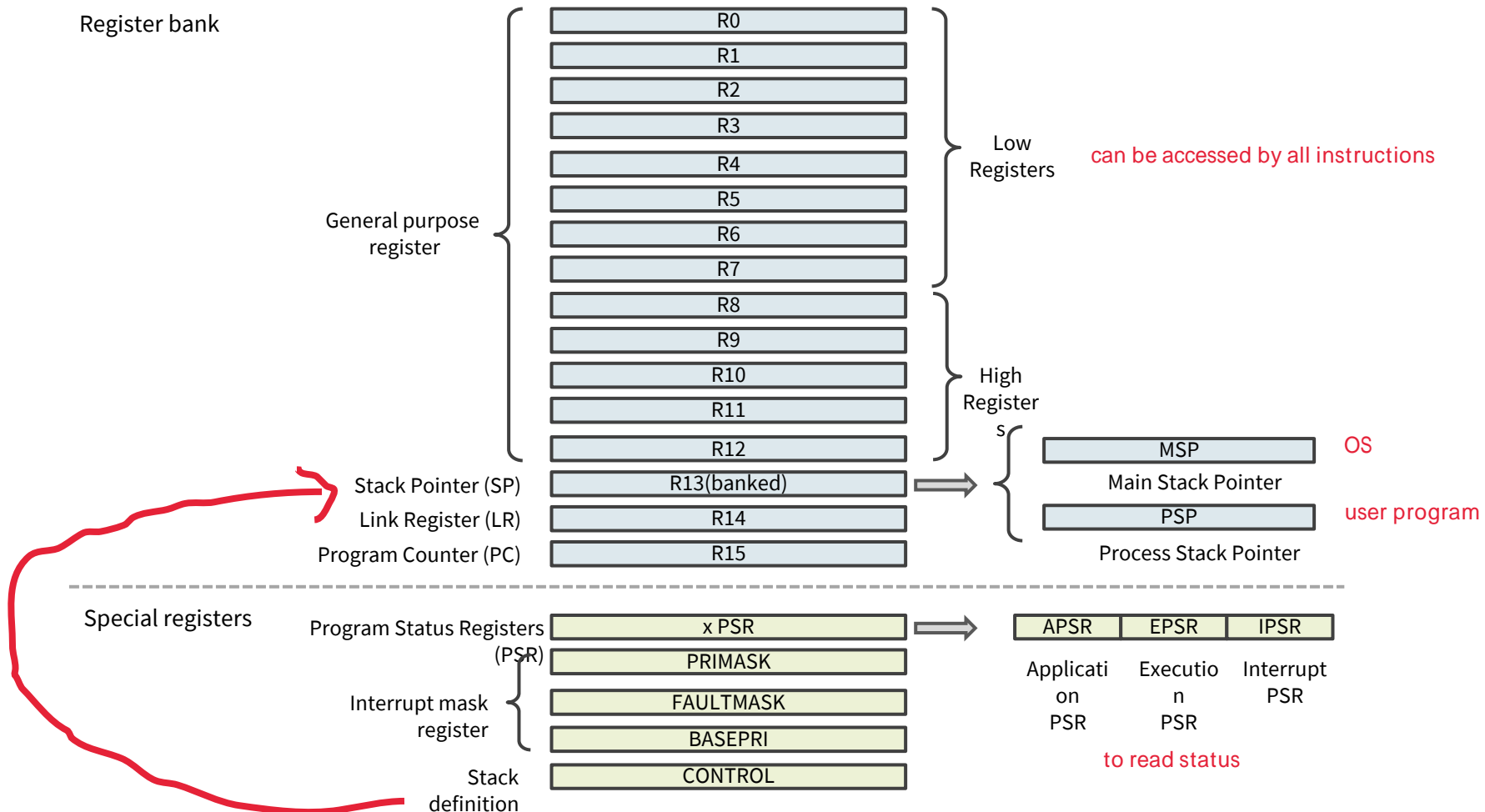
- Bus interconnect
  - Allows data transfer to take place on different buses simultaneously
  - Provides data transfer management, e.g. a write buffer, bit-oriented operations (bit-band)
  - Includes the internal bus system, the data path in the processor core, and the AHB LITE protocol unit including ICode, Dcode and System interfaces
  - May include bus bridges (e.g. AHB-to-APB bus bridge) to connect different buses into a network using a single global memory space
- Debug subsystem
  - Handles debug control, program breakpoints, and data watchpoints
  - When a debug event occurs, it can put the processor core in a halted state, where developers can analyse the status of the processor at that point, such as register values and flags

# ARM Cortex-M4 Processor Registers

# Cortex-M4 Registers

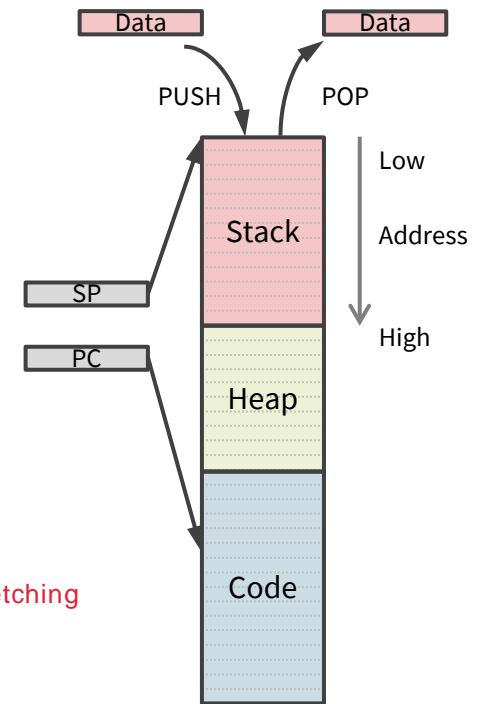
- Processor registers
  - The internal registers are used to store and process temporary data within the processor core
  - All registers are inside the processor core, hence they can be accessed quickly
  - Load-store architecture
    - load: MEM->REG
    - store: REG->MEM
    - To process memory data, they have to be first loaded from memory to registers, processed inside the processor core using register data only, and then written back to memory if needed
- Cortex-M4 registers
  - Register bank
    - Sixteen 32-bit registers (thirteen are used for general-purpose);
  - Special registers

# Cortex-M4 Registers



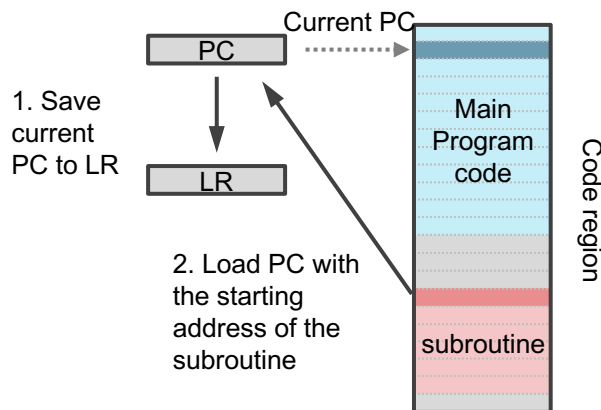
# Cortex-M4 Registers

- R0 – R12: general purpose registers
  - Low registers (R0 – R7) can be accessed by any instruction
  - High registers (R8 – R12) sometimes cannot be accessed e.g. by some Thumb (16-bit) instructions
- R13: Stack Pointer (SP)
  - Records the current address of the stack
  - Used for saving the context of a program while switching between tasks
  - Cortex-M4 has two SPs: Main SP, used in applications that require privileged access e.g. OS kernel, and exception handlers, and Process SP, used in base-level application code (when not running an exception handler)
- R15: Program Counter (PC)
  - Records the address of the next instruction for execution *after fetching*
  - Automatically incremented by 4 at each operation (for 32-bit instruction code), except branching operations
  - A branching operation, such as function calls, will change the PC to a specific address, meanwhile it saves the current PC to the Link Register (LR)

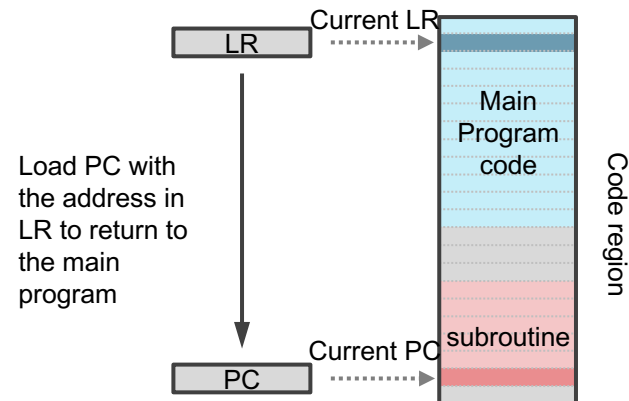


# Cortex-M4 Registers

- R14: Link Register (LR)
  - The LR is used to store the return address of a subroutine or a function call
  - The program counter (PC) will load the value from LR after a function is finished



**Call a subroutine**

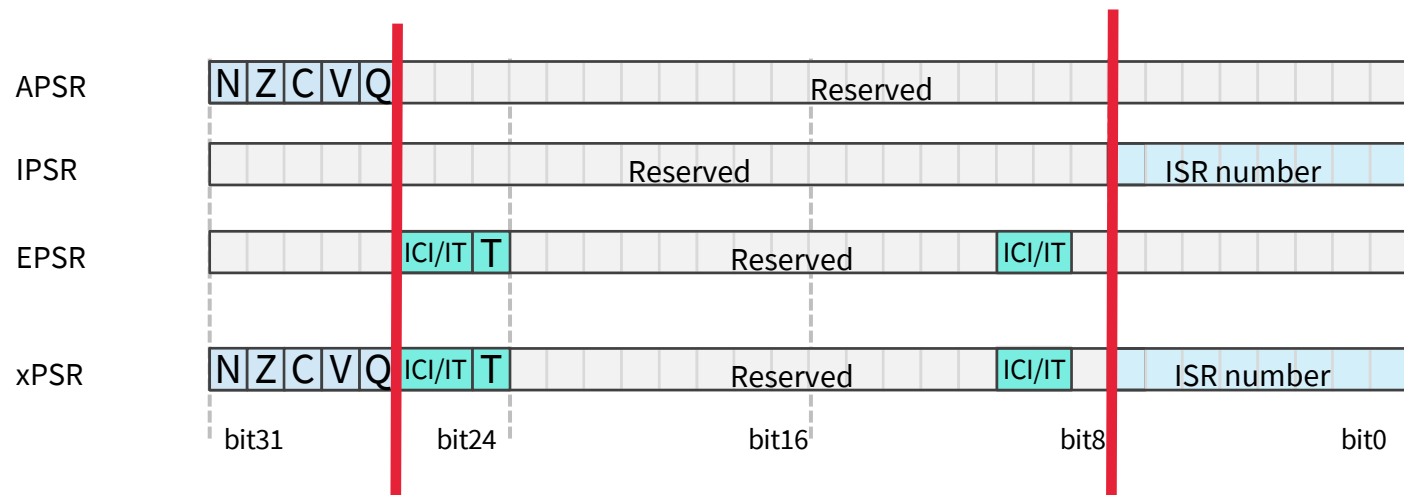


**Return from a subroutine to the main program**

# Cortex-M4 Registers

- xPSR, combined Program Status Register
  - Provides information about program execution and ALU flags
    - Application PSR (APSR)
    - Interrupt PSR (IPSR)
    - Execution PSR (EPSR)

PSR只有一个，但32bits，分为三个部分，实现APSR, IPSR, EPSR



interrupt service routine (ISR)



# Cortex-M4 Registers

- APSR

5-7 = -2 N = 1 Z = 0

- N: negative flag – set to one if the result from ALU is negative
- Z: zero flag – set to one if the result from ALU is zero
- C: carry flag – set to one if an unsigned overflow occurs
- V: overflow flag – set to one if a signed overflow occurs
- Q: DSP overflow and saturation flag – set to one if saturation has occurred in saturating arithmetic instructions, or overflow has occurred in certain multiply instructions

- IPSR

- ISR number – current executing interrupt service routine number

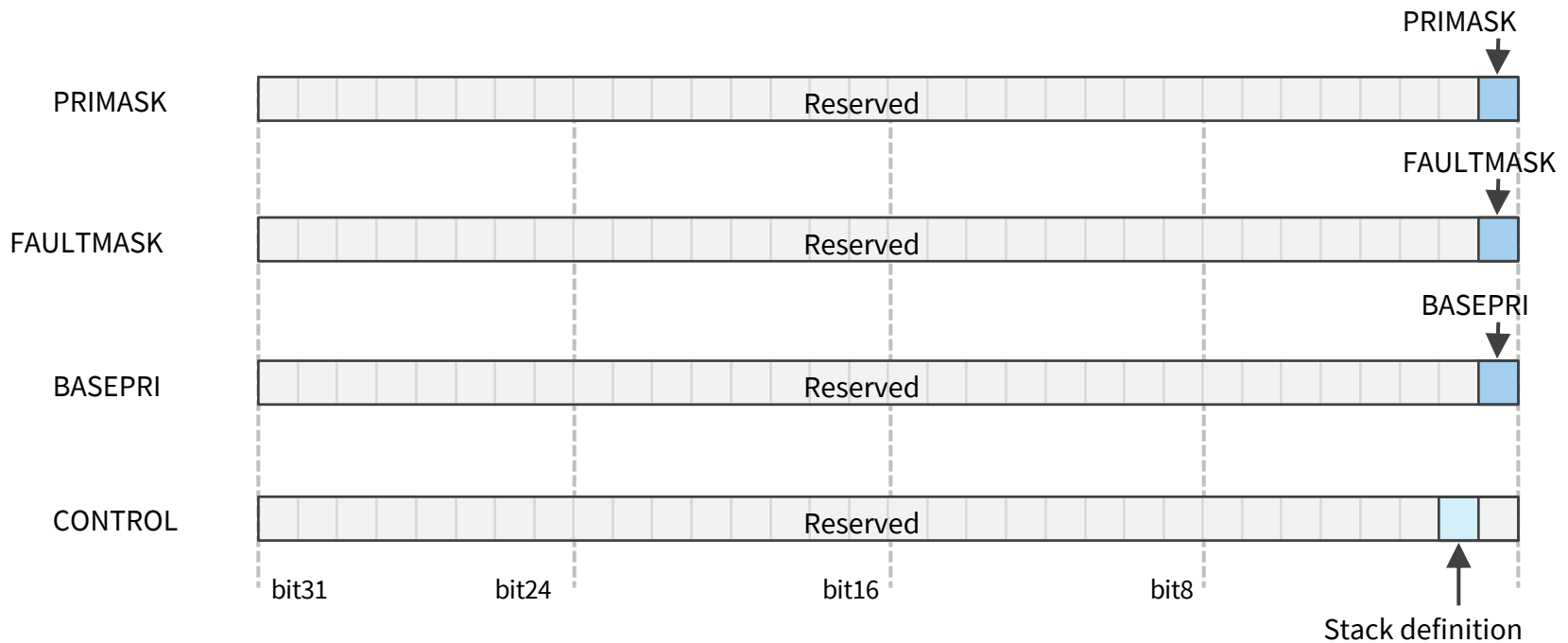
- EPSR

- T: Thumb state – always one since Cortex-M4 only supports the Thumb state (more on processor states in the next module)
- IC/IT: Interrupt-Continuable Instruction (ICI) bit, IF-THEN instruction status bit

# Cortex-M4 Registers

- Interrupt mask registers
  - 1-bit PRIMASK  
Set to one will block all the interrupts apart from non-maskable interrupt (NMI) and the hard fault exception
  - 1-bit FAULTMASK  
Set to one will block all the interrupts apart from NMI
  - 1-bit BASEPRI  
Set to a non zero value will block all interrupts of the same or lower level (only allow for interrupts with higher priorities)
- CONTROL: special register
  - 1-bit stack definition  
Set to one: use the process stack pointer (PSP)  
Clear to zero: use the main stack pointer (MSP)

# Cortex-M4 Registers



# Useful Resources

- Architecture Reference Manual:

<http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0403c/index.html>

- Cortex-M4 Technical Reference Manual:

[http://infocenter.arm.com/help/topic/com.arm.doc.ddi0439d/DDI0439D\\_cortex\\_m4\\_processor\\_r0p1\\_trm.pdf](http://infocenter.arm.com/help/topic/com.arm.doc.ddi0439d/DDI0439D_cortex_m4_processor_r0p1_trm.pdf)

- Cortex-M4 Devices Generic User Guide:

[http://infocenter.arm.com/help/topic/com.arm.doc.dui0553a/DUI0553A\\_cortex\\_m4\\_dgug.pdf](http://infocenter.arm.com/help/topic/com.arm.doc.dui0553a/DUI0553A_cortex_m4_dgug.pdf)