Homework 10 - Datapath and Control

Course: CO20-320241

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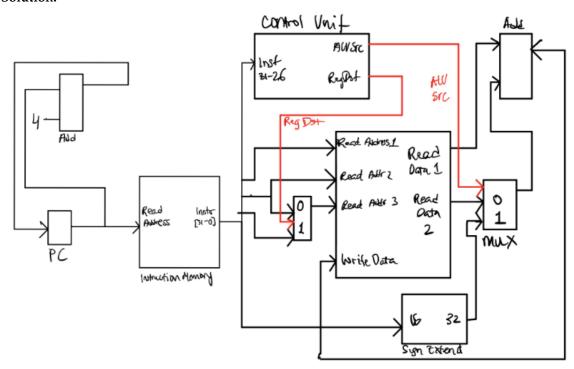
Problem 10.1

Solution:

Control lines are necessary because together with the multiplexors, it does the selection for the single cycle datapath. Control lines are determined by the opcode fields of the instruction and those instructions are being passed through the multiplexer in order to output the multiple single line inputs to one single output.

Problem 10.2

Solution:



Problem 10.3 Solution:

a) We must pick the longest path to determine the clock cycle time, therefore, all we need to do is compare the latencies between the four possible paths for the ALU instructions

```
1. I-mem \rightarrow RegF \rightarrow ALU \rightarrow Mux3 \rightarrow WBacktoRegF

2. 450 ps 250 ps 120ps 30ps - = 850 ps

2. I-mem \rightarrow RegF \rightarrow Mux2 \rightarrow ALU \rightarrow Mux3 \rightarrow WBacktoRegF

3. 450 ps 250 ps 30ps 120ps 30ps - = 880 ps

3. I-mem \rightarrow Mux1 \rightarrow RegF (Write address)

450 ps 30 ps 250ps = 730 ps

4. Add \rightarrow Mux4 \rightarrow PCWrite

110 ps 30 ps - = 140 ps
```

The clock cycle time is 880ps from the second path.

```
b) 1. I-mem \rightarrow RegF \rightarrow ALU \rightarrow D-mem

. 450 ps 250 ps 120ps 350ps = 1170 ps

2. I-mem \rightarrow RegF \rightarrow D-mem

. 450 ps 250 ps 350ps = 1050 ps

3. I-mem \rightarrow Sign Extend \rightarrow Mux2 \rightarrow ALU \rightarrow D-Mem

. 450 ps 20 ps 30ps 120ps 350ps = 970 ps

4. Add \rightarrow Mux4 \rightarrow PCWrite (update PC)

. 110 ps 30 ps - = 140 ps
```

The clock cycle time is 1170 ps from the first path.

c) Now, we must compare part a and b with the paths for beq and lw. For lw:

```
1. I-mem \rightarrow RegF \rightarrow ALU \rightarrow D-mem \rightarrow Mux3 \rightarrow WBack to RegF
. 450 ps 250 ps 120ps 350ps
                                                  30ps
                                                                                          = 1200 \text{ ps}
2. I-mem \rightarrow Mux1 \rightarrow RegF(Write Address)
. 450 ps 30 ps 250ps
                                                                                           = 730 \text{ ps}
3. I-mem \rightarrow Sign Extend \rightarrow Mux2 \rightarrow ALU \rightarrow D-Mem \rightarrow Mux3 \rightarrow WBack to RegF
                   20 ps
                                    30ps
                                             120ps 350ps 30ps
                                                                                           = 1000 \text{ ps}
4. Add \rightarrow Mux4 \rightarrow PCWrite (update PC)
                                                                                             = 140 \text{ ps}
. 110 ps 30 ps
For beq:
1. I-mem \rightarrow RegF \rightarrow ALU \rightarrow Mux4 \rightarrow PCWrite (update PC)
. 450 ps 250 ps 120ps 30ps
                                                                                            = 850 \text{ ps}
2. I-mem \rightarrow RegF \rightarrow Mux2 \rightarrow ALU \rightarrow Mux4 \rightarrow PCWrite (Update PC)
                                                                                                = 880 \text{ ps}
. 450 ps 250 ps 30ps 120ps 30ps
3. I-mem \rightarrow Sign Extend \rightarrow Shift-left-2 \rightarrow Add \rightarrow Mux4 \rightarrow PCWrite (update PC)
. 450 ps
                     20 ps
                                    30ps
                                               120ps
                                                           30ps
                                                                                           = 650 \text{ ps}
4. Add \rightarrow Mux4 \rightarrow PCWrite (update PC)
. 110 ps 30 ps
                                                                                             = 140 \text{ ps}
```

The clock cycle time is 1200ps from the first path of lw.