Computer Architecture and Programming Languages
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Homework 9 - Datapath and Control

Problem 9.1

Solution:

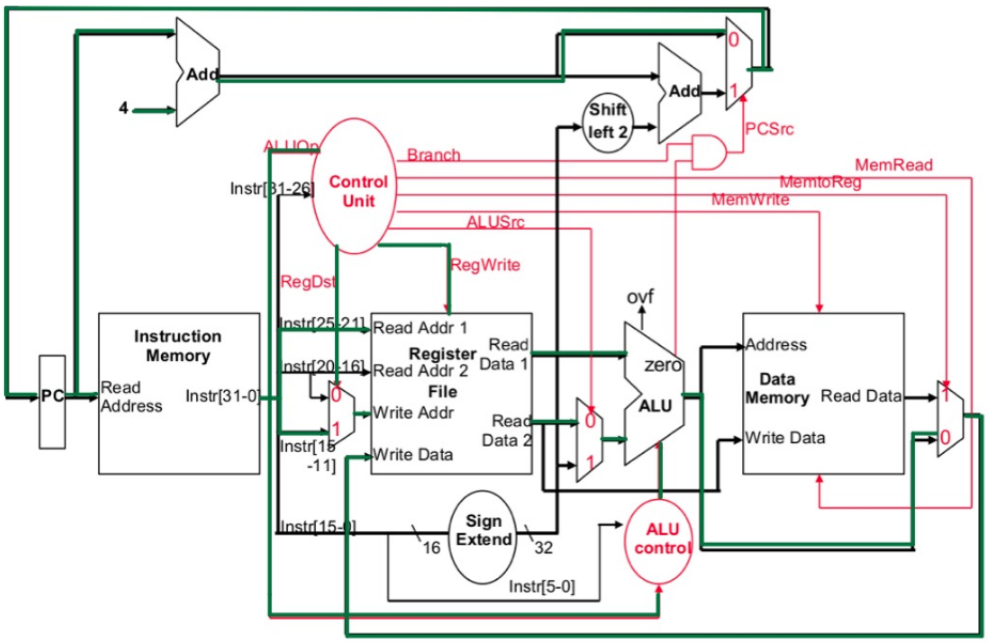
(a) The PC does not need an explicit write signal in a single-cycle datapath because the PC is updated every cycle. The instruction memory reads the PC and then it incrememnts by 4 bytes, which is 1 word.

(b) An explicit write control signal is needed in a multicycle datapath because it doesn't have an ALU to increment. In order to do so, it needs to be explicitly written by the control signal.

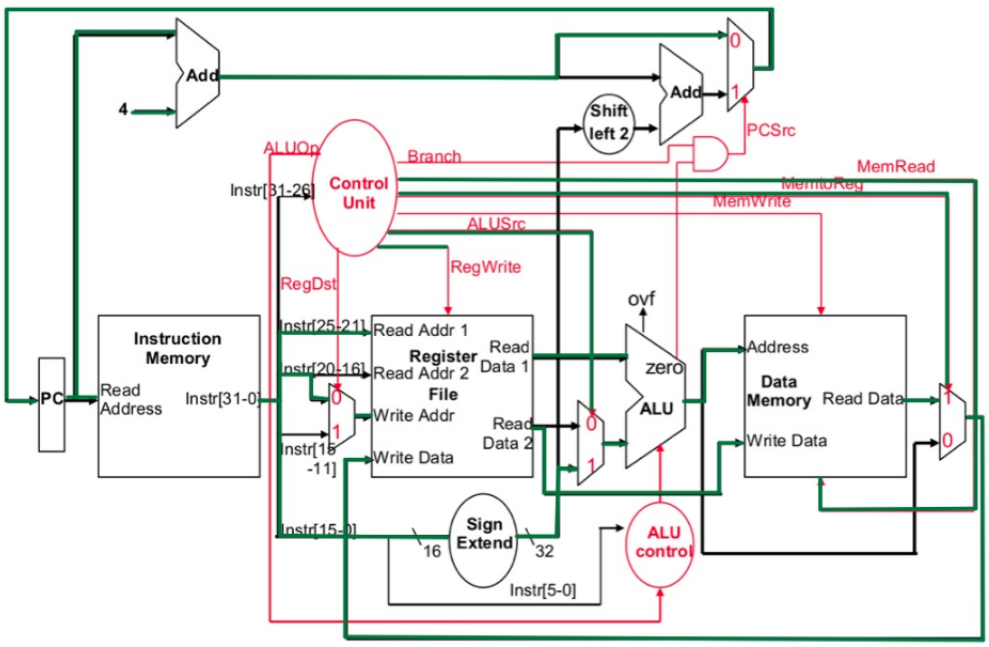
Problem 9.2

Solution:

(a) For the addition $s0 $s1 $2



For the load word lw $s3 16($s2)



Instruction	RegDst	ALUSrc	MemtoReg	RegWrite	MemRead	MemWrite	Branch	ALUOp
add	1	0	0	1	0	0	0	1
lw	0	1	1	1	1	0	0	0

(b) The ALU needs to add its inputs when it is equal to 0010. Two examples include in the case of lw or sw, which are I-type, that has a base address of a register and then the offset is added; and another example is the add, which is a R-type, that adds two values together.