BÁO CÁO LAB 3A

Lớp L04 - nhóm 7

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Step 1: Prepare your RTL and put to below path ./Genus_BoundFlasher/RTL/

Step 2: Prepare constraints as below at

```
[l04group7@ktmt ~]$ cd vlsi/2013053/work/synthesis_env
[l04group7@ktmt synthesis_env]$ vi ./Genus_BoundFlasher/constraints/bound_flashe
r_gate.sdc
```

File bound_flasher_gate.sdc

```
# Set the current design
current_design bound_flasher

create_clock -name "clk" -add -period 1.5 -waveform {0.0 0.75} [get_ports clk]

set_input_delay -clock [get_clocks clk] -add_delay 0.75 [get_ports flick]
set_input_delay -clock [get_clocks clk] -add_delay 0.75 [get_ports rst_n]
set_output_delay -clock [get_clocks clk] -add_delay 0.75 [get_ports LED ]

set_max_fanout 15.000 [current_design]
set_max_transition 1.2 [current_design]
~
```

Step 3: Modify environment a bit to map current design

```
[l04group7@ktmt synthesis_env]$ vi ./Genus_BoundFlasher/LAB1/run.tcl
```

File run.tcl:

```
################################################################################
## Preset global variables and attributes
################################################################################


set DESIGN bound_flasher
```

```
################################################################
## Load Design
################################################################

read_hdl "bound_flasher.v"
#read_hdl " pllclk.v accum_stat.v alu_32.v arb.v data_bus_mach.v data_sample_mux
.v decode_i.v decoder.v \
        digit_reg.v conv_subreg.v dma.v dtmf_recvr_core.v execute_i.v m16x16.v m
ult_32_dp.v \
        port_bus_mach.v prog_bus_mach.v ram_128x16_test.v ram_256x16_test.v resu
lts_conv.v spi.v \
        tdsp_core_glue.v tdsp_core_mach.v tdsp_core.v tdsp_data_mux.v tdsp_ds_cs
.v test_control.v \
        ulaw_lin_conv.v power_manager.v bound_flasher.v "
elaborate $DESIGN
```

```
################################################################
## Constraints Setup
################################################################

read_sdc ../constraints/bound_flasher_gate.sdc
```

```
## Optimize Netlist
################################################################################
########################

## Uncomment to remove assigns & insert tiehilo cells during Incremental synthes
is
##set_db / .remove_assigns true
##set_remove_assign_options -buffer_or_inverter <libcell> -design <design|subdes
ign>
##set_db / .use_tiehilo_for_const <none|duplicate|unique>
set_db / .syn_opt_effort $MAP_OPT_EFF
syn_opt
write_snapshot -outdir $_REPORTS_PATH -tag syn_opt
report_summary -directory $_REPORTS_PATH

puts "Runtime & Memory after 'syn_opt'"
time_info OPT



write_snapshot -outdir $_REPORTS_PATH -tag final
report_summary -directory $_REPORTS_PATH
write_hdl  > ${_OUTPUTS_PATH}/${DESIGN}_m.v
```

```
################################
### write_do_lec
################################


write_do_lec -golden_design fv_map -revised_design ${_OUTPUTS_PATH}/${DESIGN}_m.
v -logfile  ${_LOG_PATH}/intermediate2final.lec.log > ${_OUTPUTS_PATH}/intermedi
ate2final.lec.do
##Uncomment if the RTL is to be compared with the final netlist..
##write_do_lec -revised_design ${_OUTPUTS_PATH}/${DESIGN}_m.v -logfile ${_LOG_PA
TH}/rtl2final.lec.log > ${_OUTPUTS_PATH}/rtl2final.lec.do

puts "Final Runtime & Memory."
time_info FINAL
puts "============================"
puts "Synthesis Finished ........."
puts "============================"

file copy [get_db / .stdout_log] ${_LOG_PATH}/.

quit
```

Step 4: Source Genus & license files. Then, execute Synthesis

```
[l04group7@ktmt ~]$ cd /home/share_file/cadence
[l04group7@ktmt cadence]$ source add_path
[l04group7@ktmt cadence]$ source add_license
[l04group7@ktmt cadence]$ cd -
/home/l04group7
[l04group7@ktmt ~]$ cd vlsi/2013053/work/synthesis_env
[l04group7@ktmt synthesis_env]$ cd Genus_BoundFlasher/LAB1
[l04group7@ktmt LAB1]$ genus -f run.tcl | tee -i sync.log
```

Step 5: Check synthesis Log file to confirm no "Error" occur

```
[l04group7@ktmt LAB1]$ vi sync.log
```

File sync.log

```
Info    : An output library pin lacks a function attribute. [LBR-41]
        : Output pin 'CDK_R512x16/ROM_OUT[15]' has no function.
Warning : Libcell has no area attribute.  Defaulting to 0 area. [LBR-43]
        : Assigning 0 area to library cell 'CDK_S128x16/CDK_S128x16'.
Info    : An output library pin lacks a function attribute. [LBR-41]
        : Output pin 'CDK_S128x16/DATA_OUT[0]' has no function.
Info    : An output library pin lacks a function attribute. [LBR-41]
        : Output pin 'CDK_S128x16/DATA_OUT[1]' has no function.
Info    : An output library pin lacks a function attribute. [LBR-41]
        : Output pin 'CDK_S128x16/DATA_OUT[2]' has no function.
Info    : An output library pin lacks a function attribute. [LBR-41]
        : Output pin 'CDK_S128x16/DATA_OUT[3]' has no function.
Warning : Libcell has no area attribute.  Defaulting to 0 area. [LBR-43]
        : Assigning 0 area to library cell 'CDK_S256x16/CDK_S256x16'.
Warning : Libcell has no area attribute.  Defaulting to 0 area. [LBR-43]
        : Assigning 0 area to library cell 'pll/pll'.
Warning : Found libraries with and without pg_pin construct. [LBR-12]
        : Libraries with and without pg_pin construct have been loaded.
        : This can lead to issues later in the flow.
Info    : Ignoring specified timing sense. [LBR-170]
        : The 'timing_sense' definition 'positive_unate' for library pin 'TLATNS
RX4/Q' is ignored.
        : Timing sense should never be set with 'rising_edge' or 'falling_edge'
timing type.
                                                              202,1         5%
```

Step 6: Check Synthesis Report

```
[l04group7@ktmt LAB1]$ vi reports_Apr13-17:17:42/final_area.rpt
[l04group7@ktmt LAB1]$ vi reports_Apr13-17:17:42/final_qor.rpt
[l04group7@ktmt LAB1]$ vi reports_Apr13-17:17:42/final_time.rpt
```

File final_area.rpt

```
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 13 2024  05:17:56 pm
  Module:                 bound_flasher
  Technology libraries:   slow_1v0
                          pll 0.0
                          CDK_S128x16 0.0
                          CDK_S256x16 0.0
                          CDK_R512x16 0.0
                          physical_cells
  Operating conditions:   slow
  Interconnect mode:      global
  Area mode:              physical library
====================================================================

   Instance    Module  Cell Count  Cell Area  Net Area   Total Area
--------------------------------------------------------------------
bound_flasher              164     521.516   184.072      705.588
```

File final_qor.rpt

```
================================================================

Timing
--------

Clock Period
-------------
clk   1500.0


  Cost    Critical         Violating
 Group   Path Slack  TNS     Paths
-------------------------------------
clk             0.3   0.0         0
default    No paths   0.0
-------------------------------------
Total                 0.0         0

Instance Count
--------------
Leaf Instance Count             164
Physical Instance count           0
Sequential Instance Count        13
Combinational Instance Count    151
                                                      34,1          46%
```

File final_time.rpt

```
================================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 13 2024  05:17:56 pm
  Module:                 bound_flasher
  Operating conditions:   slow
  Interconnect mode:      global
  Area mode:              physical library
================================================================


Path 1: MET (0 ps) Setup Check with Pin N_reg[4]/CK->D
          Group: clk
     Startpoint: (R) state_reg[1]/CK
          Clock: (R) clk
       Endpoint: (R) N_reg[4]/D
          Clock: (R) clk

                     Capture       Launch
       Clock Edge:+    1500            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=   1500            0

             Setup:-    123
                                                      19,1          Top
```

Step 7: Prepare script to load NETLIST

```
[l04group7@ktmt RTL]$ cd /home/share_file/cadence
[l04group7@ktmt cadence]$ source add_path
[l04group7@ktmt cadence]$ source add_license
[l04group7@ktmt cadence]$ cd -
/home/l04group7/vlsi/2013053/work/synthesis_env/Genus_BoundFlasher/RTL
[l04group7@ktmt RTL]$ cd
[l04group7@ktmt ~]$ cd vlsi/2013053/work/synthesis_env/Genus_BoundFlasher/LAB1
[l04group7@ktmt LAB1]$ genus -f gui.tcl -gui
```

Netlist: