Control Unit Design: -

While executing instruction certain condition may arise like after performing addition operation carry may be generated, in conditional jump operation depending on condition processor has to execute particular instruction, this type of operation and many other types of operations are initiated by control unit.

Two general approaches to control unit design have envolved.one approach views the controller as a sequential logic circuit that generate specific sequence of control signals in respond to externally supplied instructions. It is designed with the usual goals of minimizing the numbers of components used and maximised the speed of operation. Once the unit is constructed, the only way to implement change in the control-unit behaviour is by redesigning the entire unit, such a circuit is therefore said to be hardwired.

Different hardwired control unit designed technique are available, we discus following two techniques.

1. State table method:

T - States	Instructions			
	I_1	I_2	...	I_N
T_1	$C_{1,1}$	$C_{1,2}$	...	$C_{1,N}$
T_2	$C_{2,1}$	$C_{2,2}$	...	$C_{2,N}$
...	...	...	...	...
T_M	$C_{M,1}$	$C_{M,2}$	...	$C_{M,N}$

$C_{1,1}$ means control signal to be produced in T-state(T_1) of Instruction (I_1)

State table method

- Here the behaviour of control unit is represented in the form of a table, which is known as the **state table**.
- Here, each row represents the T-states and the columns represent the instructions.
- Every intersection of the specific column to each row indicates which control signal will be produced in the corresponding T- state of an instruction.
- Here the hardware circuitry is designed for each column (i.e. for a specific instruction) for producing control signals in different T-states.

Advantage –

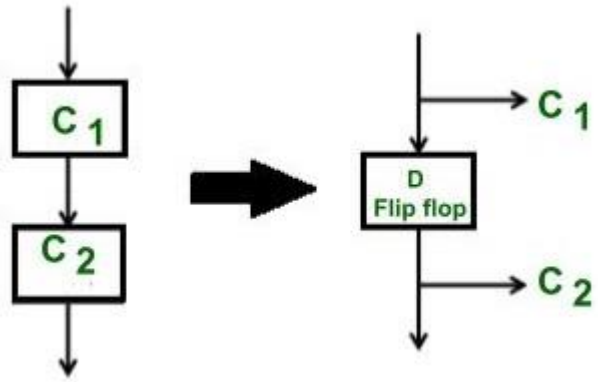
- It is the simplest method.
- This method is mainly used for small instruction set processors (i.e. in RISC processors).

Disadvantage –

- In modern processors, there is a very large number of instructions set. Therefore, the circuit becomes complicated to design, difficult to debug, and if we make any modifications to the state table then the large parts of the circuit need to be changed.
- Therefore, this is not widely used for these kinds of processors.
- There are many redundancies in circuit design like the control signals are required for fetching the instruction is common and which is repeated for N number of instructions. So, the cost of circuitry design may increase.

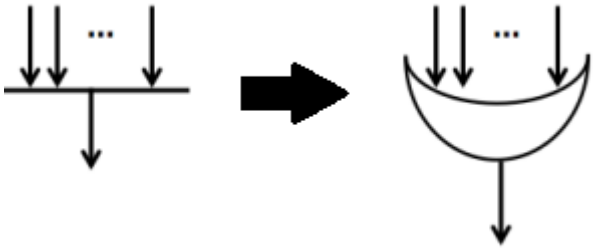
2. Delay element method:

- Here the control unit behaviour is represented in the form of a **flowchart**.
- Each step in the flowchart represents a control signal that needs to be produced for processing the instructions.
- If all the steps of the instructions are performed, this means the instruction is executed completely.
- **Control signals perform micro-operations and each micro-operation requires one T-state.**
- For the micro-operations which are independent, they are required to be performed in different T-state. Therefore, for every consecutive control signal an exactly 1-state delay is required, which can be produced with the help of D FF.
- Therefore. D Flip-Flops are inserted between every two consecutive control signals.

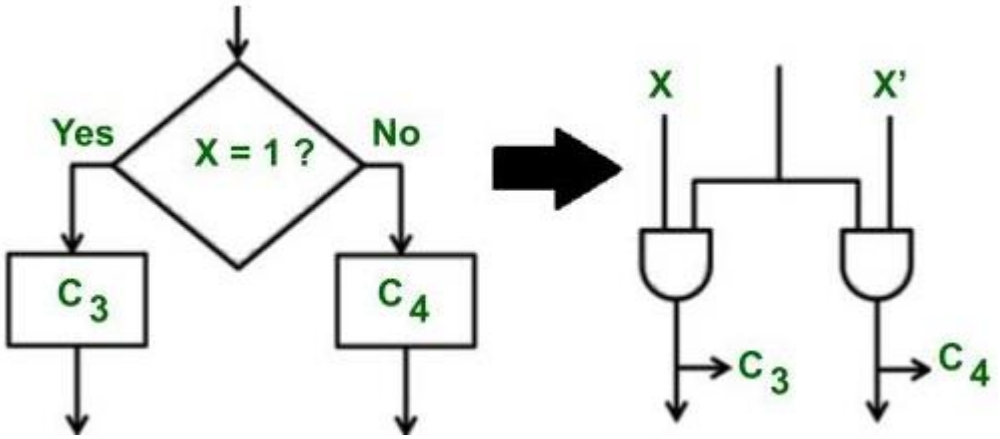


- As we can observe, the D FF is introduced between each pair of control signals. Therefore, after a control signal is generated, then the delay element before that control signal is not in use until before the next instruction required that control signal. Therefore, of all D Flip-Flops, only one will be active at a time. Therefore, this method is also known as **one hot method**.

- In a flowchart, if there is a multiple entry point for control signal then to combine two or more paths, we use an OR gate.

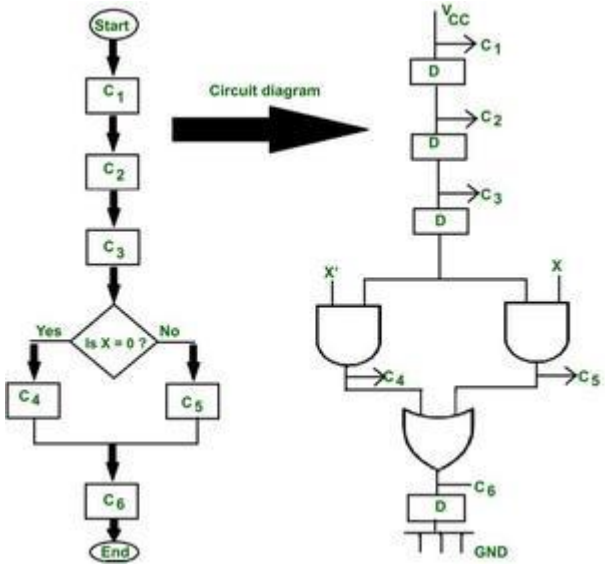


- A decision box is converted into a set of two complementing AND gates.



Example –

Suppose the processor has two instructions add or subtract (Therefore an opcode of 1 bit is needed in which 0 opcode for add instruction and 1 for subtract is used.



Delay element method for generating control signals.

Flowchart design –

Say C_1,C_2,C_3 is the control signals for fetching the instruction. When X= 0, then C_4 control signal is produced (i.e. decoding) which is used for performing add operation, and when x=1, then control signal C_5 will be produced for performing the subtract operation. And c_6 control signal is used for storing the result and the process ends.

Circuit design –

Between two consecutive control signals which are independent, one delay element is introduced between them to produce a delay of 1 T state. The decision box is converted into and complemented AND gate circuit (i.e. if x= 0 then x'= 1, so, a c_4 control signal is generated.

Advantage –

- This method has a logical approach; therefore it helps to reduce the circuit complexity.
- For the common control signals which need to be generated in every instruction, for them only one circuitry can be designed.

Disadvantage –

- As the number of instructions increases, the number of D FF for generating delay is increased, so overall circuit complexity and cost increases.