# DIGISIM

PROBLEM STATEMENT 1 (PART 2)

Team: Cool Bits

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APPROACH

To traverse the doubly linked list, we start with user given address of a node (say, address X), which may or may not be the head of list. We save the value of data at this node and then move to the address at which X+1 points. Now we compare the value of this node to the previously stored value, keeping the minimum value for further use. We repeat this process until the data at X_n+1 becomes 255. Once we obtain a 255, this implies we have reached one end of doubly linked list. We get back to the user given address, this time traversing at address X+2 and comparing values for minimum of all nodes. Again when data at address X_n+2 becomes 255, the circuit is stoped. At completion a LED will light up denoting that traversal is completed. Example of traversal alogrithm is shown in below figure.
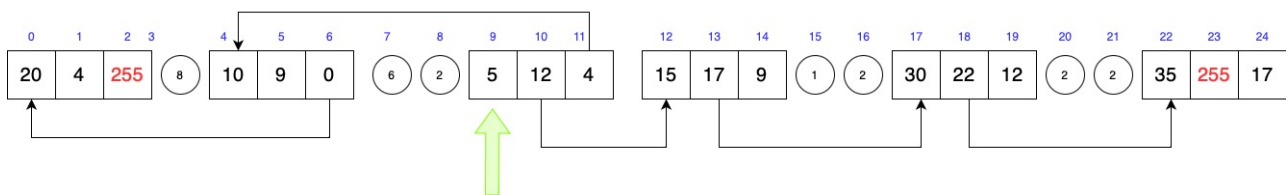
COMPONENTS USED

ROM (2732)	Multiplexer (74157)	Adder (74283)
Register (74179)	JK Flip Flop (74109)	Comparator (7485)
Counter (74161)	Buffer (74125)	LED-RED
Clock	2-input Logic Gates (AND, OR, NOT, XNOR)	

COST

QUANTITY	COMPONENT CODE	COMPONENT NAME	UNIT COST
1	2732	ROM	75
2	74157	Multiplexer	2
1	74283	Adder	2
4	74179	Register	2
3	74109	JK Flip Flop	1
3	7485	Comparator	2
1	74161	Counter	2
1	74125	Buffer	0.1
6	AND	2 input AND gate	0.1
6	NOT	NOT Gate	0.1
5	OR	2 input OR gate	0.1
1	4077	2 input XNOR gate	0.1
1	CLOCK		40
TOTAL			**141.90**

Cost of LED and 7-Segment Display Setup is not included.

Additional Features

- The algorithm has **fastest** traversal over doubly linked list.
- Stoping the circuit when traversal is completed.
- Display of **traversal completion** using LED.
- Display of answers using **7-Segment Display**.
- If the minimum data value is same, and address is different, the circuit will show minimum address out of those.

NOTE: File PS1_Part2.pdsprj is made in Proteus version 8.9, FilePS1_Part2_7SEG.pdsprj is made in Proteus version 8.13 as it was version 8.9 was giving error while running simulation of 7-segment display.