

- 1) We want to design a circuit that input two 2-bit unsigned numbers, and output a 3-bit signed number that represents the difference between the two input numbers (i.e., it is the result of the first number minus the second number). Derive the truth table, write the Boolean equation in sum of products form, and simplifying it with Karnaugh Maps. Write the simplified Boolean equation. Draw the simplified circuit with only 2-input AND, 2-input OR and NOT gates.

1) 设输入的第1个数为  $[1:0]X$ , 输入的第2个数为  $[1:0]Y$ , 输出的数为  $[2:0]Q$

真值表:

$x_1$	$x_0$	$y_1$	$y_0$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0	0	0
0	0	0	1	1	1	1
0	0	1	0	1	1	0
0	0	1	1	1	0	1
0	1	0	0	0	0	1
0	1	0	1	0	0	0
0	1	1	0	1	1	1
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	0	1	0	0	1
1	0	1	0	0	0	0
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	0	1	0	1	0
1	1	1	0	0	0	1
1	1	1	1	0	0	0

布尔方程:

$$Q_0 = \bar{x}_1 \bar{x}_0 \bar{y}_1 y_0 + \bar{x}_1 \bar{x}_0 \bar{y}_1 \bar{y}_0 + \bar{x}_1 x_0 \bar{y}_1 \bar{y}_0 + \bar{x}_1 x_0 y_1 \bar{y}_0 + x_1 \bar{x}_0 \bar{y}_1 y_0 + x_1 \bar{x}_0 y_1 \bar{y}_0 + x_1 x_0 \bar{y}_1 \bar{y}_0 + x_1 x_0 y_1 \bar{y}_0$$

$$Q_1 = \bar{x}_1 \bar{x}_0 \bar{y}_1 y_0 + \bar{x}_1 \bar{x}_0 y_1 \bar{y}_0 + \bar{x}_1 x_0 \bar{y}_1 \bar{y}_0 + \bar{x}_1 x_0 y_1 y_0 + x_1 \bar{x}_0 \bar{y}_1 y_0 + x_1 \bar{x}_0 y_1 \bar{y}_0 + x_1 x_0 \bar{y}_1 y_0 + x_1 x_0 y_1 \bar{y}_0$$

$$Q_2 = \bar{x}_1 \bar{x}_0 \bar{y}_1 y_0 + \bar{x}_1 \bar{x}_0 y_1 \bar{y}_0 + \bar{x}_1 x_0 \bar{y}_1 \bar{y}_0 + x_1 \bar{x}_0 \bar{y}_1 y_0 + x_1 \bar{x}_0 y_1 \bar{y}_0 + x_1 x_0 \bar{y}_1 y_0 + x_1 x_0 y_1 \bar{y}_0$$

卡诺图:  $Q_0$

$y_1 y_0 \backslash x_1 x_0$	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	1	0	0	1
10	0	1	1	0

化简得:  $Q_0 = \bar{x}_0 y_0 + x_0 \bar{y}_0$

卡诺图:  $Q_1$

$y_1 y_0 \backslash x_1 x_0$	00	01	11	10
00	0	0	1	1
01	1	0	1	0
11	0	1	0	1
10	1	1	0	0

化简得:  $Q_1 = x_1 \bar{y}_1 \bar{y}_0 + x_1 x_0 \bar{y}_1 + \bar{x}_1 y_1 \bar{y}_0 + \bar{x}_1 x_0 y_1 + \bar{x}_1 \bar{x}_0 \bar{y}_1 y_0 + x_1 \bar{x}_0 y_1 y_0$

- 1) We want to design a circuit that input two 2-bit unsigned numbers, and output a 3-bit signed number that represents the difference between the two input numbers (i.e., it is the result of the first number minus the second number). Derive the truth table, write the Boolean equation in sum of products form, and simplifying it with Karnaugh Maps. Write the simplified Boolean equation. Draw the simplified circuit with only 2-input AND, 2-input OR and NOT gates.

Handwritten solution for the circuit design problem:

Truth Table for  $Q_2$ :

$X_1 X_0$	$Y_1 Y_0$	$Q_2$
00	00	0
00	01	0
00	11	0
00	10	0
01	00	1
01	01	0
01	11	0
01	10	0
11	00	1
11	01	0
11	11	0
11	10	0

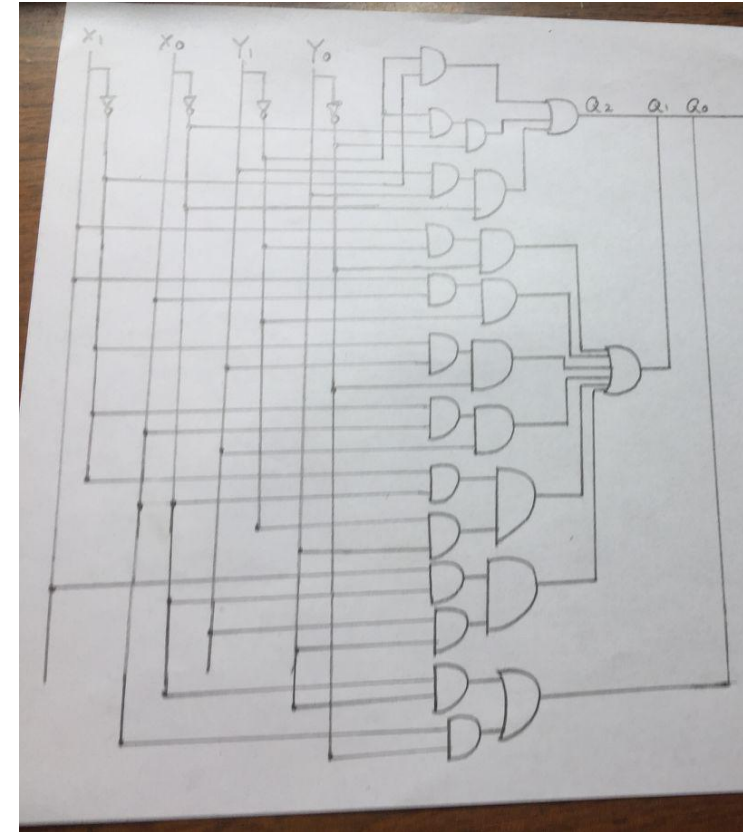
Simplified Boolean equation for  $Q_2$ :

$$Q_2 = \bar{X}_1 Y_1 + \bar{X}_1 \bar{X}_0 Y_0 + \bar{X}_0 Y_1 Y_0$$

化简后的布尔方程:

$$Q_0 = \bar{X}_0 Y_0 + X_0 Y_0$$

$$Q_1 = X_1 \bar{Y}_1 \bar{Y}_0 + X_1 X_0 \bar{Y}_1 + \bar{X}_1 Y_1 \bar{Y}_0 + \bar{X}_1 X_0 Y_1 + \bar{X}_1 \bar{X}_0 \bar{Y}_1 Y_0 + X_1 \bar{X}_0 Y_1 Y_0$$

$$Q_2 = \bar{X}_1 Y_1 + \bar{X}_1 \bar{X}_0 Y_0 + \bar{X}_0 Y_1 Y_0$$




2) Design a circuit that input a 3-bit number. The circuit outputs a 1 if the input number is larger than or equal to 3. Otherwise, it output a 0.

- a. Derive the truth table of the circuit, write the Boolean equation in sum of products form, and simplifying it with Karnaugh Maps. Write the simplified Boolean equation, and draw the simplified circuit with only 2-input AND, 2-input OR and NOT gates.

a. 设输入的数字为  $[2:0]X$ , 输出的值为  $Y$

真值表:

$X_2$	$X_1$	$X_0$	$Y$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

布尔方程:

$$Y = \bar{X}_2 X_1 X_0 + X_2 \bar{X}_1 \bar{X}_0 + X_2 \bar{X}_1 X_0 + X_2 X_1 \bar{X}_0 + X_2 X_1 X_0$$

卡诺图:

$X_2 \backslash X_1 X_0$	00	01	11	10
0	0	0	1	1
1	0	1	1	1

化简后的布尔方程:

$$Y = \bar{X}_2 \bar{X}_1 \bar{X}_0 + X_2 X_1 X_0$$

电路图:

```

graph LR
    X2 --- XOR
    X1 --- AND
    X0 --- AND
    AND --- XOR
    XOR --- Y
  
```

- b. Write the Verilog module of the circuit with ① gate level description, ② Boolean equation description with Continuous Assignment, i.e. with “assign” statement, ③ behavior level description with “always” and “if-else” statement, ④ behavior level description with “always” and “case” statement.

①使用门级电路

module comparer(

input [2:0] X,

output Y

);

wire out;

and i0(out,X[1],X[0]);

or i1(Y,out,X[2]);

endmodule

②使用 assign 语句

module comparer(

input [2:0] X,

output Y

);

assign Y=X[2]||(X[1]&X[0]);

endmodule

③使用 always 语句和 if-else 语句

module comparer(

input [2:0] X,

output reg Y

);

always@(\*) begin

if(X[2]||(X[1]&X[0])==1)

Y=1;

else

Y=0; end

endmodule

④使用 always 语句和 case 语句

module comparer(

input [2:0] X,

output reg Y

);

always@(\*) begin

case(X[2]||(X[1]&X[0]))

1'b1:Y=1;

1'b0:Y=0; endcase

end

endmodule

- 3) We want to design a circuit that input 6-bit number. The circuit with output a 1 if the input number is larger than or equal to 27 (hint:  $27_{(10)}=011011_{(2)}$ ). Write the verilog module of this circuit by using the verilog module of problem 2) and AND/OR/NOT gates in a Hierarchy form. Validate your design in your Basys3 board.

设计源代码:

```
module topcomparer(  
  
    input [5:0] X,  
  
    output Y  
  
);  
  
    wire out1,out2,out3;  
  
    comparer c1(X[5:3],out1);  
  
    comparer c2(X[2:0],out2);  
  
    and(out3,out1,out2);  
  
    or(Y,out3,X[5]);  
  
    endmodule
```