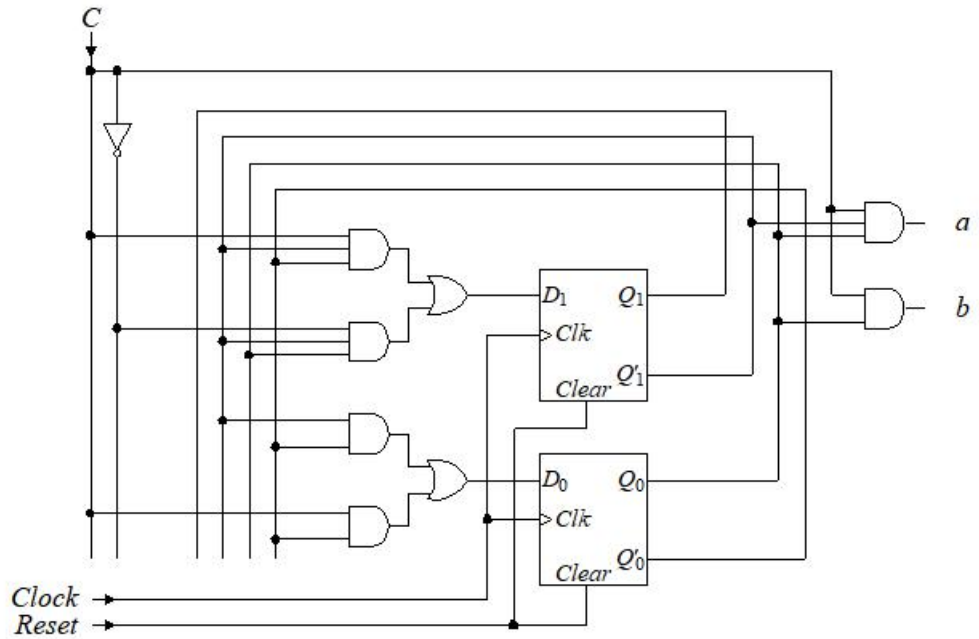
3) Analyze the following two FSM circuits.



(a)

① 次态方程 $Q_{1next} = CQ_1'Q_0' + C'Q_1'Q_0$

$Q_{0next} = Q_1'Q_0' + CQ_0'$

② 次态表

当前状态 Q_1Q_0	次态 $Q_{1next}Q_{0next}$	
	$C=0$	$C=1$
0 0	0 1	1 1
0 1	1 0	0 0
1 0	0 0	0 1
1 1	0 0	0 0

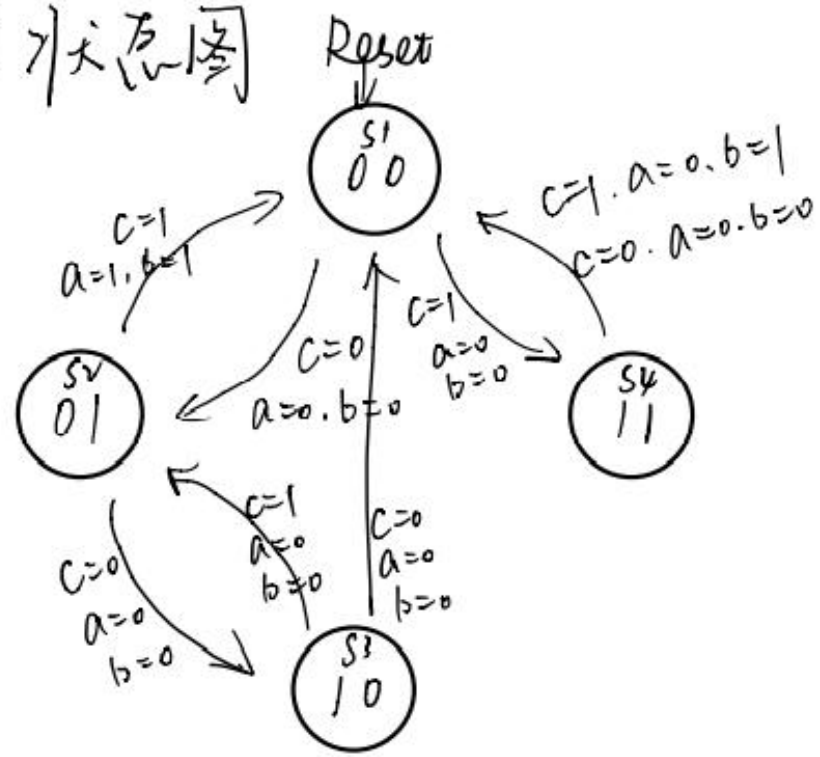
③ 输出方程 $a = CQ_1'Q_0$

$b = CQ_0$

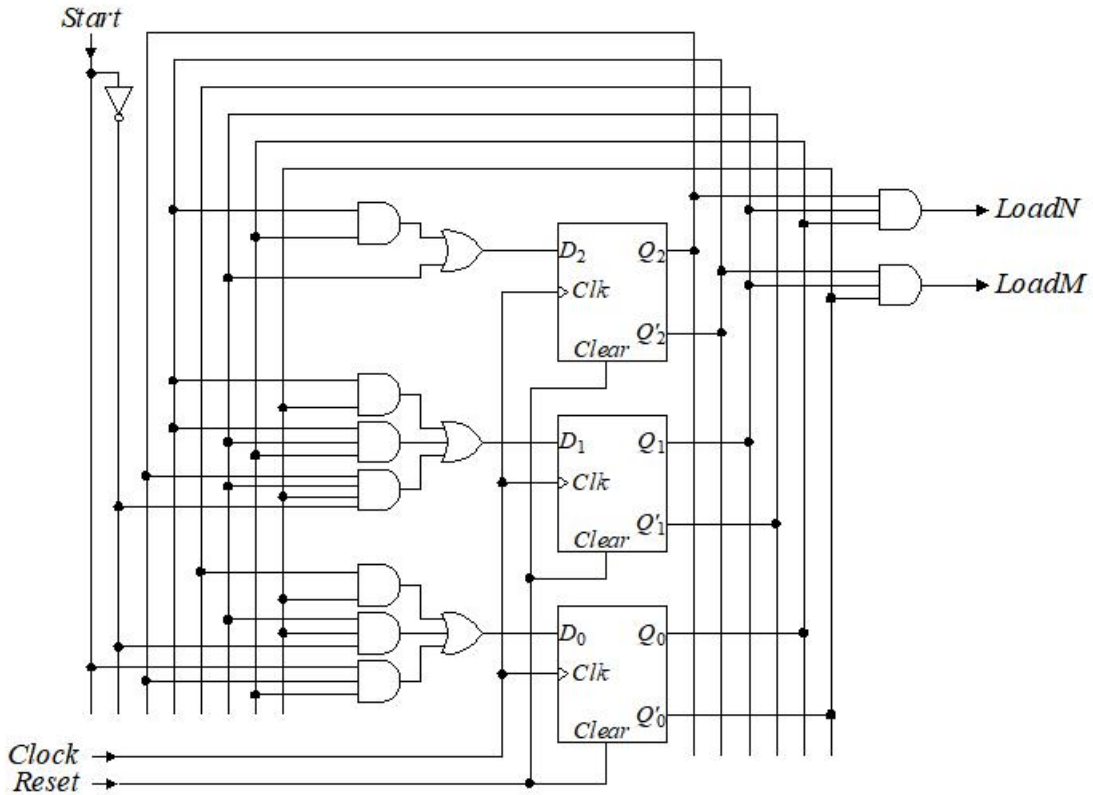
④ 输出表

当前状态	当前输出 a		当前输出 b	
Q_1Q_0	C=1	C=0	C=1	C=0
S_1 0 0	0	0	0	0
S_2 0 1	1	0	1	0
S_3 1 0	0	0	0	0
S_4 1 1	0	0	1	0

⑤ 状态图



3) Analyze the following two FSM circuits.



① 次态方程

$Q_{2next} = Q_2' Q_0 + Q_1'$

$Q_{1next} = Q_2' Q_0' + Q_2' Q_1' Q_0 + Q_2 Q_1' Q_0' Start'$

$Q_{0next} = Q_1 Q_0' + Q_1' Q_0' Start' + Q_2 Q_0 Start$

② 次态表

	现态 $Q_2Q_1Q_0$	次态 $Q_{2next}Q_{1next}Q_{0next}$ Start=1	次态 $Q_{2next}Q_{1next}Q_{0next}$ Start=0
S1	0 0 0	1 1 0	1 1 1
S2	0 0 1	1 1 0	1 1 0
S3	0 1 0	0 1 1	0 1 1
S4	0 1 1	1 0 0	1 0 0
S5	1 0 0	1 0 0	1 1 1
S6	1 0 1	1 0 1	1 0 0
S7	1 1 0	0 0 1	0 0 1
S8	1 1 1	0 0 1	0 0 0

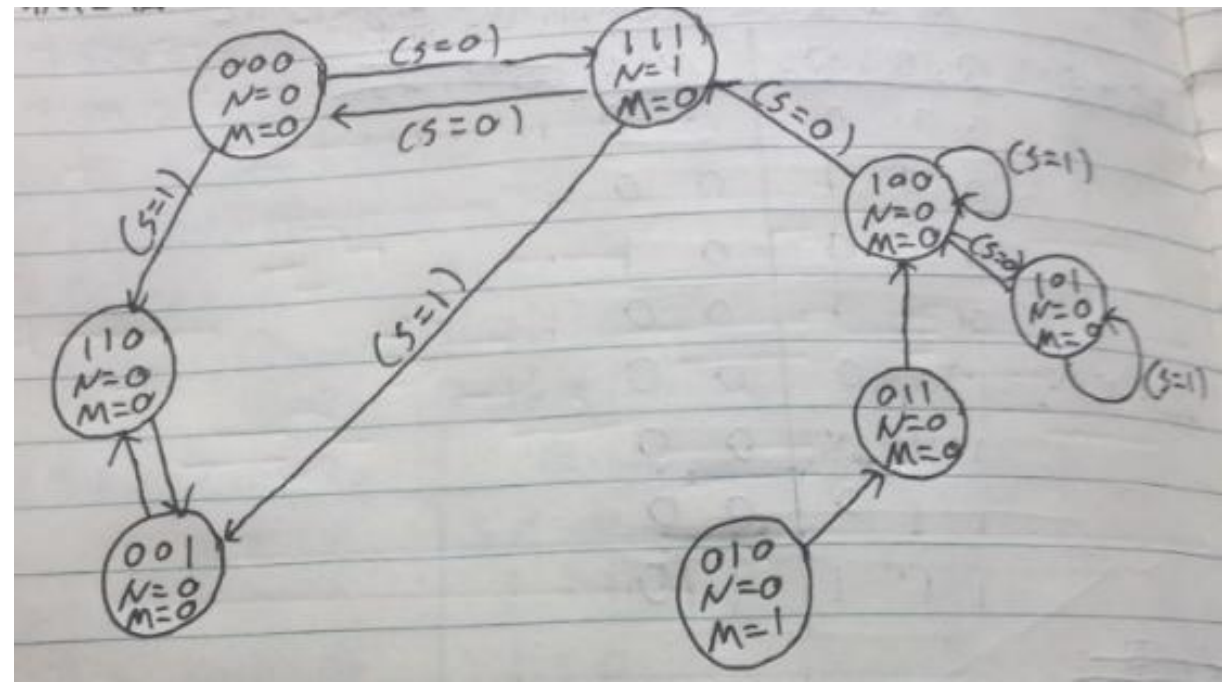
③ 输出方程 $Load\,N = Q_2Q_1Q_0$

$Load\,M = Q_2'Q_1Q_0'$

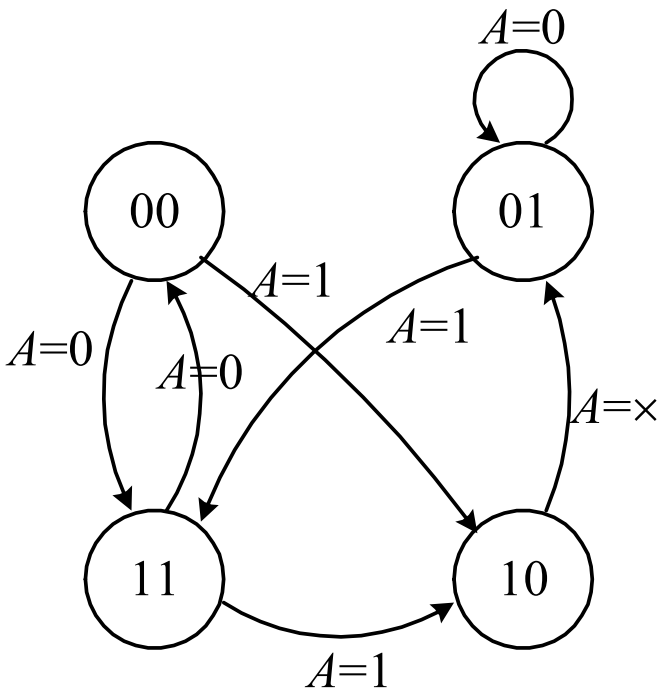
④ 输出表

当前状态	输出	
$Q_2Q_1Q_0$	Load N	Load M
0 0 0	0	0
0 0 1	0	0
0 1 0	0	1
0 1 1	0	0
1 0 0	0	0
1 0 1	0	0
1 1 0	0	0
1 1 1	1	0

⑤ 状态图



4) Synthesize FSM circuits for the following two state diagrams, respectively.



3) 综合第一个FSM状态图：

次态表：

Q_1Q_0	Q_{1next} A=0	Q_{1next} A=1	Q_{0next} A=0	Q_{0next} A=1
00	1	1	1	0
01	0	1	1	1
10	0	1	0	1
11	0	0	1	0

次态方程：Q_{1next}

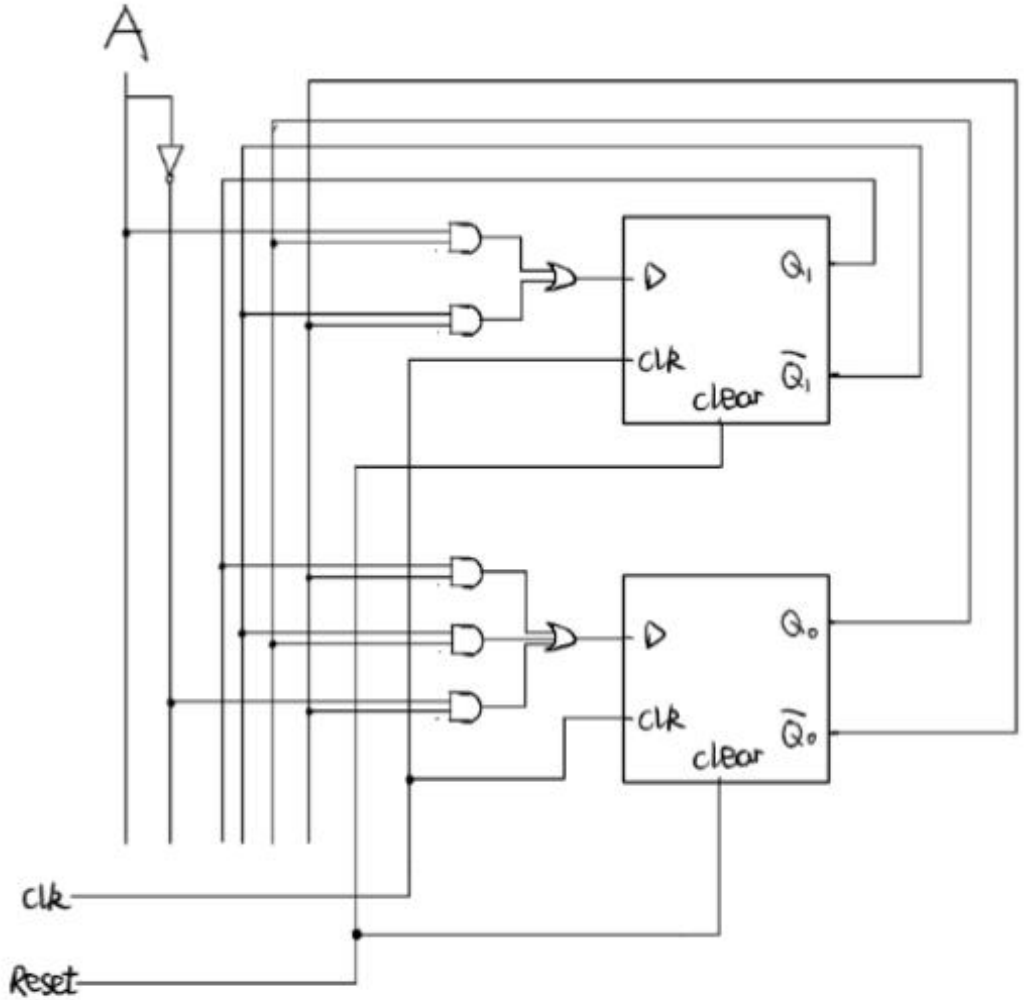
Q_1Q_0 \ A	0	1
00	1	1
01	0	1
11	0	1
10	0	0

$Q_{1next} = Q_1'Q_0' + Q_0A$

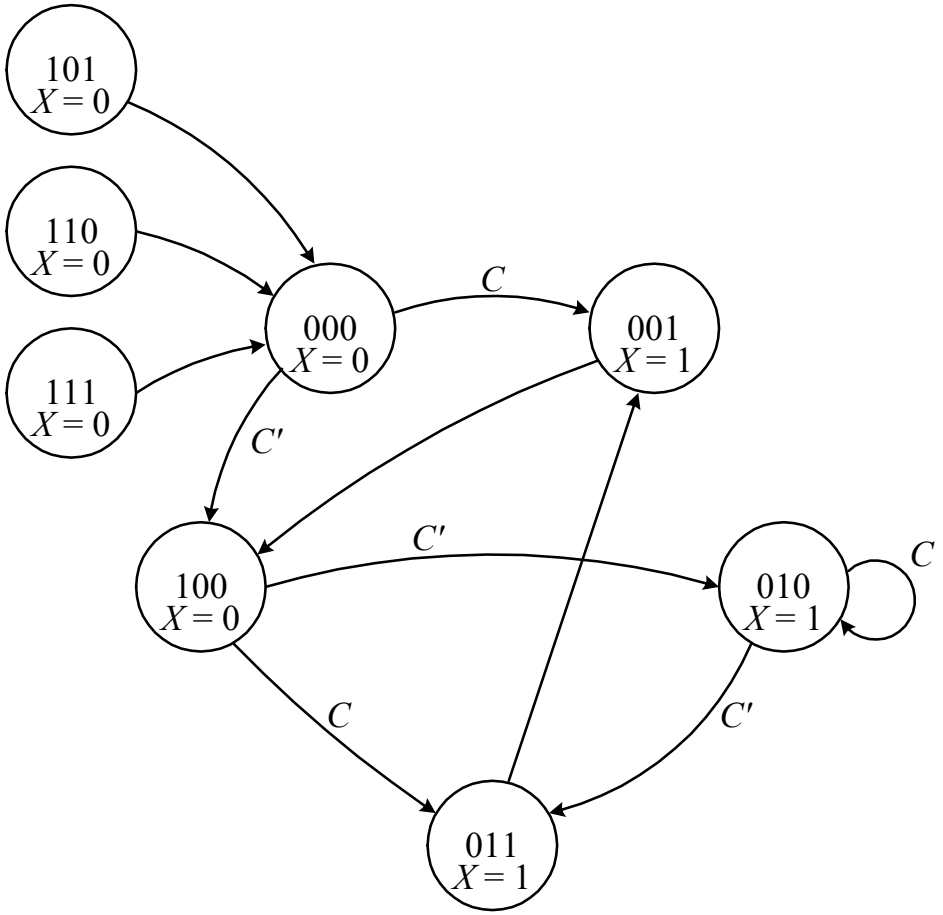
Q_{0next}

Q_1Q_0 \ A	0	1
00	1	0
01	1	1
11	0	0
10	1	1

$Q_{0next} = Q_1'A' + Q_1'Q_0 + Q_1Q_0'$


A
D
Q1
clk
clear
Q̄1
D
Q0
clk
clear
Q̄0
clk
Reset

4) Synthesize FSM circuits for the following two state diagrams, respectively.



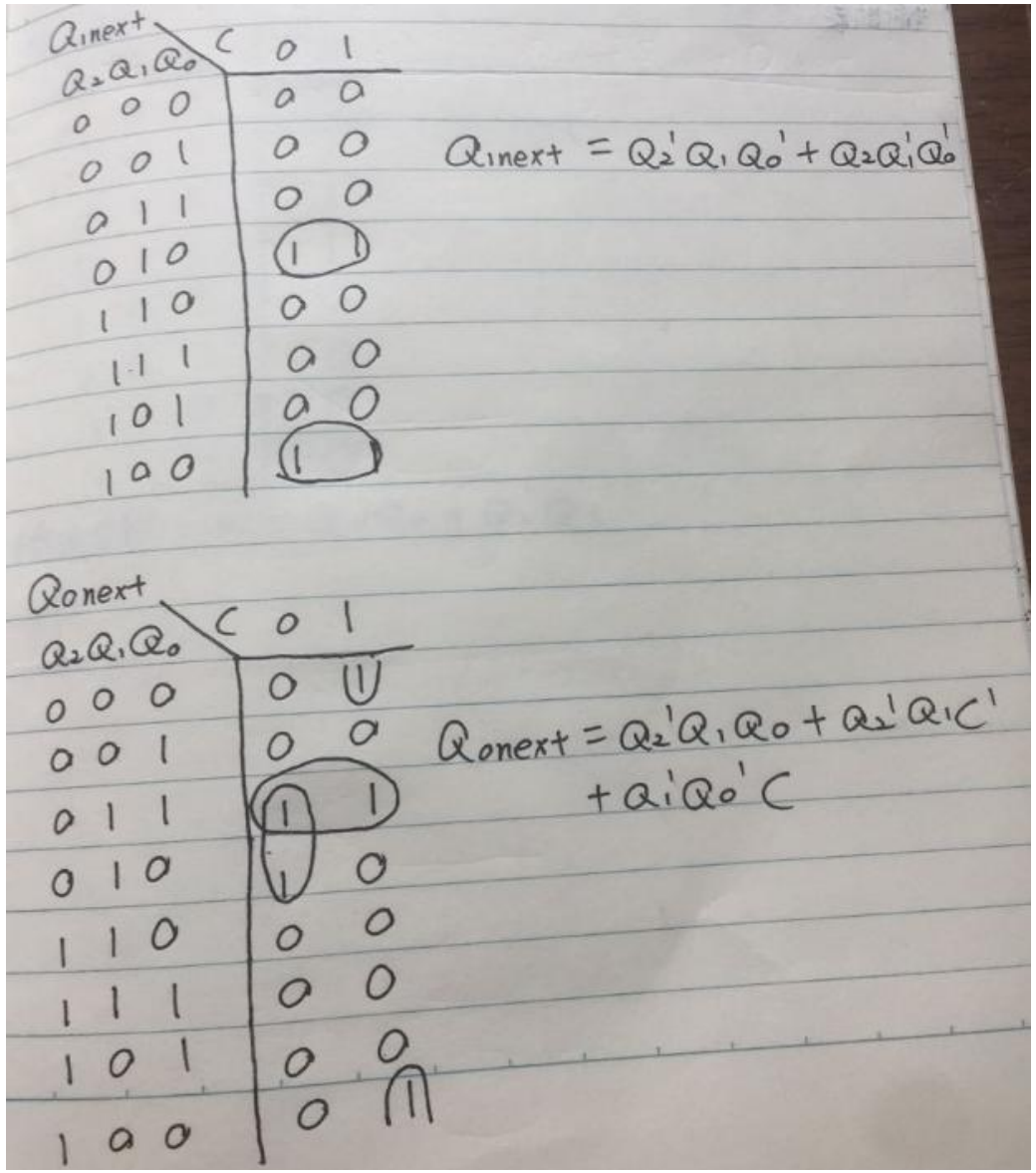
次态表：$Q_2Q_1Q_0$

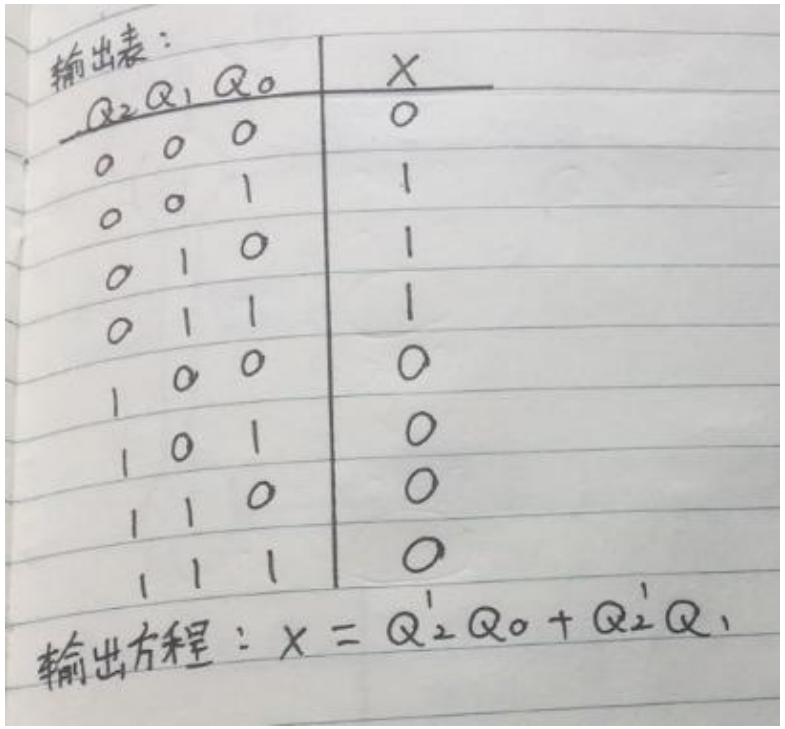
$Q_2Q_1Q_0$	$Q_{2next}Q_{1next}Q_{0next}$ C=0	C=1
000	100	001
001	100	100
010	011	010
011	001	001
100	010	011
101	000	000
110	000	000
111	000	000

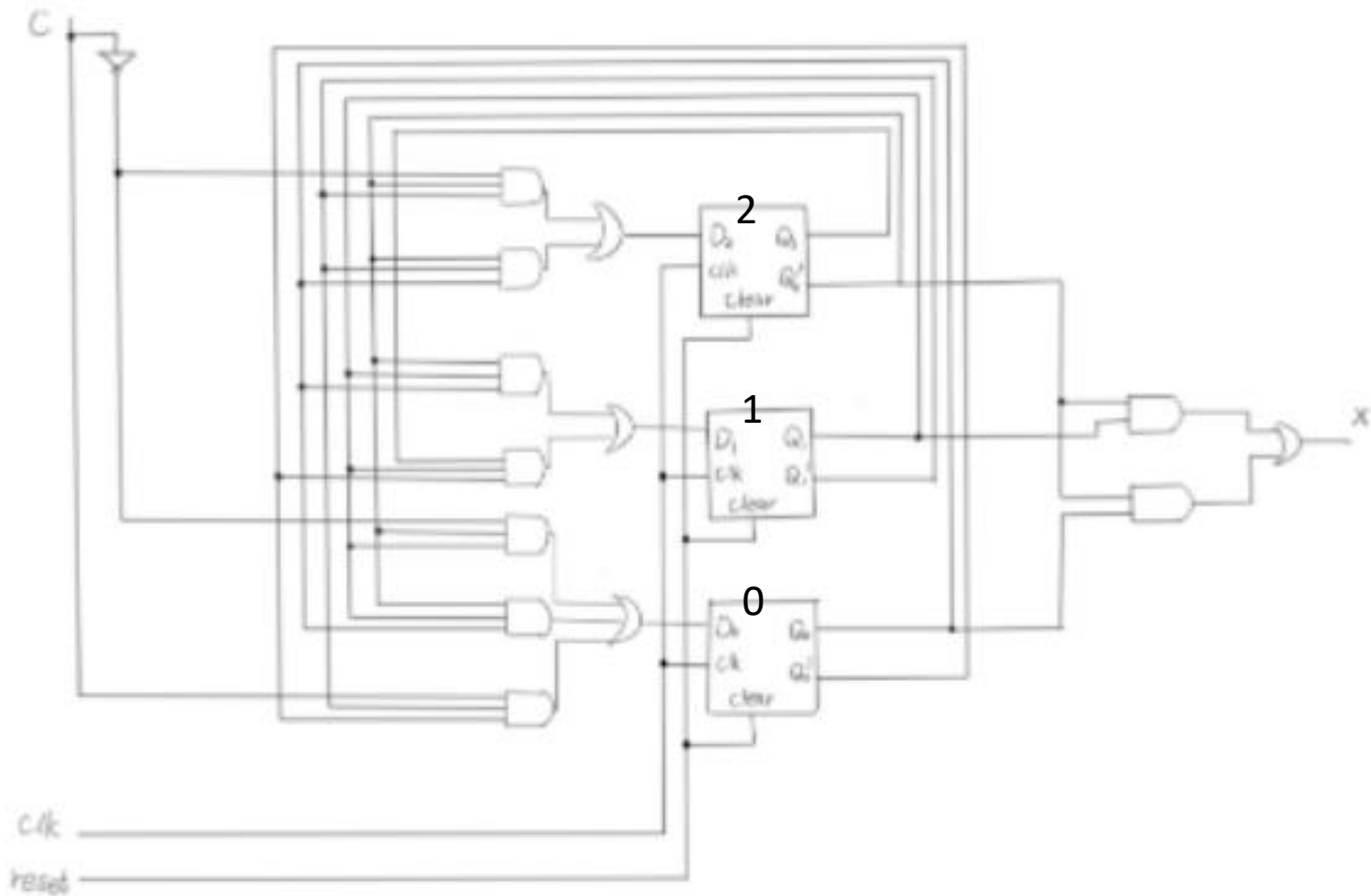
次态方程：Q_{2next}

$Q_2Q_1Q_0$	C 0	1
000	1	0
001	1	1
011	0	0
010	0	0
110	0	0
111	0	0
101	0	0
100	0	0

$Q_{2next} = C'Q_2'Q_1' + Q_2'Q_1'Q_0$


Q1next
Q2Q1Q0 C 0 1
000 0 0
001 0 0
011 0 0
010 1 1
110 0 0
111 0 0
101 0 0
100 1
Q1next = Q2'Q1Q0' + Q2Q1'Q0'
Qonext
Q2Q1Q0 C 0 1
000 0 1
001 0 0
011 1 1
010 1 0
110 0 0
111 0 0
101 0 0
100 0 1
Qonext = Q2'Q1Q0 + Q2'Q1C'
+ Q1'Q0'C


输出表：
Q2Q1Q0 X
000 0
001 1
010 1
011 1
100 0
101 0
110 0
111 0
输出方程：X = Q2'Q0 + Q2'Q1


C
2
1
0
x
clk
reset

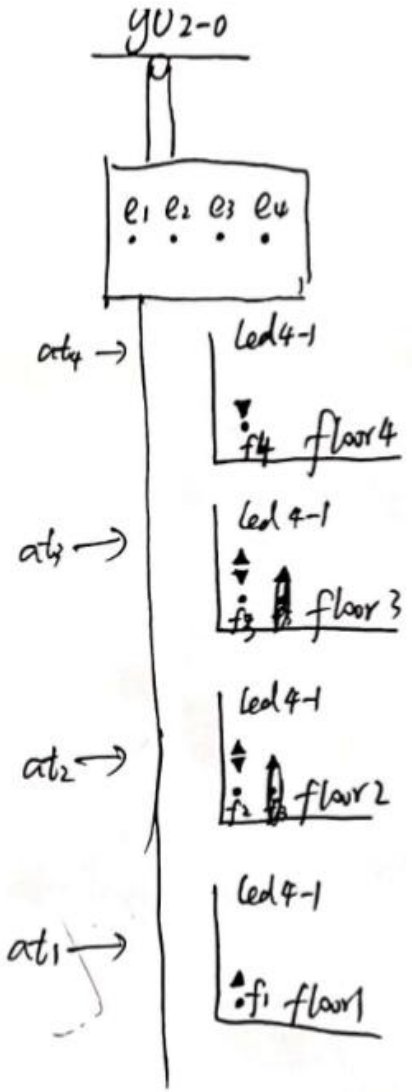
5) In class we discussed the design and synthesis of a controller for an elevator of a two floor building. In this problem we want to extend the design to a four floor building. Draw the state diagrams of the Moore FSM and Mealy FSM. Write the corresponding Verilog module of the two FSMs, respectively.

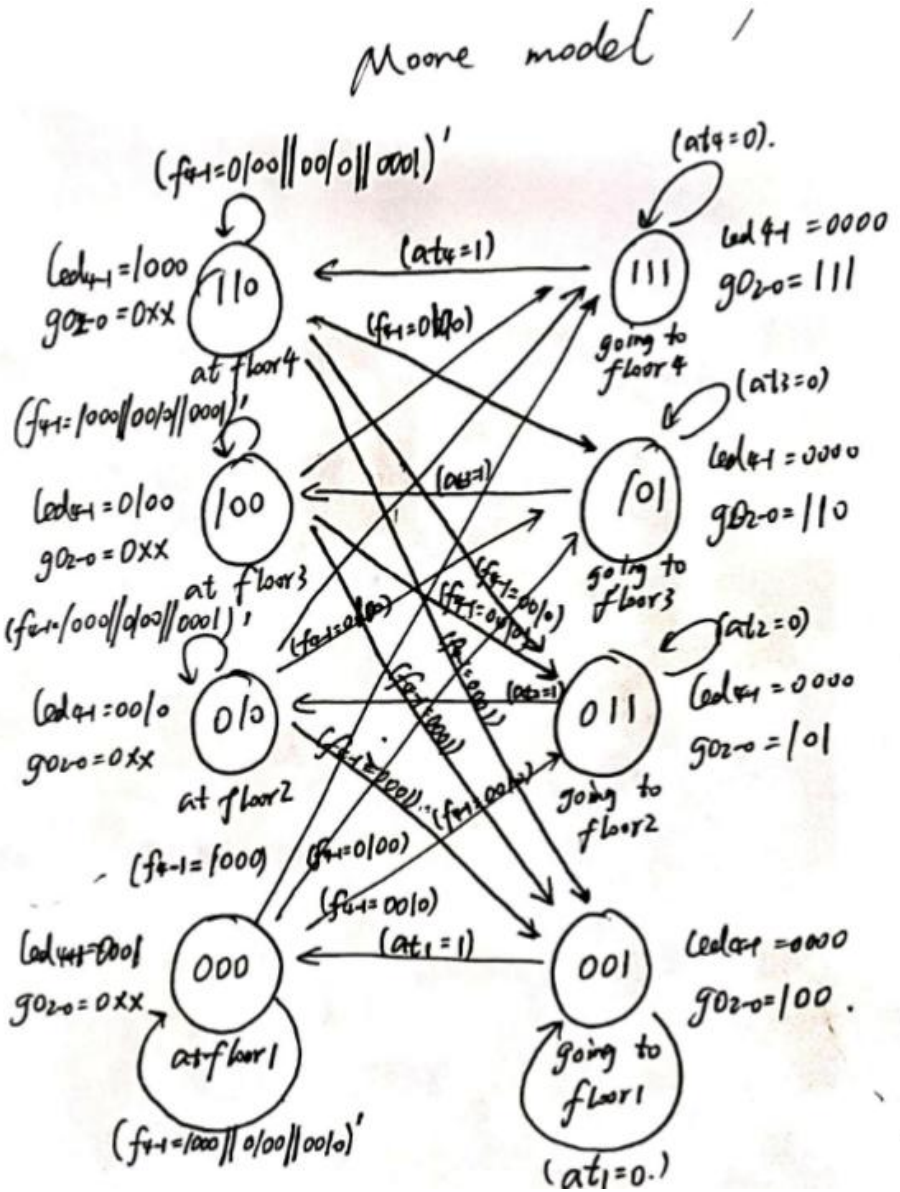
输入：

- f1,f2,f3,f4：指示电梯去往哪层，如f4(1000)即去往第四层，f3(0100)即去往第三层；
- at1,at2,at3,at4：指示电梯目前在哪层，如0000表示哪层都不在，at4=1(1000)表示在第四层；

输出：

- g2：指示电梯运动状态，1表示运动中，0表示静止中（可以从这个信号入手理解状态图）；
- g1-0：指示电梯运动时的运动目的地，可理解为当g2==1时有效，如g1-0=00，表示运动目的地为第一楼；
- led4-1：指示电梯目前在哪层，如0000表示哪层都不在，led4-1==1000表示在第四层。





输入：

- f1,f2,f3,f4：指示电梯去往哪层，如f4(1000)即去往第四层，f3(0100)即去往第三层；
- at1,at2,at3,at4：指示电梯目前在哪层，如0000表示哪层都不在，at4=1(1000)表示在第四层；

输出：

- g2：指示电梯运动状态，1表示运动中，0表示静止中（可以从这个信号入手理解状态图）；
- g1-0：指示电梯运动时的运动目的地，可理解为当g2==1时有效，如g1-0=00，表示运动目的地为第一楼；
- led4-1：指示电梯目前在哪层，如0000表示哪层都不在，led4-1==1000表示在第四层。