homework3

1. We have the following Verilog code. Please draw the circuit with only AND/OR/NOT gates.

```
////////////////////////////////////
// Sequential always block with a
//   combinational always block

 reg [3:0] count1, next_count1;

 always @(posedge clk)
   count1 <= next_count1;

 always @*  begin
   if (reset) next_count1 = 0;
   else next_count1 =
        (count1 == 4) ? 0 : count1 + 1;
   end

 assign enable1 = (count1 == 4);
////////////////////////////////////
```

5进制计数器，二段式写法

注意同步置零，D触发器上升沿触发，

代码里用了4个D触发器

Q3	Q2	Q1	Q0	D3	D2	D1	D0	Y
0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	1	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	0	0	0	1

Q1Q0

D3 \ Q3Q2	00	01	11	10
00	0	0	0	0
01	0	X	X	X
11	X	X	X	X
10	X	X	X	X

Q1Q0

D2 \ Q3Q2	00	01	11	10
00	0	0	1	0
01	0	X	X	X
11	X	X	X	X
10	X	X	X	X

Q1Q0

Y \ Q3Q2	00	01	11	10
00	0	0	0	0
01	1	X	X	X
11	X	X	X	X
10	X	X	X	X

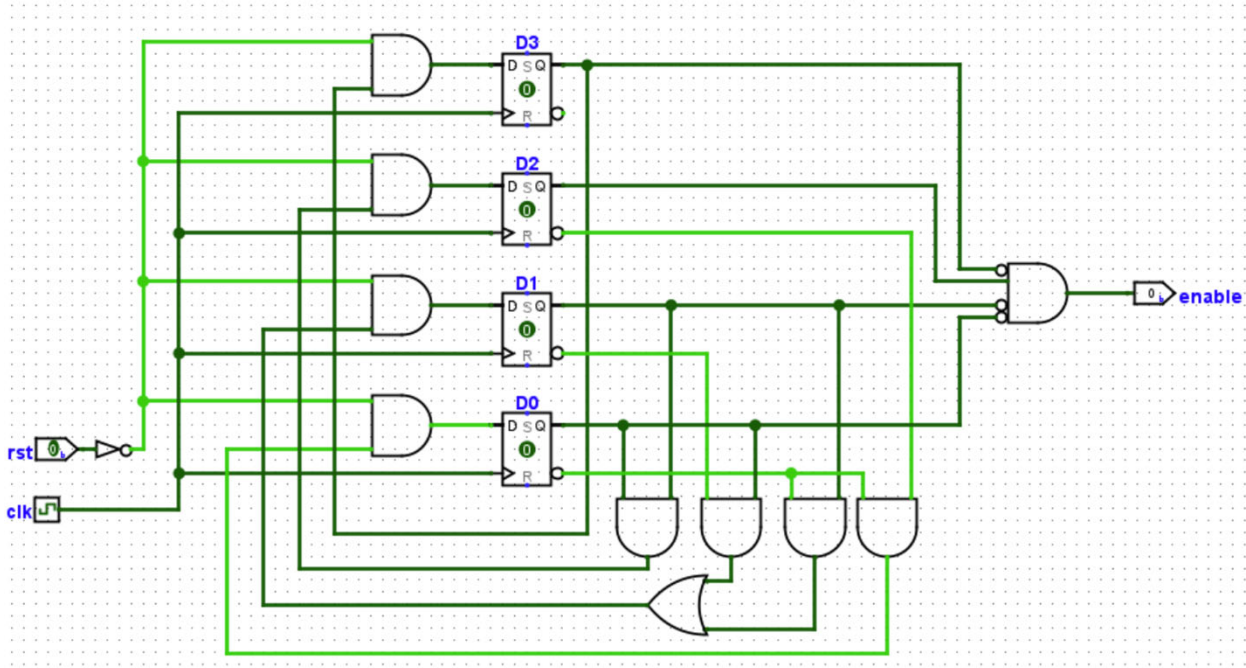
Q1Q0

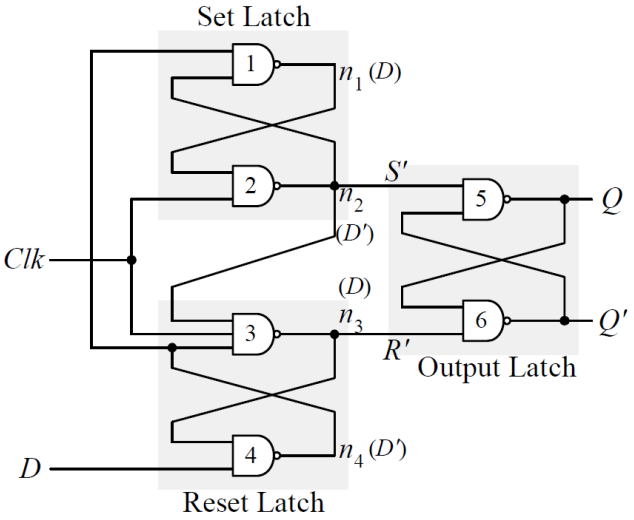
D1 \ Q3Q2	00	01	11	10
00	0	1	0	1
01	0	X	X	X
11	X	X	X	X
10	X	X	X	X

Q1Q0

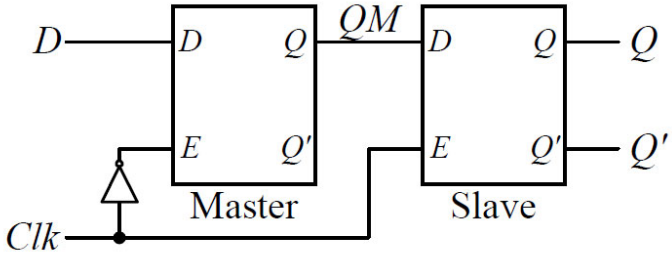
D0 \ Q3Q2	00	01	11	10
00	1	0	0	1
01	0	X	X	X
11	X	X	X	X
10	X	X	X	X

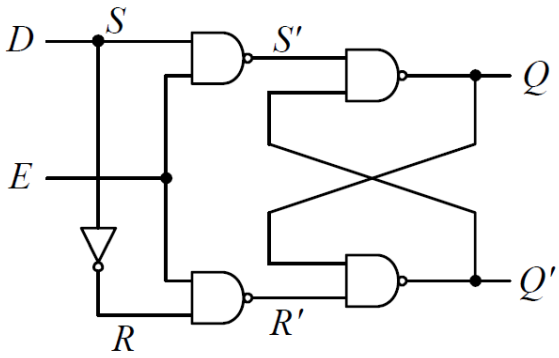
D3=Q3
D2=Q1Q0
D1=Q1'Q0+Q1Q0′
D0= Q2'Q0′
enable=Q2





或者





2. A binary coded decimal (BCD) up counter uses four bits to count the decimal digits from 0 to 9 and then cycles back to 0. Write the Verilog code of it. Draw the circuit of it, with AND/OR/NOT/DFF as the basic circuit elements.

```
module counter_10(clk,r,q);
    input clk, r;
    output [3:0] q;
    reg [3:0] q=0;
    always @(posedge clk)
    begin
        if(r) q=0;
        else
            begin
                if(q==(9)) q=0;
                else q=q+1;
            end
    end
endmodule
```

Q3	Q2	Q1	Q0	D3	D2	D1	D0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

Q1Q0

D3 / Q3Q2	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	1	0	X	X

Q1Q0

D2 / Q3Q2	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	X	X
10	0	0	X	X

D3=Q3Q0'+Q2Q1Q0

D2=Q2Q1'+ Q2Q0'+ Q2'Q1Q0

Q1Q0

D1 / Q3Q2	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	0	0	X	X

Q1Q0

D0 / Q3Q2	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

D1=Q1Q0'+Q3'Q1'Q0

D0=Q0’

D3=Q3Q0'+Q2Q1Q0
D2=Q2Q1'+ Q2Q0'+
Q2'Q1Q0
D1=Q1Q0'+Q3'Q1'Q0
D0=Q0’