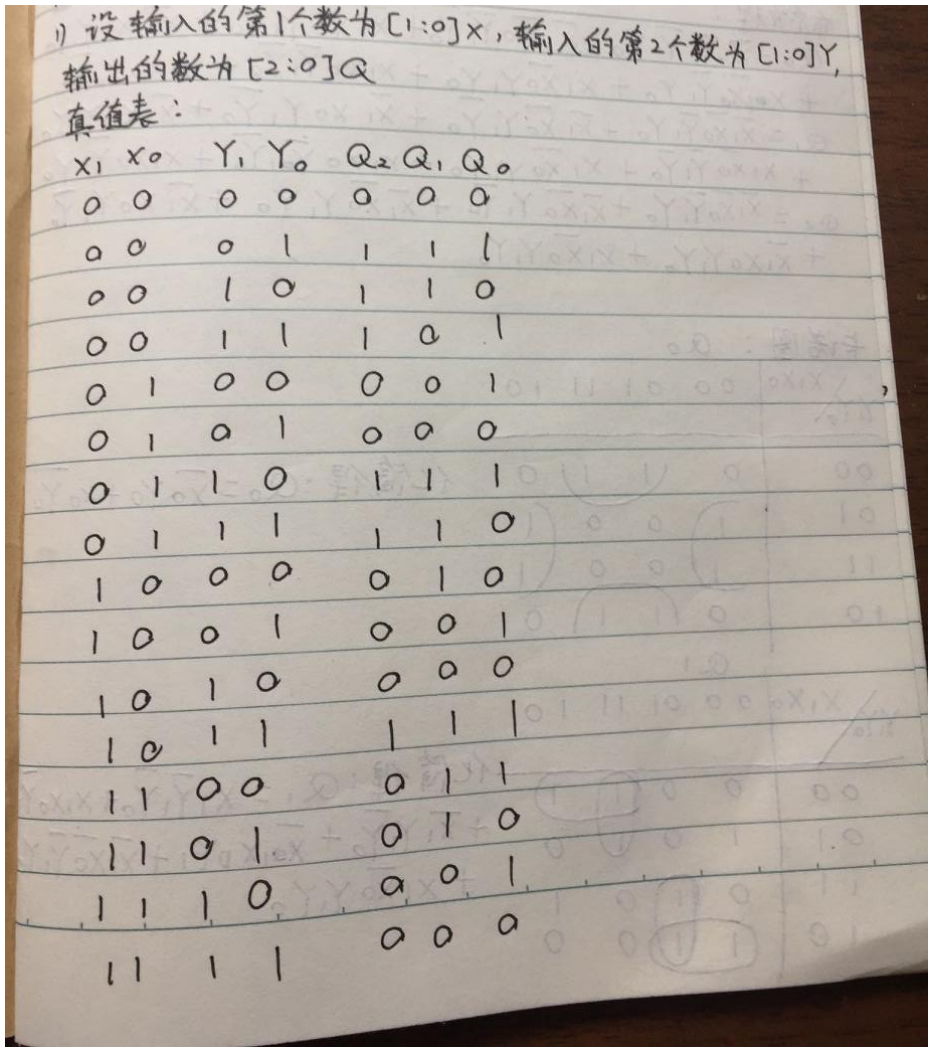
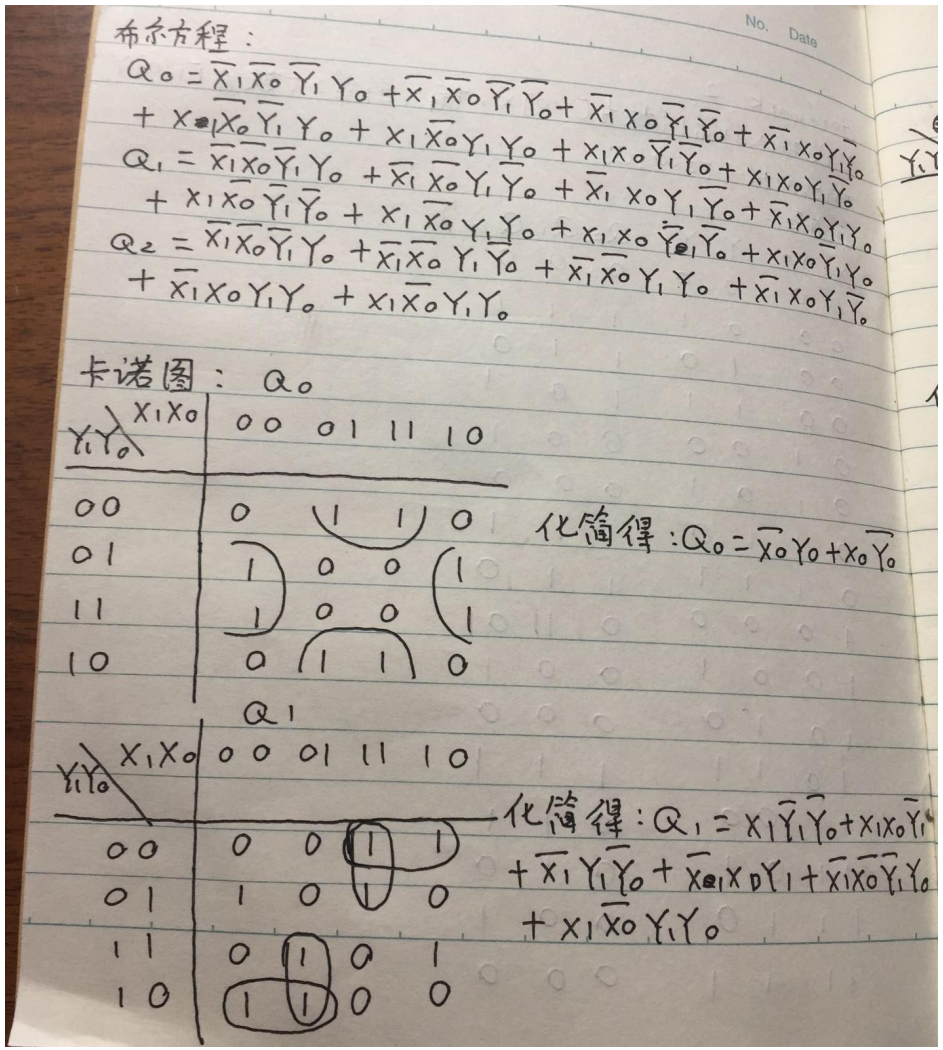
1) We want to design a circuit that input two 2-bit unsigned numbers, and output a 3-bit signed number that represents the difference between the two input numbers (i.e., it is the result of the first number minus the second number). Derive the truth table, write the Boolean equation in sum of products form, and simplifying it with Karnaugh Maps. Write the simplified Boolean equation. Draw the simplified circuit with only 2-input AND, 2-input OR and NOT gates.





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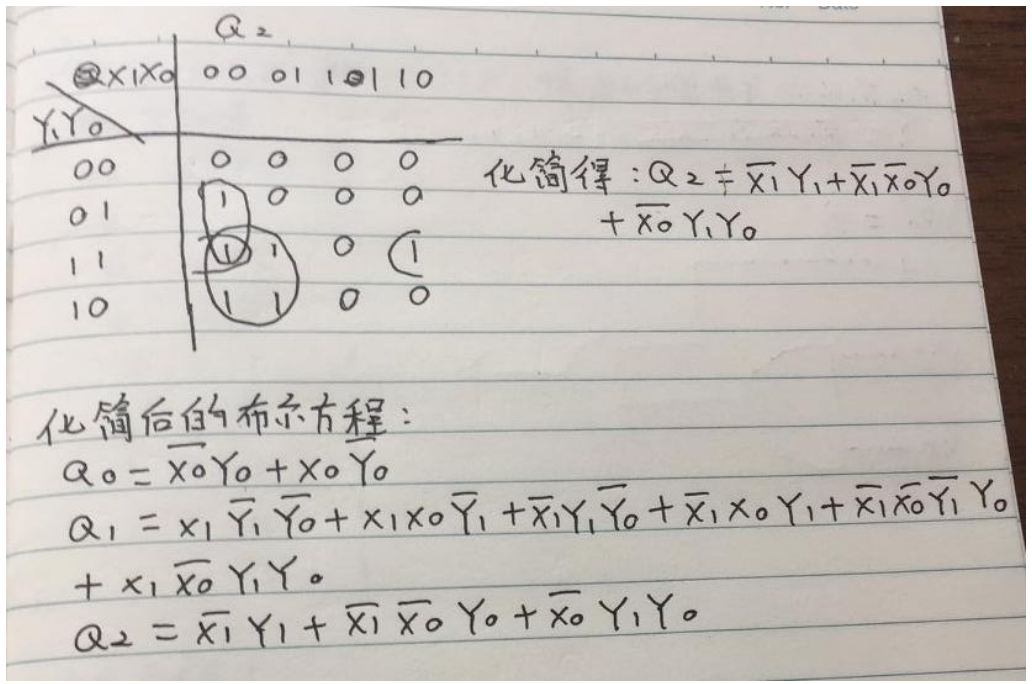
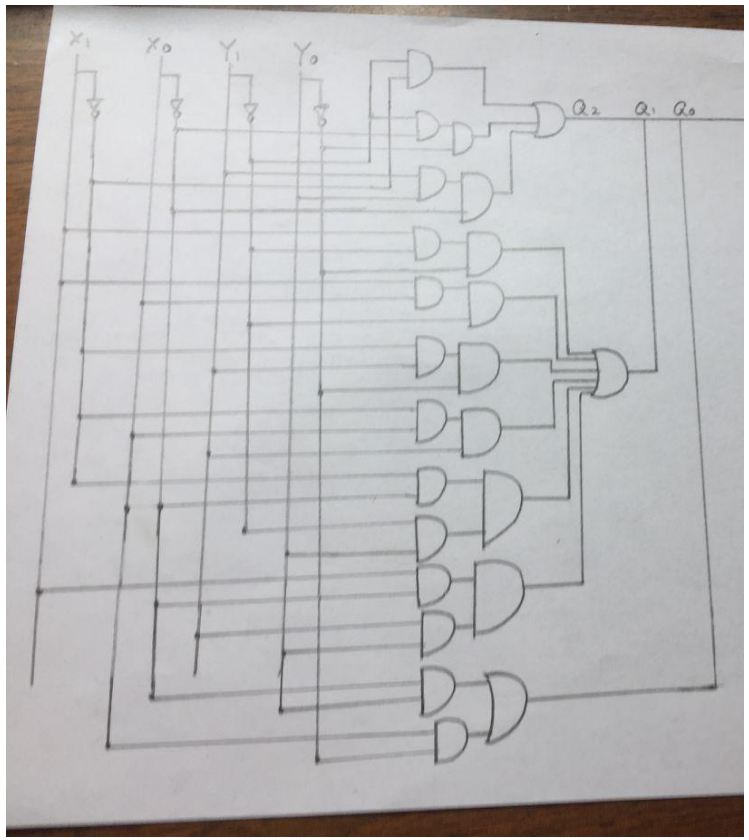




2) Design a circuit that input a 3-bit number. The circuit outputs a 1 if the input number is larger than or equal to 3. Otherwise, it output a 0.

a. Derive the truth table of the circuit, write the Boolean equation in sum of products form, and simplifying it with Karnaugh Maps. Write the simplified Boolean equation, and draw the simplified circuit with only 2-input AND, 2-input OR and NOT gates.

a.

设输入的数字为[2:0]X，输出的值为Y

真值表：

X_2	X_1	X_0	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

布尔方程：

$Y=\bar{X_2}X_1X_0+X_2\bar{X_1}\bar{X_0}+X_2\bar{X_1}X_0+X_2X_1\bar{X_0}+X_2X_1X_0$

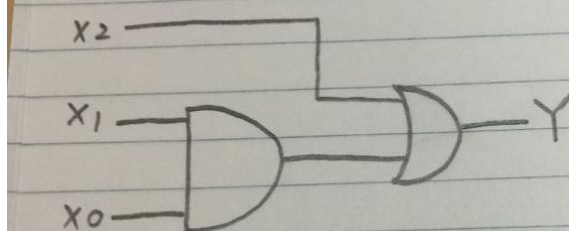
卡诺图：

X_0 \ X_2X_1	00	01	11	10
0	0	0	1	1
1	0	1	1	1

化简后的布尔方程：

$Y=X_2+X_1X_0$

电路图：



b. Write the Verilog module of the circuit with ① gate level description, ②Boolean equation description with Continuous Assignment, i.e. with "assign" statement, ③ behavior level description with "always" and "if-else" statement, ④behavior level description with "always " and "case" statement.

①使用门级电路

```
module comparer(
    input [2:0] X,
    output Y
    );
    wire out;
and i0(out,X[1],X[0]);
or i1(Y,out,X[2]);
endmodule
```

②使用 assign 语句

```
module comparer(
    input [2:0] X,
    output Y
    );
assign Y=X[2]|(X[1]&X[0]);
endmodule
```

③使用 always 语句和 if-else 语句

```
module comparer(
    input [2:0] X,
    output reg Y
    );
always@(*)  begin
if(X[2]|(X[1]&X[0])==1)
Y=1;
else
Y=0;  end
endmodule
```

④使用 always 语句和 case 语句

```
module comparer(
    input [2:0] X,
    output reg Y
    );
always@(*)  begin
case(X[2]|(X[1]&X[0]))
1'b1:Y=1;
1'b0:Y=0;  endcase
end
endmodule
```

3) We want to design a circuit that input 6-bit number. The circuit with output a 1 if the input number is larger than or equal to 27 (hint: $27_{(10)}=011011_{(2)}$). Write the verilog module of this circuit by using the verilog module of problem 2) and AND/OR/NOT gates in a Hierarchy form. Validate your design in your Basys3 board.

设计源代码：

```
module topcomparer(

input [5:0] X,

output Y

);

wire out1,out2,out3;

comparer c1(X[5:3],out1);

comparer c2(X[2:0],out2);

and(out3,out1,out2);

or(Y,out3,X[5]);

endmodule
```