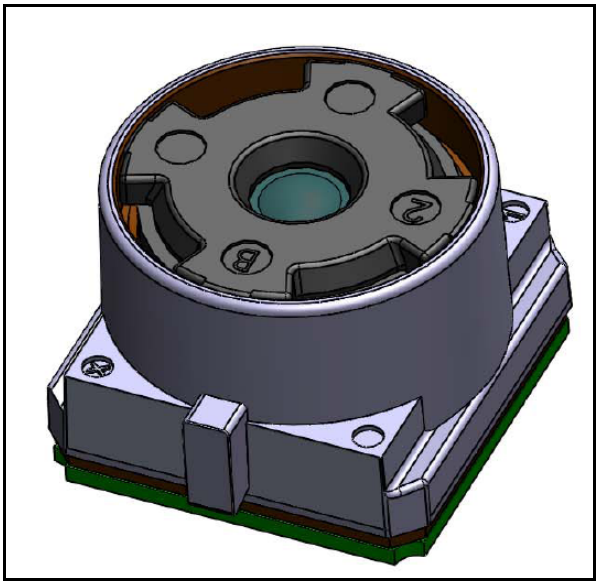
VX6953CB

5.1 megapixel EDOF camera module

Datasheet - production data



Features

- Extended depth of field (EDoF) technology
- Data formats: RAW8, RAW10 and 10-8 compressed
- SMIA profile 2 compliant
- MIPI CSI-2 (D-PHY v1.0 compliant) and SMIA CCP2 video data interface
- Maximum data rate: 640 Mbps for CCP2 and 800 Mbps for CSI-2
- 100 KHz to 400 KHz CCI command interface
- EMC shielding
- Ultra low power standby mode, 30 µW (typ.)
- Binning modes (2 x 2)
- HD video formats (1080p30, 720p30)
- Pixel defect correction
- Nine terms lens shading corrections, bi-cubic correction data available
- 512-byte NVM memory for calibration

Description

The VX6953CB camera module is designed for use across a range of mobile phone handsets and accessories. It embeds high quality still camera functions and also supports HD video.

The VX6953CB produces raw Bayer 5 Mpixel images at 15 fps in RAW10. It supports the CCI control as well as CCP 2.0 and CSI-2 data interfaces.

The module design is optimized for both footprint and height. It provides excellent image quality at focus distances from 15 cm in “Super macro mode” (bar code) and from 40 cm to infinity in “Normal mode”.

A separate hardware accelerator device (for example, an STV0987) can be integrated in the phone system to run the associated image processing algorithms in hardware where the baseband cannot support this processing load.

The sensor is designed to work with any other host with a MIPI or SMIA interface.

Contents

1 Overview 11

1.1 VX6953CB use in a system with a hardware coprocessor 12

1.2 VX6953CB use in a system with software image processing 13

1.3 Reference documents 14

2 Device pinout 15

3 Functional description 17

3.1 Analog video block 17

3.1.1 Block diagram 17

3.2 Digital video block 18

3.2.1 Dark calibration algorithm 18

3.3 Device operating modes 18

3.3.1 Power off 19

3.3.2 Hardware standby 19

3.3.3 Software standby 19

3.3.4 Streaming 19

3.4 Power management 19

3.4.1 Power-up procedure 20

3.4.2 Power-down procedure 23

3.4.3 Internal power-on reset (POR) 25

3.4.4 Failsafe signals 26

3.5 Clock and frame rate timing 26

3.5.1 Video frame rate control 26

3.5.2 PLL and clock input 26

3.5.3 Clock input type 27

3.6 Control and video interface formats 27

3.6.1 CCP serial data link 27

3.6.2 CSI-2 serial data link 28

3.6.3 CCI serial control bus 28

4 Register map 29

4.1 Status registers [0x0000 to 0x000F] 29

4.2 Frame format description registers [0x0040 to 0x007F] 30
4.3 Analog gain description registers [0x0080 to 0x0097] 31
4.4 Data format description registers [0x00C0 to 0x00FF] 32
4.5 Setup registers [0x0100 to 0x01FF] 32
4.6 Integration time and gain registers [0x0200 to 0x02FF] 34
4.7 Video timing registers [0x0300 to 0x03FF] 35
4.8 Image scaling registers [0x0400 to 0x04FF] 36
4.9 Image compression registers [0x0500 to 0x05FF] 37
4.10 Test pattern registers [0x0600 to 0x06FF] 37
4.11 Fifo water mark [0x0700 to 0x0701] 38
4.12 DPHY [0x0810 to 0x0811] 38
4.13 Binning [0x0900 to 0x0902] and [0x170C to 0x1719] 38
4.14 Shading correction [0x0B00] 39
4.15 Defect correction [0x0B05 to 0x0B09] 39
4.16 EDOF [0x0B80 to 0x0B8A] 40
4.17 Color feedback registers [0x0B8C to 0x0B95] 40
4.18 Integration time and gain parameter limit registers [0x1000 to 0x10FF] . 41
4.19 Video timing parameter limit registers [0x1100 to 0x11FF] 42
4.20 Image scaling parameter limit registers [0x1200 to 0x120B] 46
4.21 Image compression parameter registers [0x1300 to 0x13FF] 46
4.22 CSI lane mode capability [0x1600 to 0x1602] 46
4.23 Binning capability [0x1700 to 0x170B] 46
4.24 Manufacturer specific registers - Clipper 1 [0x31E8 to 0x31EB] 47

5 Video data interface 48
5.1 Frame format 48

6 Video timing 51
6.1 Output size 51
6.1.1 Programmable addressable region of the pixel array 51
6.1.2 Programmable width and height for output image data 52
6.1.3 Scaling 52
6.1.4 Subsampling 54
6.1.5 Binning 55

6.2 Video timing . . . 56
6.2.1 PLL block . . . 56
6.2.2 Spread spectrum clock generator . . . 57
6.2.3 Framerate . . . 58
6.2.4 Derating . . . 60
6.3 Bayer pattern . . . 62
6.4 Image compression . . . 64
6.5 Exposure and gain control . . . 64
6.5.1 Analogue gain model . . . 64
6.5.2 Digital gain . . . 66
6.5.3 Integration and gain parameter retiming . . . 66

7 Application . . . 67
7.1 Schematics . . . 67
7.2 Personality file and firmware updates . . . 68

8 EDOF control . . . 69
8.1 EDoF capabilities . . . 70
8.2 Control Interface . . . 71
8.3 EDOF control registers [0x0B80 to 0x0B8A] . . . 71
8.3.1 EDoF_Mode (0xB80) . . . 72
8.3.2 EDoF_est_focus_distance (0x0B82) . . . 73
8.3.3 EDoF tuning sliders (0xB83 to 0x0B85) . . . 73
8.3.4 EDoF focus distance (0x0B88) . . . 73
8.3.5 EDoF estimation control (0x0B8A) . . . 74
8.4 Supermacro mode . . . 74
8.5 Video modes and EDoF . . . 75
8.6 EDoF and white balance . . . 75

9 Image optimization . . . 77
9.1 Defect categorization . . . 78
9.1.1 Pixel defects . . . 78
9.1.2 Sensor array area definition . . . 78
9.1.3 Pixel fault numbering convention . . . 79
9.1.4 Single pixel faults . . . 79
9.1.5 Couplet definition . . . 80

9.1.6 Physical aberrations 80
9.2 Defect correction 82
9.3 Mapped couplet correction (Bruce) 84
9.4 Green imbalance correction 85
9.5 Lens shading correction 86

10 NVM contents 87
10.1 Green imbalance corrector 87
10.2 Lens shading gridiron correction 87
10.3 Sensitivity data 87
10.4 NVM map 88

11 EMC recommendations 89

12 Electrical characteristics 90
12.1 Operating conditions 90
12.2 Absolute maximum ratings 91
12.3 Power supply - VDIG, VANA 92
12.3.1 Power supply (peak current) - VDIG, VANA 92
12.3.2 Power supply ripple requirement 93
12.4 System clock - EXTCLK 94
12.5 Power down control - XSHUTDOWN 94
12.6 CCI interface - SDA, SCL 95
12.6.1 CCI interface - DC specification 95
12.6.2 CCI interface - timing characteristics 95
12.7 CCP interface 96
12.7.1 CCP interface - DC specification 96
12.7.2 CCP interface - timing characteristics 97
12.8 CSI-2 interface 98
12.8.1 CSI-2 interface - DC specification 98
12.8.2 CSI-2 interface - AC specification 98

13 Optical specification 99
13.1 Lens characteristics 99
13.2 Text, 1D and 2D codes reading 100

14 Mechanical 101
14.1 Packaging and delivery 101
14.2 Inner box labelling 102
14.3 Packing 102
14.4 Module outline 102

15 Ordering information 103

16 User precaution 104

17 Acronyms and abbreviations 105

18 Revision history 106

List of tables

Table 1. Technical specification . . . 11
Table 2. Reference documents . . . 14
Table 3. Pin descriptions . . . 15
Table 4. Power management matrix . . . 19
Table 5. Power-up sequence timing constraints for CCP2/CSI2 communications . . . 20
Table 6. Power-down sequence timing constraints for CSI2 communications . . . 23
Table 7. POR cell characteristics . . . 25
Table 8. System input clock frequency range . . . 26
Table 9. Status registers [0x0000 to 0x000F] . . . 29
Table 10. Frame format description registers [0x0040 to 0x007F] . . . 30
Table 11. Analog gain description [0x0080 to 0x0093] . . . 31
Table 12. Data format description registers [0x00C0 to 0x00FF] . . . 32
Table 13. Setup registers [0x0100 to 0x01FF] . . . 32
Table 14. Integration time and gain registers [0x0200 to 0x02FF] . . . 34
Table 15. Video timing registers [0x0300 to 0x03FF] . . . 35
Table 16. Image scaling registers [0x0400 to 0x04FF] . . . 36
Table 17. Image compression registers [0x0500 to 0x05FF] . . . 37
Table 18. Test pattern registers [0x0600 to 0x06FF] . . . 37
Table 19. Fifo water mark registers [0x0700 to 0x0701] . . . 38
Table 20. DPHY registers [0x0810 to 0x0811] . . . 38
Table 21. Binning registers [0x0900 to 0x0902] . . . 38
Table 22. Shading correction registers [0x0B00] . . . 39
Table 23. Defect correction registers [0x0B05 to 0x0B09] . . . 39
Table 24. EDOF registers [0x0B80 to 0x0B8A] . . . 40
Table 25. Color feedback registers [0x0B8C to 0x0B95] . . . 40
Table 26. Integration time and gain parameter limit registers [0x1000 to 0x10FF] . . . 41
Table 27. Video timing parameter limit registers [0x1100 to 0x11FF] . . . 42
Table 28. Image scaling parameter limit registers [0x1200 to 0x120B] . . . 46
Table 29. Image compression parameter limit registers [0x1300 to 0x13FF] . . . 46
Table 30. CSI lane mode capability registers [0x1600 - 0x1602] . . . 46
Table 31. Binning capability registers [0x1700 to 0x170B] . . . 46
Table 32. Manufacturer specific registers [0x31E8 to 0x31EB] . . . 47
Table 33. Binning register settings . . . 55
Table 34. External clock frequency examples - 5.0 Mpixel RAW10 14.5 fps (CSI-2) . . . 58
Table 35. External clock frequency examples - 5.0 Mpixel RAW10 15 fps (CSI-2) . . . 58
Table 36. External clock frequency examples - 5.0 Mpixel 10-8 compressed 15 fps . . . 59
Table 37. Example - 5.0 Mpixel 10-8 compressed 16.65 fps (CSI-2) . . . 59
Table 38. External clock frequency examples - 1080x1920 in 10-8 bit @ 30fps (CCP) . . . 59
Table 39. 720x1280 @ 30 fps in RAW10 (CSI2/CCP2) . . . 60
Table 40. Analog gain control . . . 65
Table 41. EDOF registers [0x0B80 to 0x0B8A] . . . 71
Table 42. Color feedback registers [0x0B8C to 0x0B95] . . . 75
Table 43. Operating conditions . . . 90
Table 44. Absolute maximum ratings . . . 91
Table 45. Power supplies VDIG, VANA . . . 92
Table 46. In-rush current VDIG, VANA for CCP2 interface . . . 92
Table 47. In-rush current VDIG, VANA for CSI-2 interface . . . 93
Table 48. Ripple requirement . . . 93

Table 49. System clock - EXTCLK . . . 94
Table 50. Power down control - XSHUTDOWN . . . 94
Table 51. CCI interface . . . 95
Table 52. CCI interface - timing characteristics . . . 95
Table 53. CCP interface - DC specification . . . 96
Table 54. CCP interface - timing characteristics . . . 97
Table 55. CSI-2 interface - high speed mode - DC specification . . . 98
Table 56. CSI-2 interface - low power mode - DC specification . . . 98
Table 57. CSI-2 interface - high speed mode - AC specification . . . 98
Table 58. CSI-2 interface - low power mode - AC specification . . . 98
Table 59. Typical lens design characteristics for first source lens supplier . . . 99
Table 60. QR code (2D)resolution reading capability . . . 100
Table 61. Substrate marking codification . . . 101
Table 62. Outline drawing information . . . 102
Table 63. Device summary . . . 103
Table 64. Acronyms and abbreviations . . . 105
Table 65. Document revision history . . . 106

List of figures

Figure 1. VX6953CB in system with processor . . . 12
Figure 2. VX6953CB in a system with software image processing . . . 13
Figure 3. VX6953CB module pinout (viewed from bottom of camera module) . . . 15
Figure 4. Overview of analog video block . . . 17
Figure 5. System state diagram . . . 18
Figure 6. VX6953CB power-up sequence for CCP2 mode . . . 21
Figure 7. VX6953CB power-up sequence for CSI-2 mode . . . 22
Figure 8. VX6953CB power-down sequence for CSI-2 mode . . . 24
Figure 9. POR timing . . . 25
Figure 10. Clock input types . . . 27
Figure 11. CSI serial data link . . . 28
Figure 12. VX6953CB CCP frame format . . . 49
Figure 13. VX6953CB CSI-2 frame format . . . 49
Figure 14. Programmable addressable region of the pixel array . . . 51
Figure 15. Output size within a CCP data frame . . . 52
Figure 16. Scaling modes . . . 53
Figure 17. Scaler quality . . . 53
Figure 18. Example image full scaled by a downscale factor of 2 . . . 54
Figure 19. Subsample readout example . . . 55
Figure 20. Binning repair . . . 56
Figure 21. VX6953CB clock relationships . . . 57
Figure 22. Timing block diagram . . . 60
Figure 23. SMIA output timing . . . 61
Figure 24. FIFO water mark control . . . 61
Figure 25. Bayer pattern . . . 63
Figure 26. Analogue gain register format . . . 65
Figure 27. Example of a mobile camera application (CCP2) . . . 67
Figure 28. Example of a mobile camera application (CSI2) . . . 68
Figure 29. What is sharp? . . . 69
Figure 30. EDoF main principle . . . 70
Figure 31. Focus strategy weightings . . . 74
Figure 32. Processing pipe . . . 77
Figure 33. VX6953CB pixel defect test area . . . 78
Figure 34. Pixel numbering notation . . . 79
Figure 35. Single pixel fault . . . 79
Figure 36. General couplet example . . . 80
Figure 37. Test region definition . . . 80
Figure 38. Scan array for blemish . . . 81
Figure 39. Fail map . . . 81
Figure 40. Contiguous pixel example . . . 82
Figure 41. Image showing defective pixels . . . 82
Figure 42. Block diagram of dynamic defect correction block . . . 83
Figure 43. Dynamic defect correction output example . . . 83
Figure 44. Corrected Bayer pattern . . . 84
Figure 45. Green imbalance correction plots . . . 85
Figure 46. Lens shading images . . . 86
Figure 47. CCI AC characteristics . . . 96
Figure 48. SubLVDS AC timing . . . 97

Figure 49. Barcode and QR code examples 100
Figure 50. Marking diagram 101

1 Overview

The VX6953CB image sensor produces raw 5.0 Mpixel digital video data at up to 16.5 frames per second.

The VX6953CB has both CCP2.0 and MIPI CSI-2 video data interfaces selectable over the camera control interface (CCI). The VX6953CB is compliant with the SMIA 1.0[a] Specification Profile 2. The VX6953CB can also be used as a Profile 0 or Profile 1 device. The sensor supports full horizontal and vertical scaling and output frequency derating as defined in the specification. The VX6953CB supports 2 x 2 binning mode which supports 720p30 video format.

The image data is digitized using an internal 10-bit column ADC. The resulting pixel data is output as 8-bit, 10-bit or 10-8 bit compressed data and includes checksums and embedded codes for synchronization. The interface conforms to both the CCP 2.0 and MIPI CSI-2 interface standards. The sensor is fully configurable through a CCI serial interface.

The module is available in a SMOP type package measuring 6.5 x 6.5 x 4.6 mm. It is designed to be used with a board mounted SMIA65 socket or flex.

Table 1. Technical specification

Feature	Detail
Optical format	1/4"
Pixel resolution	2608 x 1960 (5.0 megapixel)
Sensor technology	IMG140 STs 65nm based CMOS Imaging Process
Pixel size	1.4 µm x 1.4 µm
Exposure control	+ 81 dB
Analogue gain	+ 24 dB (max)
Digital gain	+ 3 dB (max)
Dynamic range	63 dB
Signal to noise	36 dB (@ 100 lux)
Supply voltages	Analog: 2.3V to 2.9V (2.8V nom.) Digital: 1.7V to 1.9V (1.8V nom.)
Power consumption	<300 mW
Package size (L x H x W)	6.5 x 6.5 x 4.6 mm (without lens cover)
Lens	58° +/-2° HFOV F/2.8
Relative illumination	75 % (typ.)
System attach	SMIA65 socket or flex
Temperature range	Normal operating: -25C to +55C Storage: -40C to +85C

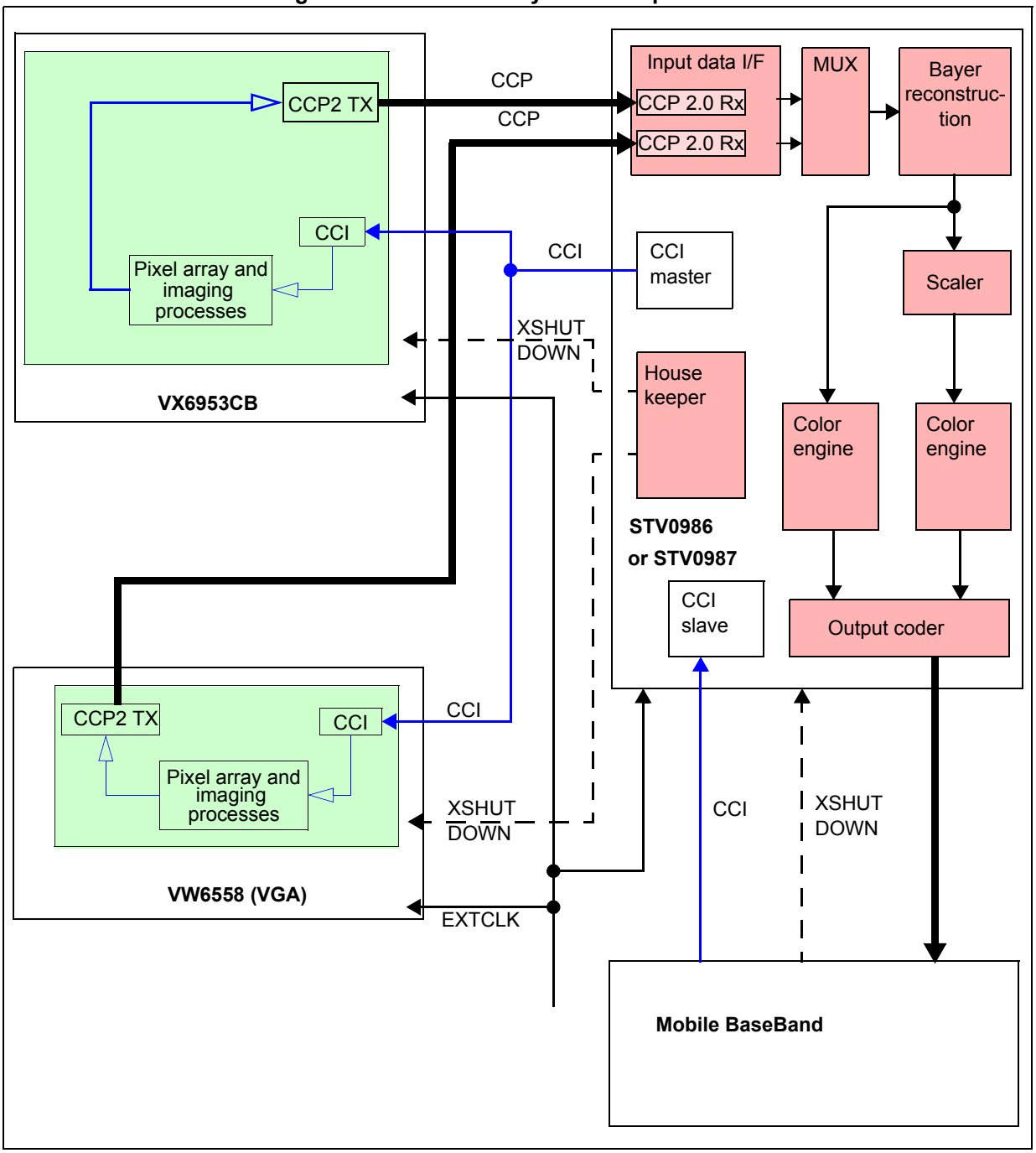
a. Including up to ECR0002.

1.1 VX6953CB use in a system with a hardware coprocessor

The VX6953CB is an image sensor and it can be paired with either STV0986 or STV0987 STMicroelectronics companion processor. The coprocessor and the sensor together form a complete imaging system.

Figure 1 illustrates a typical system using VX6953CB, a coprocessor and a secondary camera VW6558 (CIF + camera for video conferencing).

Figure 1. VX6953CB in system with processor



The sensor main function is to convert the viewed scene into a data stream. The companion processor function is to manage the sensor so that it can produce the best possible pictures and to process the data stream into a form which is easily handled by up-stream mobile baseband or multi-media processor (MMP) chipsets.

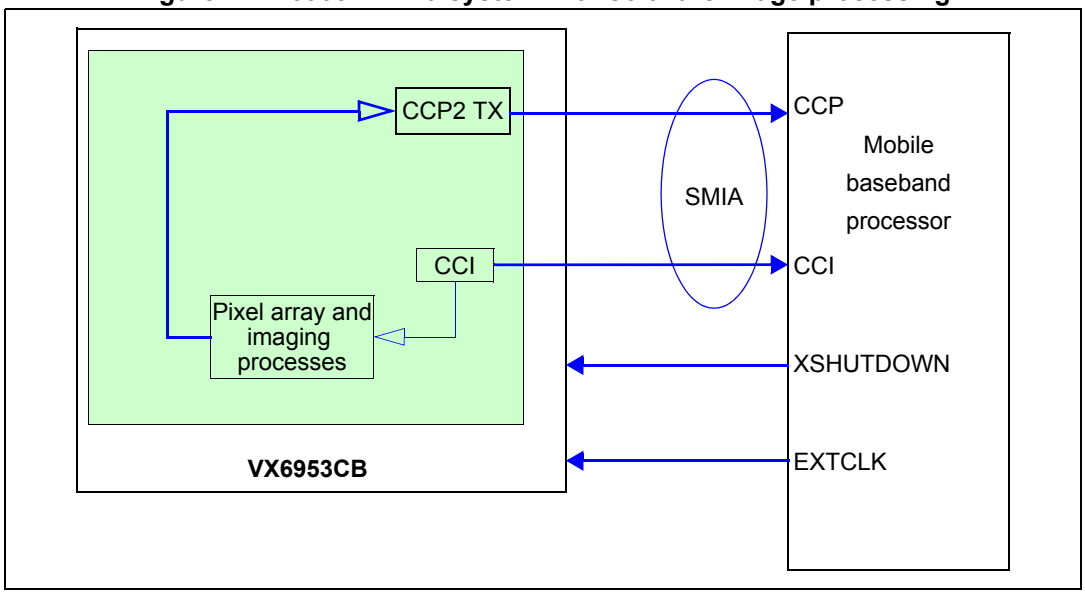
The sensor supplies high-speed clock signals to the processor and provides the embedded control sequences which allow the coprocessor to synchronize with the frame and line level timings. The processor then performs the color processing on the raw image data from the sensor before supplying the final image data to the host.

With the coprocessor system, the clock is sent by host to both the VX6953CB and the coprocessor. The high-speed clock for the coprocessor is supplied from the VX6953CB. It is generated using the VX6953CB PLL and is provided as the continuous data qualification clock.

1.2 VX6953CB use in a system with software image processing

The VX6953CB image sensor can be directly connected to a baseband or multimedia processor. No dedicated coprocessor is used in this configuration. The image processing is done in software or hardware within the baseband processor.

Figure 2. VX6953CB in a system with software image processing



Systems with a CCP 2.0 interface can operate with this device, however they may have a maximum CCP link speed of 650 Mbps and therefore will not be able to achieve 15 fps with this device.

Systems with CSI-2 interface (MIPI) can operate with this sensor. With a 800 Mbps CSI-2 link speed, they can achieve 15 fps in full size image.

1.3 Reference documents

Table 2. Reference documents

Title	Date
SMIA 1.0 Functional Specification	30/06/2004
SMIA 1.0 Characterization Specification Rev A	10/03/2005
SMIA 1.0 CCP2 Specification	30/06/2004
SMIA 1.0 Mechanical Specification	30/06/2004
SMIA 1.0 Functional Specification ECR0001 ver 1	11/02/2005
SMIA 1.0 CCP2 Specification ECR0002 version 1.0	11/02/2005
MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) v1.0	Nov 2005
MIPI Alliance D-PHY Specification (v00-90-00)	Oct 2007

2 Device pinout

Figure 3 provides the pin positions and *Table 3* provides the signal descriptions.

Figure 3. VX6953CB module pinout (viewed from bottom of camera module)

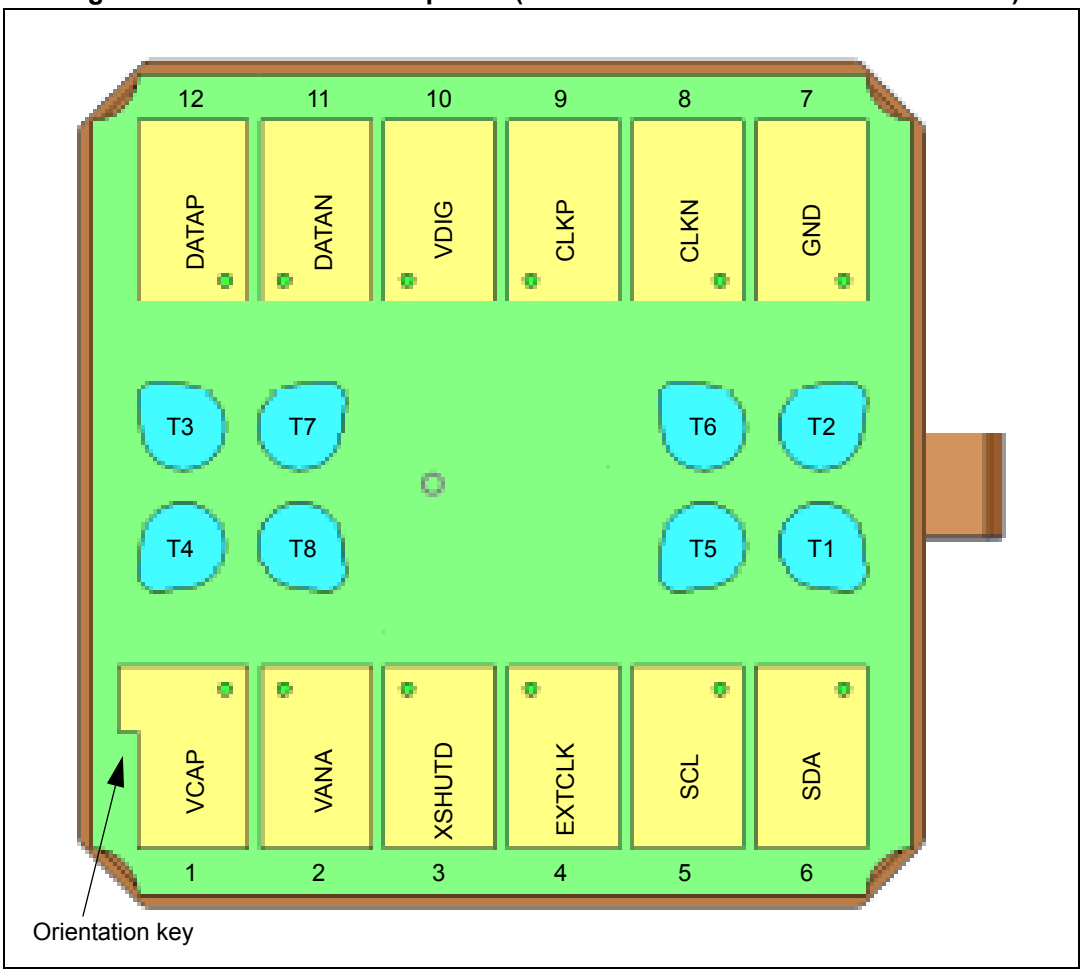


Table 3. Pin descriptions

Pad number	Pad name	I/O type	Description
Power supplies			
1	VCAP	PWR	No connection required(1)
7	GND	PWR	Ground (combined)
2	VANA	PWR	Analog power supply (typically 2.8V)
10	VDIG	PWR	Digital power supply (typically 1.8V)
System			
3	XSHUTDOWN	I	Power down control(2)
4	EXTCLK	I	System clock input (6 MHz to 27 MHz) (3)

Table 3. Pin descriptions (continued)

Pad number	Pad name	I/O type	Description
Control			
5	SCL	I	Serial communication clock
6	SDA	I/O	Serial communication data
Data			
8	CLK-	SubLVDS output	Output qualifying clock
9	CLK+	SubLVDS output	Output qualifying clock
11	DATA-	SubLVDS output	Serial output data
12	DATA+	SubLVDS output	Serial output data
ST test			
T1 to T8		ST test pins	Do not connect(4)

1. VCAP is internal to the module.
2. Signal is active low.
3. The EXTCLK pad has a Schmitt trigger input.
4. Test pins are not floating.

3 Functional description

This chapter details the main blocks in the device:

- analog video block, see *Section 3.1*
- digital video block, see *Section 3.2*
- power management, see *Section 3.4 on page 19*

This chapter also describes:

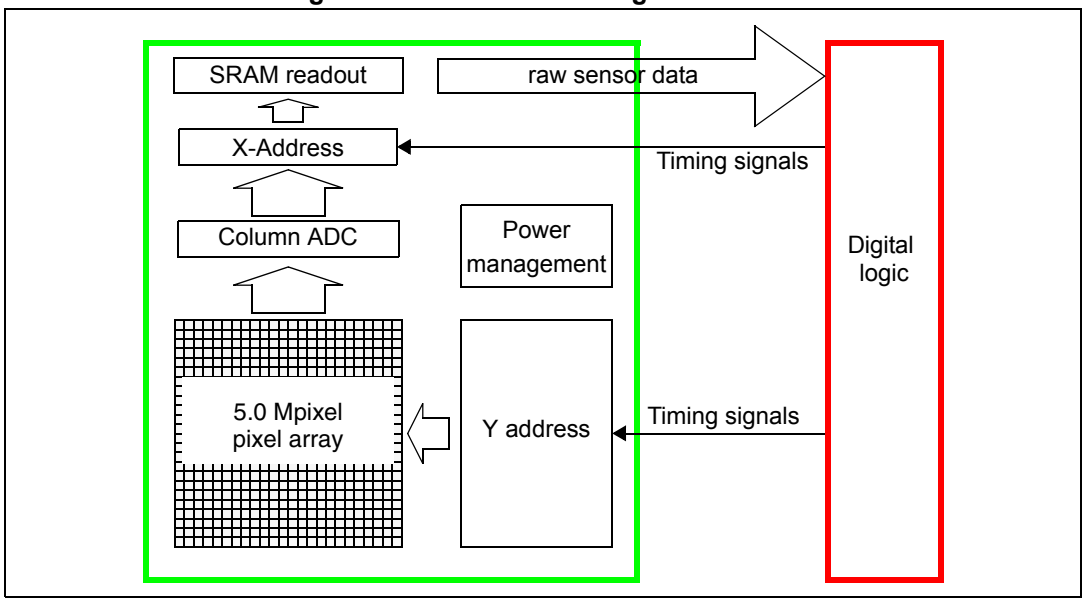
- the device's operating modes, *Section 3.3 on page 18*
- clock and frame rate control, see *Section 3.5 on page 26*
- control and video interface formats, see *Section 3.6 on page 27*

3.1 Analog video block

3.1.1 Block diagram

The analog video block, shown in *Figure 4*, consists of a 5.0 Mpixel resolution pixel array, power management circuitry. The digital block provides all timing signals to drive the analog block.

Figure 4. Overview of analog video block



Pixel voltage values are read out and digitized using the address decoders and column ADC.

3.2 Digital video block

The main features of the digital video block are:

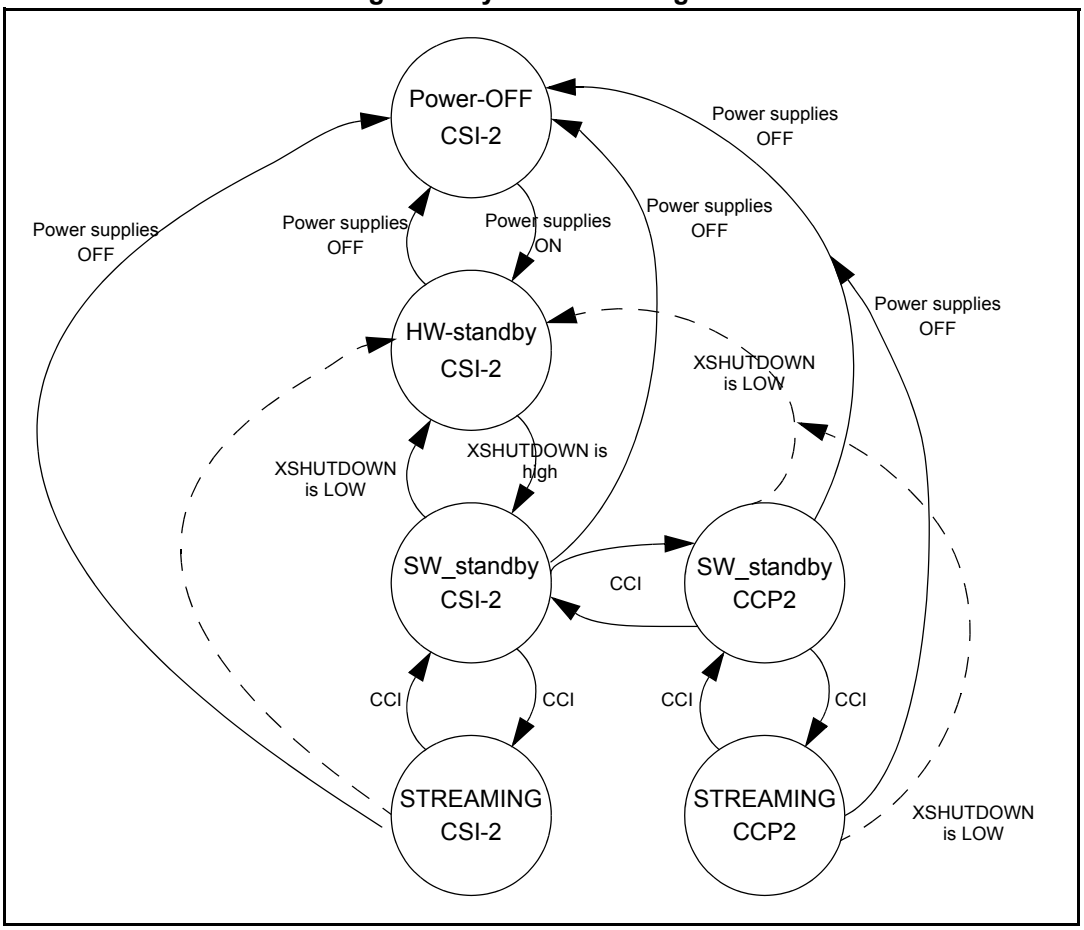
- frame rate: 16.65 frame/s maximum can be reduced down to less than 3 frame/s (5.0 Mpixel) using frame extension
- automatic dark calibration to ensure consistent video level over varying scenes
- on-chip power-on-reset cell
- output format: 5.0 Mpixel 2608 x 1960 (maximum)

3.2.1 Dark calibration algorithm

The VX6953CB runs a dark calibration algorithm on the raw image data to control the video offsets caused by dark current. This ensures that a high quality image is output over a range of operating conditions. The first frame dark level is correctly calibrated, for subsequent frames the adjustment of the dark level is damped by a leaky integrator function to avoid possible frame to frame flicker.

3.3 Device operating modes

Figure 5. System state diagram



3.3.1 Power off

Power supplies are off.

3.3.2 Hardware standby

This is the lowest power consumption mode. CCI communications are not supported in this mode. The clock input pad, PLL and the video blocks are powered down. This state is entered by pulling the control pin XSHUTDOWN down. All registers are returned to their default values.

3.3.3 Software standby

Software standby mode preserves the contents of the CCI register map. CCI communications are supported in this mode. The software standby mode is selected using a serial interface command. If this state is entered from hardware standby, the data pads remain high impedance. If this state is entered from streaming, then the data pads go high impedance at the end of the current frame. At this point, the video block and PLL power down. The internal video timing is reset to the start of a video frame in preparation for the enabling of active video. The values of the serial interface registers like exposure and gain are preserved. The system clock must remain active when communicating with the sensor.

This state is entered by releasing the device from hard reset by: setting XSHUTDOWN high, writing 0x00 to the mode control register (0x0100) or commanding a soft reset by writing 0x01 to the software reset register (0x0103). After a soft reset or the transition of XSHUTDOWN to high, all registers are returned to their default values.

3.3.4 Streaming

The VX6953CB streams live video. This mode is entered by writing 0x01 to the mode control register (0x0100).

3.4 Power management

VX6953CB requires a dual power supply. The analog circuits are powered by a nominal 2.8V supply while the digital logic and digital I/O are powered by a 1.8V supply. Different sections of the sensor are powered depending on the system state. See *Table 4* for details.

Table 4. Power management matrix

Mode	Functional block powered down					Video data inhibit
	CCI	Digital	Internal and output clocks(1)	Output pins	Analog	
Hardware standby	Yes	Yes	Yes	Yes	Yes	Yes
Software standby	No	Yes	Yes	Yes	Yes	Yes
Streaming	No	No	No	No	No	No

1. PLL block and data CLK+ and CLK- pins

3.4.1 Power-up procedure

The digital and analog supply voltages can be powered up in any order for example, VDIG then VANA or VANA then VDIG. See *Table 5* for timing constraints.

On power-up the on-chip power-on reset cell ensures that the CCI register values are initialized correctly to their default values.

The EXTCLK clock can either be initially low and then enabled during software standby mode or EXTCLK can be a free running clock.

Table 5. Power-up sequence timing constraints for CCP2/CSI2 communications

Symbol	Parameter	Min.	Max.	Units
t0	VANA rising – VDIG rising	VANA and VDIG may rise in any order The rising separation can vary from 0 ns to indefinite		ns
t1	VDIG rising – VANA rising			ms
t2	VANA/VDIG – XSHUTDOWN rising	XSHUTDOWN must rise coincident with, or later than, both power supplies (VDIG and VANA)		us
t3	XSHUTDOWN – first I^2C transaction with free running clock	5(1)	-	ms
t4	Minimum period with EXTCLK present prior to the first I^2C transaction. Gated clock.	5(2)	-	ms
t5	PLL start up/lock time	-	1	ms
t6	Entering streaming mode – first frame start sequence (fixed part)	-	10	ms
t7	Entering streaming mode – first frame start sequence (variable part) = Integration time	fine_integration_time_min	-	ms

1. 5 ms is necessary to upload the NVM data into firmware registers and get the FW ready for sensor initialization through I^2C writes.
2. For gated clock.

Figure 6. VX6953CB power-up sequence for CCP2 mode

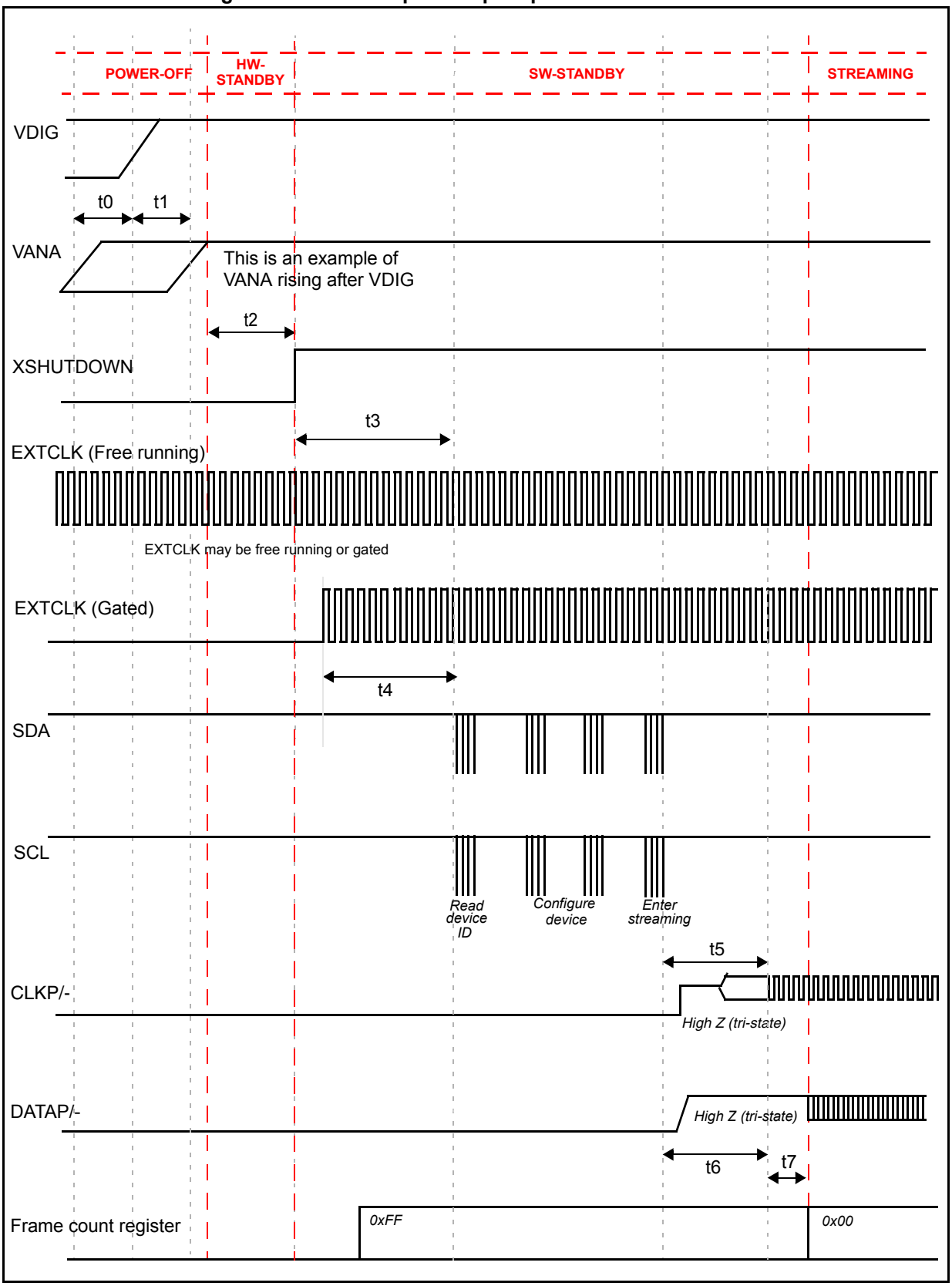
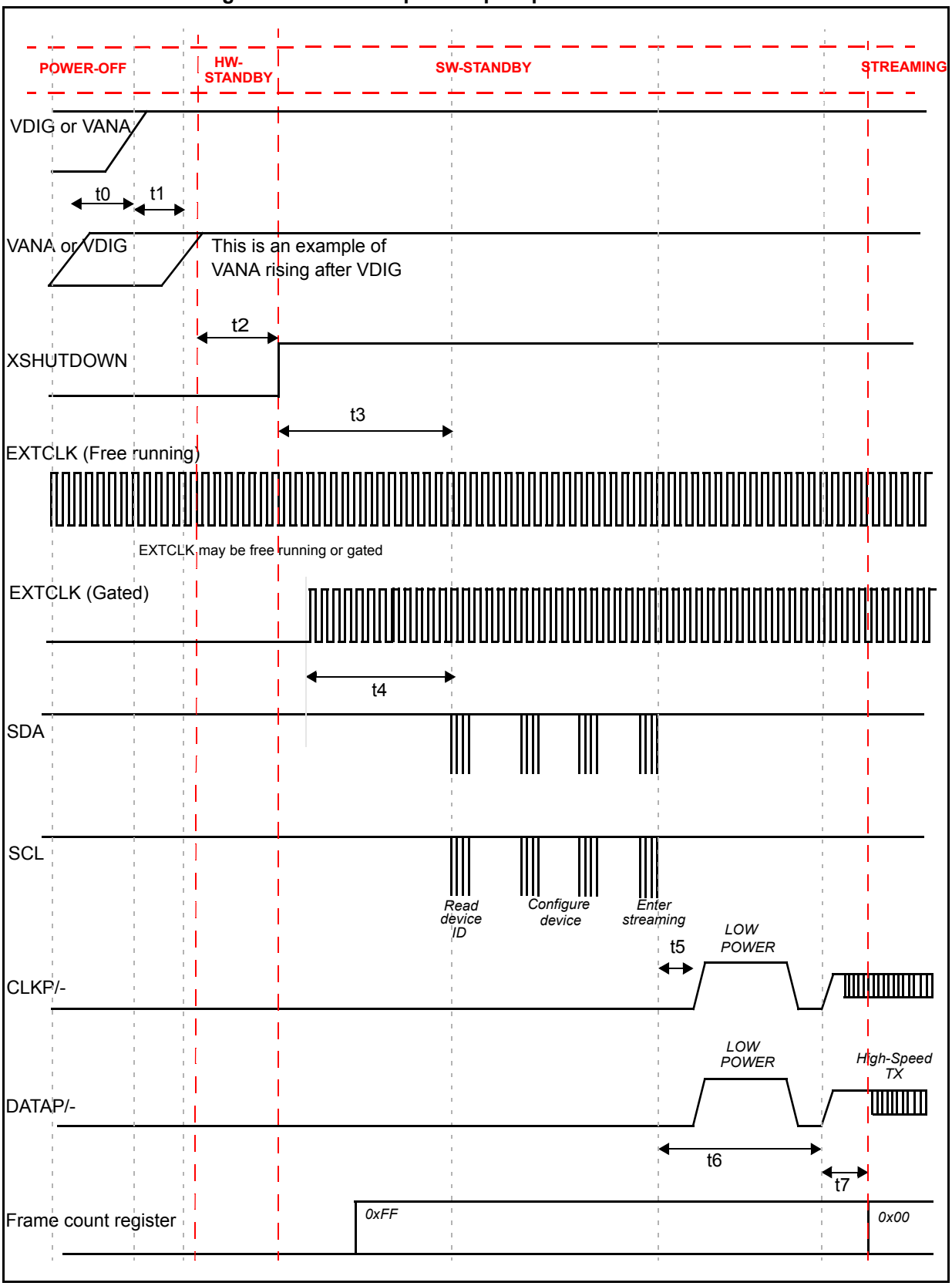


Figure 7. VX6953CB power-up sequence for CSI-2 mode



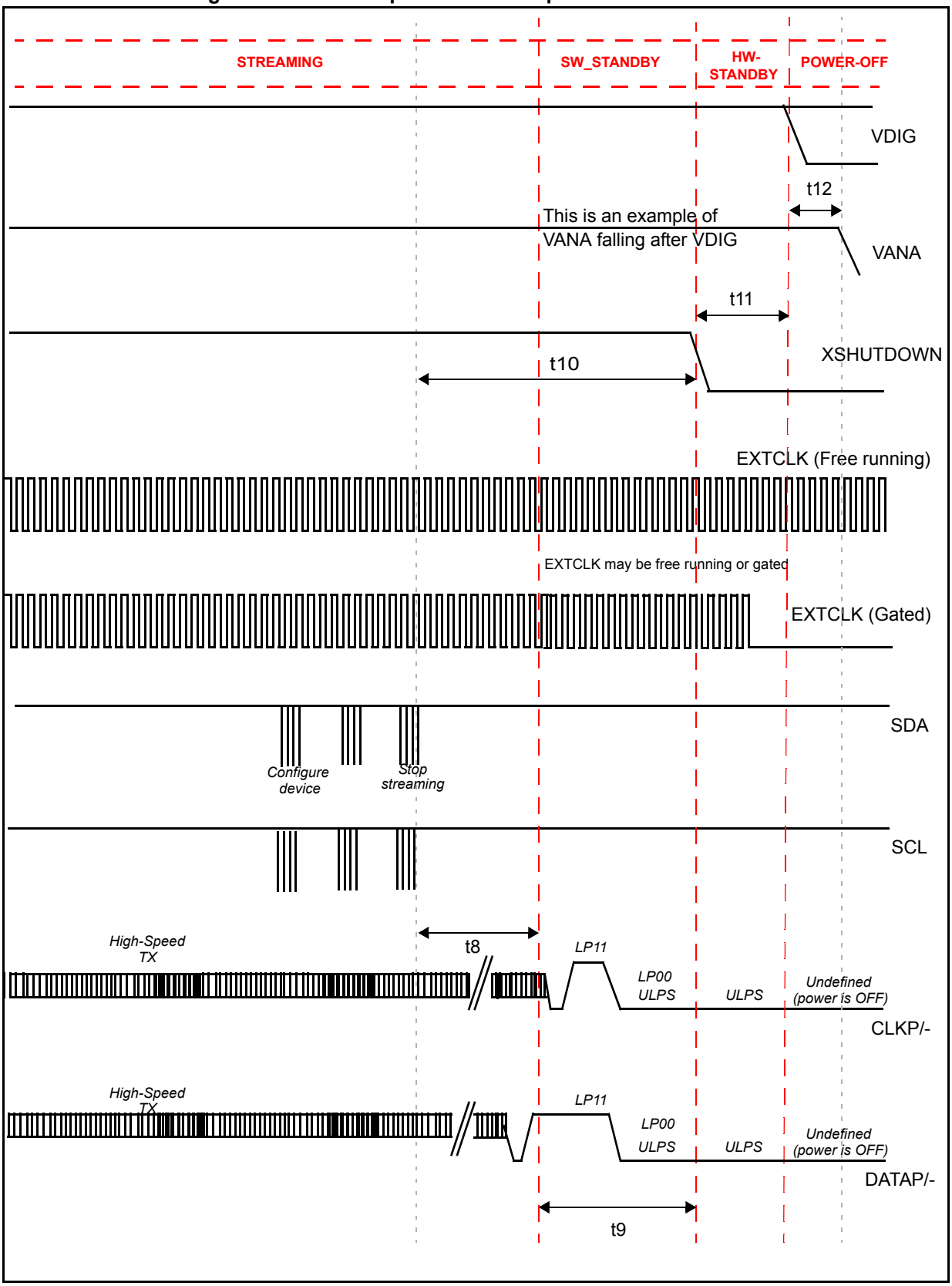
3.4.2 Power-down procedure

Table 6. Power-down sequence timing constraints for CSI2 communications

Symbol	Parameter	Min.	Max.	Units
t8	Last I^2C transaction to MIPI frame end(1)	-	1 frame	
t9	Minimum EXTCLK cycles required after last I^2C transaction or MIPI frame end(2)	512	-	clock cycles
t10	Last I^2C transaction or MIPI frame end to XSHUTDOWN failling(3)	t8+t9	-	
t11	XSHUTDOWN to VANA/VDIG falling	XSHUTDOWN must fall at the same time as, or earlier than, both power supplies (VDIG and VANA)		
t12	VANA to VDIG or VDIG to VANA falling	VANA and VDIG may fall in any order, the rising separation can vary from 0 ns to indefinite		

1. The whole power down sequence is triggered by the CCI power down request, however the power down sequence will only start after the end of the frame when all active data are consumed on CSI-2 DN/DP pins. When this is done, the CSI-2 DN/DP signals enter LP11. The CSI-2 clock will enter LP11 with a delay of 5us (corresponding to Tclk_post + Tclk_trail) compared to DN/DP pins. The device is then SW_STANDBY and will enter LP00 and stay in Ultra Low power mode.
2. After the last frame completion, the gated clock needs to be kept for 512 cycles at least so the system can enter Ultra Low power state. After the system enters ULPS mode, you can keep or stop the EXTCLK.
3. Note: XSHUTDOWN can be asserted at any time. This immediately removes the core-supply, causing the POR to trigger and reset all the digital logic and macros - it does not depend on the presence of the clock. When XSHUTDOWN is asserted, the clock can be running or not - it does not matter.

Figure 8. VX6953CB power-down sequence for CSI-2 mode



3.4.3 Internal power-on reset (POR)

The VX6953CB internally performs a power-on reset (POR) when the 1V2 Vcore digital supply rises through the trigger level, Vtrig_rising. Similarly, if the 1V2 Vcore digital power supply falls through the trigger level, Vtrig_falling, then the power-on reset will also trigger.

Definitions

Rise threshold voltage (VTRIGR) is the supply voltage level that is recognised by the POR as voltage “HIGH”. Only after the supply reaches this level does the output of POR change to high level if it is off, after a specified amount of delay.

Fall threshold voltage (VTRIGF) is the supply voltage level that is recognised by the POR as voltage “LOW”. Only after the supply reaches this level does the output of POR change to low (ground) level if it is on.

Burst width (pw). Burst is the negative pulse riding the supply signal. The burst width is measured as the amount of duration for which the supply signal dropped beyond the threshold levels.

Delay duration (TPOR) is defined as the time duration for which POR stays off before repowering. Each reset of POR will impart a specified delay duration before POR repowers.

Figure 9. POR timing

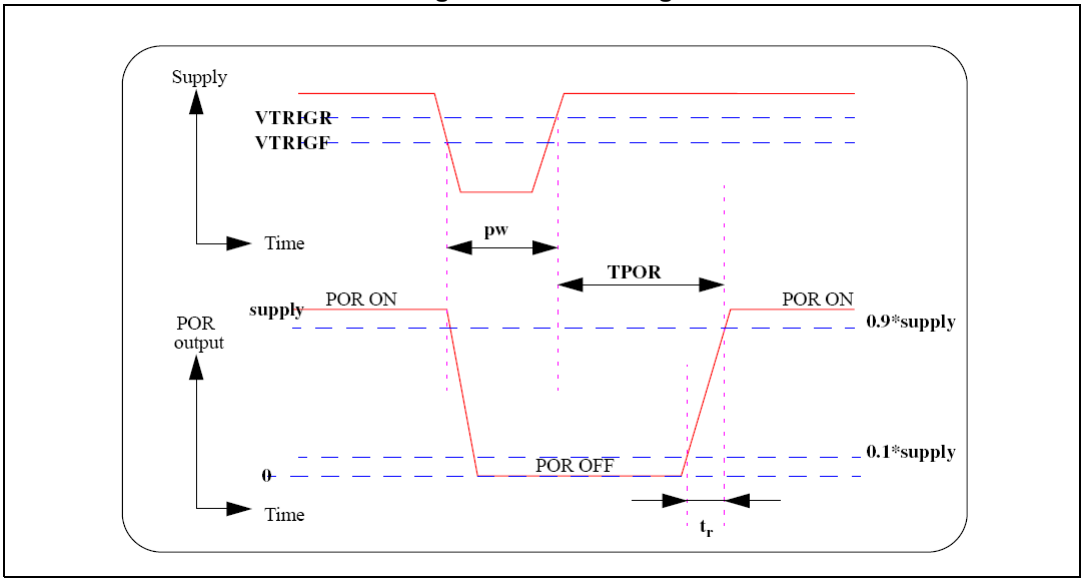


Table 7. POR cell characteristics

Symbol	Constraint	Min	Typ.	Max	Units
VTRIGR	POR rise voltage detection	-	-	0.95	V
VTRIGF	POR fall voltage detection	0.4	-	-	V
Tburst (pw)	Burst filter	-	2	8	µs
Tpor	Delay duration	-	20	45	µs

3.4.4 Failsafe signals

All signals going into the VX6953CB must be at either a low state or a high impedance when power is removed from the device. The exceptions to this rule are the EXTCLK, XSHUTDOWN and the CCI signals. These pads have been designed to be high impedance when the VX6953CB is powered-down. This means that the input signal on the specified pads can either be high or low with no leakage problems.

3.5 Clock and frame rate timing

3.5.1 Video frame rate control

The output frame rate of VX6953CB can be reduced by extending either the line length or the frame length. The extension is achieved by adding extra blanking bytes at the end of a line or ‘blank’ video lines to act as timing padding. The frame rate can be reduced from the default 15 frame/s at 5.0 Mpixel resolution to less than 3 frame/s at 5.0 Mpixel resolution.

The advantage of the frame extension approach is that it does not reduce the pixel readout rate or the active frame time and therefore does not introduce unwanted motion distortion effects to the image.

3.5.2 PLL and clock input

The VX6953CB has an embedded PLL block. This block generates all necessary internal clocks from an input range defined in *Table 8*. The input clock pad accepts up to 27 MHz signals. The input clock can be a sine wave or square wave.

Table 8. System input clock frequency range

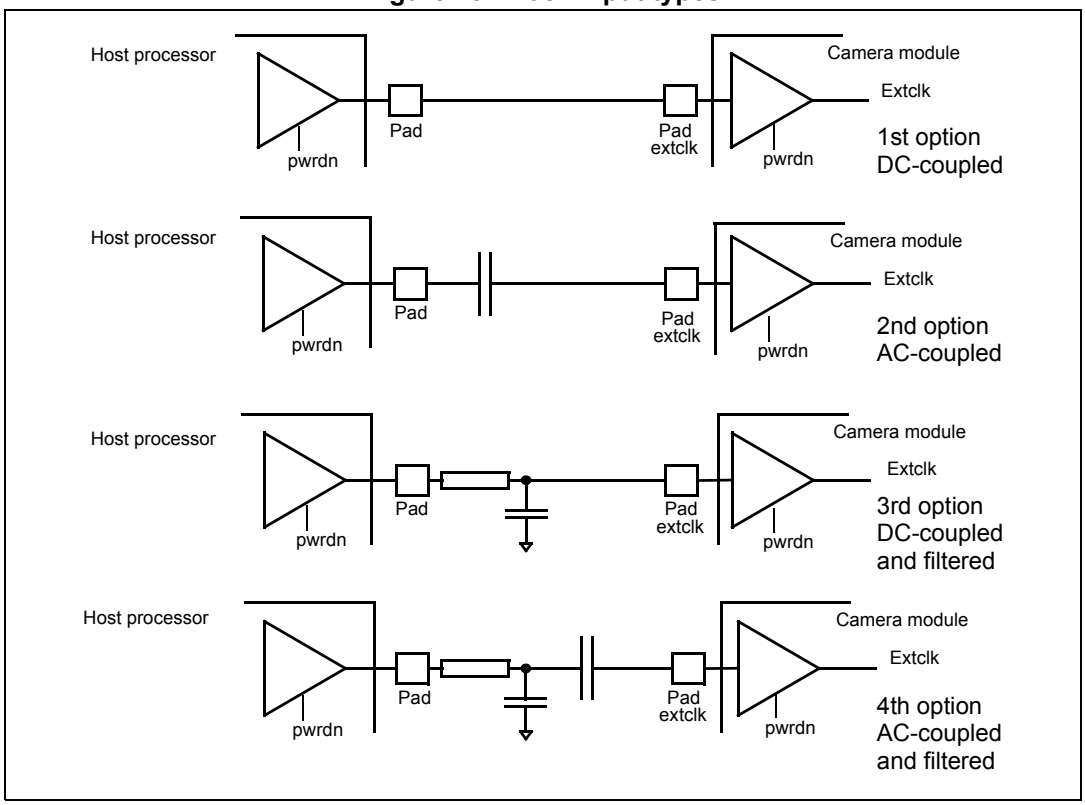
Min. (MHz)	Max. (MHz)
6	27

3.5.3 Clock input type

As required by the SMIA specification the VX6953CB can receive the clock types shown in *Figure 10*.

The clock is fail-safe/high impedance when in either AC or DC coupled and in any mode including the power off state. The pad has a SCHMITT TRIGGER input.

Figure 10. Clock input types



3.6 Control and video interface formats

Image data is transferred from the VX6953CB using a high speed subLVDS serial link.The serial control data is transferred to and from the VX6953CB on a CCI bus.

- Video maximum link speeed: 640 Mbps for CCP2 and 800 Mbps for CSI-2.
- CCI command speed: from 100 KHz to 400 KHz.

3.6.1 CCP serial data link

Data signals (DATA+ and DATA-) and clock signals (CLK+ and CLK-) are transferred from VX6953CB on two pairs of balanced 100 Ω impedance transmission lines.

The transmission line pairs and custom transmitters/receivers realize a very low voltage differential (subLVDS) signalling scheme that can transfer information in a potentially noisy environment.

As implemented in VX6953CB, the CCP link supports the transmission of raw bayer data at 5.0 Mpixel resolution up to 11.5 frame/s at 10-bit resolution (with de-rating).

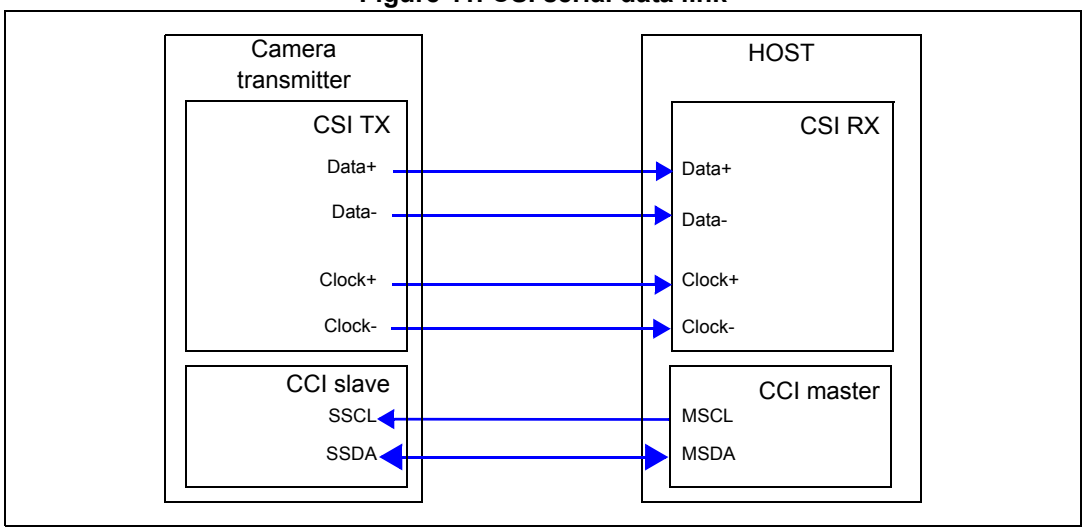
3.6.2 CSI-2 serial data link

Data signals (DATA+ and DATA-) and clock signals (CLK+ and CLK-) are transferred from VX6953CB on two pairs of balanced 100 Ω impedance transmission lines. The physical layer of the interface is the MIPI Alliance Standard D-PHY.

The transmission line pairs and custom transmitters/receivers realize a very low voltage differential (subLVDS) signalling scheme that can transfer information in a potentially noisy environment.

As implemented in VX6953CB, the CSI-2 link supports the transmission of raw Bayer data at 5.0 Mpixel resolution up to 15 frame/s at 10-bit resolution and up to 16.65 fps. in 10-8 bit compressed data format. It is to be noted that image quality between RAW10 and 10-8 bits format is very similar.

Figure 11. CSI serial data link



3.6.3 CCI serial control bus

The internal registers in VX6953CB can be configured by a master device using a CCI bus (SDA, SCL). VX6953CB sends and receives commands over this bus at up to 400 kb/s.

The CCI bus uses a device address of 0x20 for writes and 0x21 for reads.

4 Register map

In this chapter the following abbreviations are used in the Data type and Type columns:

UI	Universal integer
SR	Signed real
32UI	32-bit floating
SI	Signed integer
RO	Read only
RW	Read and write
UR	Unsigned real
B	Bit
SF	Signed float

4.1 Status registers [0x0000 to 0x000F]

Table 9. Status registers [0x0000 to 0x000F]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0000	Hi	model_id	16UI	03.B9	RO	Camera model identification 0x03B9 = 953_{10}
0x0001	Lo					
0x0002		revision_number_major	8UI	00	RO	Revision identifier of the camera for DCC change
0x0003		manufacturer_id	8UI	01	RO	Module manufacturer ID: ST
0x0004		smia_version	8UI	0A	RO	0x0A: SMIA 1.0
0x0005		frame_count	8UI	FF	RO	Frame count increments by 1 on each frame. Rolls over at 255 to 0. When moving from video to sleep the frame count is reset to 255. The frame count is also reset to 255 after a soft reset (register 0x0103).
0x0006		pixel_order	8UI	00	RO	Color pixel readout order. Defines the order of the color pixel readout. Changes with mirror and flip (register 0x0101). 0x00 - GR/BG - normal 0x01 - RG/GB - horizontal mirror 0x02 - BG/GR - vertical flip 0x03 - GB/RG - vertical flip and horizontal mirror
0x0008	Hi	data_pedestal	16UI	00.40	RO	The video data is offset by 64.
0x0009	Lo					

Table 9. Status registers [0x0000 to 0x000F] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x000C		pixel_depth	8UI	0A	RO	Pixel data resolution.
0x0010		revision_number_minor	8UI	00	RO	Module revision identifier of the camera for minor changes.
0x0016	Hi	sensor_model_id	16UI	03	RO	Silicon identification number. This may not be the same as the module identification number, for example, in the case where the same silicon is used in two different modules.
0x0017	Lo			B9	RO	
0x0018	3:0	sensor_revision_number	8UI	00	RO	
	7:4			02	RO	Silicon mask revision code. 02 = cut3.0

4.2 Frame format description registers [0x0040 to 0x007F]

For a full description of the frame format description, refer to *Chapter 5: Video data interface on page 48*.

Table 10. Frame format description registers [0x0040 to 0x007F]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0040		frame_format_model_type	8UI	01	RO	Generic frame format. 0x01: 2-byte data format.(1)
0x0041		frame_format_model_subtype	8UI	12	RO	Contains the number of 2-byte data format descriptors used. Upper nibble defines the number of column descriptors that is, 1. The lower nibble defines the number of row descriptors that is, 2.
0x0042	Hi	frame_format_descriptor_0	16UI	5A.30	RO	Pixel data code: 5 (visible columns) Number of pixels : readout dependent (maximum of 2608)
0x0043	Lo					
0x0044	Hi	frame_format_descriptor_1	16UI	10.02	RO	Pixel data code: 1 (embedded data lines) Number of lines: 2
0x0045	Lo					
0x0046	Hi	frame_format_descriptor_2	16UI	57.A8	RO	Pixel data code: 5 (visible lines) Number of lines: readout dependent (maximum of 1960)
0x0047	Lo					

1. See section 4.5 of SMIA 1.0 functional specification.

4.3 Analog gain description registers [0x0080 to 0x0097]

These registers are not dynamic but are required to be output on the status line so that it is possible to interpret the meaning of the analog gain code(s). For a full description of the analog gain description registers, refer to *Section 6.5.1: Analogue gain model on page 64*.

Table 11. Analog gain description [0x0080 to 0x0093]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0080	Hi	analogue_gain_capability	16UI	00.00	RO	Analogue gain capability 0 – single global analogue gain only
0x0081	Lo					
0x0084	Hi	analogue_gain_code_min	16UI	00.00	RO	Minimum recommended analogue gain code that is, 0 (x1 gain)
0x0085	Lo					
0x0086	Hi	analogue_gain_code_max	16UI	00.F0	RO	Maximum recommended analogue gain code that is, 240 (x16 gain)
0x0087	Lo					
0x0088	Hi	analogue_gain_code_step	16UI	00.10	RO	Analogue gain code step size(1)
0x0089	Lo					
0x008A	Hi	analogue_gain_type	16UI	00.00	RO	Analog gain type
0x008B	Lo					
0x008C	Hi	analogue_gain_m0	16SI	00.00	RO	Analog gain m0 constant. m0 = 0
0x008D	Lo					
0x008E	Hi	analogue_gain_c0	16SI	01.00	RO	Analog gain c0 constant. c0 = 256
0x008F	Lo					
0x0090	Hi	analogue_gain_m1	16SI	FF.FF	RO	Analog gain m1 constant. m1 =-1
0x0091	Lo					
0x0092	Hi	analogue_gain_c1	16SI	01.00	RO	Analog gain c1 constant c1 = 256
0x0093	Lo					

1. For above gains of 0xE0, the step size is four. See *Figure 26* for gain values. This additional feature of the VX6953CB is outside of the SMIA specification.

4.4 Data format description registers [0x00C0 to 0x00FF]

The data format description registers specify which CCP CSI-2 data formats the SMIA camera module supports. Specifically VX6953CB supports RAW 8, 10-8 compressed and RAW10.

Table 12. Data format description registers [0x00C0 to 0x00FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x00C0		data_format_model_type	8UI	01	RO	2-byte generic data format model. Always 0x01.
0x00C1		data_format_model_subtype	8UI	03	RO	Number of descriptors, that is, 3
0x00C2	Hi	data_format_descriptor_0	16UI	08.08	RO	Top 8-bits of internal pixel data transmitted as RAW 8.
0x00C3	Lo					
0x00C4	Hi	data_format_descriptor_1	16UI	0A.0A	RO	Top 10-bits of internal pixel data transmitted as RAW 10.
0x00C5	Lo					
0x00C6	Hi	data_format_descriptor_2	16UI	0A.08	RO	Compress top 10-bits of internal pixel data to 8. Transmitted as RAW 8 mode.
0x00C7	Lo					

4.5 Setup registers [0x0100 to 0x01FF]

Table 13. Setup registers [0x0100 to 0x01FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0100		mode_select	8UI	00	RW	Mode select 0x00 - Software standby 0x01 - Streaming Refer to *Section 3.3: Device operating modes on page 18*.
0x0101		image_orientation	8UI	00	RW	Image orientation, that is, horizontal mirror and vertical flip. Bit 0: 0 - no mirror, 1 - horizontal mirror enable Bit 1: 0 - no flip, 1 - vertical flip enable
0x0103		software_reset	8UI	00	RW	Software reset. Setting this register to 1 resets the sensor to its power up defaults. The value of this bit is also reset. 0x00 - normal 0x01 - soft reset Refer to *Section 3.3: Device operating modes on page 18*

Table 13. Setup registers [0x0100 to 0x01FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0104		grouped_parameter_hold	8UI	00	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters. 0x00 - consume parameters as normal 0x01 - hold parameters, do not consume values while set high Refer to *Section 6.5.3: Integration and gain parameter retiming on page 66*
0x0105		mask_corrupted_frames	8UI	00	RW	Setting this register to 1 prevents the sensor outputing frames that have been corrupted by video timing parameter changes. 0x00 - normal 0x01 - mask corrupted frames
0x0110		csi_channel_identifier	8UI	00	RW	The DMA (CCP2) or virtual (CSI2) channel identifier Valid range for CCP2: 0 to 7 Valid range for CSI2: 0 to 3
0x0111		csi_signalling_mode	8UI	02	RW	0x00 - CCP2 data/clock signalling: 0x01 - CCP2 data/strobe signalling 0x02 - CSI-2: This register should not be changed while the device is streaming data.
0x0112	Hi	csi_data_format	16UI	0A.0A	RW	The MS byte contains the bit width of the uncompressed pixel data. The LS byte contains the bit width of the compressed pixel data. 0A.0A - RAW10 mode 0A.08 - 10-8 compressed mode 08.08 - RAW8 mode
0x0113	Lo					
0x0114		csi_lane_mode	8UI	00	RW	Number of data lanes in use. 00 - 1-lane
0x0120		gain_mode	8UI	00	RO	0x00 – Global analog gain. VX6953CB supports only global gain modes.
0x0136	Hi	EXTCLK_FREQUENCY_MHZ	16UR	06.00	RW	8.8 fixed point representation of the external clock frequency in MHz
0x0137	Lo					

4.6 Integration time and gain registers [0x0200 to 0x02FF]

These registers are used to control the image exposure. See *Section 6.5: Exposure and gain control on page 64* for more information.

Table 14. Integration time and gain registers [0x0200 to 0x02FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0200	Hi	fine_integration_time	16UI	02.54	RW	Fine integration time (pixels).
0x0201	Lo					
0x0202	Hi	coarse_integration_time	16UI	00.00	RW	Coarse integration time (lines).
0x0203	Lo					
0x0204	Hi	analogue_gain_code_global	16UI	00.00	RW	Global analog gain parameter (coded). See *Section 6.5.1: Analogue gain model on page 64* for details of how to use this parameter.
0x0205	Lo					
0x020E	Hi	digital_gain_greenr	16UR	01.00	RW	Gain code for greenr channel.
0x020F	Lo					
0x0210	Hi	digital_gain_red	16UR	01.00	RW	Gain code for red channel.
0x0211	Lo					
0x0212	Hi	digital_gain_blue	16UR	01.00	RW	Gain code for blue channel.
0x0213	Lo					
0x0214	Hi	digital_gain_greenb	16UR	01.00	RW	Gain code for greenb channel.
0x0215	Lo					

4.7 Video timing registers [0x0300 to 0x03FF]

For a full description of the video timing registers please refer to *Chapter 6: Video timing on page 51*.

Table 15. Video timing registers [0x0300 to 0x03FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0300	Hi	vt_pix_clk_div	16UI	00.0A	RW	Number of system clocks per pixel clock.
0x0301	Lo					
0x0302	Hi	vt_sys_clk_div	16UI	00.01	RW	System clock divider value.
0x0303	Lo					
0x0304	Hi	pre_pll_clk_div	16UI	00.01	RW	Pre PLL clock divider value.
0x0305	Lo					
0x0306	Hi	pll_multiplier	16UI	00.84	RW	PLL multiplier value. Only even numbers should be used (odd values will result in the nearest lower even value being used). Value: 132
0x0307	Lo					
0x0308	Hi	op_pix_clk_div	16UI	00.0A	RW	Number of output system clocks per pixel clock.
0x0309	Lo					
0x030A	Hi	op_sys_clk_div	16UI	00.01	RW	Output system clock divider value.
0x030B	Lo					
0x0340	Hi	frame_length_lines	16UI	08.86	RW	Frame length. Value: 2182 Units: Lines
0x0341	Lo					
0x0342	Hi	line_length_pck	16UI	0A.BE	RW	Line length. Value: 2750 Units: Pixel clocks
0x0343	Lo					
0x0344	Hi	x_addr_start	16UI	00.00	RW	X-address of the top left corner of the visible pixel data. Units: Pixels
0x0345	Lo					
0x0346	Hi	y_addr_start	16UI	00.00	RW	Y-address of the top left corner of the visible pixel data.(1) Units: Lines
0x0347	Lo					
0x0348	Hi	x_addr_end	16UI	0A.2F	RW	X-address of the bottom right corner of the visible pixel data. Units: Pixels
0x0349	Lo					
0x034A	Hi	y_addr_end	16UI	07.A7	RW	Y-address of the bottom right corner of the visible pixel data. Units: Lines
0x034B	Lo					
0x034C	Hi	x_output_size	16UI	0A.30	RW	Width of image data output from the sensor module. Units: Pixels
0x034D	Lo					

Table 15. Video timing registers [0x0300 to 0x03FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x034E	Hi	y_output_size	16UI	07.A8	RW	Height of image data output from the sensor module. Units: Lines
0x034F	Lo					
0x0380	Hi	x_even_inc	16UI	00.01	RW	Increment for even pixels. x_even_inc must = 1 for focus_estimation to operate effectively. Units: Pixels
0x0381	Lo					
0x0382	Hi	x_odd_inc	16UI	00.01	RW	Increment for odd pixels. Units: Pixels
0x0383	Lo					
0x0384	Hi	y_even_inc	16UI	00.01	RW	Increment for even pixels. y_even_inc must = 1 for focus_estimation to operate effectively. Units: Pixels
0x0385	Lo					
0x0386	Hi	y_odd_inc	16UI	00.01	RW	Increment for odd pixels. Units: Pixels
0x0387	Lo					

1. Has to be modulo 4 for correct operation of device.

4.8 Image scaling registers [0x0400 to 0x04FF]

Table 16. Image scaling registers [0x0400 to 0x04FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0400	Hi	scaling_mode	16UI	00.00	RW	0 – No scaling 1 – Horizontal scaling 2 – Full scaling (horizontal and vertical)
0x0401	Lo					
0x0402	Hi	spatial_sampling	16UI	00.00	RW	0 – Bayer sampling 1 – Co-sited sampling
0x0403	Lo					
0x0404	Hi	scale_m	16UI	00.10	RW	Down scale factor M component (denominator)
0x0405	Lo					
0x0406	Hi	scale_n	16UI	00.10	RO	Down scale factor N component (numerator, always 16)
0x0407	Lo					

4.9 Image compression registers [0x0500 to 0x05FF]

Table 17. Image compression registers [0x0500 to 0x05FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0500	Hi	compression_mode	16UI	00.01	RO	1 – DPCM/PCM compression (simple predictor)
0x0501	Lo					

4.10 Test pattern registers [0x0600 to 0x06FF]

Table 18. Test pattern registers [0x0600 to 0x06FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0600	Hi	test_pattern_mode	16UI	00.00	RW	0 – normal operation (default) 1 – solid color bars 2 – 100% color bars 3 – fade to grey' color bars 4 – PN9 5 to 255 - reserved
0x0601	Lo					
0x0602	Hi	test_data_red	16UI	00.00	RW	The test data used to replace red pixel data. Range 0 to 1023.(1)
0x0603	Lo					
0x0604	Hi	test_data_greenR	16UI	00.00	RW	The test data used to replace green pixel data on rows that also have red pixels. Valid range 0 to 1023.(1)
0x0605	Lo					
0x0606	Hi	test_data_blue	16UI	00.00	RW	The test data used to replace blue pixel data. Range 0 to 1023.(1)
0x0607	Lo					
0x0608	Hi	test_data_greenB	16UI	00.00	RW	The test data used to replace green pixel data on rows that also have blue pixels. Range 0 to 1023.(1)
0x0609	Lo					
0x060A	Hi	horizontal_cursor_width	16UI	00.00	RW	Defines the width of the horizontal cursor (in pixels).
0x060B	Lo					
0x060C	Hi	horizontal_cursor_position	16UI	00.00	RW	Defines the top edge of the horizontal cursor.
0x060D	Lo					
0x060E	Hi	vertical_cursor_width	16UI	00.00	RW	Defines the width of the vertical cursor (in pixels).
0x060F	Lo					
0x0610	Hi	vertical_cursor_position	16UI	00.00	RW	Defines the left hand edge of the vertical cursor. A value of 0x0FFF switches the vertical cursor into automatic mode where it automatically advances every frame.
0x0611	Lo					

1. Some clipping of these values may occur to prevent false sync codes being generated

4.11 Fifo water mark [0x0700 to 0x0701]

Table 19. Fifo water mark registers [0x0700 to 0x0701]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0700	Hi	fifo_water_mark_pixels	16UI	00.28	RW	The level at which data starts to be transmitted out of the FIFO (default is 40)
0x0701	Lo					

4.12 DPHY [0x0810 to 0x0811]

Table 20. DPHY registers [0x0810 to 0x0811]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0810	Hi	dphy_channel_mbps_for_ui	16UI	00.00	RW	CSI-2 DPHY channel in Mbps (10.4 fixed point). This is used by the DPHY to calculate UI (unit interval) value. It does not control the sensor clock set-up, but should normally correspond to those settings.
0x0811	Lo					

4.13 Binning [0x0900 to 0x0902] and [0x170C to 0x1719]

Table 21. Binning registers [0x0900 to 0x0902]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0900		binning_mode	8UI	00	RW	Binning mode 0 - Disable 1 - Enable
0x0901		binning_type	8UI	00	RW	High-nibble - column binning factor Low-nibble - row binning factor
0x0902		binning_weighting	8UI	00	RW	1 - Averaged 2 - Bayer corrected
0x170C	Hi	Min_frame_length_lines_bin	16UI	00.28	R	Minimum frame length (lines) allowed in binning mode: 40 lines
0x170D	Lo					
0x170E	Hi	Max_frame_length_lines_bin	16UI	FF.FF	R	Maximum frame length (lines) allowed in binning mode
0x170F	Lo					
0x1710	Hi	Min_line_length_pck_bin	16UI	0A.BE	R	Minimum line length (pixel clocks) allowed in binning mode
0x1711	Lo					
0x1712	Hi	Max_line_length_pck_bin	16UI	03.FF	R	Maximum possible number of pixel clocks per line in binning mode
0x1713	Lo					
0x1714	Hi	Min_line_blanking_pck_bin	16UI	00.82	R	Minimum line blanking allowed in binning mode: 130 pixel clocks
0x1715	Lo					

Table 21. Binning registers [0x0900 to 0x0902] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x1716	Hi	Fine_integration_time_min_bin	16UI	02.04	R	Minimum fine integration time allowed in binning mode (in pixels)
0x1717	Lo					
0x1718	Hi	Fine_integration_time_max_margin_bin	16UI	08.80	R	Margin used to determine the maximum fine integration time allowed in binning mode (in pixels)
0x1719	Lo					

4.14 Shading correction [0x0B00]

Table 22. Shading correction registers [0x0B00]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B00		shading_correction_enable	8UI	01	RW	Shading correction 0 - disable 1 - enable

4.15 Defect correction [0x0B05 to 0x0B09]

Table 23. Defect correction registers [0x0B05 to 0x0B09]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B05		mapped_couplet_correct_enable	8UI	01	RW	Mapped couplet correction 0 - disable 1 - enable
0x0B06		single_defect_correct_enable	8UI	01	RW	Single defect correction 0 - disable 1 - enable
0x0B07		single_defect_correct_weight	8UI	40	RW	Single defect correction weight
0x0B08		dynamic_couplet_correct_enable	8UI	00	RW	Dynamic couplet correction 0 - disable 1 - enable
0x0B09		dynamic_couplet_correct_weight	8UI	00	RW	Dynamic couplet correction weight

4.16 EDOF [0x0B80 to 0x0B8A]

Table 24. EDOF registers [0x0B80 to 0x0B8A]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B80		edof_mode	8UI	00	RW	EDOF control 0 - EDOF disabled (power saving) 1 - EDOF application (capture) 2 - EDOF estimation (preview)
0x0B81		edof_est_depth_of_field	8UI	00	RO	Not used in VX6953CB
0x0B82		edof_est_focus_distance	8UI	32	RO	The estimated focus point (cm)
0x0B83		edof_sharpness	8UI	00	RW	EDOF sharpness control
0x0B84		edof_denoising	8UI	00	RW	EDOF denoising control
0x0B85		edof_module_specific	8UI	00	RW	EDOF noise vs details control
0x0B88	Hi	edof_focus_distance	16UI	00.32	RW	Value supplied by the host which is used by VX6953CB for focus distance (in cm). 0x0000 to 0x7FFF - manual mode 0x8000 to 0xFFFF - limited auto
0x0B89	Lo					
0x0B8A		edof_estimation_control	8UI	00	RW	EDOF estimator control 1 - uniform 2 - centre weight 4 - large spot 8 - narrow spot

4.17 Color feedback registers [0x0B8C to 0x0B95]

Table 25. Color feedback registers [0x0B8C to 0x0B95]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B8C	Hi	colour_temperature	16SR	00.00	RW	Not supported by VX6953CB
0x0B8D	Lo					
0x0B8E	Hi	host_WB_stats_green_red	16UR	01.00	RW	White balance gains to be applied by the host. These stats are used by the EDOF and the adaptive AV to estimate the color temperature of the scene.
0x0B8F	Lo					
0x0B90	Hi	host_WB_stats_red	16UR	01.00	RW	
0x0B91	Lo					
0x0B92	Hi	host_WB_stats_blue	16UR	01.00	RW	
0x0B93	Lo					
0x0B94	Hi	host_WB_stats_green_blue	16UR	01.00	RW	
0x0B95	Lo					

4.18 Integration time and gain parameter limit registers [0x1000 to 0x10FF]

These registers are used to define exposure limits for the integration control registers (0x200 to 0x203). See *Section 6.5: Exposure and gain control on page 64* for more information.

Table 26. Integration time and gain parameter limit registers [0x1000 to 0x10FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1000	Hi	integration_time_capability	16UI	00.01	RO	0x0001 – coarse and smooth (1 pixel) fine integration.
0x1001	Lo					
0x1004	Hi	coarse_integration_time_min	16UI	00.00	RO	Minimum coarse integration time. Line periods.
0x1005	Lo					
0x1006	Hi	coarse_integration_time_max_margin	16UI	00.09	RO	Current frame length – current max coarse exposure. Line periods.
0x1007	Lo					
0x1008	Hi	fine_integration_time_min	16UI	02.54	RO	Minimum fine integration time. Pixel periods.
0x1009	Lo					
0x100A	Hi	fine_integration_time_max_margin	16UI	03.BE	RO	Current line length – current max fine exposure. Pixel periods.
0x100B	Lo					
0x1080	Hi	digital_gain_capability	16UI	00.01	RO	0x01 – supports digital gain.
0x1081	Lo					
0x1084	Hi	digital_gain_min	16UR	00.08	RO	1/32 (0.03125) minimum
0x1085	Lo					
0x1086	Hi	digital_gain_max	16UR	01.F8	RO	1.96875 maximum
0x1087	Lo					
0x1088	Hi	digital_gain_step_size	16UR	00.08	RO	0.03125 step size
0x1089	Lo					

4.19 Video timing parameter limit registers [0x1100 to 0x11FF]

For a full description of the video timing parameter limit registers, refer to *Chapter 6: Video timing on page 51*.

Table 27. Video timing parameter limit registers [0x1100 to 0x11FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1100	Hi	min_ext_clk_freq_mhz	32SF	40.C0 00.00	RO	Minimum external clock frequency Units: MHz Value: 6.0
0x1101	3rd					
0x1102	2nd					
0x1103	Lo					
0x1104	Hi	max_ext_clk_freq_mhz	32SF	41.D8 00.00	RO	Maximum external clock frequency Units: MHz Value: 27.0
0x1105	3rd					
0x1106	2nd					
0x1107	Lo					
0x1108	Hi	min_pre_pll_clk_div	16UI	00.01	RO	Minimum Pre PLL divider value Value: 1
0x1109	Lo					
0x110A	Hi	max_pre_pll_clk_div	16UI	00.04	RO	Maximum Pre PLL divider value Value: 4
0x110B	Lo					
0x110C	Hi	min_pll_ip_freq_mhz	32SF	40.C0 00.00	RO	Minimum PLL input clock frequency Units: MHz Value: 6.0
0x110D	3rd					
0x110E	2nd					
0x110F	Lo					
0x1110	Hi	max_pll_ip_freq_mhz	32SF	41.40 00.00	RO	Maximum PLL input clock frequency Units: MHz Value: 12.0
0x1111	3rd					
0x1112	2nd					
0x1113	Lo					
0x1114	Hi	min_pll_multiplier	16UI	00.25	RO	Minimum PLL multiplier Value: 37
0x1115	Lo					
0x1116	Hi	max_pll_multiplier	16UI	00.85	RO	Maximum PLL multiplier Value: 133
0x1117	Lo					
0x1118	Hi	min_pll_op_freq_mhz	32SF	43.E1 00.00	RO	Minimum PLL output clock frequency Units: MHz Value: 450.0
0x1119	3rd					
0x111A	2nd					
0x111B	Lo					

Table 27. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x111C	Hi	max_pll_op_freq_mhz	32SF	44.48 00.00	RO	Maximum PLL output clock frequency Units: MHz Value: 800.0
0x111D	3rd					
0x111E	2nd					
0x111F	Lo					
0x1120	Hi	min_vt_sys_clk_div	16UI	00.01	RO	Minimum video-timing system clock divider value Value: 1 In data/clock mode, the minimum value is 2.
0x1121	Lo					
0x1122	Hi	max_vt_sys_clk_div	16UI	00.04	RO	Maximum video-timing system clock divider value Value: 4
0x1123	Lo					
0x1124	Hi	min_vt_sys_clk_freq_mhz	32SF	43.30 00.00	RO	Minimum video-timing system clock frequency Units: MHz Value: 176.0
0x1125	3rd					
0x1126	2nd					
0x1127	Lo					
0x1128	Hi	max_vt_sys_clk_freq_mhz	32SF	44.48 00.00	RO	Maximum video-timing system clock frequency Units: MHz Value: 800.0
0x1129	3rd					
0x112A	2nd					
0x112B	Lo					
0x112C	Hi	min_vt_pix_clk_freq_mhz	32SF	42.30 00.00	RO	Minimum video-timing pixel clock frequency Units: MHz Value: 44.0
0x112D	3rd					
0x112E	2nd					
0x112F	Lo					
0x1130	Hi	max_vt_pix_clk_freq_mhz	32SF	42.B8 00.00	RO	Maximum video-timing pixel clock frequency Units: MHz Value: 92.0
0x1131	3rd					
0x1132	2nd					
0x1133	Lo					
0x1134	Hi	min_vt_pix_clk_div	16UI	00.04	RO	Minimum video-timing pixel clock divider Value: 4
0x1135	Lo					
0x1136	Hi	max_vt_pix_clk_div	16UI	00.0A	RO	Maximum video-timing pixel clock divider Value: 10
0x1137	Lo					
0x1140	Hi	min_frame_length_lines	16UI	00.28	RO	Minimum frame length allowed. Value = 40 Units: Lines
0x1141	Lo					

Table 27. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x1142	Hi	max_frame_length_lines	16UI	FF.FF	RO	Maximum possible number of lines per Frame. Value = 65535 Units: Lines
0x1143	Lo					
0x1144	Hi	min_line_length_pck	16UI	0A.BE	RO	Minimum line length allowed. Value = 2750 Units: Pixel clocks
0x1145	Lo					
0x1146	Hi	max_line_length_pck	16UI	3F.FF	RO	Maximum possible number of pixel clocks per line. Value = 16383 Units: Pixel clocks
0x1147	Lo					
0x1148	Hi	min_line_blanking_pck	16UI	00.82	RO	Minimum line blanking time in pixel clocks. Value = 130 Units: Pixel clocks
0x1149	Lo					
0x114A	Hi	min_frame_blanking_lines	16UI	00.22	RO	Minimum frame blanking in video lines is 34.
0x114B	Lo					
0x1160	Hi	min_op_sys_clk_div	16UI	00.01	RO	Minimum output system clock divider. Value = 1
0x1161	Lo					
0x1162	Hi	max_op_sys_clk_div	16UI	00.68	RO	Maximum output system clock divider Value = 104
0x1163	Lo					
0x1164	Hi	min_op_sys_clk_freq_mhz	32SF	40.8A 76.27	RO	Minimum output system clock frequency Units: MHz Value: 4.327
0x1165						
0x1166						
0x1167	Lo					
0x1168	Hi	max_op_sys_clk_freq_mhz	32SF	44.48 00.00	RO	Maximum output system clock frequency Units: MHz Value: 800.0
0x1169						
0x116A						
0x116B	Lo					
0x116C	Hi	min_op_pix_clk_div	16UI	00.08	RO	Minimum output pixel clock divider. Value = 8
0x116D	Lo					
0x116E	Hi	max_op_pix_clk_div	16UI	00.0A	RO	Maximum output pixel clock divider Value = 10
0x116F	Lo					
0x1170	Hi	min_op_pix_clk_freq_mhz	32SF	3E.DD 89.D9	RO	Minimum output pixel clock frequency Units: MHz Value: 0.433 (433 kHz)
0x1171						
0x1172						
0x1173	Lo					

Table 27. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x1174	Hi	max_op_pix_clk_freq_mhz	32SF	42.B8 00.00	RO	Maximum output pixel clock frequency Units: MHz Value: 92.0
0x1175						
0x1176						
0x1177	Lo					
0x1180	Hi	x_addr_min	16UI	00.00	RO	Minimum X-address of the addressable pixel array Value: Always 0
0x1181	Lo					
0x1182	Hi	y_addr_min	16UI	00.00	RO	Minimum Y-address of the addressable pixel array Value: Always 0
0x1183	Lo					
0x1184	Hi	x_addr_max	16UI	0A.2F	RO	Maximum X-address of the addressable pixel array Value = 2607
0x1185	Lo					
0x1186	Hi	y_addr_max	16UI	07.A7	RO	Maximum Y-address of the addressable pixel array Value = 1959
0x1187	Lo					
0x1188	Hi	min_x_output_size	16UI	01.00	RO	Minimum x output size in pixels. Value: 256
0x1189	Lo					
0x118A	Hi	min_y_output_size	16UI	00.04	RO	Minimum y output size in pixels. Value: 4
0x118B	Lo					
0x118C	Hi	max_x_output_size	16UI	0A.30	RO	Maximum x output size in pixels. Value: 2608
0x118D	Lo					
0x118E	Hi	max_y_output_size	16UI	07.A8	RO	Maximum y output size in pixels: Value: 1960
0x118F	Lo					
0x11C0	Hi	min_even_inc	16UI	00.01	RO	Minimum increment for even pixels
0x11C1	Lo					
0x11C2	Hi	max_even_inc	16UI	00.07	RO	Maximum increment for even pixels. even_inc must equal 1 for focus_estimation to operate effectively.
0x11C3	Lo					
0x11C4	Hi	min_odd_inc	16UI	00.01	RO	Minimum increment for odd pixels
0x11C5	Lo					
0x11C6	Hi	max_odd_inc	16UI	00.07	RO	Maximum increment for odd pixels
0x11C7	Lo					

4.20 Image scaling parameter limit registers [0x1200 to 0x120B]

Table 28. Image scaling parameter limit registers [0x1200 to 0x120B]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1200	Hi	scaling_capablility	16UI	00.02	RO	VX6953CB supports full (horizontal and vertical) scaling.
0x1201	Lo					

4.21 Image compression parameter registers [0x1300 to 0x13FF]

Table 29. Image compression parameter limit registers [0x1300 to 0x13FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1300	Hi	compression_capablility	16UI	00.01	RO	VX6953CB supports DPCM/PCM compression
0x1301	Lo					

4.22 CSI lane mode capability [0x1600 to 0x1602]

Table 30. CSI lane mode capability registers [0x1600 - 0x1602]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1600		ui_and_manual_dphy_ctrl_capability	8UI	00	RO	CSI2 DPHY control capability UI enough
0x1601		csi_lane_capability	8UI	01	RO	One CSI-2 data lane supported
0x1602		csi_signallingmode_capability	8UI	07	RO	Number of data lanes available. Bit[0]: 1 = CCP2 Data/Clock supported. 0 = Not supported. Bit[1]: 1 = CCP2 Data/Strobe supported. 0 = Not supported. Bit[2]: 1 = CSI2 supported. 0 = Not supported.

4.23 Binning capability [0x1700 to 0x170B]

Table 31. Binning capability registers [0x1700 to 0x170B]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1700		binning_capability	8UI	01	RO	VX6953CB supports binning
0x170B		binning_weighting_capability	8UI	05	RO	VX6953CB supports averaged and Bayer corrected weighting

4.24 Manufacturer specific registers - Clipper 1 [0x31E8 to 0x31EB]

By default, black level is 64. The end user can remove or modify it if needed to get the maximum output depth.

Table 32. Manufacturer specific registers [0x31E8 to 0x31EB]

Index	Byte	Register name	Data type	Default	Type	Comment
0x31E8		ENABLE	8UI	01	RW	Clipper 1 If set to 0: disabled If set to 1: enabled
0x31EA	Hi	OFFSET_REQ	16SI	00.20	RW	Clipper offset request (Signed bit)
0x31EB	Lo					

5 Video data interface

The video stream which is output from the VX6953CB through the compact camera port (CCP) or camera serial interface (CSI) contains both video data and other auxiliary information. This chapter describes the frame formats.

The VX6953CB is SMIA version 1.0 and MIPI CSI-2 version 1.00 and D-PHY v1.00 compliant meaning it is compatible with both v0.90 and v1.00 D-PHY receivers.

The selection of the video data format is controlled using the register CSI_SIGNALLING_MODE (0x0111):

0 - CCP2 data/clock

1 - CCP2 data/strobe

2 - CSI-2 (default)

Changing the video data format must be performed when the sensor is in software standby.

The VX6953CB has one CSI-2 data lane capable of transmitting at 800 Mbps. However, while in CCP2 interface the maximum data rate is 640 Mbps.

The CSI-2 data lane transmitter supports:

- Unidirectional master
- HS-TX
- LP-TX (ULPS)
- CIL-MUYN function

The CSI-2 clock lane transmitter supports:

- Unidirectional master
- HS-TX
- LP-TX (ULPS)
- CIL-MCNN function

5.1 Frame format

The frame format for the VX6953CB is described by the frame format descriptors, see *Table 10 on page 30*. For CCP this results in a frame as shown in *Figure 12* and for CSI it results in a frame as shown in *Figure 13*.

Figure 12. VX6953CB CCP frame format

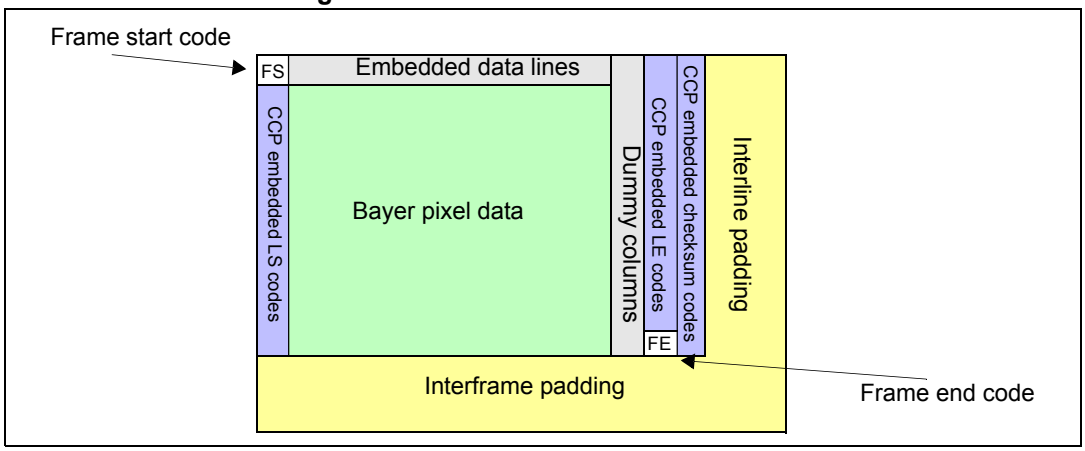
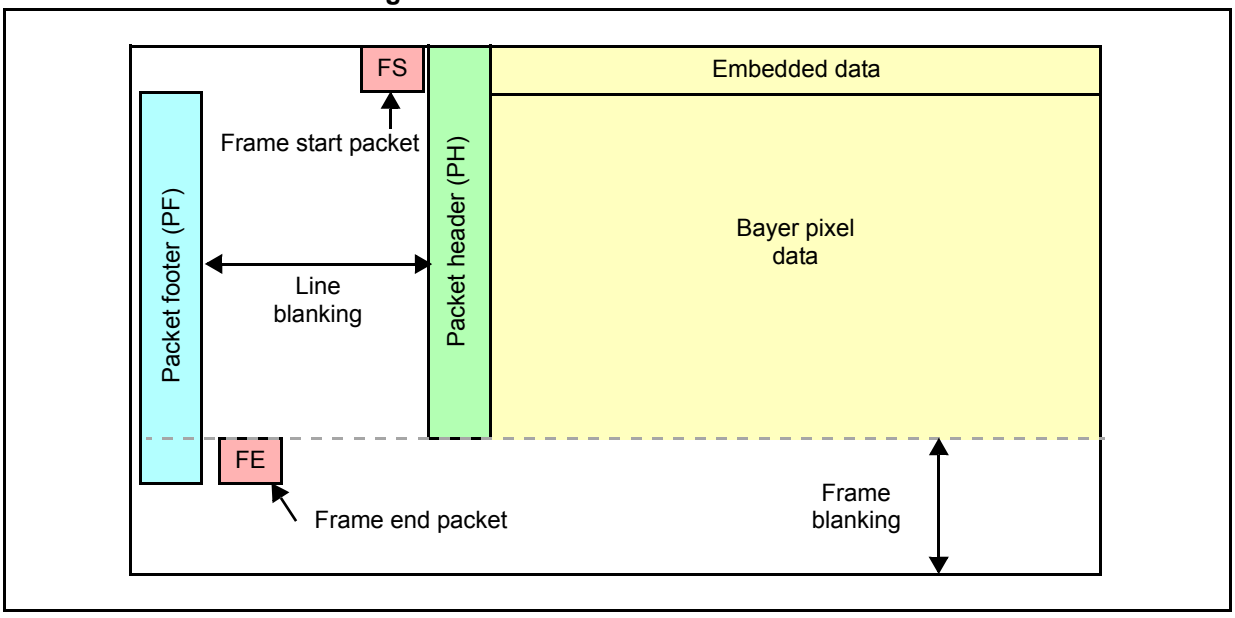


Figure 13. VX6953CB CSI-2 frame format



Data format

VX6953CB allows different data formats such as RAW10, RAW8 and 10-8 bit compressed:

- RAW10 is a 10-bit depth RAW Bayer format
- RAW8 is an 8-bit depth RAW Bayer format
- 10-8 is a 10-bit RAW format compressed in 8-bit depth

Embedded data lines

The embedded data lines provide a mechanism to embed non-image data such as sensor configuration details and image statistics values with a frame of data.

VX6953CB has two embedded data lines at the start of the frame.

Dummy columns

The VX6953CB has zero dummy columns.

Visible pixel data

The visible pixels contain valid image data. The correct integration time and analog gain for the visible pixels is specified in the embedded data lines at the start of the frame. The number of visible pixels can be varied.

Black pixel data (zero integration time)

The VX6953CB has zero black pixels.

Dark pixel data (light shielded pixels)

The VX6953CB has zero dark pixels.

Manufacturer specific pixel data

The VX6953CB has zero manufacturer specific pixels.

Interline padding/line blanking

During interline padding all bits in the data stream in a CCP frame are set to 1.

In a CSI-2 frame there is no concept of line blanking being transmitted, the sensor will simply spend a longer time in the LP state between active line data.

Interframe padding/frame blanking

During interframe padding all bits in the data stream in a CCP frame are set to 1.

In a CSI-2 frame there is no concept of frame blanking being transmitted, the sensor will simply spend a longer time in the LP state at the end of the active data for a frame.

6 Video timing

6.1 Output size

The VX6953CB has the following methods available to achieve the required output size, these can be used independently or in conjunction with any other:

- programmable addressable region of the pixel array
- programmable width and height for output image data
- scaling
- subsampling

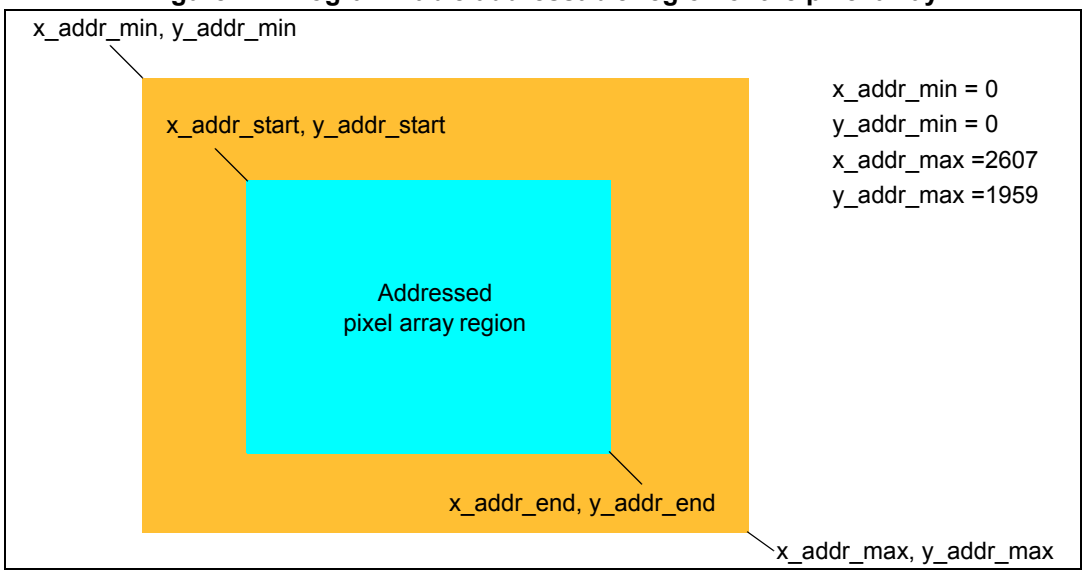
The programmable image size and output size are independent functions. It is the responsibility of the host to ensure that these functions are programmed correctly for the intended application. These functions also reduce the amount of data and therefore reduce the peak data rate of CCP2/CSI-2.

6.1.1 Programmable addressable region of the pixel array

The native size for the VX6953CB is 2592 x 1944, the maximum addressable array is 2608 x 1960 which gives border pixels (outer eight rows and eight columns) for the color reconstruction algorithms to use at the edges of the array.

By programming the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers it is possible to use the full size of the array as you would do for a native size output or you can select a ‘window of interest’. The addressed region of the array is used in any subsequent sub-sampling or scaling. See *Figure 14*.

Figure 14. Programmable addressable region of the pixel array



The host must ensure the following rules are kept;

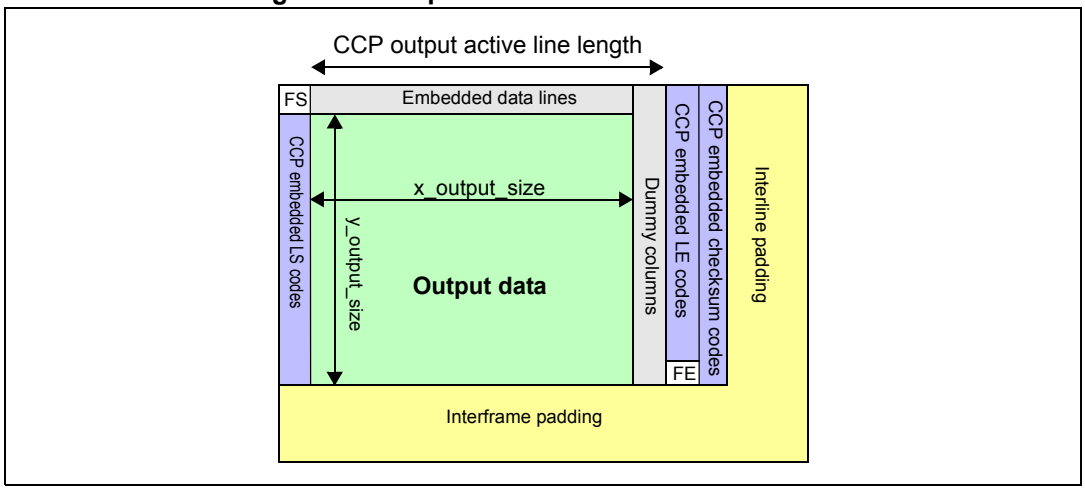
- the end address must be greater than the start address
- the x and y start addresses are restricted to even numbers only, and the x and y end addresses are restricted to odd numbers only, to ensure that there is always a even number of pixels readout

6.1.2 Programmable width and height for output image data

The x_output_size and y_output_size registers are not intended as the primary cropping controls.

They are intended to define the position of the LE/FE codes in the CCP data frame so that the sensor does not need to calculate this based on region of interest or sub-sampling settings. It should be expected that the host will set the output sizes to exactly enclose the output image data. If the host should not do this, the VX6953CB treats the output sizes as being calculated from the top left hand corner of the output array. So in the case where output sizes are smaller than the output data, the data is cropped from its right hand and lower limits. In the case where output sizes are larger than the output data, the lines shall be padded out to the defined output size with undefined data.

Figure 15. Output size within a CCP data frame



CCP2 requires that the number of pixels between the line start and the line end sync codes is:

- a multiple of 4 pixels for RAW8
- a multiple of 16 pixels for RAW10

The host must control the x_output_size to ensure that the above criteria is met.

6.1.3 Scaling

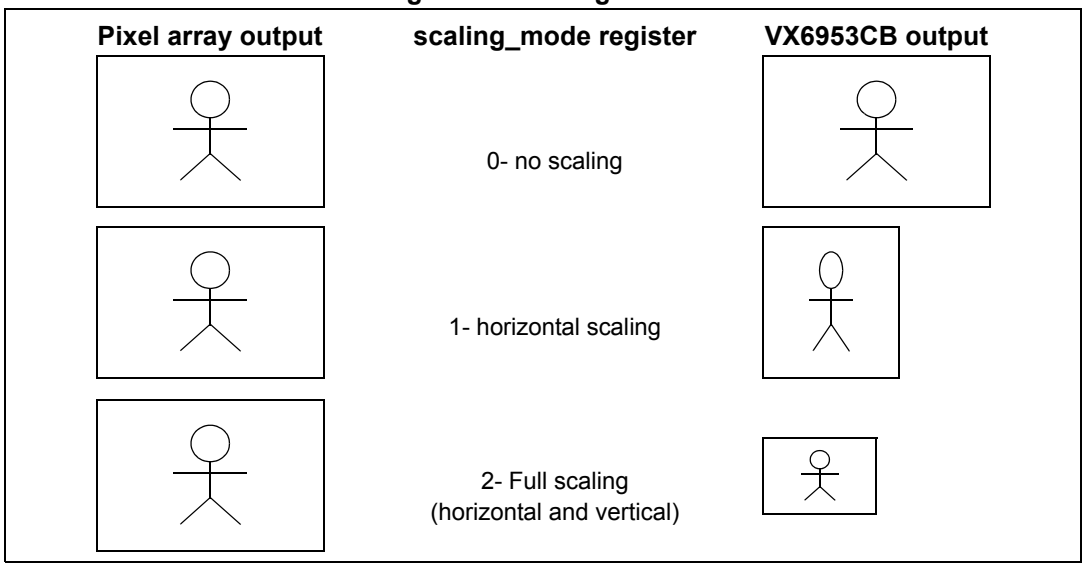
The VX6953CB module is compliant with the ‘Profile Level 2 - Full (Horizontal and Vertical)’ level of image scaling.

The image scaling function within the sensor module provides a flexible way of generating lower resolution full field of view image data, at a reduced data rates, for viewfinder and video applications.

The scaler is able to scale the full resolution of the sensor module down to within 10% of a the target image size (the smallest output size is 256 x 192). This flexibility means that the VX6953CB module can support a wide range of LCD viewfinder sizes and different codec resolutions.

The VX6953CB has three scaling modes which are controlled by the scaling_mode register shown in *Figure 16*.

Figure 16. Scaling modes



Scaler quality

The scaler supports two options for the spatial sampling of the scaled image data: (see *Figure 17*):

- Bayer sampled scaled image data

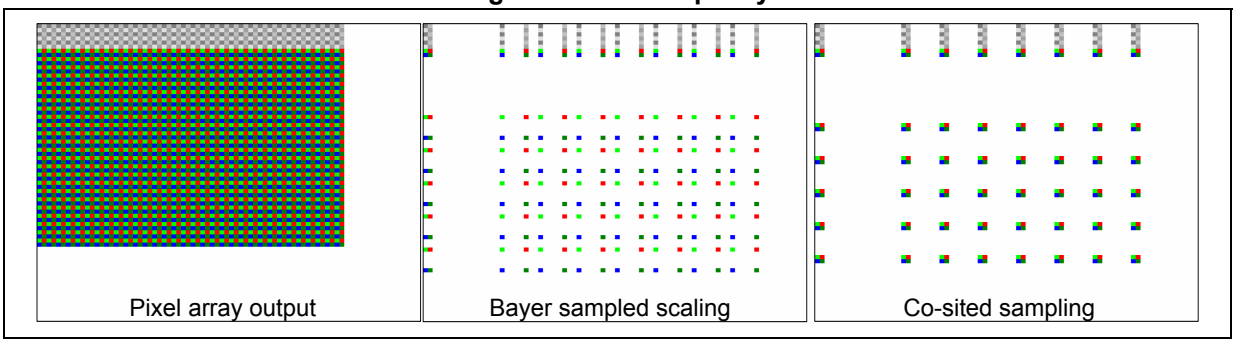
  The sampling point for the scaler for the output Gr value appears to be in the centre of the Gr pixel (i.e. between the 1st and 2nd pixels and between the 1st and 2nd rows of the original input Bayer pixel data). The R (or B) sampling points are similarly in the centre of the R pixel (or B pixel).

- co-sited scaled image data

  The sampling point for the Gr, R. Gb and B vales in each output ‘quad’ are functions of the same colour input array pixels such that the spatial sampling point for all four appears to be in the centre of the ‘quad’ i.e. between the 2nd and 3rd pixels and between the 1st and 2nd rows.

The spatial sampling mode is controlled by the spatial_sampling register.

Figure 17. Scaler quality



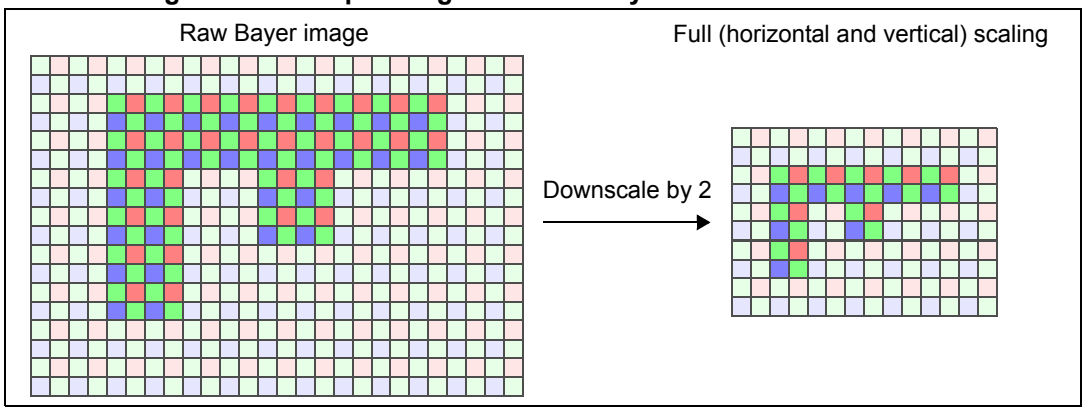
Down scaler factor

The down scaler factor is controlled by an M/N ratio, scale_m is >= 16 and scale_n is fixed at 16. scale_m is in the range 16 to 164.

$$\text{down\_scale\_factor} = \frac{\text{scale\_m}}{\text{scale\_n}} = \frac{\text{scale\_m}}{16}$$

This single down scale factor is used by both the horizontal and vertical scalers. The scaler acts upon the addressed region of the array which is determined by the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers.

Figure 18. Example image full scaled by a downscale factor of 2



6.1.4 Subsampling

Subsampling is achieved by programming the x _odd_inc, y_odd_inc, x_even_inc and y_even_inc registers.

If the pixel being readout has an even address then the address is incremented by the even increment value either x_even_inc or y_even_inc. If the pixel being readout has an odd address then the address is incremented by the odd increment value either x _odd_inc or y_odd_inc.

The subsampled readout is disabled by setting the odd and even increment values to 1.

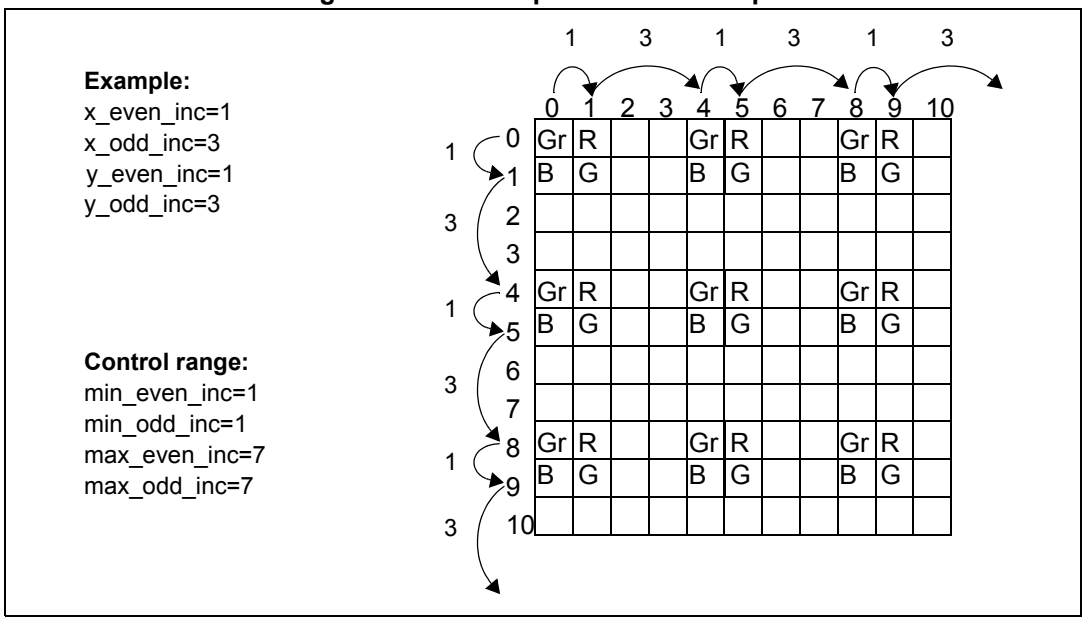
Subsampling acts upon the addressed region of the array which is determined by the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers.

For the EDOF focus estimation to operate effectively, the x_even_inc and y_even_inc registers must be 1.

The equation for the subsampling factor is given below:

$$\text{sub\_sampling\_factor} = \frac{\text{even\_inc} + \text{odd\_inc}}{2}$$

Figure 19. Subsample readout example



6.1.5 Binning

The VX6953CB also has a binning mode that offers a reduced size full field of view image. The binning mode averages row and column pixel data.

The binning mode results in a reduced number of lines and so can be used to give a higher image frame rate. Compared to subsampling, binning makes use of the light gathered from the whole pixel array and it results in higher image quality.

The binning mode will scale by 2 x 2 in the X and Y directions.

Entering and exiting binning mode may or may not be performed when the sensor is in software standby.

Table 33 summarizes the register settings for each of the binning modes. Refer to the personality file for further image quality settings.

Table 33. Binning register settings

Register	Address	Normal(1)	2x2
binning_mode	0x0900	0	1
binning_type	0x0901	N/A	0x22
binning_weighting	0x0902	N/A	5
x_odd_inc	0x0383	1	3
y_odd_inc	0x0387	1	3

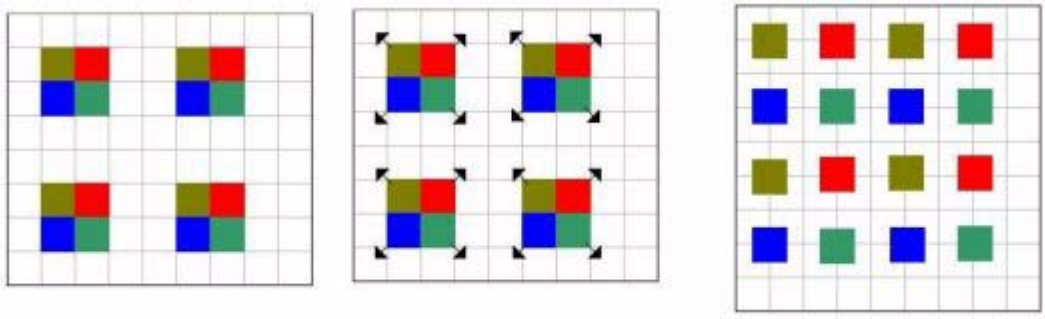
1. min_fine_integration and max_fine_integration values for 2 x 2 subsampling modes are the same as Normal (full resolution) mode.

Binning repair

Binning can introduce some phases errors from the image perspective as it clusters the output of each color channel. Gr,R,B and Gb binned pixels are located around the same intersection point on the output lattice.

To reduce this error, a binning IP is integrated into the imaging data path. The IP moves each binned color channel by 1/8 of an inter-pixel distance. Therefore the top-left Gr pixel moves into the top-left corner, the R pixel in the top-right moves in the top-right direction. This is shown in *Figure 20*.

Figure 20. Binning repair



6.2 Video timing

This section specifies the timing for the image data that is readout from the pixel array and the output image data. These are not necessarily the same size.

The application of all of the video timing read/write parameters must be retimed to the start of the frame boundary to ensure that the parameters are consistent within a frame.

The video stream which is output from the VX6953CB contains both video data and other auxiliary information. The VX6953CB output coding conforms to the CCP RAW8 and RAW10 data format (see SMIA 1.0 Part 2:CCP2 Specification) including line checksums.

Reference SMIA 1.0 Specification section 5 for a detailed description of video timing.

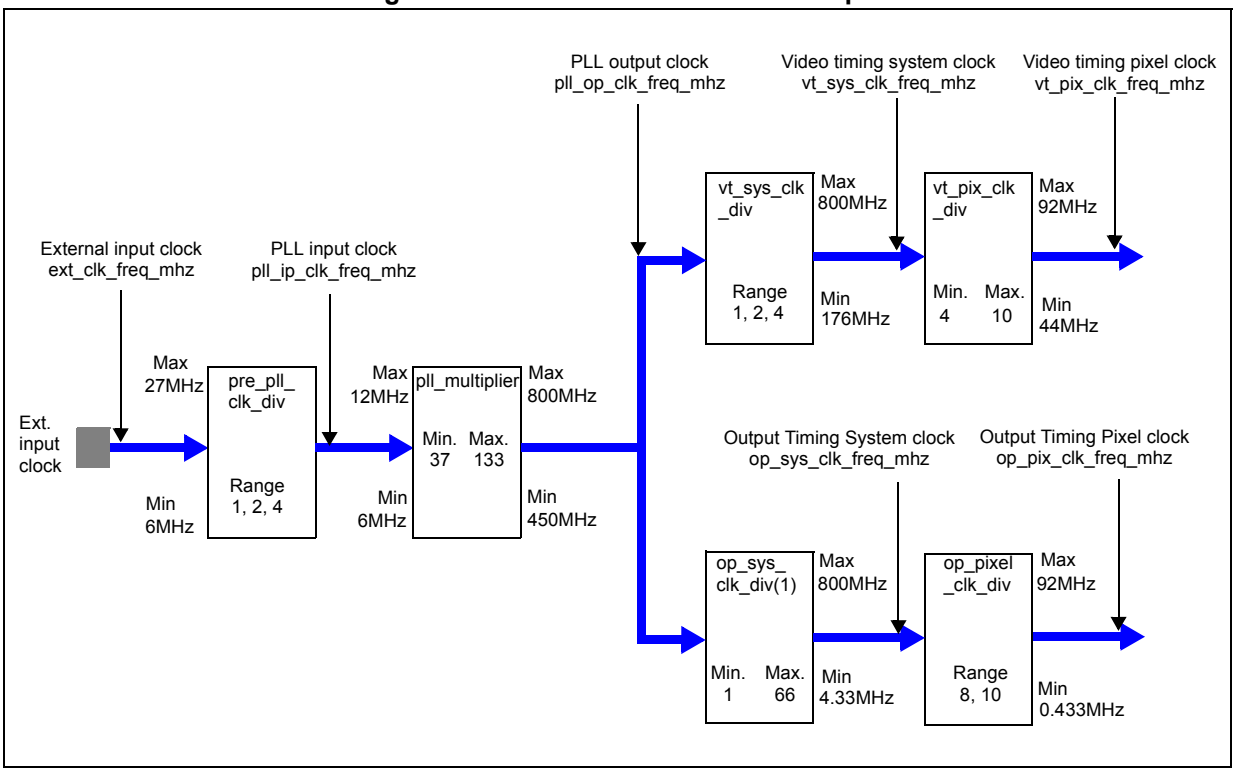
6.2.1 PLL block

The VX6953CB contains a phase locked loop (PLL) block, which generates all the necessary internal clocks from the external clock input. Changes to the PLL settings on the VX6953CB will only be consumed on the software standby to streaming mode transition.

Figure 21 shows the internal functional blocks, which define the relationship between the external input clock frequency and the pixel clock frequency.

The majority of the logic within the device is clocked by vt_sys_clk however the CCI block is clocked by the external input clock.

Figure 21. VX6953CB clock relationships



1. In order to comply with CSI-2 D-PHY specification, the op_sys_clk_freq_mhz minimum output frequency should be higher than 80 MHz.
In order to comply with SMIA 1.0 Part 2: CCP2 Specification v1.0, the maximum op_sys_clk_freq_mhz for CCP2 is 640 MHz.

The equations relating the input clock frequency to pixel clock frequencies are:

$$op\_pix\_clk\_freq\_mhz = \frac{ext\_clk\_freq\_mhz \times pll\_multiplier}{pre\_pll\_clk\_div \times op\_sys\_clk\_div \times op\_pix\_clk\_div}$$

$$vt\_pix\_clk\_freq\_mhz = \frac{ext\_clk\_freq\_mhz \times pll\_multiplier}{pre\_pll\_clk\_div \times vt\_sys\_clk\_div \times vt\_pix\_clk\_div}$$

6.2.2 Spread spectrum clock generator

The PLL contains a spread spectrum clock generator (SSCG) block for the purposes of EMI reduction. This feature is off by default and is intended for use if channel blocking becomes an issue on the baseband platform. A primary source of EMI is the high speed CCP serial data link. The modulation period and depth are fully programmable. The spread mode is selectable between center spread (default) or down spread. The SSCG registers can only be reprogrammed with new values when the sensor is in software standby mode.

6.2.3 Framerate

The framerate of the array readout and therefore the output framerate is governed by the line length, frame length and the video timing pixel clock frequency.

- Line length is specified as a number of pixel clocks, line_length_pck.
- Frame length is specified as a number of lines, frame_length_lines.
- Video timing pixel clock is specified in MHz, vt_pix_clk_freq_mhz.

The equation relating the framerate to the line length, frame length and the video timing pixel clock frequency is:

$$\text{Framerate} = \frac{\text{vt\_pix\_clk\_freq\_mhz}}{\text{line\_length\_pck} \times \text{frame\_length\_lines}}$$

The maximum frame rate that can be achieved in profile 0 is 14.5 fps using CSI-2 communication. *Table 34* provides examples of frame timing for RAW10 mode for 14.5 fps for a variety of external clock frequencies.

Table 34. External clock frequency examples - 5.0 Mpixel RAW10 14.5 fps (CSI-2)

Ext Clk Freq	Pre-PLL Clk Div	PLL multiplier	VT Sys Clk Div	VT pixel Clk Div	VT pixel clock	OP Sys Clk Div	OP pixel Clk Div	OP pixel clock	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
9.60	1	83	1	10	79.68	1	10	79.68	2750	1996
12.00	2	133	1	10	79.80	1	10	79.80	2750	1996
13.00	2	123	1	10	79.95	1	10	79.95	2750	1996

For CSI-2 in order to achieve 15 fps it is necessary to use profile 2 to enable derating. *Table 35* provides examples of frame timing for RAW10 for 15 fps for a variety of external clock frequencies.

Table 35. External clock frequency examples - 5.0 Mpixel RAW10 15 fps (CSI-2)

Ext Clk Freq	Pre-PLL Clk Div	PLL multiplier	VT Sys Clk Div	VT pixel Clk Div	VT pixel clock	OP Sys Clk Div	OP pixel Clk Div	OP pixel clock	Line length (1)	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
9.60	1	83	1	9	88.5	1	10	79.68	2950	2000
12.00	2	133	1	9	86.67	1	10	79.80	2950	2003
13.00	2	123	1	9	88.83	1	10	79.95	2950	2007

1. The min_line_length_blanking = 356ns + 88*UI for CSI-2.

For CCP-2 in order to achieve 15 fps it is necessary to use 10-8 compressed data and profile 2 to enable derating. *Table 36* provides examples of frame timing for 10-8 compressed mode for 15 fps for a variety of external clock frequencies.

Table 36. External clock frequency examples - 5.0 Mpixel 10-8 compressed 15 fps

Ext Clk Freq	Pre-PLL Clk Div	PLL multiplier	VT Sys Clk Div	VT pixel Clk Div	VT pixel clock	OP Sys Clk Div	OP pixel Clk Div	OP pixel clock	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
9.60	1	66	1	7	90.5	1	8	79.2	3027	1996
12.00	2	106	1	7	90.9	1	8	79.5	3027	2002
13.00	2	98	1	7	91	1	8	79.63	3027	2004

CSI-2 maximum output frame rate in 5 Mpixel image

Using 10-8 compression can be an option for the end user to increase the frame rate and keep a high quality image. There is no visible loss in using 10-8 compressed data format over RAW10 format.

Table 37. Example - 5.0 Mpixel 10-8 compressed 16.65 fps (CSI-2)

Ext Clk Freq	Pre-PLL Clk Div	PLL multiplier	VT Sys Clk Div	VT pixel Clk Div	VT pixel clock	OP Sys Clk Div	OP pixel Clk Div	OP pixel clock	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
12.00	2	122	1	8	91.5	1	8	91.5	2750	1998
24.00	4	122	1	8	91.5	1	8	91.5	2750	1998

1080p30 HD video format

In order to achieve 1080p30, it is necessary to use CSI2 mode with RAW8 or 10-8 compressed data and profile 2 to enable derating. *Table 38* provides examples of frame timing for 1080p30.

Table 38. External clock frequency examples - 1080x1920 in 10-8 bit @ 30fps (CCP)

Ext Clk Freq	Pre-PLL Clk Div	PLL multiplier	VT Sys Clk Div	VT pixel Clk Div	VT pixel clock	OP Sys Clk Div	OP pixel Clk Div	OP pixel clock	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
12.00	2	122	1	8	91.5	1	8	91.5	2750	1108
24.00	4	122	1	8	91.5	1	8	91.5	2750	1108

720p30 video format

In order to achieve 720p30, either CCP2 or CSI2 can be used in profile 2 to enable derating. *Table 39* provides examples of frame timing for 720p30.

Table 39. 720x1280 @ 30 fps in RAW10 (CSI2/CCP2)

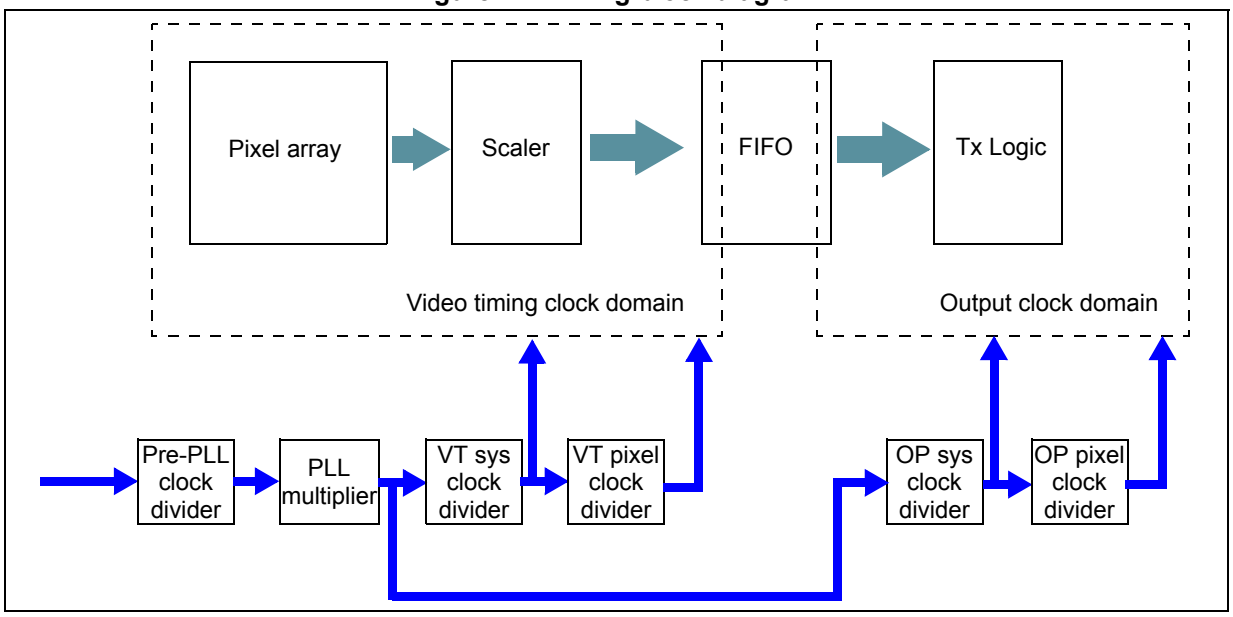
Ext Clk Freq	Pre-PLL Clk Div	PLL multiplier	VT Sys Clk Div	VT pixel Clk Div	VT pixel clock	OP Sys Clk Div	OP pixel Clk Div	OP pixel clock	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
12.00	2	106	1	10	63.6	1	10	63.6	2750	770

6.2.4 Derating

To provide a wide range of data rate reduction options the full image scaler is able to reduce the data and therefore data rates in both the horizontal and vertical directions. In the VX6953CB this is achieved by the use of a FIFO between video timing and output clock domains.

It is therefore necessary for the host to configure the OP clock domain to ensure that the FIFO neither overflows or underflows

Figure 22. Timing block diagram



Derating shows the difference between the video timing domain and the output clock domain.

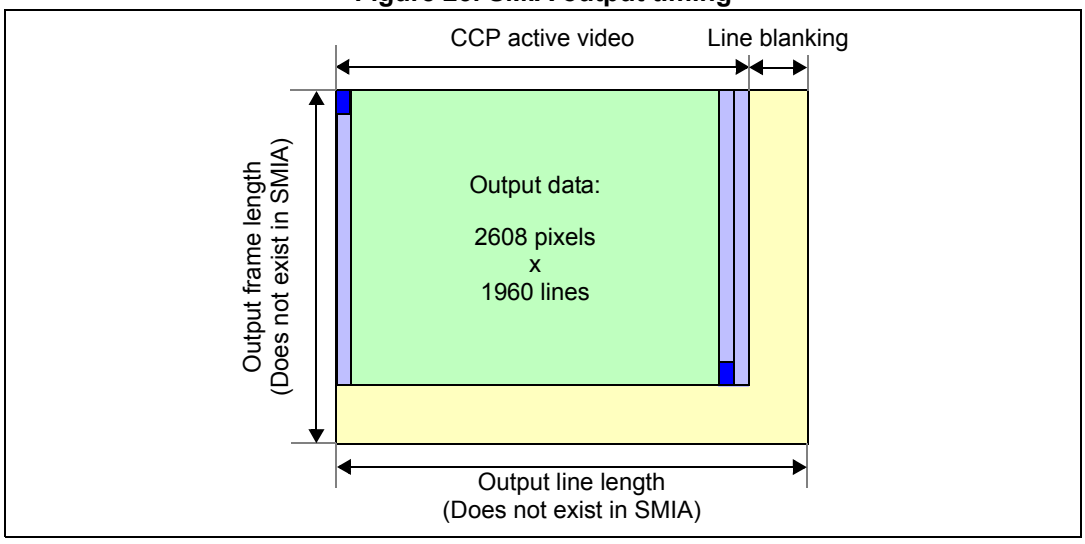
$$\text{derating} = \frac{\text{op\_sys\_clk\_div} * \text{op\_pix\_clk\_div}}{\text{vt\_sys\_clk\_div} * \text{vt\_pix\_clk\_div}}$$

FIFO

The FIFO is used to implement the data rate reduction required for profile 1 and 2 operation.

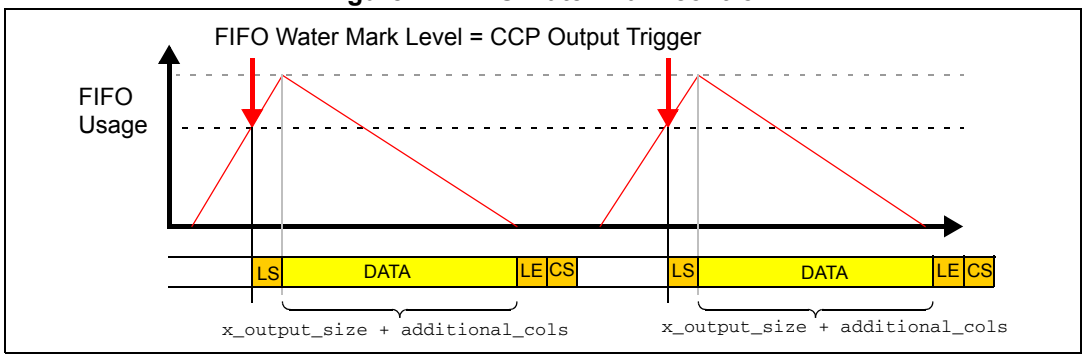
The concept of an output frame length and a line length for the output timing domain does not exist for SMIA devices such as the VX6953CB. This is a result of the FIFO input data patterns being different depending on scaling factor and if the data is co-sited or Bayer sampled, which results in variable interframe and interline blanking time between lines and between frames.

Figure 23. SMIA output timing



When the FIFO reaches a certain level of usage the CCP transmitter starts outputting a line containing x_output_size pixels. This then naturally tracks any variation in the input data rate, if the water mark is set correctly underflow is not possible.

Figure 24. FIFO water mark control



If the derating factor >= downscale factor then the average input rate of a burst of a line of scaler output data into the FIFO is always faster than the output data rate, in this case the fifo_water_mark_pixels can be set to eight as the FIFO input data rate is always faster than the FIFO output data rate.

If the derating factor < downscale factor then the average input rate of a burst of a line of scaler output data into the FIFO is slower than the output data rate, in this case the fifo_water_mark_pixels must be set to avoid underflow.

Calculate the floating point value of the fifo_water_mark_pixels:

$$\text{fifo\_water\_mark\_pixels(flt)} = \frac{\text{scale\_factor - derating}}{\text{scale\_factor}} * \text{x\_output\_size}$$

Then round up this value;

$$\text{fifo\_water\_mark\_pixels} = \text{fifo\_water\_mark\_pixels(flt)} + 40$$

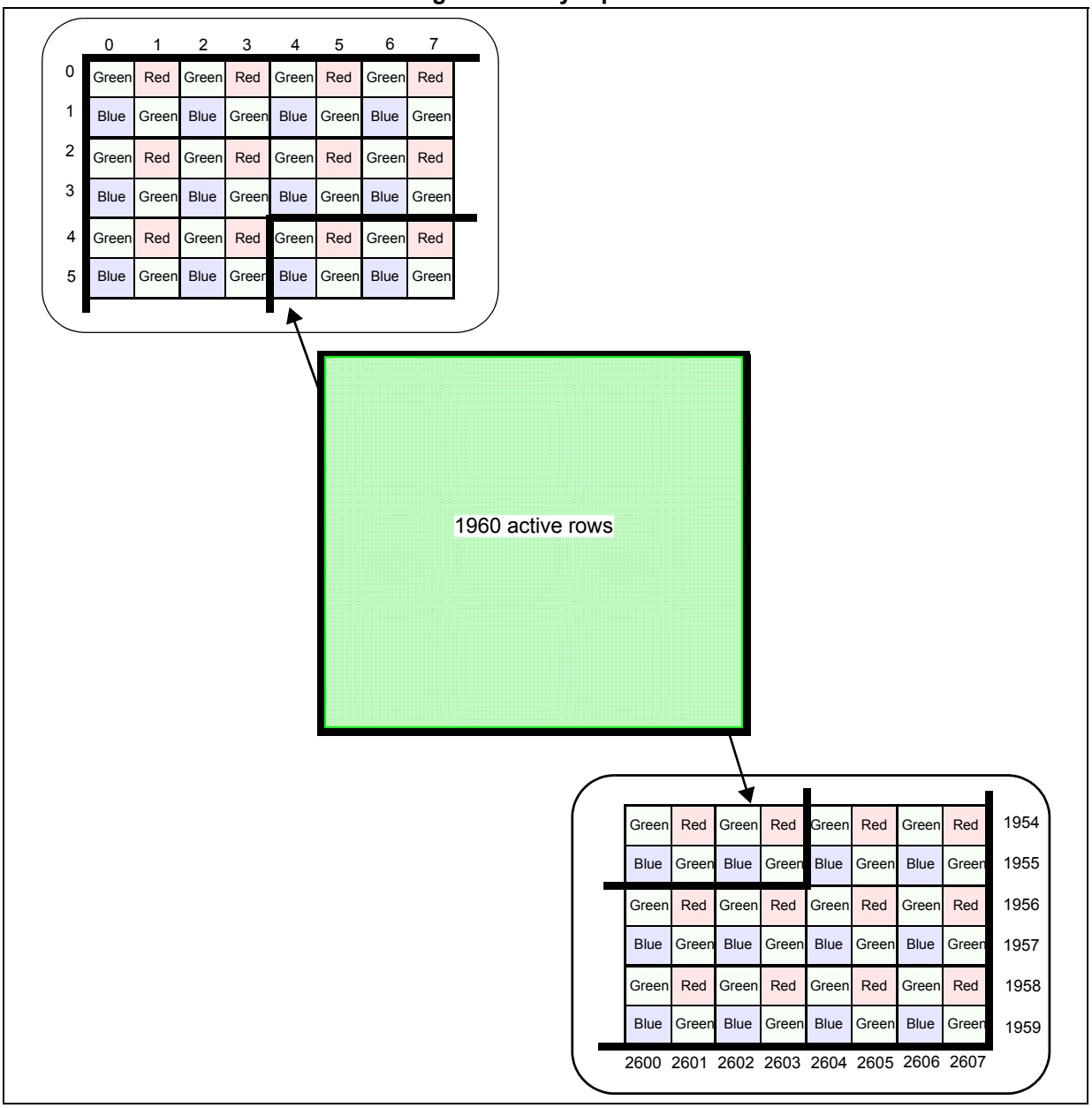
6.3 Bayer pattern

The three color (red, green, blue) filters are arranged over the pixel array in a repeated 2 x 2 arrangement known as the Bayer pattern. When the sensor array is read, the output order of red, green, blue depends on the settings of vertical flip and horizontal mirror.

See *Figure 25* for read-out order for the default settings of vertical flip and horizontal mirror both turned off. Vertical flip will change the first line to be output from a green/red line to a blue/green line and horizontal mirror will change the sequence within a line, say, green/red to red/green.

As shown in *Figure 25*, the first pixel to be readout from the imaging array will be green followed by red.

Figure 25. Bayer pattern



6.4 Image compression

The objective of the image compression is to reduce the required bandwidth in transmission between the sensor and the host.

The key features of the DPCM/PCM compression algorithm are:

- visually lossless
- low cost implementation (no line memories are required)
- fixed rate compression

The 10-bit to 8-bit DPCM/PCM image compression algorithm is supported by VX6953CB. 10-bit to 8-bit compression has the additional advantage that one pixel value equals 1 byte of data.

The level of compression is controlled through the CSI_data_format register. The same register is also used to enable and disable compression.

The compression_mode register is used to select the compression algorithm. Currently only the DPCM/PCM technique is supported. Therefore the value of this register is always 0x01.

The compression_capability register tells the host whether a sensor module does or does not have compression and, if it has compression, what is the compression technique. Again currently only the DPCM/PCM technique is supported.

Please also refer to section 10 of the SMIA1.0 specification document.

6.5 Exposure and gain control

VX6953CB does not contain any form of automatic exposure control. To produce a correctly exposed image the integration period and analogue gain for the pixels must be calculated by an exposure control algorithm implemented externally. The parameters are the written to the VX6953CB using the CCI interface.

The exposure control parameters available on VX6953CB are:

- fine integration time
- coarse integration time
- analog gain
- digital gain

The exposure control parameter registers are defined in *Chapter 4 on page 29*.

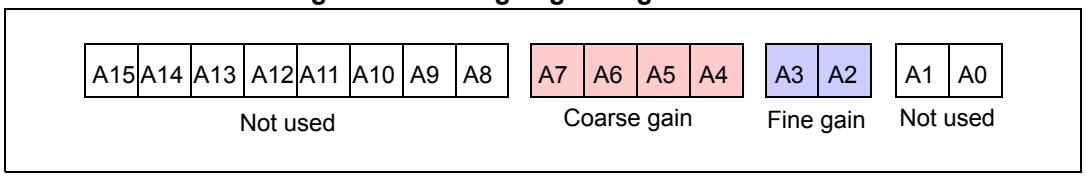
Integration time and analogue gain capability registers should be used to determine the exposure control parameter limits for a given video timing configuration. See Section 6.7 of the SMIA 1.0 part 1 specification for more information on how to interpret the integration and gain capability registers and how to calculate exposure and gain limits.

6.5.1 Analogue gain model

VX6953CB only supports the single global analog gain mode. VX6953CB has a 16-bit register (0x0204 and 0x0205) to control analog gain. However, only 4 bits are supported by the SMIA1.0 description. Two extra bits can be used for fine gain between values 8 and 16 but their description is not currently supported by SMIA1.0 specification.

Figure 26 shows how the analog gain bits are used for VX6953CB. **Use only Coarse Gain bits for standard 1/x functionality.**

Figure 26. Analogue gain register format



The following generic equation describes VX6953CB coarse gain behavior specified by the analog gain description registers 0x008A - 0x0093:

$$gain = c0 / (m1 \cdot x + c1)$$

where:

- m1 = -1
- c0 = 256
- c1 = 256

Table 40 specifies the valid analog gain values for VX6953CB.

Table 40. Analog gain control

Gain value (0x0204/0x0205)	Coarse gain code [A7:A4]	Coarse analog gain	Fine gain code [A3:A2]	Fine analog gain
0x0000	0000	0.0 dB (x1.00)	00	N/A
0x0010	0001	0.6 dB (x 1.07)	00	N/A
0x0020	0010	1.2 dB (x1.1)	00	N/A
0x0030	0011	1.8 dB (x1.2)	00	N/A
0x0040	0100	2.5 dB (x1.3)	00	N/A
0x0050	0101	3.3 dB (x1.5)	00	N/A
0x0060	0110	4.1 dB (x1.6)	00	N/A
0x0070	0111	5.0 dB (x1.8)	00	N/A
0x0080	1000	6.0 dB(x2.0)	00	N/A
0x0090	1001	7.2 dB (x2.3)	00	N/A
0x00A0	1010	8.5 dB (x2.7)	00	N/A
0x00B0	1011	10.1 dB (x3.2)	00	N/A
0x00C0	1100	12.0 dB (x4.0)	00	N/A
0x00D0	1101	14.5 dB (x5.3)	00	N/A
0x00E0	1110	18.1 dB (x8.0)	00	N/A
0x00E4	1110	fine ctrl	01	19.2 dB (x9.1)
0x00E8	1110	fine ctrl	10	20.6 dB (x10.7)
0x00EC	1110	fine ctrl	11	22.1 dB (x12.8)
0x00F0	1111	24.1 dB (x16.0)	00	N/A

Also refer to section 6.3 of the SMIA1.0 specification document.

6.5.2 Digital gain

To help compensate for the relatively coarse analog gain steps, VX6953CB contains a digital multiplier to “fill” in the missing steps. By mixing analog and digital gain it is possible to implement 3% gain steps across the full 1x to 16x gain range.

The details of the digital gain implementation are:

- four individual 16-bit digital channel gains - one per Bayer channel
  - digital_gain_greenR (0x020E and 0x020F)
  - digital_gain_red (0x0210 and 0x0211)
  - digital_gain_blue (0x0212 and 0x0213)
  - digital_gain_greenB (0x0214 and 0x0215)
- the digital gain range for each channel is 1.000 to 1.96875 in steps of 0.03125 (1/32) that is, five fractional bits
  - digital_gain_min {0x1084:0x1085} = 0x0100 (1.00)
  - digital_gain_max {0x1086:0x1087} = 0x01F8 (1.96875)
  - digital_gain_step {0x1088:0x1089} = 0x0008 (0.03125)

6.5.3 Integration and gain parameter retiming

The modification of exposure parameter (coarse, fine, clock division or gain) register values does not take effect immediately.

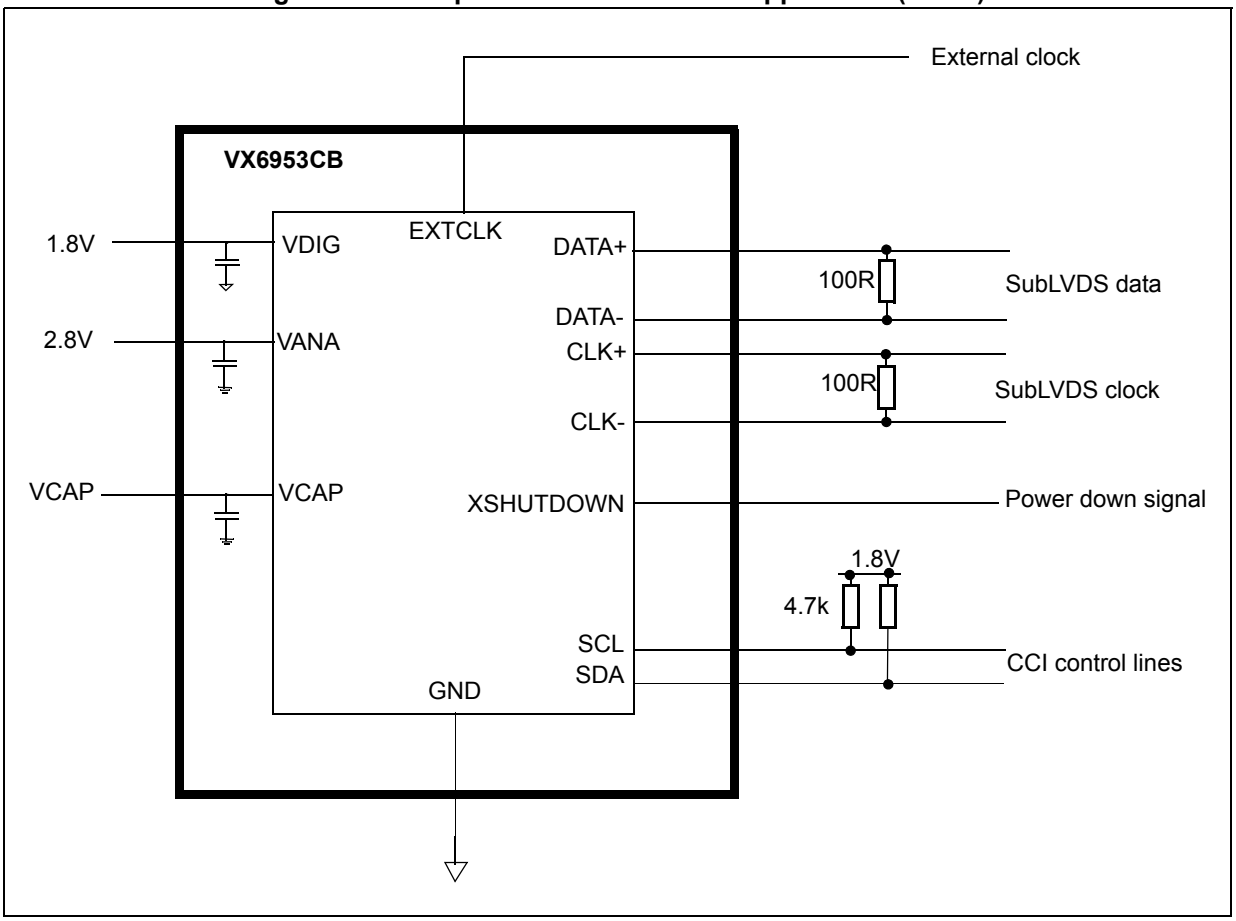
The exact time at which changes to certain parameters take effect is controlled both to ensure that each frame of image data produced has consistent settings and that changes in groups of related parameters can be synchronized.

A group of parameter changes is marked by the host using a dedicated Boolean control parameter, grouped_parameter_hold (register 0x0104). Any changes made to “retimed” parameters while the grouped_parameter_hold signal is in the “hold” state will be considered part of the same group. Only when the grouped_parameter_hold control signal is moved back to the default “no-hold” state will the group of changes be executed.

7 Application

7.1 Schematics

Figure 27. Example of a mobile camera application (CCP2)



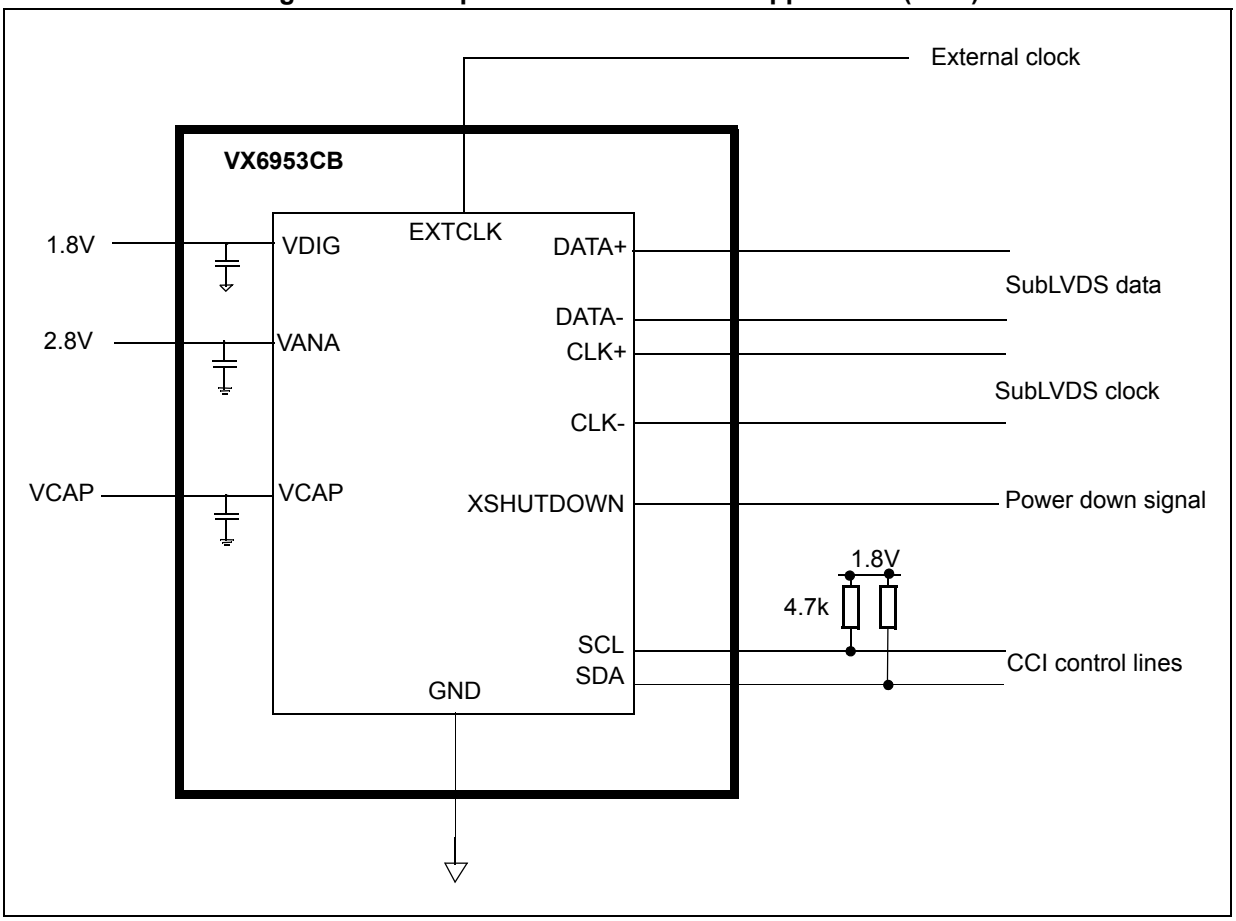
Note: CCP 100R termination may be internal to a subLVDS receiver (for example, STV0986/STV0987).

Note: No external supply decoupling capacitors are required as the necessary components are integrated into the module.

Note: If the master CCI bus is powered to voltage > VDIG+0.5V, it is mandatory to insert a level shifter on the sensor SCL and SDA lines to prevent from any electrical damage.

Note: EXTCLK has a SCHMITT TRIGGER input.

Figure 28. Example of a mobile camera application (CSI2)



Note: The CSI-2 receiver is mandated to have an internal termination which is dynamically switched in and out depending on whether the link is in HIGH SPEED mode or in LOW POWER mode. This transition happens every line.

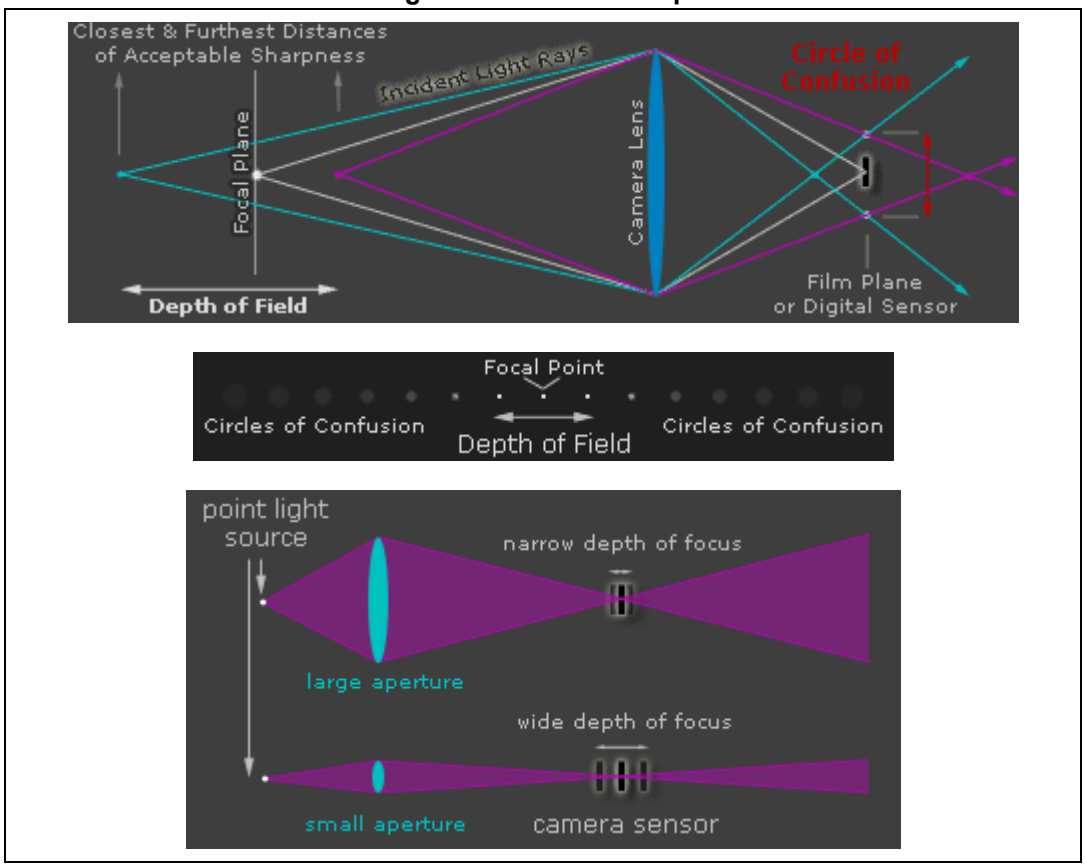
7.2 Personality file and firmware updates

Contact ST for the latest copy of the sensor “Startup procedure application note” that details the procedure to initialize the sensor prior to streaming. It includes FW and sensor optimization settings. The settings must be written through the CCI link to overwrite the default register settings, see *Chapter 4: Register map on page 29*.

8 EDOF control

The VX6953CB module uses a fixed focused lens with optical aberrations that the EDoF reconstruction engine is designed for so as to recover the resolution and increase the depth of field in the range of 15 cm to infinity. The focus is tuned for far distances > 2m but for closer distances where a standard fixed focus camera would show a blur image, the EDoF correction is capable of recovering significantly the resolution.

Figure 29. What is sharp?



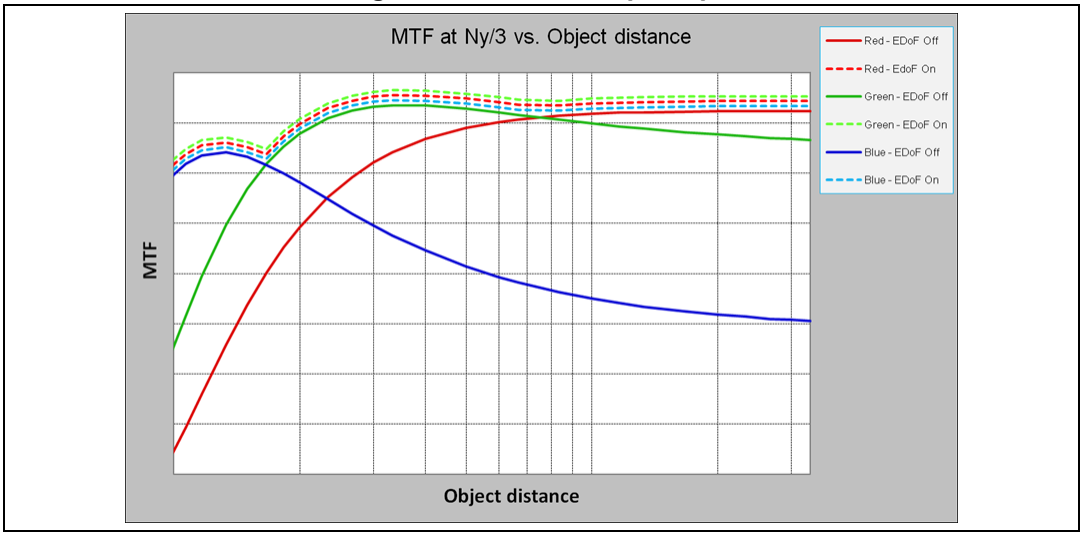
Some optics facts:

- The depth of focus narrows with reduction in object distance or with aperture increase.
- If the lens is focussed at the hyper-focal distance, the sharpness will be the same from hyperfocal/2 to infinity.
- The Depth of field is defined by the range of scene distances that appears acceptably sharp in the image.
- The size of a pixel (1.4um) can be defined as a blurred spot. A blurred spot smaller than 1.4um is registered as sharp. Above that value the spot will look blurred (refer to circle of confusion graph).

Considering the above points, EDoF aims to make the blur spot invariant (or change its reference) over a range of objects distances, thus defeating the obvious geometric optical effects to enhance the Depth of Field.

The plot in *Figure 30* shows the EDoF main principle:

Figure 30. EDoF main principle



8.1 EDoF capabilities

The EDoF reconstruction engine is applied to the image after defect correction. It has denoising, sharpening, deconvolution algorithms among others that allow recovering the resolution.

The end user should not use the EDoF IP as a sharpness block. EDoF has a depth of field recovery role. Oversharpening the image using EDoF before the HOST image processing might alter the final image quality.

The EDoF reconstruction engine can improve the depth of field for a coloured image in the range of 30 cm to infinity and for a monochrome image below 30 cm.

The EDoF block works with ranges of distances for which the correction applied will be different:

- 5 Mpixel EDoF camera:
  - Super Macro mode: < 30cm
  - Macro mode: 30cm to 59cm
  - Portrait: 60cm to 249cm
  - Landscape: 250cm to infinity

The distance estimation analyzes gradients and relative sharpness among channels.

It first returns a measure of the sharpest channel in the image giving a macro ‘vote’ when the sharpest channel is the blue one, portrait when it’s the green and landscape when it’s the red.

The relative sharpness among channel varies with the object distance but also in the field of the image (field curvature), so the votes are then weighted by calibration data in order to obtain the most appropriate mode or distance at the output.

Note: The aim of the distance estimation is not to obtain a precise distance but to select the best parameterization for the correction to be applied in capture, therefore the returned distance or specified distances range is indicative only.

Like an auto-focus module:

- The algorithm has failure cases, but the correction is constrained in order to always have acceptable image quality even if not optimal.
- For a single image several modes are often possible and giving same level of image quality.

  For overlap distances (between macro and portrait modes, or between portrait and landscape modes), two of the channels may have the same level of sharpness, so any of the two corresponding distances could be returned, depending on scene content and field curvature of the module.

For scenes with objects at different distances, any of the three distances could be returned depending on content of the scene, field curvature of the module and spatial weights used for estimation (edof_estimation_control).

Supermacro mode is used for bar code and business card reading. Supermacro mode uses a monochrome image. Below 30cm distance, the MTF is lost and there is too little Green and Red pixel information to build a colored image. However, the blue pixel has enough MTF to reconstruct a monochrome image.

8.2 Control Interface

VX6953 has a 100 kHz/400 kHz I^2C compatible 2-wire control interface. It uses the SMIA 16-bit index, 8-bit data message format. The CCI interfaces allows the programming of the EDoF control register.

8.3 EDOF control registers [0x0B80 to 0x0B8A]

Table 41. EDOF registers [0x0B80 to 0x0B8A]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B80		edof_mode	8UI	00	RW	EDOF control 0 - EDOF disabled (power saving) 1 - EDOF application (Capture) 2 - EDOF estimation (Preview)
0x0B82		edof_est_focus_distance	8UI	32	RO	The estimated focus point (cm)
0x0B83		edof_sharpness	8UI	00	RW	EDOF sharpness control 0x7F: Manual mode 0x80 to 0xFF: Automatic mode
0x0B84		edof_denoising	8UI	00	RW	EDOF denoising control
0x0B85		edof_module_specific	8UI	00	RW	EDOF noise vs details control

Table 41. EDOF registers [0x0B80 to 0x0B8A] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B88	Hi	edof_focus_distance	16UI	00.32	RW	Value supplied by the host which is used by VX6953CB for focus distance (in cm). 0x0000 to 0x7FFF - manual mode 0x8000 to 0xFFFF - limited auto
0x0B89	Lo					
0x0B8A		edof_estimation_control	8UI	00	RW	EDOF estimator control 1 - uniform 2 - centre weight 4 - large spot 8 - narrow spot

8.3.1 EDoF_Mode (0xB80)

The EDoF block can be disabled or enabled. The interest of disabling this block would be to save some power consumption. When enabled, EDoF has two modes:

- Estimation mode

  This mode is dedicated to image preview (Viewfinder) only. EDoF correction is not applied but statistics are gathered for distance estimation. Estimation mode can be full resolution, subsampled or binned image up to a maximum of x4 in both directions. If too much subsampling is performed the image out of the sensor becomes sharp and focus distance estimation is not possible. This is similar to the mechanical auto focus control which requires an image large enough to allow detecting sharpness variation with focus.

  ISP should therefore ensure that at least the last frame before capture is set to either one quarter of the full resolution in each direction or a higher resolution.

  In other words, as an example, this means that the minimum input image size when no crop is applied on the sensor is approximately 640 x 480 for a 5 Mpixel sensor.

- Application mode

  This mode is for capture (or snapshot) mode. The EDoF distance calculated during estimation is applied to the image. The application mode can only be enabled after the estimation mode has been selected, otherwise the EDoF correction will not be applied. EDoF cannot be applied to subsampled or binned images as it is not necessary to correct images when they are subsampled as the image blur introduced by the lens does not need to be corrected when images are downscaled. No focus distance estimates are performed in application mode, even in multi-shot mode.

For preview mode, set the 0x0B80 register in estimation mode:

```
0x0B80 = 0x02; // EDOF enabled for estimation mode
```

For capture mode, set the 0x0B80 register in application mode:

```
0x0B80 = 0x01; // EDOF enabled for application mode
```

Note: Before enabling application mode, estimation mode has to be applied for a minimum of one frame so as to estimate the EDoF focus distance. This information is used in application mode when the image data is corrected. If estimation mode is not enabled prior to application mode, no correction will be applied to the captured image.

8.3.2 EDoF_est_focus_distance (0x0B82)

The edof_est_focus_distance register (0x0B82) is Read Only. This register tells the user the estimated focus point that the EDoF function has calculated. Register values for a 5 Mpixel EDoF camera are:

- Macro mode: 0x1E
- Portrait: 0x3F
- Landscape: 0xFA

8.3.3 EDoF tuning sliders (0xB83 to 0x0B85)

The three key registers for the end user tuning are the sharpness, denoising and noise versus detail registers.

Recommended settings

For the recommended settings of the EDoF sliders (0x0B83 to 0x0B85) refer to the relevant personality file, see *Section 7.2 on page 68*.

Note: Upon request, ST can provide the EDoF application note that gives details for HOST tuning.

8.3.4 EDoF focus distance (0x0B88)

For automatic mode, the value range is 0x8000 to 0xFFFF. Whatever value is selected within this range will enable automatic distance estimation. ST recommends setting the EDoF estimation mode to automatic mode. In this mode, when the user selects capture mode, the EDoF processing will automatically use the last estimate of the focus distance obtained in preview mode.

Note: If it is necessary to switch between estimation mode and application mode while in software standby, then a patch must be loaded to enable this feature. If the patch is not loaded, switching must be performed whilst streaming. Otherwise the host must read the estimation data (from register 0x0B82) immediately before going to software standby and rewrite that data (to register 0x0B88) before restarting streaming in application mode.

For manual mode, the value to be set in the register is the value of the distance in cm. The range is 0x0000 to 0x7FFF. If you want to go to one of the following modes, apply the specified value for a 5 Mpixel EDoF camera:

- Super Macro mode: 0 to 29cm
- Macro mode: 30 to 59cm
- Portrait: 60 to 249cm
- Landscape: 250 to 32767cm

Supermacro mode only works in manual mode. Refer to *Section 8.4: Supermacro mode* for more detailed information.

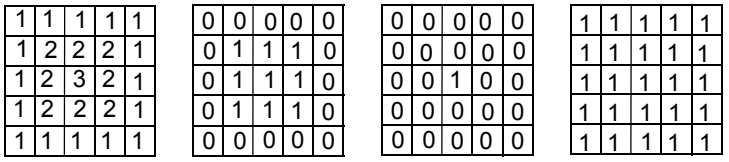
8.3.5 EDoF estimation control (0x0B8A)

This register selects the region of interest (ROI) on which to apply the distance estimation processing. Four different ROIs are available:

- 0 or 1: uniform
- 2: center-weighted
- 4: spot (large)
- 8: spot (narrow)

Considering the above order, with increasing values, the estimation will increase focus on objects in the centre of the image.

Figure 31. Focus strategy weightings



The image is arranged as 5x5 regions for the weightings.

8.4 Supermacro mode

Unlike the other modes (macro, portrait and landscape), supermacro mode cannot be managed by the automated distance range estimator. The reason is that at distances below 30cm, there is very little information in green and red channels though there is a significant energy in the blue channel. The distance estimator needs the four color channel information to estimate the distance. Below 30cm, unless the distance is manually programmed using register 0x0B88, the EDoF correction will not be accurate.

For text or bar code reading, a monochromatic image can be used. EDoF supermacro mode can be used for that purpose as the EDoF reconstruction engine would use the blue channel information to calculate the suitable sharpness and denoising.

To enable supermacro mode, the user has to manually program the register 0x0B88 to set a value for distances below 30cm. The register value being the value of the distance in cm.

8.5 Video modes and EDoF

Setting a video mode implies targetting a reduction in the image size and an increase of the frame rate. The ST 5 Mpixel cameras are SMIA profile 2 compliant therefore output images can be downscaled in both X and Y dimensions either using a digital scaling post EDoF engine or by subsampling pixels before the EDoF engine.

Downsampling or binning by a factor of two or more in each direction increases the sharpness enough to remove the need to process the raw image. Therefore image processing is disabled in Preview mode within the EDoF processor in order to save power and the image is simply copied on the output. The consequence is that the image must be subsampled by a factor of 2x2 at least to get distance information and a usable raw image.

To summarize, it is recommended that EDoF is forced to landscape mode when in video:

- if subsampling or binning is used and output image is at least full size image/4
- if a scaling+cropping method is used from a full size image to output a smaller image and output image < (2*full size image)/3
- for a crop of a full resolution image

8.6 EDoF and white balance

The EDoF reconstruction engine requires the white balance gains to be programmed by the HOST (by I2C writes) frame after frame to the colour feedback register (0x0B8E-0x0B95) of the sensor. These white balance gains MUST BE corresponding the WB output ones to prevent from fringing artefacts. These gains are also used for the sensor adaptive lens shading correction if enabled.

The white balance gains are required in both preview and Capture modes.

The four host white balance gains to be programmed are listed in *Table 42*.

Table 42. Color feedback registers [0x0B8C to 0x0B95]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B8C	Hi	colour_temperature	16SR	00.00	RW	Not supported by VX6953CB
0x0B8D	Lo					
0x0B8E	Hi	host_WB_stats_green_red	16UR	01.00	RW	White balance gains to be applied by the host. These stats are used by the EDOF and the adaptive AV to estimate the color temperature of the scene.
0x0B8F	Lo					
0x0B90	Hi	host_WB_stats_red	16UR	01.00	RW	
0x0B91	Lo					
0x0B92	Hi	host_WB_stats_blue	16UR	01.00	RW	
0x0B93	Lo					
0x0B94	Hi	host_WB_stats_green_blue	16UR	01.00	RW	
0x0B95	Lo					

As a preliminary correlation exercise between ST, the end user and the EDoF engine provider, we recommend that the end user verifies that the white balance gains calculated by the host auto-white balance processing engine for a 18% grey chart under D65 illuminant at 1000 lux are equal to the following values (normalized on green channels):

- Green channels gain = 1 (normalized gain)
- Red channel gain = 1.5
- Blue channel gain = 1.12

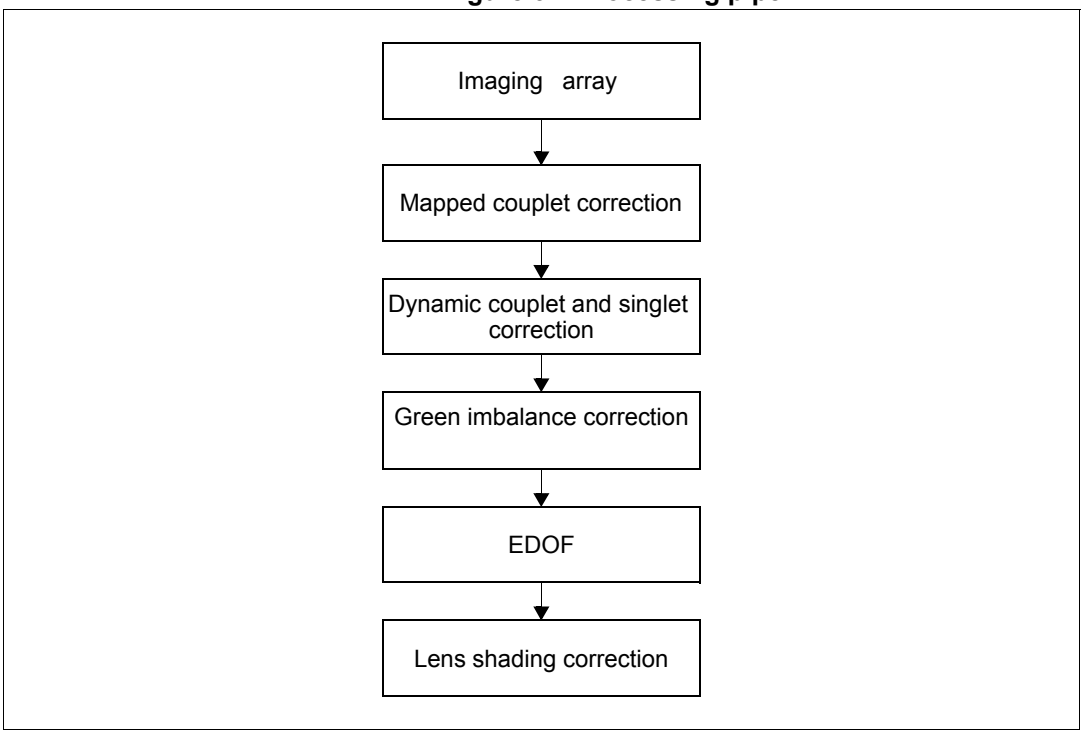
9 Image optimization

The sensor has the following image optimizations:

- mapped couplet correction (using couplet location stored in NVM memory)
- dynamic couplet and singlet correction
- green imbalance correction
- depth of field correction (EDoF)
- lens shading correction

Figure 32 shows the processing pipe.

Figure 32. Processing pipe



Note: Defect correction must be enabled as it occurs before the EDoF processing. Defect correction settings are given in the Personality file (parameters to be loaded during sensor initialisation), see Section 7.2 on page 68.

9.1 Defect categorization

9.1.1 Pixel defects

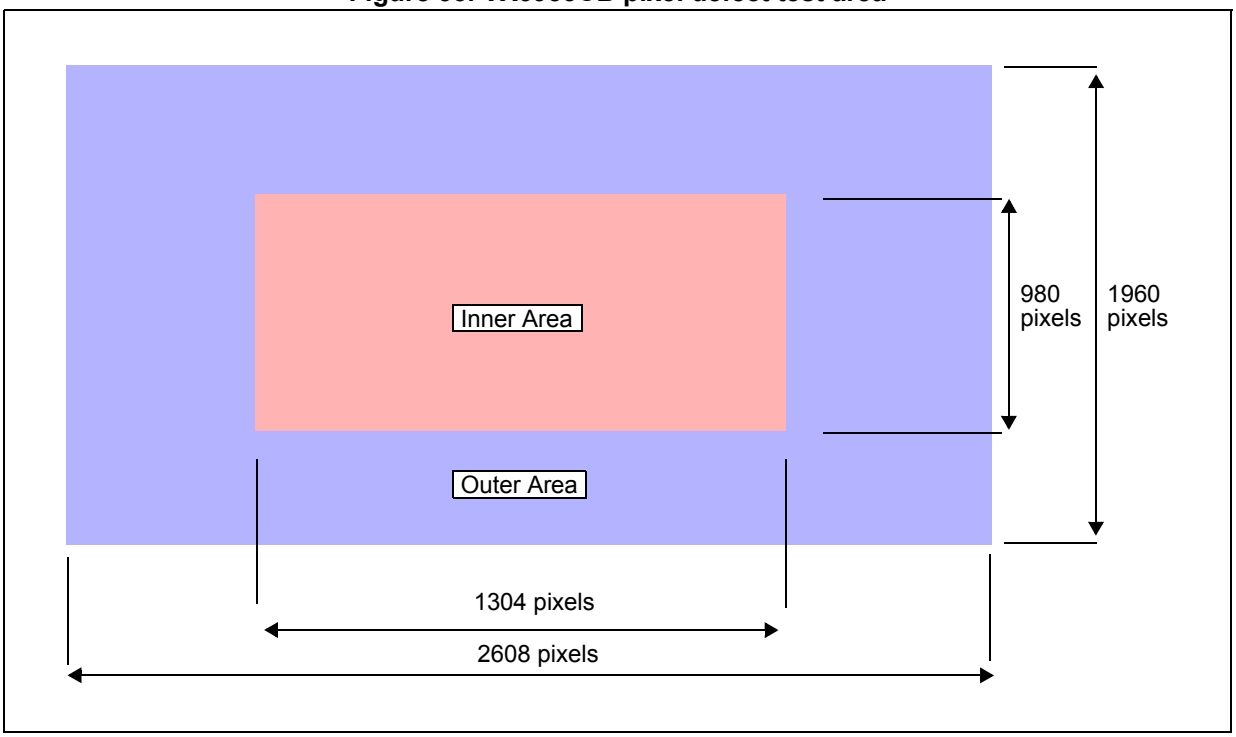
Illuminated defects are tested with a flat field illumination and a pass-fail criteria that is a percentage deviation from a local mean. In order to effectively test the sensor in a reasonable test time, it is necessary to put the limits of gain error above the normal noise distribution of photon shot noise and sensor noise otherwise false single pixel fails are detected. A typical defect criteria for single-pixel gain errors is ± 9%. In fact, any element in the array outside ±9% is a “minor” fail, and outside of ± 25% is a “major” fail.

Note: The defect detection method is applied to raw Bayer images.

9.1.2 Sensor array area definition

For specific aspects of pixel defect testing the image sensor array is subdivided into two regions as illustrated in *Figure 33*.

Figure 33. VX6953CB pixel defect test area



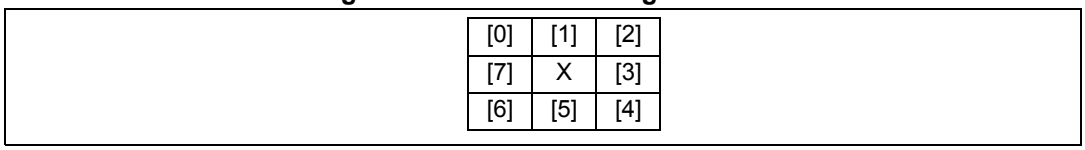
The inner array in *Figure 33* is centre justified, in the x and y axis, with respect to the outer array. The inner array is 50% of the full width and 50% of the full height of the larger outer array, therefore the inner array is one quarter of the area of the outer array.

Note: The border pixels (outer eight rows and columns) affect the image quality of the reconstructed picture to a lesser degree than the actual image pixels (2592 x 1944), due to their lower contribution within the reconstruction algorithm, but for simplicity we test them as the image pixels, hence the test image size for defects will be 2608 x 1960.

9.1.3 Pixel fault numbering convention

The pixel notation is shown in *Figure 34*. For the purposes of the test the 3 x 3 array describes nine Bayer pixels of a common color, that is, all the pixels will either be Red, Green[(a)] or Blue. The pixel under test is **X**. If a pixel under test is on the edge, the array is reduced to its existing neighbor pixels (that is, the first pixel uses only a 2 x 2 array).

Figure 34. Pixel numbering notation



9.1.4 Single pixel faults

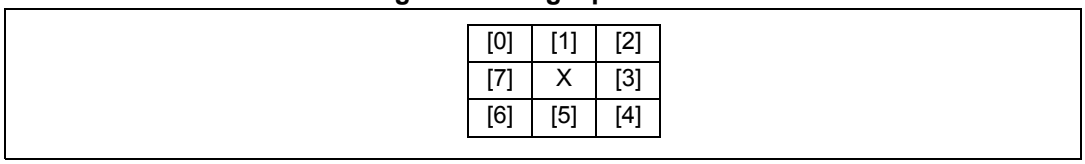
STMicroelectronics defines a single pixel fail as a failing pixel with no adjacent failing same color neighbors.

A single pixel fail can be:

- “stuck at white” where the output of the pixel is permanently saturated regardless of the level of incident light and exposure level
- “stuck at black” where the pixel output is zero regardless of the level of incident light and exposure level (major fail) or simply a pixel that differs from it’s immediate neighbors by more than the test threshold (minor fail).

In the example in *Figure 35*, the pixel **X** is a fail. For this pixel to be a single pixel fail the pixels at positions [0], [1], [2], [3], [4], [5], [6] and [7] must be “good” pixels that pass final test. The implemented test program will pass a sensor with up to the defined limit of single pixel faults per color channel. Defect correction algorithms will correct the pixel faults in the final image.

Figure 35. Single pixel fault



a. The Green pixels are split over two common channels, Green1 and Green2.

9.1.5 Couplet definition

A failing pixel at **X** with a failing pixel at position [0], [1], [2], [3], [4], [5], [6] or [7] such that there is a maximum of two failing pixels from the group of nine pixels illustrated in *Figure 36*. The example shown in *Figure 36* has the centre pixel and the pixel at position [7] failing the test criteria.

Figure 36. General couplet example

[0]	[1]	[2]
[**X**]	X	[3]
[6]	[5]	[4]

The basic couplet definition is further subdivided into minor and major couplets. With respect to the example in *Figure 36*, a minor couplet is defined as a defect pixel pair where one pixel can be an extreme fail, that is a stuck at black or stuck at white, but the second pixel in the pair must differ from the local pixel average by less than 25% of that average value. If the second pixel in the couplet differs by more than 25% of the local pixel average value then this would be defined as a major couplet.

In addition, couplets will be classified as being in the inner or outer area.

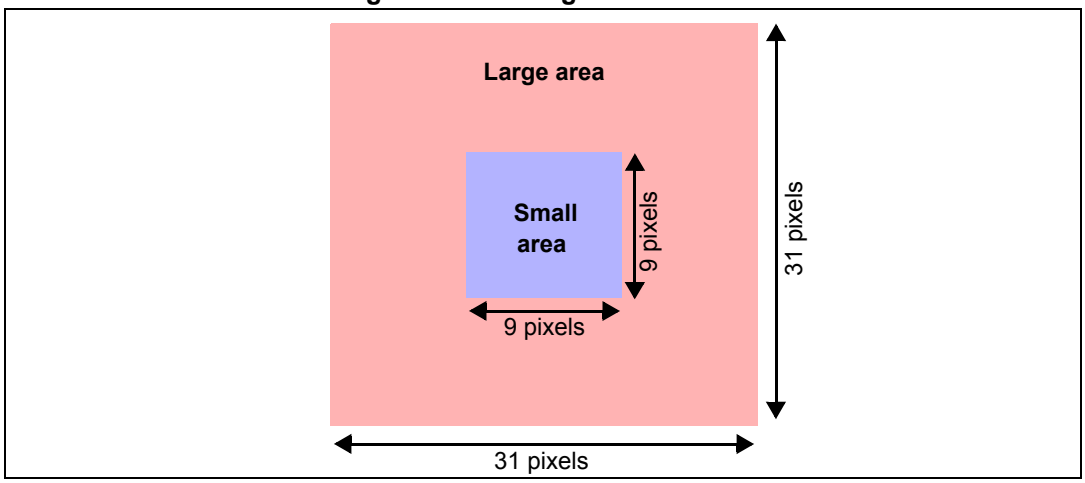
9.1.6 Physical aberrations

A specific test algorithm is also applied in production to identify and reject samples that display defocussed artefacts often referred to as blemishes or shapes. These artefacts are caused by scratches or contamination in the optical path away from the focal plane that is, on the IR glass or lens.

The test requires two regions to be defined:

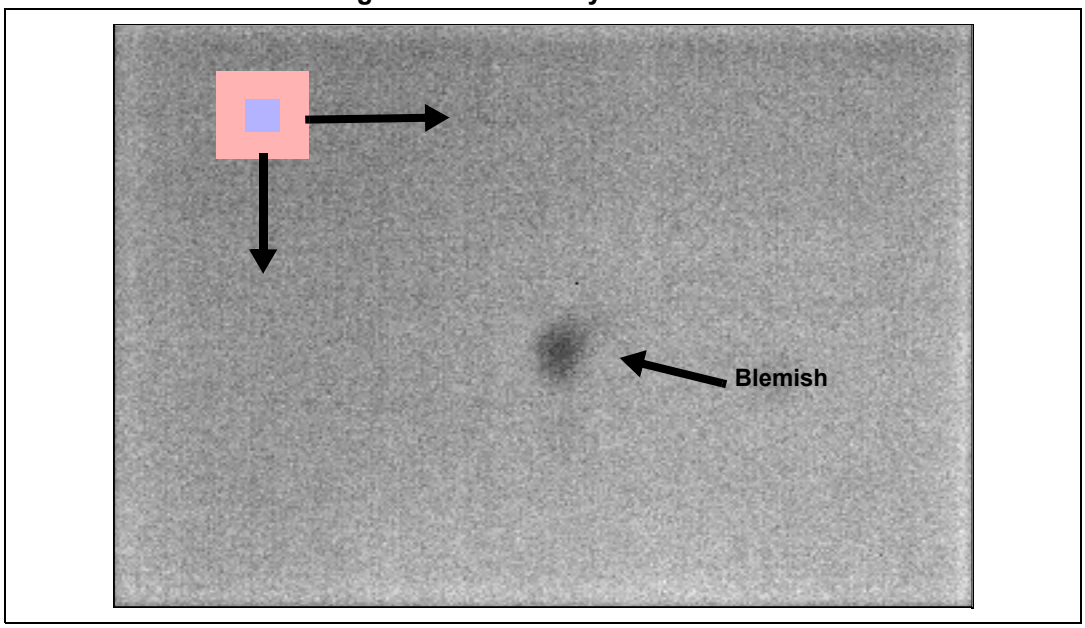
- a small area: 9 by 9 pixels with the pixel under test at the centre of this area (shaded blue in *Figure 37*)
- a large region, 31 by 31 pixels (shaded red in *Figure 37*)

Figure 37. Test region definition



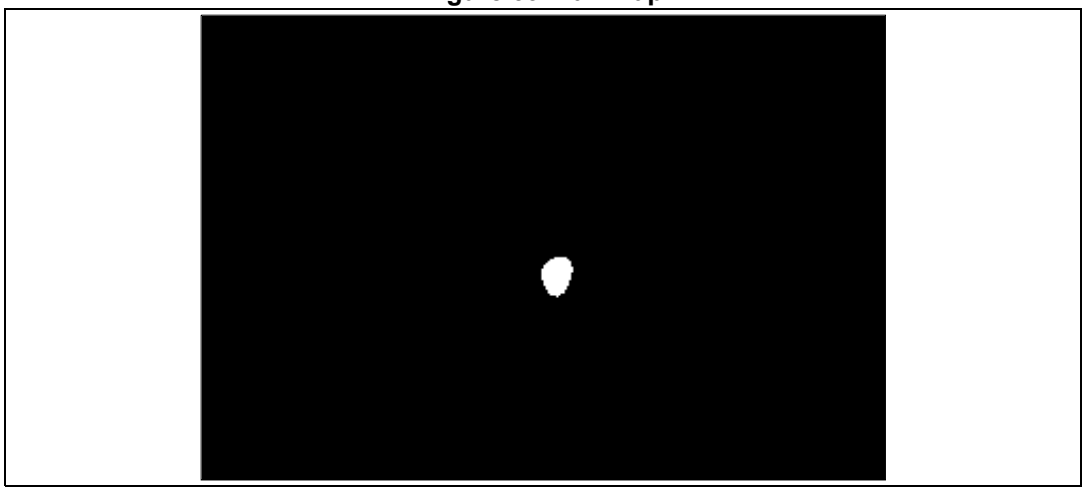
An average value is calculated for both the ‘small’ and ‘large’ areas. The areas are then scanned across each color channel separately.

Figure 38. Scan array for blemish



The next stage of the test is the creation of a pixel map for each color channel with the coordinates of the failing pixels. See *Figure 39*.

Figure 39. Fail map



A pixel location is identified as a fail in the map if it satisfies the following criteria:

Small_average < Large_average - (1.2% of Large_average)

or

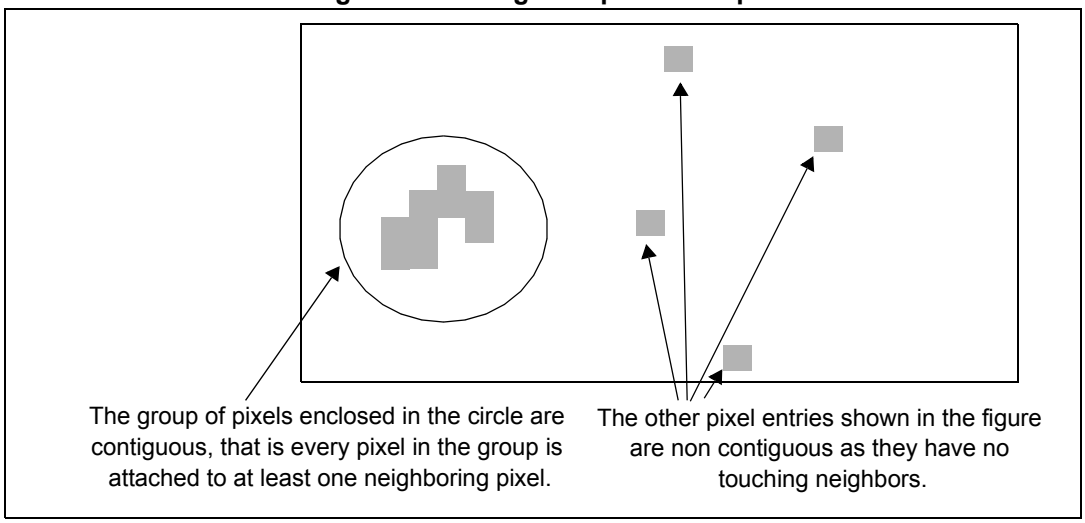
Small_average > Large_average + (1.2% of Large_average)

The contents of the fail map determines whether the sensor fails the physical aberration test. The module fail criteria is:

- Pass if <= 82 contiguous pixel entries in the failure map for each color channel.

An example of contiguous pixels entries is given in *Figure 40*.

Figure 40. Contiguous pixel example

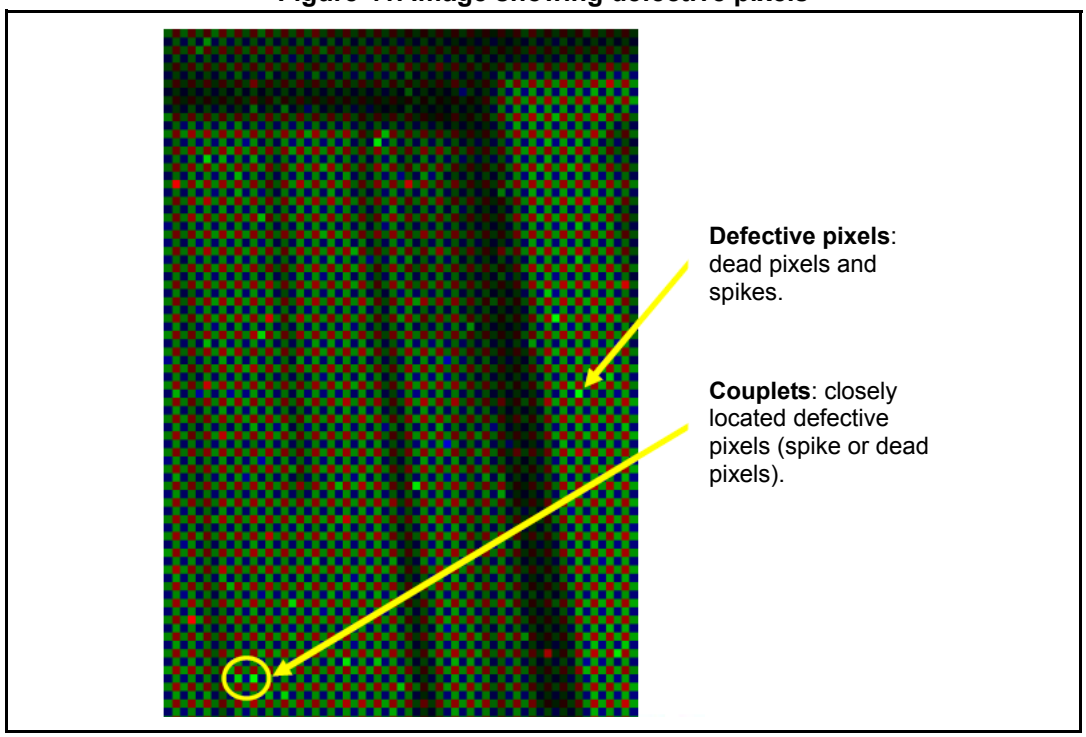


9.2 Defect correction

The defect correction algorithm dynamically detects and corrects single and couplet defective pixels in the imaging array. The weight of both correction filters can be adjusted. For recommended settings refer to the personality file.

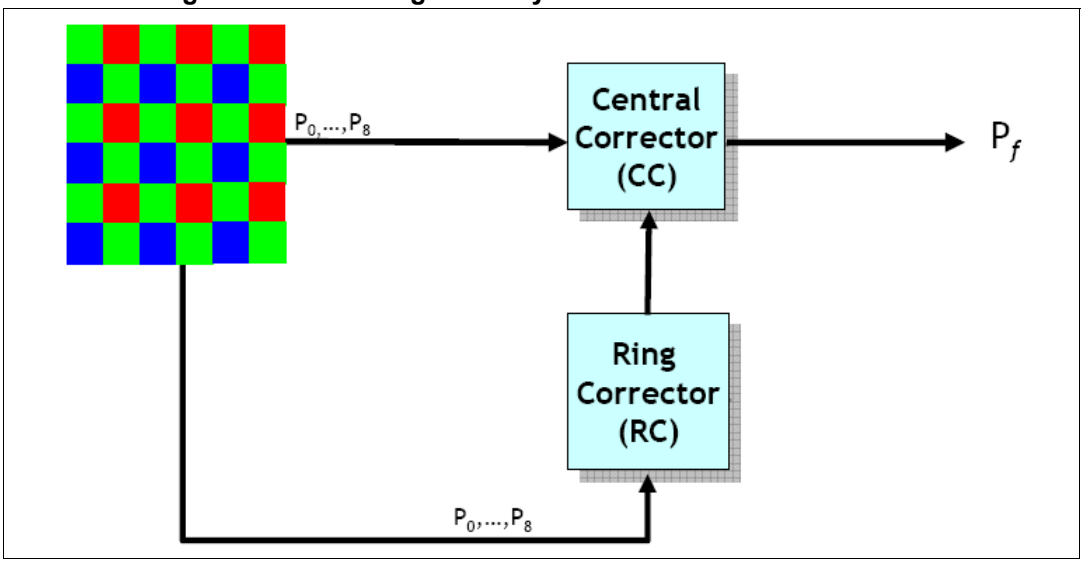
An image showing an example of defective pixels is shown below.

Figure 41. Image showing defective pixels



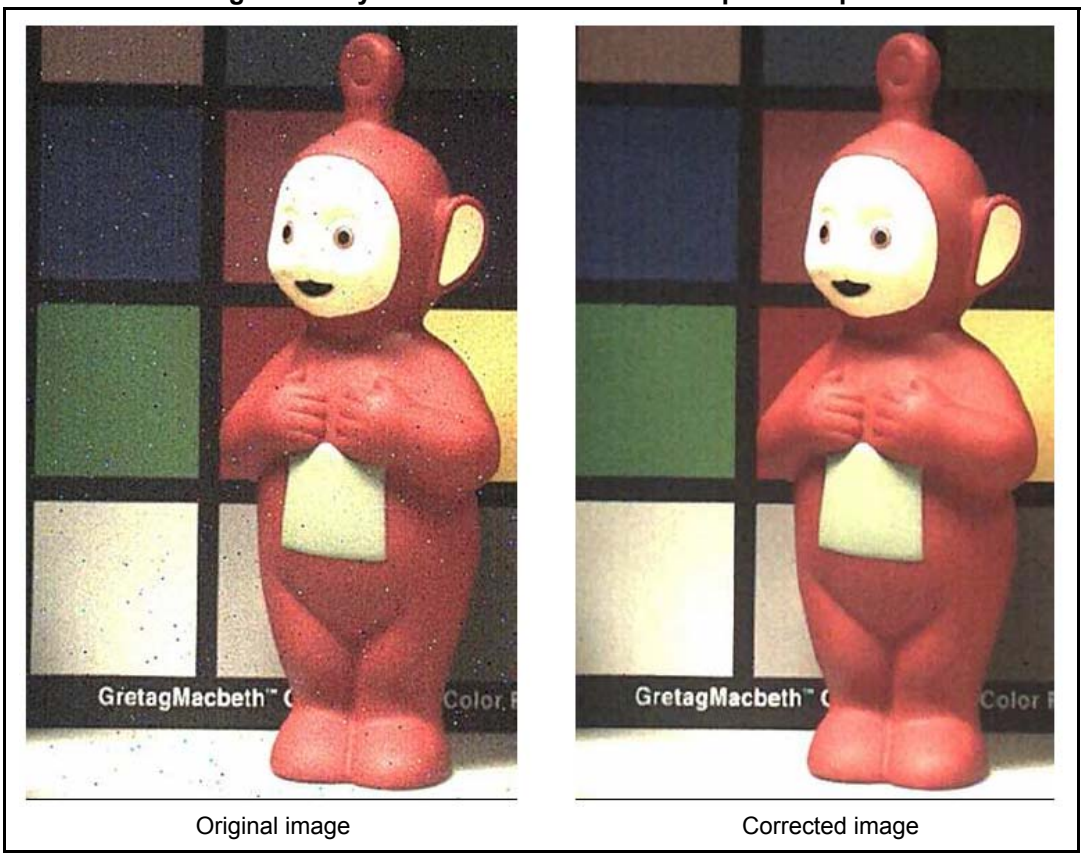
A simplified block diagram of the defective correction block is shown in *Figure 42*.

Figure 42. Block diagram of dynamic defect correction block



An example of an image before and after correction is shown in *Figure 43*.

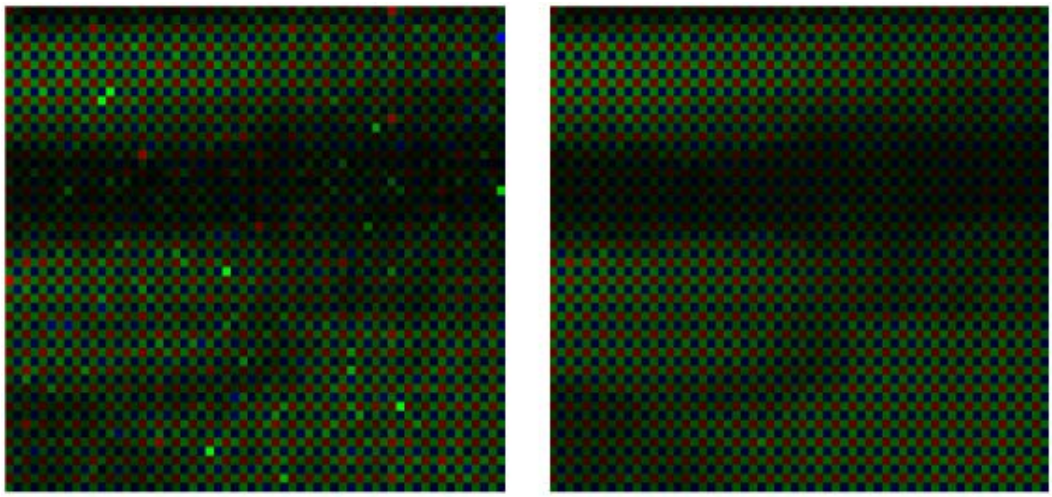
Figure 43. Dynamic defect correction output example



Original image Corrected image

An example of a corrected Bayer pattern is shown in *Figure 44*.

Figure 44. Corrected Bayer pattern



Colorized original Bayer Colorized corrected Bayer

9.3 Mapped couplet correction (Bruce)

The mapped couplet defect correction filter is designed to intelligently correct the first defect in a couplet thereby changing a couplet into a single pixel defect. Single pixel defects can then be corrected using the dynamic defect correction filter.

The mapped couplet correction filter requires exact coordinate information for each of the couplets to be repaired. The couplet coordinates are stored in non-volatile-memory (NVM) during production test. The mapped couplet correction filter does not operate in binning mode or in subsample mode and is automatically disabled.

The mapped couplet correction is controlled by register 0x0B05:

0 - Disable

1 - Enable

9.4 Green imbalance correction

Since ES2.0 modules, the sensor has an adaptive (four color temperature) green imbalance correction function which can be used to reduce the green imbalance in the sensor. Correction is carried out on the green-blue color plane only. The gain is calculated based on a term polynomial in x and y.

In order to optimize the green imbalance correction algorithm, the coefficients for each device are calculated under D65 lighting conditions and programmed in the NVM memory at production test.

Settings for three other color temperatures (cool white, TL83, and horizon) are calculated from characterization data and these are stored in the NVM memory.

The calculation of the color temperature is performed by the sensor using the color feedback registers. Therefore it is necessary for the host to supply the sensor with the white balance gains.

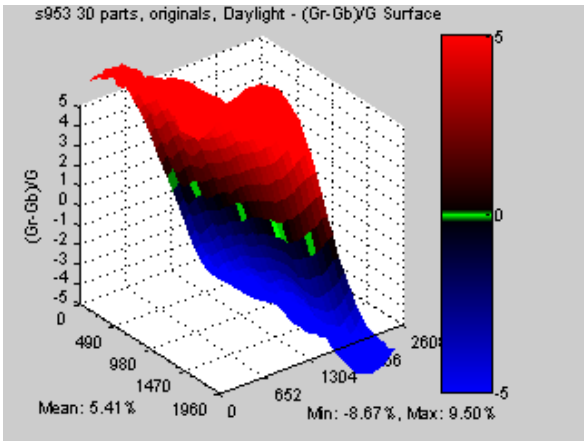
The green imbalance correction function can be used with the profile1 and profile 2 scaler and with crop and subsampling.

The green imbalance correction is controlled by register 0xFAA3 (0x3410 is the status register):

0 - Disable

1 - Enable

Figure 45. Green imbalance correction plots



Original plot

Corrected plot

9.5 Lens shading correction

The sensor has an onboard adaptive (four color temperature) lens shading correction function which can be used to reduce the effect of roll off in the optical system. Correction is carried out individually for all four color planes, each gain is calculated based on the distance from the image centre to the pixel in question using a nine parameterization term (DC offset, x, y, xy, x2, y2, xy2, x2y, x2y2).

In order to optimize the adaptive lens shading algorithm, the coefficients for each device are calculated under D65 lighting conditions and programmed in the NVM memory at production test.

Settings for three other color temperatures (cool white, TL83 and horizon) are calculated from characterization data and these are stored in the NVM memory.

The calculation of the color temperature is performed by the sensor using the color feedback registers. Therefore it is necessary for the host to supply the sensor with the white balance gains.

The lens shading function can be used with the profile1 and profile2 scaler and with crop and subsampling.

The lens shading correction is controlled by register 0x0B00:

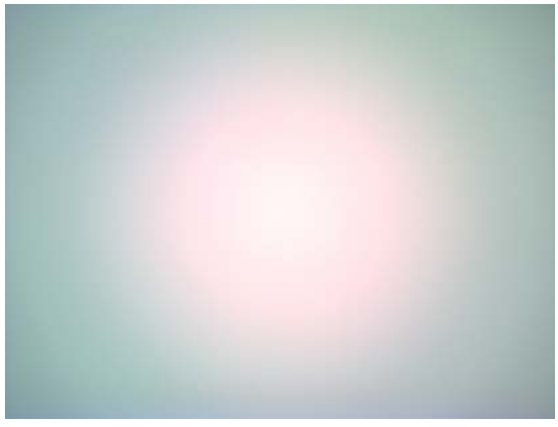
0 - Disable

1 - Enable

The correction applied is 75%.

This is meaning image corner relative illumination = 0.75 * image centre relative illumination.

Figure 46. Lens shading images



Original image

Corrected image

10 NVM contents

The sensor has the following contents in the NVM:

- revision and traceability data
- green imbalance correction data
- grid-iron correction data (option)
- sensitivity data (to be used by the host)
- defect data (used on-chip, described in *Section 9.3 on page 84*)
- lens shading AV2x2 corrector data (used on-chip, described in *Section 9.5 on page 86*)

10.1 Green imbalance corrector

The NVM is programmed with calibration data for four different illuminants that are used by the sensor to minimize green imbalance (used on-chip, see *Section 9.4 on page 85*).

10.2 Lens shading gridiron correction

This data is not used by the sensor but can be used with a host ISP based bi-cubic corrector.

The lens shading gridiron data is calculated at FMT for each device for one color temperature D65 (Fluorescent Phillips Graphica Pro 965). Each of the four color channel values are recorded. Each grid ROI in each color channel with the pedestal removed. The on board lens shading correction is disabled. The analog gain is set to x1.

10.3 Sensitivity data

This data is not used by the sensor but can be used by the host to calibrate the AWB system.

The sensitivity data is measured at FMT for each device for one color temperature D65 (Fluorescent Phillips Graphica Pro 965). Each of the four color channel values are recorded. The 10-bit average of the central 1% of the image (1% of image width, 1% of image height) is recorded, the pedestal is included in the value. The on-board lens shading correction is disabled. The analog gain is set to x1.

More details are provided in the calibration application note.

10.4 NVM map

The NVM map is a 512-byte space containing per part basis data to optimize the image quality.

The NVM map is a delivery document that ST will supply to customer upon request.

Note: The sensor must be in software standby to read the NVM.

In order to read the NVM the following registers must be programmed.

0x3E04 = 1 - Power-up the NVM

0x3640 = 0 - Access NVM register space

The registers should be reset after reading the NVM to the following:

0x3E04 = 0 - Power-down the NVM

0x3640 = 1 - Disable access to NVM register space

11 EMC recommendations

The following recommendations should be followed to ensure the EMC performance of the device is optimized in its host system.

- The VX6953CB should be sited as far as possible from resonant antenna elements to minimize coupling of RF energy into the camera.
- Power supplies should meet ripple requirements, see *Section 12.3.2: Power supply ripple requirement on page 93*.

12 Electrical characteristics

References:

- SMIA Characterization Specification - Revision 1
- SMIA CCP2 Specification ECR0002 - Revision 1
- SMIA CCP2 Specification - Revision 1

Typical values quoted for nominal voltage, process and temperature. Maximum values are quoted for worst case conditions (process, voltage and functional temperature) unless otherwise specified. Maximum values are quoted for worst case (process, voltage and test temperature).

12.1 Operating conditions

Table 43. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Voltage					
VDIG	Digital power supply	1.68	1.8	1.92	V
VANA	Analog power supply	2.3	2.8	2.9	V
VIP(DIG)	Digital input voltage(1)	0	-	1.92	V
Temperature					
T_{AS}	Temperature (storage)	-40	-	+85	°C
T_{AF}	Temperature (functional operating)	-30		+70	°C
T_{AN}	Temperature (normal operating)	-25		+55	°C
T_{AO}	Temperature (optimal operating)	+5		+40	°C
T_{AT}	Temperature (test)	+21		+25	°C

1. Digital input: EXTCLK, XSHUTDOWN, SCL, SDA.

- **Storage temperature:** Camera has no permanent degradation.
- **Functional operating temperature:** Camera is electrically functional.
- **Normal operating temperature:** Camera produces ‘acceptable’ images.
- **Optimum performance temperature:** Camera produces optimal optical performance.
- **Test temperature:** 100% tested parameters are measured at this temperature.

12.2 Absolute maximum ratings

Table 44. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DIGMAX}	Digital power supply	-0.3	2.2	V
V_{ANAMAX}	Analog power supply	-0.3	3.2	V
V_{IHMAX}	EXTCLK, XSHUTDOWN, SCL, SDA	-0.3	VDIG+0.5	V
T_{STO}	Storage temperature	-40	+ 85(1)	°C
V_{ESD}	Electrostatic discharge model			
	Human body model(2) (3)	-2.0	2.0	kV
	Charge device model(4)	-500	500	V

1. This is a maximum long term standard storage temperature, see soldering profile for short term high temperature tolerance.
2. MM 100V test is performed in compliance with JESD22-A115A if HBM pass level is less then 1000V.
3. HBM tests are performed in compliance with JESD22-A114F.
4. CDM tests are performed in compliance with JESD22-C101D.

Caution: Stresses above those listed in *Section 12.2: Absolute maximum ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

12.3 Power supply - VDIG, VANA

Table 45. Power supplies VDIG, VANA

Parameter	Digital		Analog		Unit
	Typ.	Max.	Typ.	Max.	
Hardware standby	10	90	10	135	µA
Software standby:					
Ext. clock not switching	4	20	0.7	2.0	mA
Ext. clock = 9.6 MHz(1)	6	25	0.7	2.0	mA
Streaming CCP2:					
Preview(2)	65	80	55	65	mA
Capture still(3)	90	110	55	65	mA
Streaming CSI2:					
Preview(4)	53	80	61	80	mA
Capture still(5)	80	110	62	80	mA

1. The digital current scales linearly with the external clock frequency used.
2. Binning 2x2 mode, profile 0, 28fps, 10-8 data, EDoF estimation mode, CCP-2.
3. Full resolution image, profile 2, 15fps, 10-8 data, EDoF application mode, CCP-2
4. Binning 2x2 mode, profile 0, 28fps, 10-8 data, EDoF estimation mode, CSI-2.
5. Full resolution image, profile 2, 15fps, 10-8 data, EDoF application mode, CSI-2

12.3.1 Power supply (peak current) - VDIG, VANA

The peak current (in-rush) consumption of the sensor module is defined as any current pulse >=10µs. The duty cycle of the peak to the low part of the current profile is 33% with a worst-case period of 500 µs.

Table 46. In-rush current VDIG, VANA for CCP2 interface

Parameter	Digital		Analog		Unit
	Typ.	Max.	Typ.	Max.	
Boot clock peak current(1)	65	100	170	220	mA
Start Streaming current(2)	60	90	170	220	mA
Stop Streaming current(3)	160	190	170	220	mA
In streaming mode while changing sensor settings	160	190	90	90	mA

1. This corresponds to the transient current when XSHUTDOWN is powered up and the sensor is being set SW_Standby mode. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.
2. When the sensor is changed from Software standby to Streaming mode. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.
3. When the sensor is changed from streaming to Software standby. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.

Table 47. In-rush current VDIG, VANA for CSI-2 interface

Parameter	Digital		Analog		Unit
	Typ.	Max.	Typ.	Max.	
Boot clock peak current(1)	100	140	235	260	mA
Start Streaming current(2)	175	210	150	150	mA
Stop Streaming current(3)	175	210	150	150	mA
In streaming mode while changing sensor settings	200	240	150	150	mA

1. This corresponds to the transient current when XSHUTDOWN is powered up and the sensor is being set SW_Standby mode. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.
2. When the sensor is changed from Software standby to Streaming mode. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.
3. When the sensor is changed from streaming to Software standby. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.

12.3.2 Power supply ripple requirement

It is recommended that the application meets the following requirements on the power supply signal in 10 kHz to 1.4 MHz.

Table 48. Ripple requirement

Symbol	Parameter	Max.	Unit
Ripple_VANA	Peak to peak max ripple on analogue power supply (10 kHz to 1.4 MHz)	6	mV
Ripple_VDIG	Peak to peak max ripple on digital power supply	50	mV

12.4 System clock - EXTCLK

Table 49. System clock - EXTCLK

Symbol	Parameter	Min.	Max.	Unit
	Leakage current	4(1)	30(2)	µA
V_{CL}	DC coupled square wave low level	0	0.3 * VDIG	V
V_{CH}	DC coupled square wave high level	0.7 VDIG	VDIG+0.5V	V
V_{CAC}	AC coupled sine wave	0.5	1.2	V
f_{EXTCLK}	Clock frequency input	6.0 - 1%(3)	27 + 1%(3)	MHz
Duty cycles	Clock frequency duty cycles	40	60	%
Input jitter	EXTCLK input jitter	-	Refer to Jitter application note(4)	ps

1. With DC coupled square wave clock.
2. With DC VDIG applied.
3. Nominal frequencies are 6.0 to 27 MHz with a 1% centre frequency tolerance. Tested at characterization only.
4. ST Microelectronics will provide upon request an application note detailing the EXTCLK input jitter requirements.

12.5 Power down control - XSHUTDOWN

Table 50. Power down control - XSHUTDOWN

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	0	-	0.3 * VDIG	V
V_{IH}	High level input voltage	0.7 * VDIG	-	VANA	V

12.6 CCI interface - SDA, SCL

12.6.1 CCI interface - DC specification

Table 51. CCI interface

Symbol	Parameter	Min.	Max.	Unit
V_{IL}	Low level input voltage	0	0.3 * VDIG	V
V_{IH}	High level input voltage	0.7 * VDIG	VDIG+0.5V	V
V_{OL}	Low level output voltage(1)	0	0.2 * VDIG	V
I_{IL}	Low level input current	-	-10	µA
I_{IH}	High level input current	-	10	µA

1. V_{OH} is not valid for CCI. 3 mA drive strength.

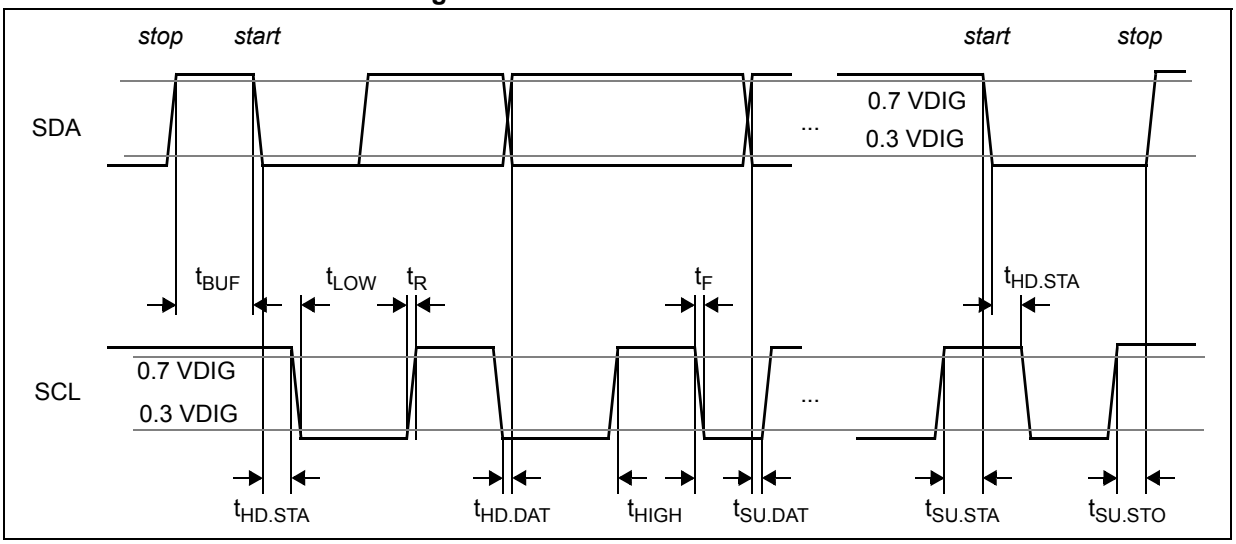
12.6.2 CCI interface - timing characteristics

Table 52. CCI interface - timing characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCL}	SCL clock frequency	0	-	400	kHz
t_{LOW}	Clock pulse width low	1.3	-	-	µs
t_{HIGH}	Clock pulse width high	0.6	-	-	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	0	-	50	ns
t_{BUF}	Bus free time between transmissions	1.3	-	-	µs
$t_{HD.STA}$	Start hold time	0.6	-	-	µs
$t_{SU.STA}$	Start set-up time	0.6	-	-	µs
$t_{HD.DAT}$	Data in hold time	0	-	0.9	µs
$t_{SU.DAT}$	Data in set-up time	100	-	-	ns
t_R	SCL/SDA rise time	20+0.1 Cb(1)	-	300	ns
t_F	SCL/SDA fall time	20+0.1 Cb(1)	-	300	ns
$t_{SU.STO}$	Stop set-up time	0.6	-	-	µs
Ci/o	Input/output capacitance (SDA)	-	-	8	pF
Cin	Input capacitance (SCL)	-	-	6	pF

1. Cb = total capacitance of one bus line in pF.

Figure 47. CCI AC characteristics



All timings are measured from either 0.3 VDIG or 0.7 VDIG.

For further information on the CCI interface, refer to the SMIA 1.0 part 2: CCP Specification document.

12.7 CCP interface

12.7.1 CCP interface - DC specification

Table 53. CCP interface - DC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OD}	Differential voltage swing(1)	100	150	200	mV
V_{CM}	Common mode voltage (self biasing)	0.8	0.9	1.0	V
R_O	Output impedance	40		140	Ω
I_{DR}	Drive current range (internally set by bias circuit)	0.5	1.5	2	mA
PSRR(2)	0 to 100 MHz	-	-	30	dB
	100 to 1000 MHz	-	-	10	dB

1. Measured over a 100 Ω load.
2. Nominal value for the interference at V_{CM} voltage through digital supply relative to the interference at digital supply over the 0-1 GHz operating range.
PSRR = 20*log10 (V_{DIG} interference (peak-to-peak) / V_{CM} interference (peak-to-peak))

Note: For further information on the subLVDS please refer to the SMIA 1.0 Part 2: CCP2 Specification document.

12.7.2 CCP interface - timing characteristics

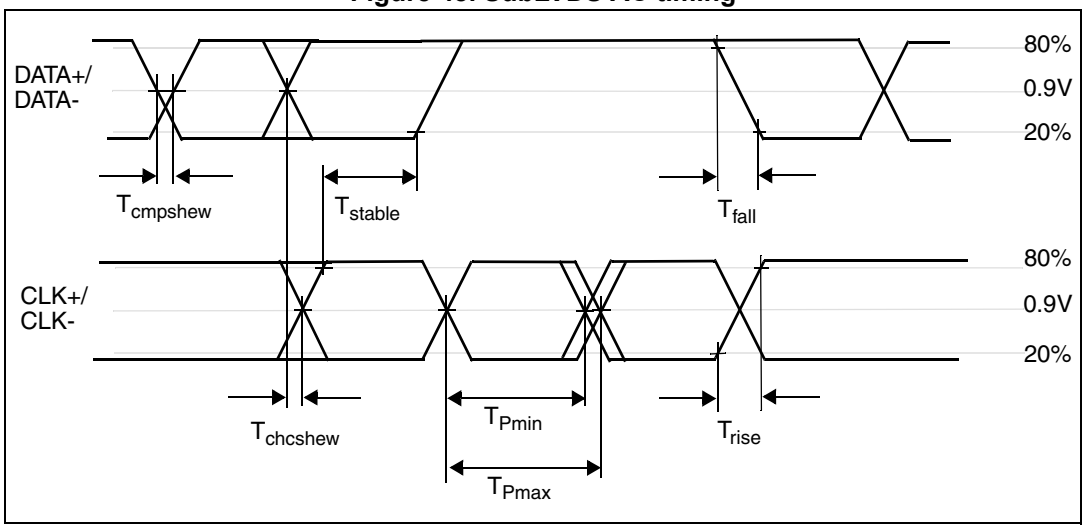
The parameters in *Table 54* are measured across a terminated 100 Ω transmission line. CCP2_signalling_mode register is set to 1, data/strobe mode.

Table 54. CCP interface - timing characteristics

Symbol	Parameter	Min.	Max.	Unit
F_p	Average data frequency	-	640	Mbits/s
T_p	Average data period	1.56	-	ns
T_{jitter}(1)	Data period jitter	-	200	ps
t_{stable}	Both data and clock at the stable level	780	-	ps
T_{rise}	Rise time of DATA+/DATA-, CLK+/CLK-	300	400	ps
T_{fall}	Fall time of DATA+/DATA-, CLK+/CLK-	300	400	ps
T_{shew}(2)	Total skew between signals	-	225	ps
t_{PWR}	Power up/down time	-	20	µs

1. T_{Pmax}-T_{Pmin}.
2. T_{shew} =$T_{cmpshew}$ + $T_{chcshew}$.

Figure 48. SubLVDS AC timing



Note: For further information on the CCP please refer to the SMIA 1.0 Part 2: CCP2 Specification 30-6-04 document.

12.8 CSI-2 interface

12.8.1 CSI-2 interface - DC specification

Table 55. CSI-2 interface - high speed mode - DC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage(1)	140	200	270	mV
V_{OHHS}	HS output high voltage(1)	-	-	360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω

1. Value when driving into load impedance anywhere in the Z_{ID} range (80-125Ω).

Table 56. CSI-2 interface - low power mode - DC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	Output high level	1.1	1.2	1.3	V
V_{OL}	Output low level	-50	-	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω

12.8.2 CSI-2 interface - AC specification

Table 57. CSI-2 interface - high speed mode - AC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Data rate	80	-	800	Mbits/s
t_{clkp}	Average data period	1.25	-	12.5	ns
t_r and t_f	20% to 80% rise time and fall time	150	-	0.3UI(1)	ps
t_{skew}	Data to clock skew	-0.15UI	-	0.15UI	ps

1. UI is equal to 1/(2*fh) where fh is the fundamental frequency of the transmission for a certain bit rate. For example, for 600 Mbps, fh is 300 MHz.

Table 58. CSI-2 interface - low power mode - AC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_r and t_f	15% - 85% rise time and fall time	-	-	25	ns

13 Optical specification

13.1 Lens characteristics

Table 59. Typical lens design characteristics for first source lens supplier

Parameter	Value					
4 element plastic lens	-					
F/number	2.8					
Effective focal length	3.32 mm					
Horizontal FOV	57.1°					
In-focus distance range	Infinity to 40 cm (EDOF applied)					
Distortion	TV: +/-1%					
Relative illumination (lens only)	48.7% at 1.0 field on green channels.					
Maximum illumination decrease over 10% of image height. (lens only)	8.5%					
Spectral weighting: Wavelength (nm) Weight	435.8 6	486.1 17	546.1 38	587.6 29	656.3 13	
Lateral chromatic aberration	<1.4 um					
Coating reflectance - All surfaces are coated. At least 50% of all surfaces must fulfil this specification.	< 400 nm 400 to 670 nm >670nm		No limitation ≤1.0% absolute, 0.35% avg Straight line with a slope of < 3% /100 nm			
Maximum chief ray angle	27.9°					

Note: The module IR filter cut-off wavelength is 650 nm.

13.2 Text, 1D and 2D codes reading

The VX6953CB camera module features a supermacro mode (*Section 8.4: Supermacro mode on page 74*) dedicated to business card and text reading as well as barcode (1D) and 2D QR code reading using a monochrome image. Refer to application note for detailed image processing optimization.

Figure 49. Barcode and QR code examples

Barcode QR code

Table 60. QR code (2D)resolution reading capability

Performances	Working distances (cm)
QR code 0.339 mm	25 to 28 cm
QR code 0.4 mm	20 to 30 cm
QR code 0.5 mm	15 to 30 cm
QR code 0.6 mm	15 to 30 cm
QR code 0.7 mm	15 to 30 cm

The performances in *Table 60* were achieved on VX6953CB cut 3.0 production limit samples in supermacro mode using ST's image processing pipe and with standard mobile phone application QR decoder software.

Refer to the EDoF application note for recommendations on host image processing pipe tuning for QR/barcode reading.

14 Mechanical

14.1 Packaging and delivery

This module has been specifically designed to ensure that the lens barrel is sub-flush to the top surface of the lens mount. ST recommends that zero pressure is applied to the top surface of the lens barrel during the assembly processes or by attaching baffles/spacers. If any pressure is applied to the lens barrel surface, this could lead to a significant degradation in image sharpness. ST's recommended SMoP package handling guidelines are available on request.

The camera module should not be subjected to any hot manufacturing process as this may lead to degradation of the image performance. Any hot manufacturing process performed on the device must be agreed with ST, without prior agreement ST will not accept liability to any degradation in module performance.

Figure 50. Marking diagram

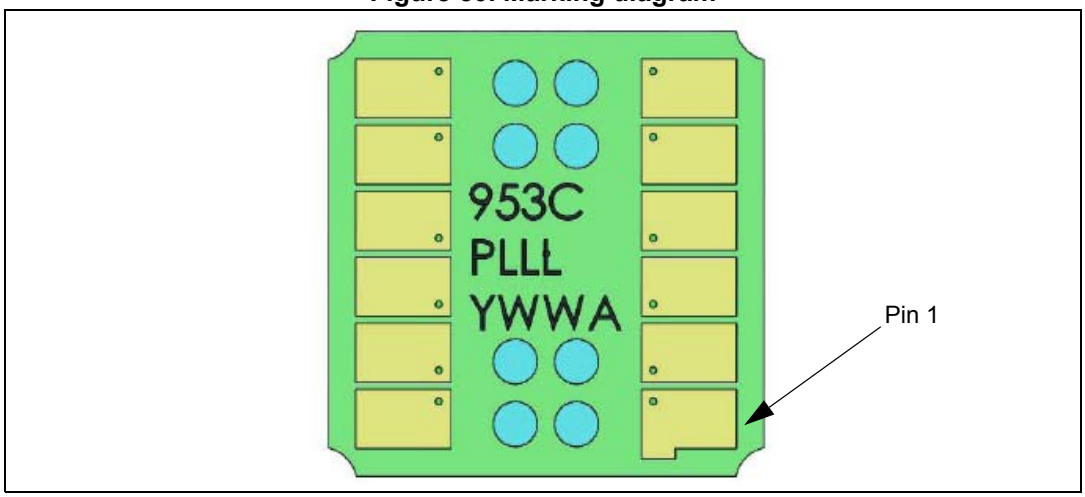


Table 61. Substrate marking codification

Line	Description
Line one (953C)	953 is the product code C is the die revision
Line two (PLLL)	P is the assembly plant
	LLL is the B/E sequence
Line three(YWWA)	Y is the year
	WW is the week number
	A is the module revision

14.2 Inner box labelling

The labelling follows the ST standard packing acceptance specification.

The information on the inner box label is as follows:

- Assembly site
- Sales type (VX6953CBQ05I/1 or VX6953CBG05I/1)
- Quantity
- Trace code
- Marking
- Bulk ID number

14.3 Packing

The VX6953CB packing will be tape and reel. ST will use a 13” reel and a full reel will contain 600 pieces. Orders must be a multiple of the appropriate number with the minimum order size being one full reel.

For detailed drawings, request the VX6953CB tape and reel specification documents.

14.4 Module outline

For details of the mechanical specification for the VX6953CB can be found in the outline drawings available on request from STMicroelectronics.

Table 62. Outline drawing information

Sales type	Outline drawing reference
VX6953CBQ05I/1	ADCS 8253333
VX6953CBG05I/1	ADCS 8289386

15 Ordering information

Table 63. Device summary

Order code	Package	Packing
VX6953CBQ05I/1	SMIA65	Tape and reel
VX6953CBG05I/1	SMIA65	Tape and reel

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

16 User precaution

As is common with many CMOS imagers the camera should not be pointed at bright static objects for long periods of time as permanent damage to the sensor may occur.

17 Acronyms and abbreviations

Table 64. Acronyms and abbreviations

Acronym/ abbreviation	Definition
CCP	Compact camera port
CCI	Camera control interface
CSI	Camera serial interface
EDOF	Extended depth of field
EMI	Electromagnetic interference
EOF	End of frame
FE	Frame end
fps	Frames per second
FS	Frame start
HWA	Hardware accelerator
I2C	Inter ICbus
LE	Line end
LS	Line start
LSB	Least significant byte
LVDS	Low voltage differential signalling
Mbps	Megabits per second
MSB	Most significant byte
MSP	Manufacturer specific pixels
PCK	Pixel clock
PCM	Pulse code modulation
PLL	Phase locked loop
RO	Read only
RW	Read/write
SMIA	Standard mobile imaging architecture
SOF	Start of frame
SubLVDS	Sub-low voltage differential signalling

18 Revision history

Table 65. Document revision history

Date	Revision	Changes
30-Jun-2010	A	Initial release.
17-Jan-2011	B	Reordered existing chapters and added *Chapter 14: Mechanical on page 101* and *Chapter 15: Ordering information on page 103*. In *Chapter 3: Functional description*, updated *Section 3.4.1: Power-up procedure on page 20* and added *Section 3.4.2: Power-down procedure on page 23*. In *Chapter 4: Register map*, added registers revision_number_minor, sensor_model_id and sensor_revision_number to *Table 9: Status registers [0x0000 to 0x000F] on page 29*. In *Chapter 8: EDOF control*, added *Section 8.5: Video modes and EDoF on page 75*. In *Chapter 12: Electrical characteristics*, updated *Section 12.3: Power supply - VDIG, VANA on page 92* and added Duty cycles to *Table 49: System clock - EXTCLK on page 94*. In *Chapter 13: Optical specification*, updated *Section 13.2: Text, 1D and 2D codes reading on page 100*. Added that EXTCLK signal has a SCHMITT-TRIGGER input
10-Feb-2011	C	Redrew *Figure 24: FIFO water mark control on page 61* as original diagram was corrupted when PDF was generated. No technical information has changed.
17-May-2011	D	In *Section 3.4.2: Power-down procedure on page 23*, added information on ULPS and added figure for Power down from Streaming. Added Jitter details to *Section 12.4: System clock - EXTCLK on page 94*. In *Section 12.3.1: Power supply (peak current) - VDIG, VANA on page 92*, added details for peak current. Removed all 1.2V references due to an issue affecting I^2C and VDIG switch pins. Removed MAN_SPEC register section. Other minor corrections and amendments throughout.
05-Mar-2013	5	Minor updates throughout.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT AUTHORIZED FOR USE IN WEAPONS. NOR ARE ST PRODUCTS DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com