STM32F052x

Medium density advanced ARM-based 32-bit MCU, up to 128 KB Flash, USB, CAN, 12 timers, ADC, DAC and comm. interfaces

Data brief

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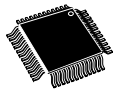
Features

- Core: ARM 32-bit Cortex™-M0 CPU, frequency up to 48 MHz
- Memories
  - 64 to 128 Kbytes of Flash memory
  - 16 Kbytes of SRAM with HW parity checking
- CRC calculation unit
- Reset and power management
  - Voltage range: 2.0 V to 3.6 V
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low power modes: Sleep, Stop, Standby
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
  - Internal 48 MHz oscillator with automatic trimming based on ext. synchronization
- Up to 87 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 68 I/Os with 5V tolerant capability and 19 with independent supply V_{DDIO2}
- 7-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply from 2.4 up to 3.6
- One 12-bit D/A converter (with 2 channels)
- Two fast low-power analog comparators with programmable input and output
- Up to 24 capacitive sensing channels for touchkey, linear and rotary touch sensors
- Serial wire debug (SWD)
- 96-bit unique ID



LQFP100 14x14 mm
LQFP64 10x10 mm
LQFP48 7x7 mm

- 12 timers
  - One 16-bit 7-channel advanced-control timer for 6 channels PWM output, with deadtime generation and emergency stop
  - One 32-bit and one 16-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - One 16-bit timer, with 2 IC/OC, 1 OCN, deadtime generation and emergency stop
  - Two 16-bit timers, each with IC/OC and OCN, deadtime generation, emergency stop and modulator gate for IR control
  - One 16-bit timers with 1 IC/OC
  - Independent and system watchdog timers
  - SysTick timer: 24-bit downcounter
  - Two 16-bit basic timers to drive the DAC
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- Communication interfaces
  - Two SPIs (18 Mbit/s) with 4 to 16 programmable bit frames, and with I^2S interface multiplexed
  - Two I^2C interfaces supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink; one supporting SMBus/PMBus and wakeup
  - Four USARTs supporting master synchronous SPI and modem control; two with ISO7816 interface, LIN, IrDA, auto baud rate detection and wakeup feature
  - CAN interface
  - USB 2.0 full-speed interface, able to run from internal 48 MHz oscillator and with BCD and LPM support
  - HDMI CEC, wakeup on header reception

Table 1. Device Overview

Reference	Part number
STM32F052x	STM32F052VB, STM32F052V8, STM32F052RB STM32F052R8, STM32F052CB, STM32F052C8

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1 Description

The STM32F052x family incorporates the high-performance ARM Cortex™-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 128 Kbytes of Flash memory and 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (two I^2Cs, two SPI/I2S, one HDMI CEC and four USARTs), one USB Full speed device (crystal less), one CAN, one 12-bit ADC, two 12-bit DAC, seven general-purpose 16-bit timers, a 32-bit timer and an advanced-control PWM timer.

The STM32F052x family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F052x family includes devices in three different packages ranging from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of peripherals proposed in this family.

These features make the STM32F052x microcontroller family suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

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Table 2. STM32F052x family device features and peripheral counts

Peripheral		STM32F052Cx		STM32F052Rx		STM32F052Vx	
Flash (Kbytes)		64	128	64	128	64	128
SRAM (Kbytes)		16		16		16	
Timers	Advanced control	1 (16-bit)					
	General purpose	5 (16-bit) 1 (32-bit)					
	Basic	2 (16-bit)					
Comm. interfaces	SPI [I2S](1)	2 [2]					
	I^2C	2					
	USART	4					
	CAN	1					
	USB	1					
	CEC	1					
12-bit synchronized ADC (number of channels)		1 (10 ext. + 3 int.)		1 (16 ext. + 3 int.)			
GPIOs		37		51		87	
Capacitive sensing channels		17		18		24	
12-bit DAC (number of channels)		1 (2)					
Analog comparator		2					
Max. CPU frequency		48 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C Junction temperature: -40 °C to 125 °C					
Packages		LQFP48		LQFP64		LQFP100	

1. The SPI interface can be used either in SPI mode or in I2S audio mode.

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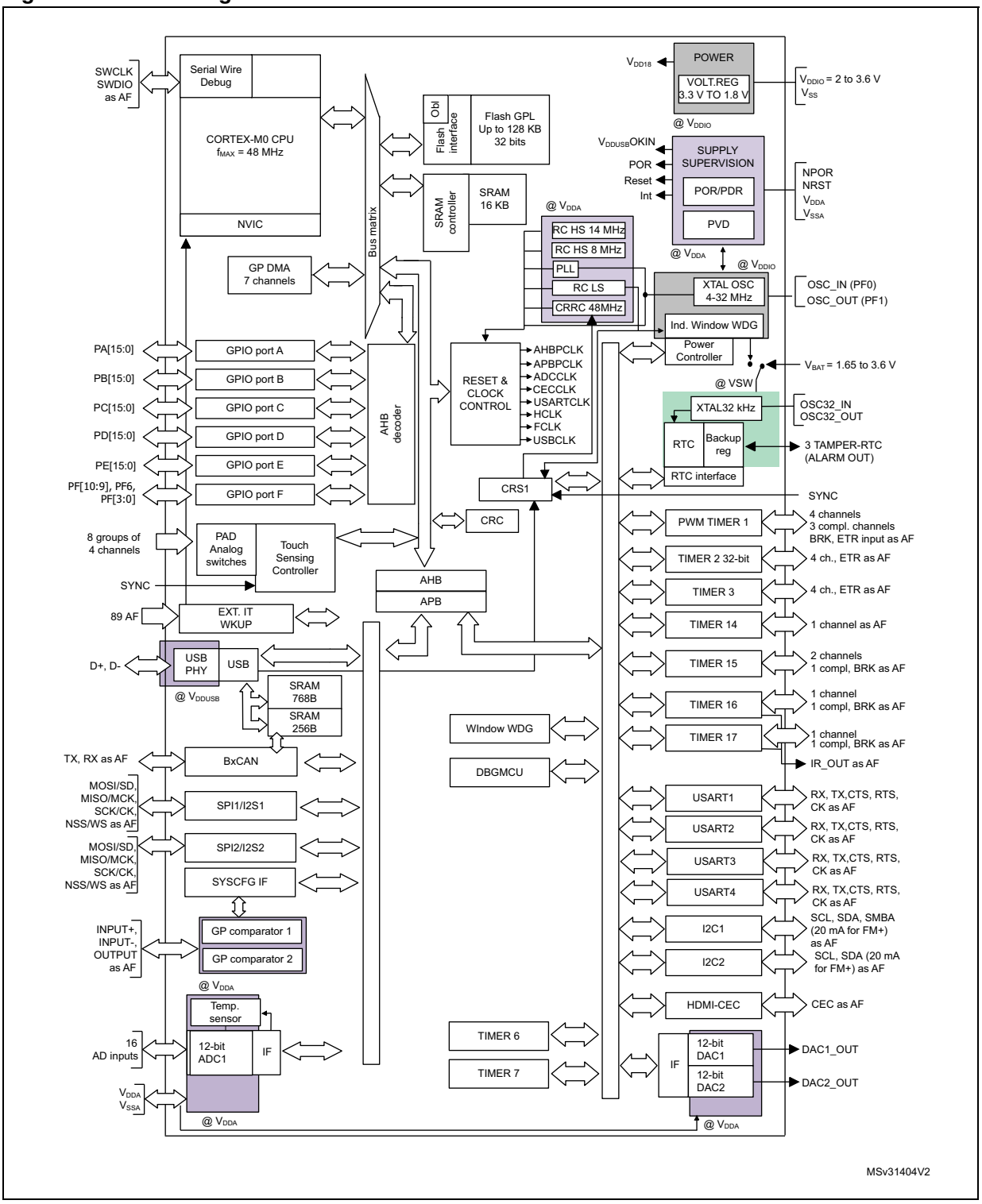
Figure 1. Block Diagram



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2 Functional overview

2.1 ARM® Cortex™-M0 core with embedded Flash and SRAM

The ARM Cortex™-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F052x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.2 Memories

The device has the following features:

- Up to 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 64 to 128 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and boot in RAM selection disabled

2.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10 or through the USB DFU interface.

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2.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.5 Power management

2.5.1 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC and DAC are used). The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{DDIO2} = 1.65 to 3.6 V: external power supply for marked I/Os. Provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}, but it must not be provided without a valid supply on V_{DD}. Refer to the pinout diagrams or tables for concerned I/Os list.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

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2.5.3 Voltage regulator

The regulator has three operating modes: main (MR), low power (LPR) and power down.

- MR is used in normal operating mode (Run)
- LPR can be used in Stop mode where the power demand is reduced
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.5.4 Low-power modes

The STM32F052x family supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC alarm, COMPx, I2C1, USART1 or the CEC.

  The I2C1, USART1 and the CEC can be configured to enable the HSI RC oscillator for processing incoming data. If this is used, the voltage regulator should not be put in the low-power mode but kept in normal mode.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pins, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

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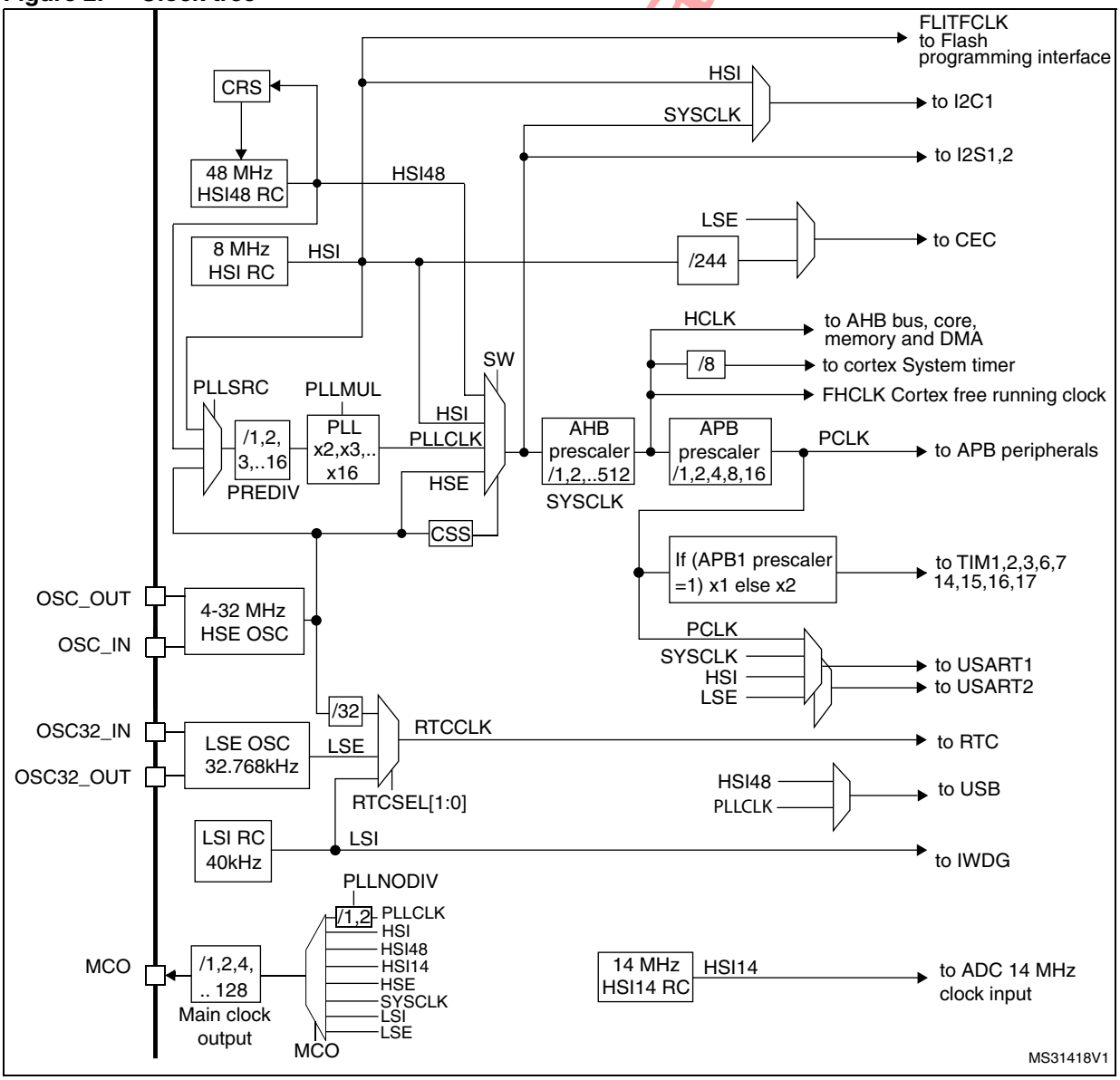
2.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Additionally to that, also the internal RC 48 MHz oscillator could be selected for system clock or PLL input source. This oscillator could be automatically fine-trimmed by the means of CRS peripheral using the external synchronization.

Figure 2. Clock tree



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2.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.8 Direct memory access controller (DMA)

The 7-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2S, I2C, USART, all TIMx timers (except TIM14), DAC and ADC.

2.9 Interrupts and events

2.9.1 Nested vectored interrupt controller (NVIC)

The STM32F052x family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.9.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 87 GPIOs can be connected to the 16 external interrupt lines.

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2.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

2.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

2.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Temperature sensor calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

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2.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

2.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

2.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

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2.13 Touch sensing controller (TSC)

The STM32F052x devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. The STM32F052x devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Table 5. Capacitive sensing GPIOs available on STM32F052x devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA11		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA12		TSC_G8_IO4	PD15

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Table 6. No. of capacitive sensing channels available on STM32F052x devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F052Vx LQFP100	STM32F052Rx LQPFP64	STM32F052Cx LQFP48
G1	3	3	3
G2	3	3	3
G3	3	3	2
G4	3	3	3
G5	3	3	3
G6	3	3	3
G7	3		
G8	3		
Number of capacitive sensing channels	24	18	17

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2.14 Timers and watchdogs

The STM32F052x family devices include up to six general-purpose timers, one basic timer and an advanced control timer.

Table 7 compares the features of the advanced-control, general-purpose and basic timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

2.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

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2.14.2 General-purpose timers (TIM2..3, TIM14..17)

There are six synchronizable general-purpose timers embedded in the STM32F052x devices (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F052x devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

2.14.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

2.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it

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operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

2.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

2.15 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Programmable alarm with wake up from Stop and Standby mode capability
- Periodic wakeup unit with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- Periodic wakeup from Stop/Standby

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The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

2.16 Inter-integrated circuit interfaces (I^2C)

Up to two I^2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on some I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Disabled when Wakeup from Stop mode is enabled

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 9* for the differences between I2C1 and I2C2.

Table 9. STM32F052x I^2C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	

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Table 9. STM32F052x I²C implementation (continued)

I2C features(1)	I2C1	I2C2
SMBus	X	
Wakeup from STOP	X	

1. X = supported.

2.17 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds up to four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART4), which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. The USART1 and USART2 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing the USART1 and USART2 to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Refer to *Table 10* for the differences between USART1, USART2, USART3 and USART4.

Table 10. STM32F052x USART implementation

USART modes/features(1)	USART1 and USART2	USART3 and USART4
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	
LIN mode	X	
Dual clock domain and wakeup from Stop mode	X	
Receiver timeout interrupt	X	
Modbus communication	X	
Auto baud rate detection	X	
Driver Enable	X	X

1. X = supported.

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2.18 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I^2S interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at simplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode they can output a clock for an external audio component at 256 times the sampling frequency.

Both SPI1 and SPI2 are identical and implement the set of features shown in the following table.

Table 11. STM32F052x SPI/I2S implementation

SPI features(1)	SPI1 and SPI2
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I2S mode	X
TI mode	X

1. X = supported.

2.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

2.20 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames

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with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.21 Universal serial bus (USB)

The STM32F052x embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signalling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB (256 Bytes are used for CAN peripheral if enabled) and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signallization) which allows crystal-less operation.

2.22 Clock recovery system (CRS)

The STM32F052x embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

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2.23 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

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3 Pinouts and pin description

Figure 3. LQFP100 100-pin package pinout

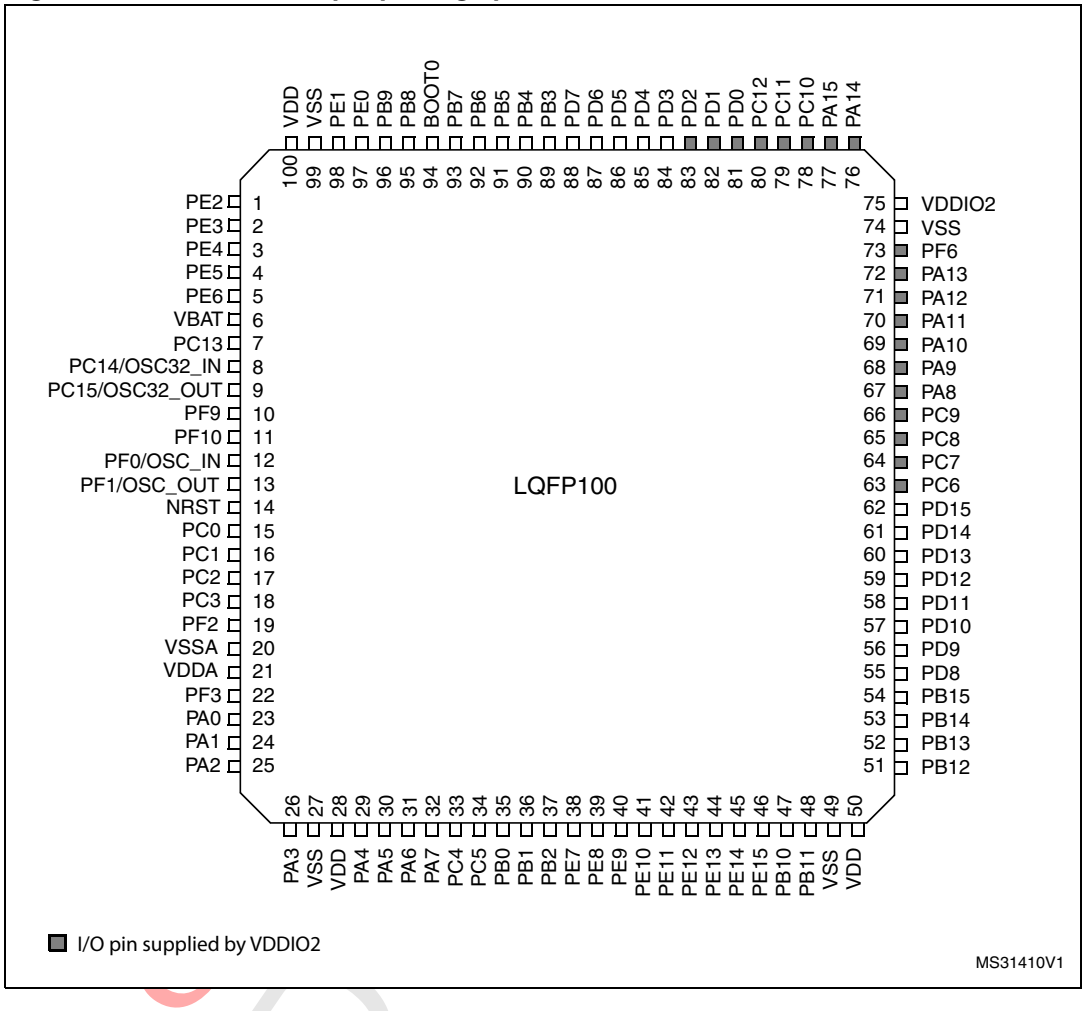

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Figure 4. LQFP64 64-pin package pinout

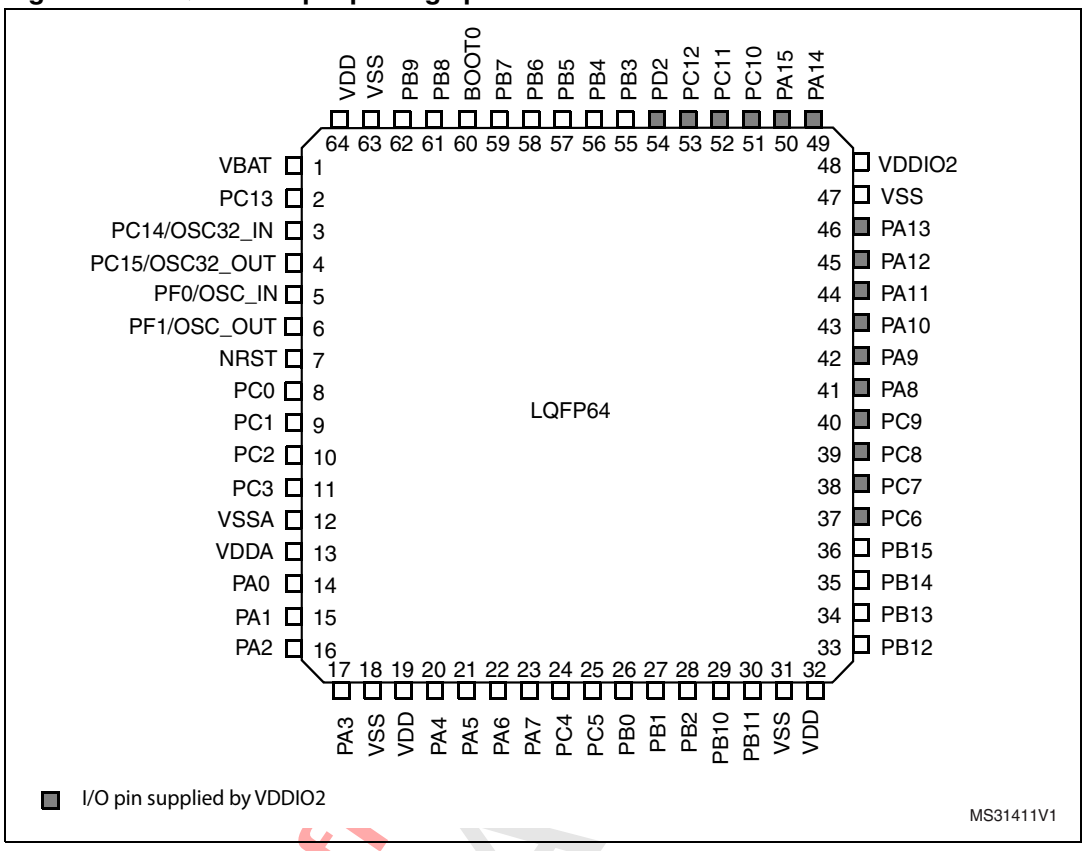

Figure 5. LQFP48 48-pin package pinout

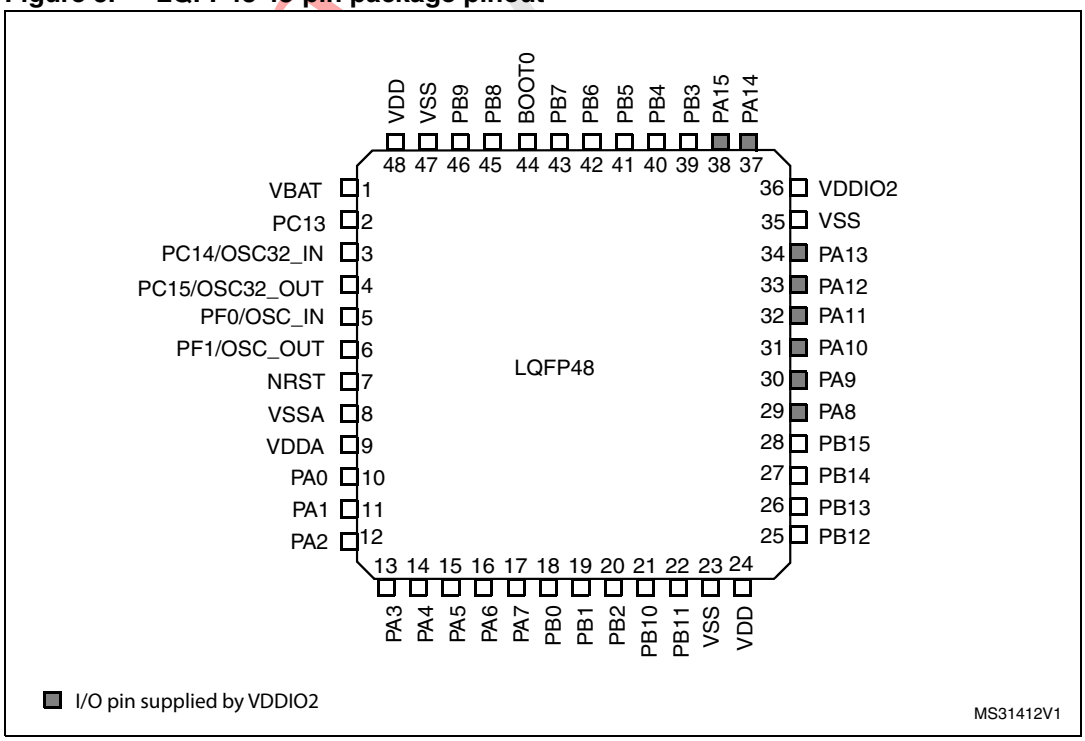

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Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F052x pin definitions

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate function	Additional functions
1			PE2	I/O	FT		TSC_G7_IO1, TIM3_ETR	
2			PE3	I/O	FT		TSC_G7_IO2, TIM3_CH1	
3			PE4	I/O	FT		TSC_G7_IO3, TIM3_CH2	
4			PE5	I/O	FT		TSC_G7_IO4, TIM3_CH3	
5			PE6	I/O	FT		TIM3_CH4	WKUP3, RTC_TAMP3
6	1	1	VBAT	S			Backup power supply	
7	2	2	PC13	I/O	TC	(1) (2)		WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
8	3	3	PC14-OSC32_IN (PC14)	I/O	TC	(1) (2)		OSC32_IN

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Table 13. STM32F052x pin definitions (continued)

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate function	Additional functions
9	4	4	PC15-OSC32_OUT (PC15)	I/O	TC	(1) (2)		OSC32_OUT
10			PF9	I/O	FT		TIM15_CH1	
11			PF10	I/O	FT		TIM15_CH2	
12	5	5	PF0-OSC_IN (PF0)	I	FT		CRS_ SYNC	OSC_IN
13	6	6	PF1-OSC_OUT (PF1)	O	FT			OSC_OUT
14	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
15	8		PC0	I/O	TTa		EVENTOUT	ADC_IN10
16	9		PC1	I/O	TTa		EVENTOUT	ADC_IN11
17	10		PC2	I/O	TTa		SPI2_MISO, I2S2_MCK, EVENTOUT	ADC_IN12
18	11		PC3	I/O	TTa		SPI2_MOSI, I2S2_SD, EVENTOUT	ADC_IN13
19			PF2	I/O	FT		EVENTOUT	WKUP8
20	12	8	VSSA	S			Analog ground	
21	13	9	VDDA	S			Analog power supply	
22			PF3	I/O	FT		EVENTOUT	
23	14	10	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, USART4_TX	RTC_ TAMP2, WKUP1, COMP1_OUT, ADC_IN0, COMP1_INM6
24	15	11	PA1	I/O	TTa		USART2_RTS, TIM2_CH2, TIM15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT	ADC_IN1, COMP1_INP
25	16	12	PA2	I/O	TTa		USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3	ADC_IN2, COMP2_OUT, COMP2_INM6, WKUP4
26	17	13	PA3	I/O	TTa		USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP
27	18		VSS	I/O	FT		Ground	
28	19		VDD	I/O	FT		Digital power supply	
29	20	14	PA4	I/O	TTa		SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1

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Table 13. STM32F052x pin definitions (continued)

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate function	Additional functions
30	21	15	PA5	I/O	TTa		SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2
31	22	16	PA6	I/O	TTa		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6
32	23	17	PA7	I/O	TTa		SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
33	24		PC4	I/O	TTa		EVENTOUT, USART3_TX	ADC_IN14
34	25		PC5	I/O	TTa		TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5
35	26	18	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8
36	27	19	PB1	I/O	TTa		TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
37	28	20	PB2	I/O	FT		TSC_G3_IO4	
38			PE7	I/O	FT		TIM1_ETR	
39			PE8	I/O	FT		TIM1_CH1N	
40			PE9	I/O	FT		TIM1_CH1	
41			PE10	I/O	FT		TIM1_CH2N	
42			PE11	I/O	FT		TIM1_CH2	
43			PE12	I/O	FT		SPI1_NSS, I2S1_WS, TIM1_CH3N	
44			PE13	I/O	FT		SPI1_SCK, I2S1_CK, TIM1_CH3	
45			PE14	I/O	FT		SPI1_MISO, I2S1_MCK, TIM1_CH4	
46			PE15	I/O	FT		SPI1_MOSI, I2S1_SD, TIM1_BKIN	
47	29	21	PB10	I/O	FT		SPI2_SCK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	

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Table 13. STM32F052x pin definitions (continued)

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate function	Additional functions
48	30	22	PB11	I/O	FT		USART3_RX, TIM2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA	
49	31	23	VSS	S			Ground	
50	32	24	VDD	S			Digital power supply	
51	33	25	PB12	I/O	FT		TIM1_BKIN, TIM15_BKIN, SPI2_NSS, I2S2_WS, USART3_CK, TSC_G6_IO2, EVENTOUT	
52	34	26	PB13	I/O	FT		SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_CTS, TIM1_CH1N, TSC_G6_IO3	
53	35	27	PB14	I/O	FT		SPI2_MISO, I2S2_MCK, I2C2_SDA, USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	
54	36	28	PB15	I/O	FT		SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	WKUP7, RTC_REFIN
55			PD8	I/O	FT		USART3_TX	
56			PD9	I/O	FT		USART3_RX	
57			PD10	I/O	FT		USART3_CK	
58			PD11	I/O	FT		USART3_CTS	
59			PD12	I/O	FT		USART3_RTS, TSC_G8_IO1	
60			PD13	I/O	FT		TSC_G8_IO2	
61			PD14	I/O	FT		TSC_G8_IO3	
62			PD15	I/O	FT		TSC_G8_IO4, CRS_SYNC	
63	37		PC6	I/O	FT	(3)	TIM3_CH1	
64	38		PC7	I/O	FT	(3)	TIM3_CH2	
65	39		PC8	I/O	FT	(3)	TIM3_CH3	
66	40		PC9	I/O	FT	(3)	TIM3_CH4	
67	41	29	PA8	I/O	FT	(3)	USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC	
68	42	30	PA9	I/O	FT	(3)	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	
69	43	31	PA10	I/O	FT	(3)	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	

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Table 13. STM32F052x pin definitions (continued)

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate function	Additional functions
70	44	32	PA11	I/O	FT	(3)	CAN_RX, USB_DM, USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	
71	45	33	PA12	I/O	FT	(3)	CAN_TX, USB_DP, USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT	
72	46	34	PA13	I/O	FT	(3) (4)	IR_OUT, SWDIO, USB_OE	
73			PF6	I/O	FT	(3)		
74	47	35	VSS	S			Ground	
75	48	36	VDDIO2	S			Digital power supply	
76	49	37	PA14	I/O	FT	(3) (4)	USART2_TX, SWCLK	
77	50	38	PA15	I/O	FT	(3)	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TIM2_CH1_ETR, EVENTOUT	
78	51		PC10	I/O	FT	(3)	USART3_TX, USART4_TX	
79	52		PC11	I/O	FT	(3)	USART3_RX, USART4_RX	
80	53		PC12	I/O	FT	(3)	USART3_CK, USART4_CK	
81			PD0	I/O	FT	(3)	SPI2_NSS, I2S2_WS, CAN_RX	
82			PD1	I/O	FT	(3)	SPI2_SCK, I2S2_CK, CAN_TX	
83	54		PD2	I/O	FT	(3)	USART3_RTS, TIM3_ETR	
84			PD3	I/O	FT		SPI2_MISO, I2S2_MCK, USART2_CTS	
85			PD4	I/O	FT		SPI2_MOSI, I2S2_SD, USART2_RTS	
86			PD5	I/O	FT		USART2_TX	
87			PD6	I/O	FT		USART2_RX	
88			PD7	I/O	FT		USART2_CK	
89	55	39	PB3	I/O	FT		SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	
90	56	40	PB4	I/O	FT		SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	

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Table 13. STM32F052x pin definitions (continued)

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate function	Additional functions
91	57	41	PB5	I/O	FT		SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6
92	58	42	PB6	I/O	FT		I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	
93	59	43	PB7	I/O	FT		I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_IO4	
94	60	44	BOOT0	I			Boot memory selection	
95	61	45	PB8	I/O	FT		I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	
96	62	46	PB9	I/O	FT		SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, CAN_TX, TIM17_CH1, EVENTOUT	
97			PE0	I/O	FT		EVENTOUT, TIM16_CH1	
98			PE1	I/O	FT		EVENTOUT, TIM17_CH1	
99	63	47	VSS	S			Ground	
100	64	48	VDD	S			Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - these GPIOs must not be used as a current sources (e.g. to drive an LED).
2. After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.
3. PC6, PC7, PC8, PC9, PA8, PA9, PA10, PA11, PA12, PA13, PF6, PA14, PA15, PC10, PC11, PC12, PD0, PD1 and PD2 I/Os are supplied by VDDIO2.
4. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on SWDIO pin and internal pull-down on SWCLK pin are activated.

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Table 14. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1	USART4_TX			COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2	USART4_RX	TIM15_CH1N		
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	TSC_G1_IO3				COMP2_OUT
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	TSC_G1_IO4				
PA4	SPI1_NSS, I2S1_WS	USART2_CK		TSC_G2_IO1	TIM14_CH1			
PA5	SPI1_SCK, I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2				
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3	USART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC			
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	TSC_G4_IO1				
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2				
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3	CAN_RX			COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4	CAN_TX			COMP2_OUT
PA13	SWDIO	IR_OUT	USB_OE					
PA14	SWCLK	USART2_TX						
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	USART4_RTS			

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Table 15. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	USART3_CK	
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	USART3_RTS	
PB2				TSC_G3_IO4		
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1		
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2		TIM17_BKIN
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA		
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3		
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	USART4_CTS	
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC	CAN_RX	
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS, I2S2_WS
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK, I2S2_CK
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1	USART3_RX	
PB12	SPI2_NSS, I2S2_WS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2	USART3_CK	TIM15_BKIN
PB13	SPI2_SCK, I2S2_CK		TIM1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL
PB14	SPI2_MISO, I2S2_MCK	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA
PB15	SPI2_MOSI, I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N		

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Table 16. Alternate functions selected through GPIOC_AFR registers for port C

Pin name	AF0	AF1
PC0	EVENTOUT	
PC1	EVENTOUT	
PC2	EVENTOUT	SPI2_MISO, I2S2_MCK
PC3	EVENTOUT	SPI2_MOSI, I2S2_SD
PC4	EVENTOUT	USART3_TX
PC5	TSC_G3_IO1	USART3_RX
PC6	TIM3_CH1	
PC7	TIM3_CH2	
PC8	TIM3_CH3	
PC9	TIM3_CH4	
PC10	USART4_TX	USART3_TX
PC11	USART4_RX	USART3_RX
PC12	USART4_CK	USART3_CK
PC13		
PC14		
PC15		

Table 17. Alternate functions selected through GPIOD_AFR registers for port D

Pin name	AF0	AF1
PD0	CAN_RX	SPI2_NSS, I2S2_WS
PD1	CAN_TX	SPI2_SCK, I2S2_CK
PD2	TIM3_ETR	USART3_RTS
PD3	USART2_CTS	SPI2_MISO, I2S2_MCK
PD4	USART2_RTS	SPI2_MOSI, I2S2_SD
PD5	USART2_TX	
PD6	USART2_RX	
PD7	USART2_CK	
PD8	USART3_TX	
PD9	USART3_RX	
PD10	USART3_CK	
PD11	USART3_CTS	
PD12	USART3_RTS	TSC_G8_IO1
PD13		TSC_G8_IO2
PD14		TSC_G8_IO3
PD15	CRS_SYNC	TSC_G8_IO4

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Table 18. Alternate functions selected through GPIOE_AFR registers for port E

Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	
PE7	TIM1_ETR	
PE8	TIM1_CH1N	
PE9	TIM1_CH1	
PE10	TIM1_CH2N	
PE11	TIM1_CH2	
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 19. Alternate functions available on port F

Pin name	AF
PF0	CRS_SYNC
PF1	
PF2	EVENTOUT
PF3	EVENTOUT
PF6	
PF9	TIM15_CH1
PF10	TIM15_CH2

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4 Memory mapping

Figure 6. STM32F052x memory map

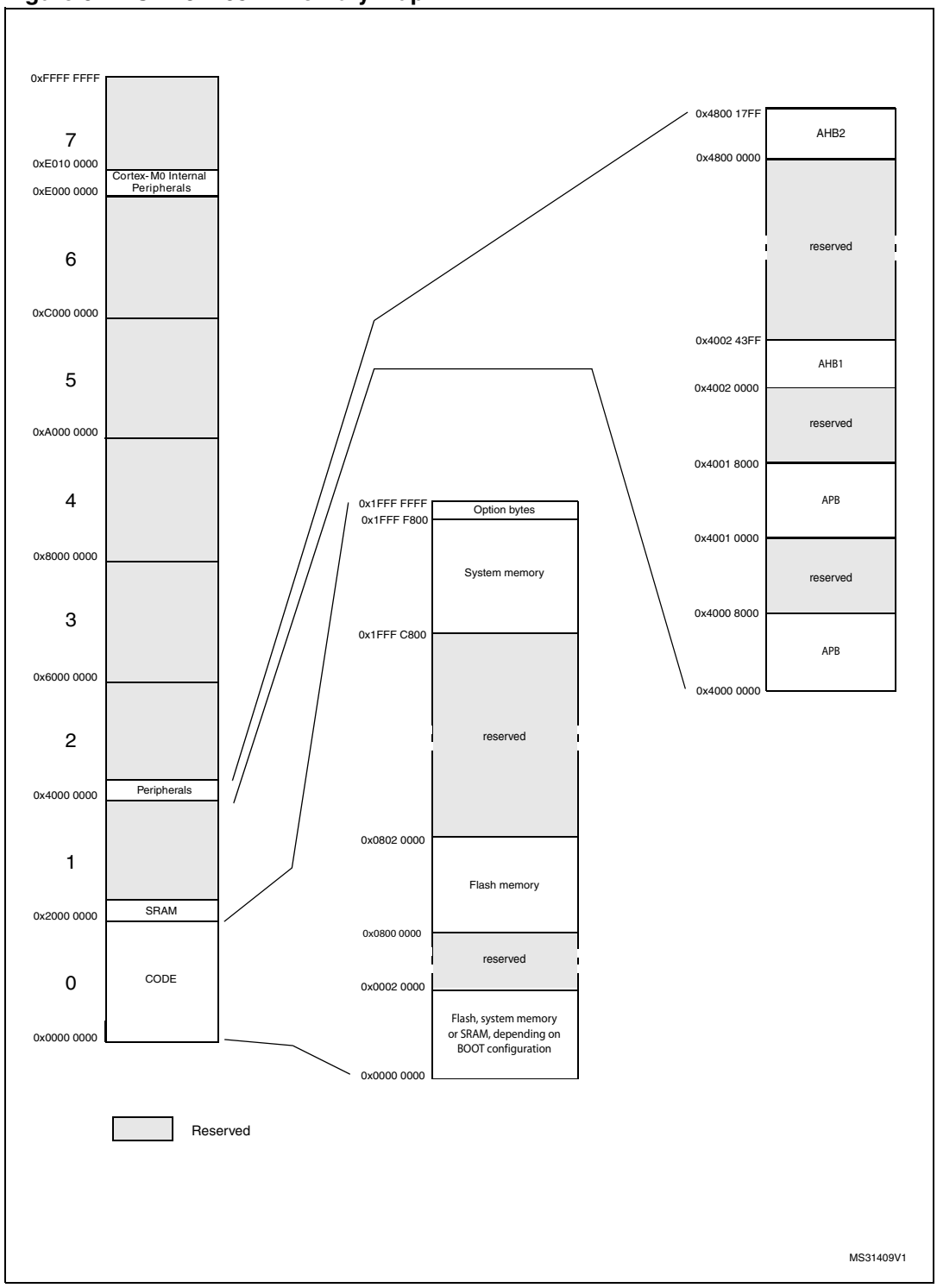

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Table 20. STM32F052x peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1KB	TSC
	0x4002 3400 - 0x4002 3FFF	3KB	Reserved
	0x4002 3000 - 0x4002 33FF	1KB	CRC
	0x4002 2400 - 0x4002 2FFF	3KB	Reserved
	0x4002 2000 - 0x4002 23FF	1KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3KB	Reserved
	0x4002 1000 - 0x4002 13FF	1KB	RCC
	0x4002 0400 - 0x4002 0FFF	3KB	Reserved
	0x4002 0000 - 0x4002 03FF	1KB	DMA
	0x4001 8000 - 0x4001 FFFF	32KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1KB	TIM17
	0x4001 4400 - 0x4001 47FF	1KB	TIM16
	0x4001 4000 - 0x4001 43FF	1KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1KB	USART1
	0x4001 3400 - 0x4001 37FF	1KB	Reserved
	0x4001 3000 - 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1KB	Reserved
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 0800 - 0x4001 23FF	7KB	Reserved
	0x4001 0400 - 0x4001 07FF	1KB	EXTI
	0x4001 0000 - 0x4001 03FF	1KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32KB	Reserved

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Table 20. STM32F052x peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1KB	CEC
	0x4000 7400 - 0x4000 77FF	1KB	DAC
	0x4000 7000 - 0x4000 73FF	1KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1KB	CRS
	0x4000 6800 - 0x4000 6BFF	1KB	Reserved
	0x4000 6400 - 0x4000 67FF	1KB	BxCAN
	0x4000 6000 - 0x4000 63FF	1KB	USB/CAN RAM
	0x4000 5C00 - 0x4000 5FFF	1KB	USB
	0x4000 5800 - 0x4000 5BFF	1KB	I2C2
	0x4000 5400 - 0x4000 57FF	1KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	Reserved
	0x4000 4C00 - 0x4000 4FFF	1KB	USART4
	0x4000 4800 - 0x4000 4BFF	1KB	USART3
	0x4000 4400 - 0x4000 47FF	1KB	USART2
	0x4000 3C00 - 0x4000 43FF	2KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1KB	SPI2
	0x4000 3400 - 0x4000 37FF	1KB	Reserved
	0x4000 3000 - 0x4000 33FF	1KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1KB	RTC
	0x4000 2400 - 0x4000 27FF	1KB	Reserved
	0x4000 2000 - 0x4000 23FF	1KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2KB	Reserved
	0x4000 1400 - 0x4000 17FF	1KB	TIM7
	0x4000 1000 - 0x4000 13FF	1KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2KB	Reserved
	0x4000 0400 - 0x4000 07FF	1KB	TIM3
	0x4000 0000 - 0x4000 03FF	1KB	TIM2

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5 Package characteristics

5.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

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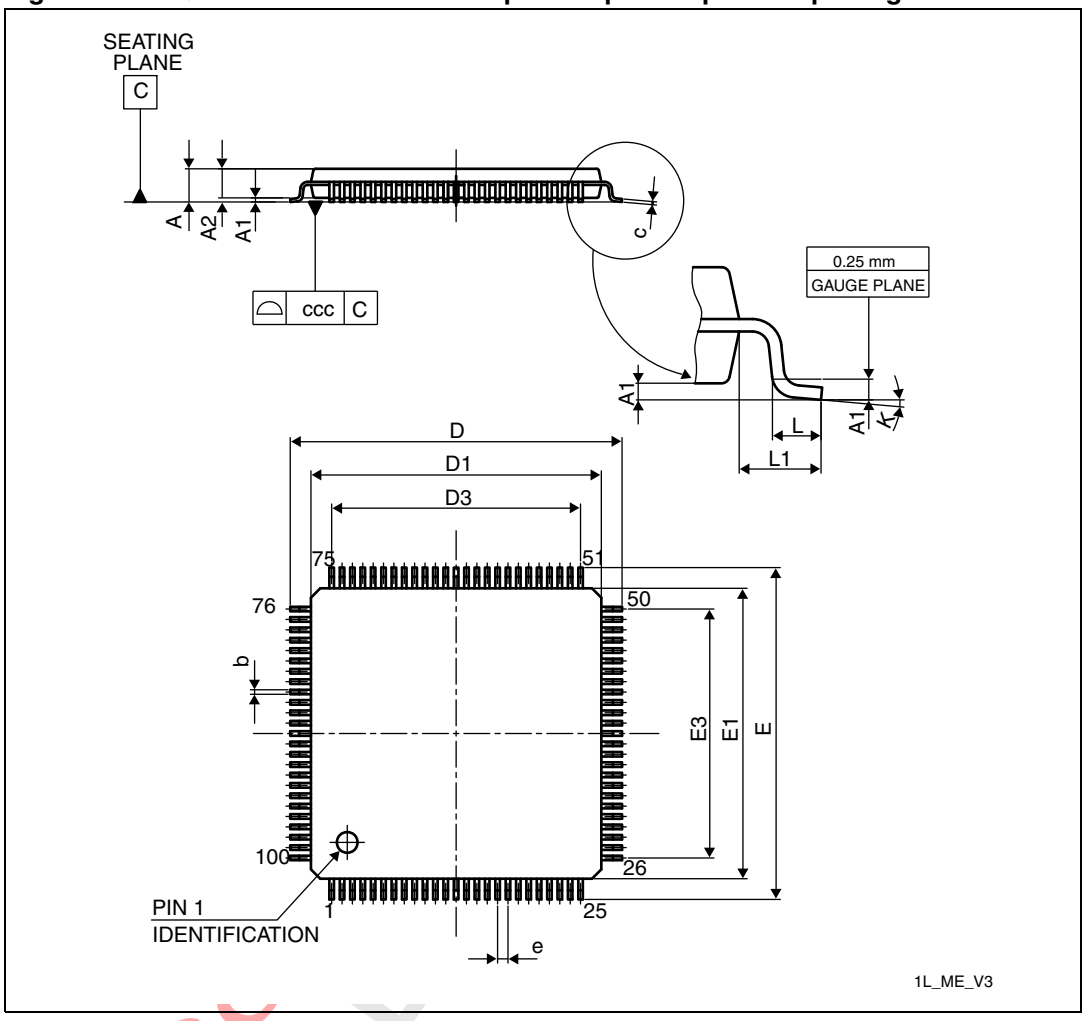
Figure 7. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 21. LQFP100 – 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.000			0.4724	
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

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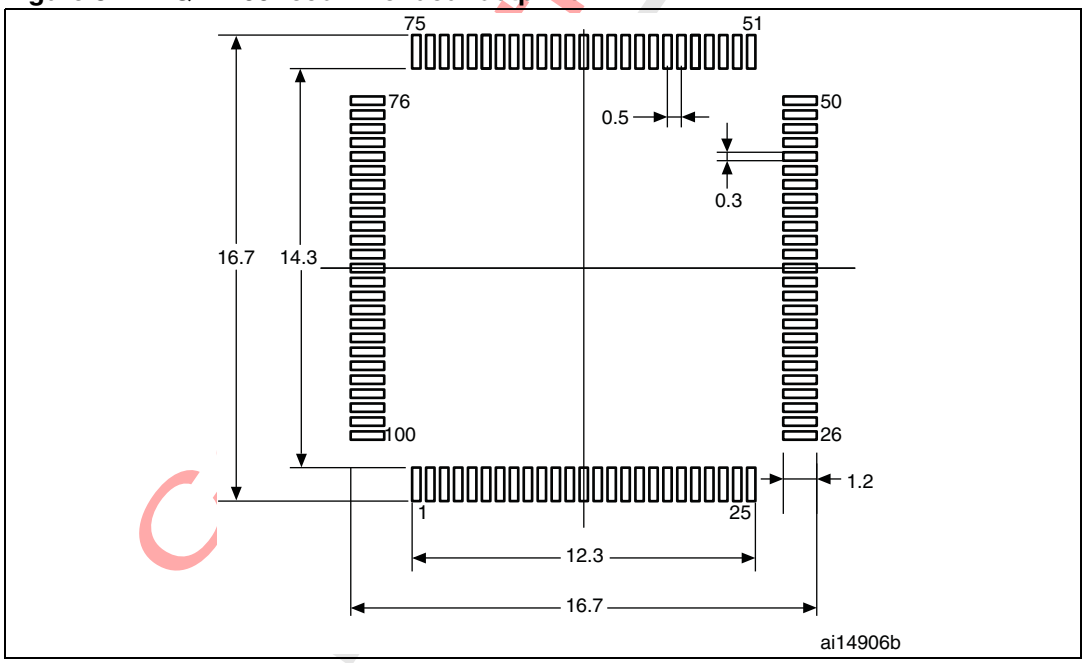
Table 21. LQFP100 – 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3		12.000			0.4724	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
ccc			0.080			0.0031
K	0°	3.5°	7°	0°	3.5°	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 8. LQFP100 recommended footprint



1. Dimensions are in millimeters.

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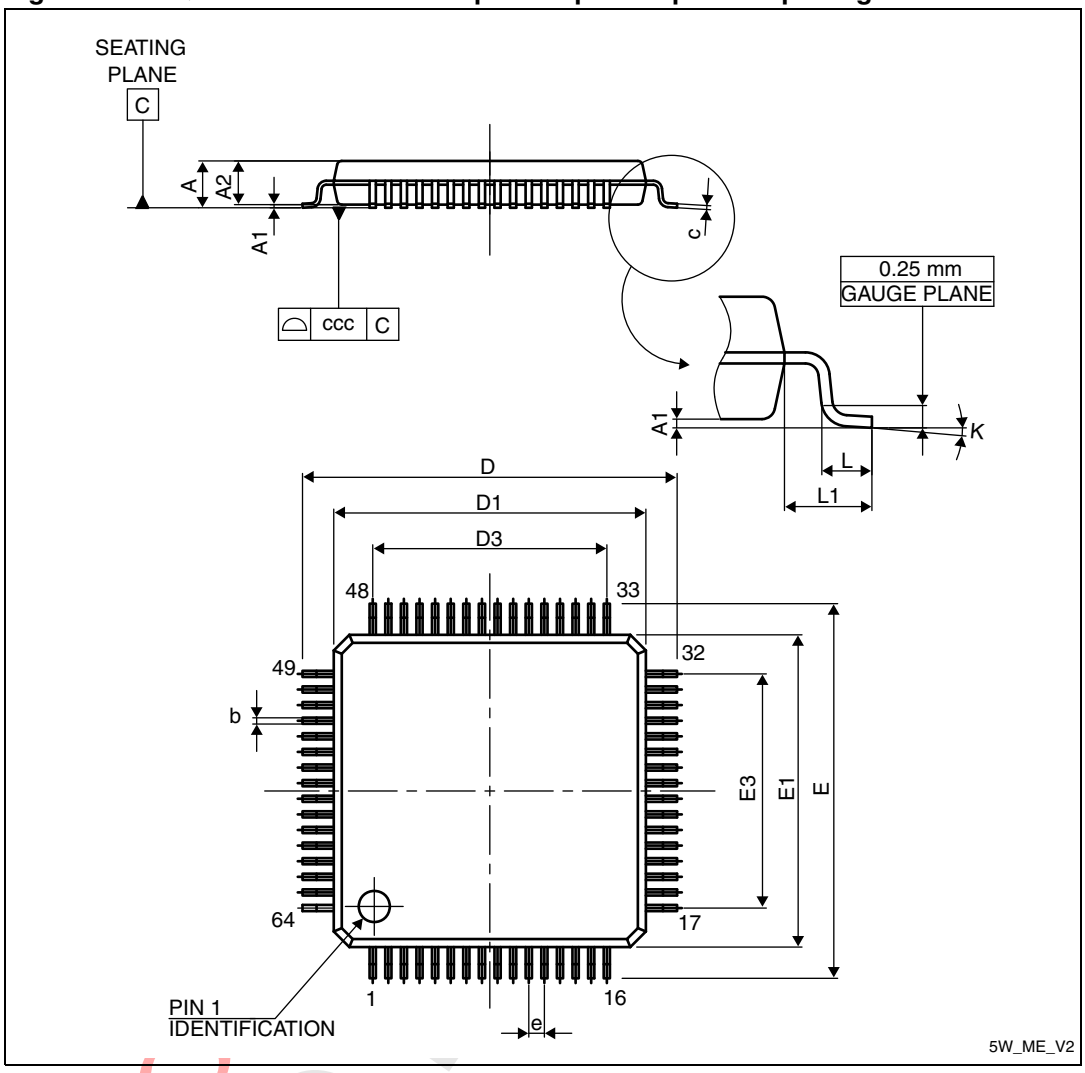
Figure 9. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 22. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D3		7.500			0.2953	

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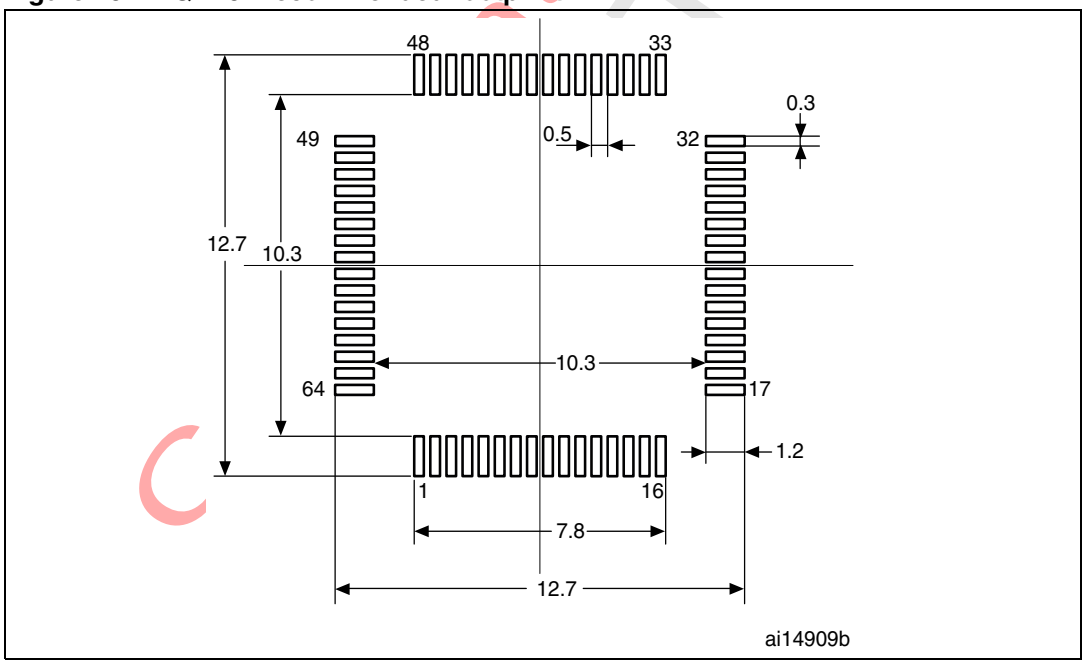
Table 22. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E3		7.500			0.2953	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
ccc			0.080			0.0031
K	0°	3.5°	7°	0°	3.5°	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 10. LQFP64 recommended footprint



1. Dimensions are in millimeters.

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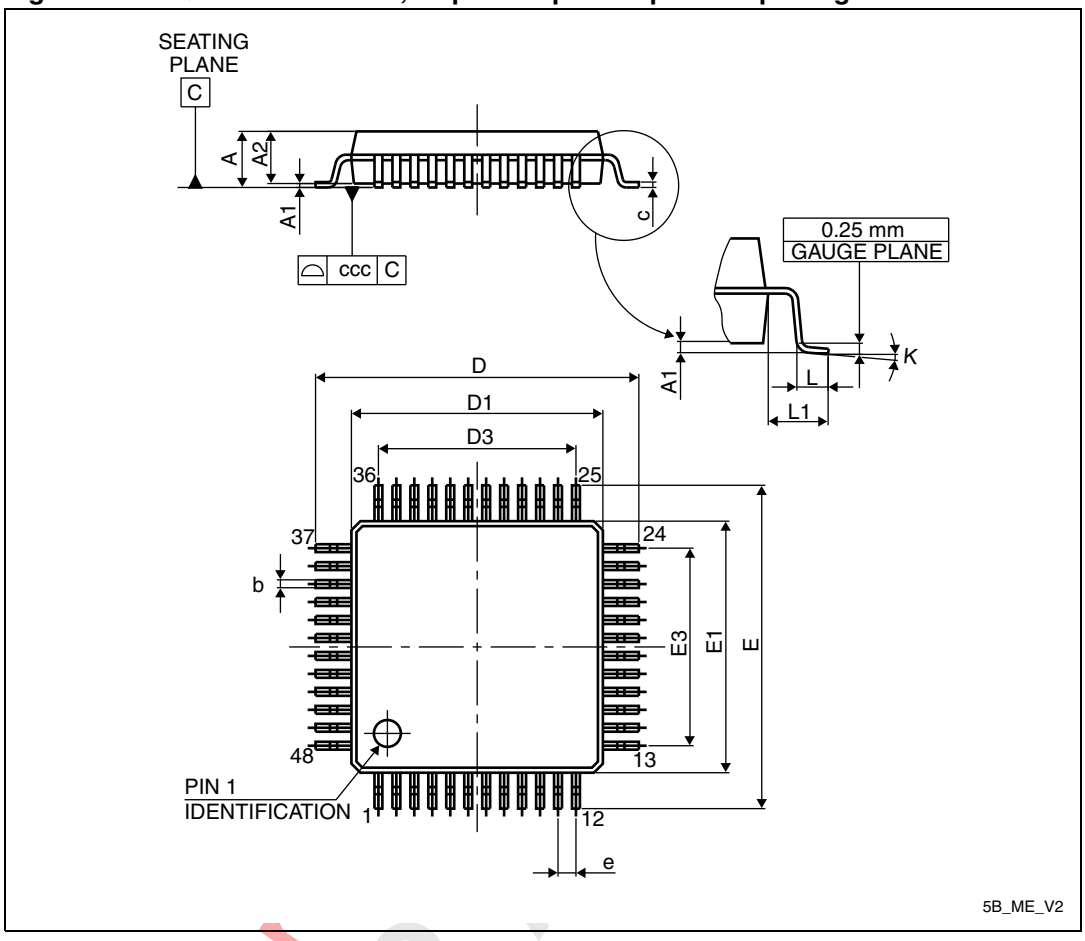
Figure 11. LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 23. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	

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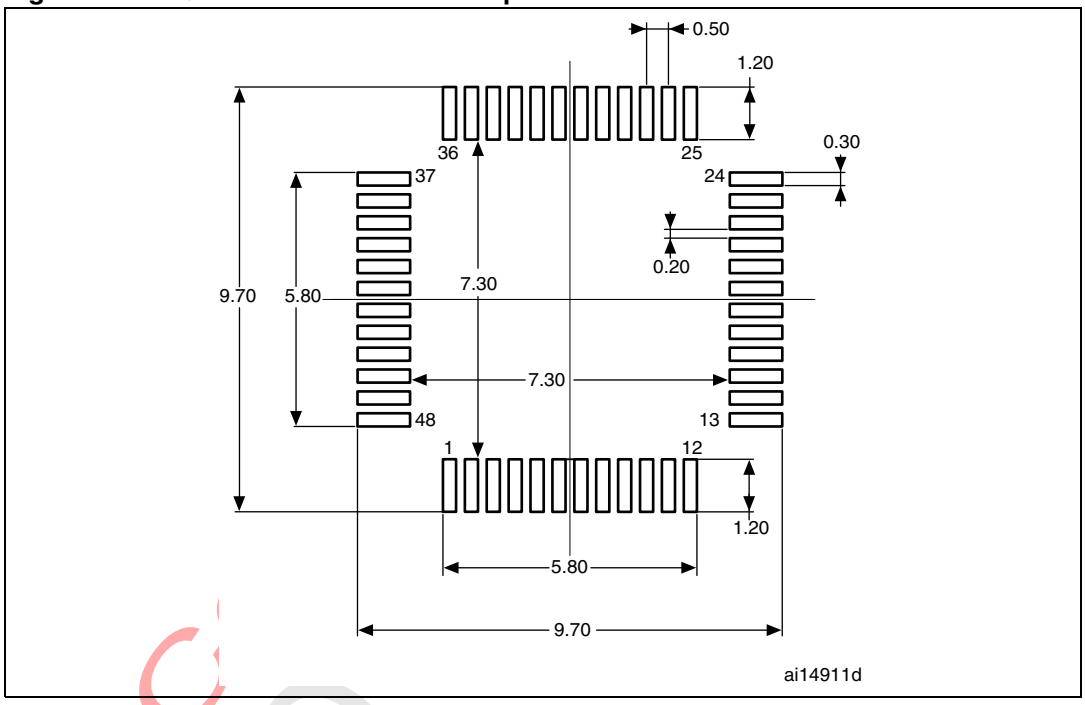
Table 23. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
ccc			0.080			0.0031
K	0°	3.5°	7°	0°	3.5°	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 12. LQFP48 recommended footprint



2. Dimensions are in millimeters.

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6 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 24. Ordering information scheme

Example: STM32 F 052 R B T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

052 = STM32F052xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

Code size

8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = –40 to 85 °C
7 = –40 to 105 °C

Options

xxx = programmed parts
TR = tape and real

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7 Revision history

Table 25. Document revision history

Date	Revision	Changes
07-Nov-2012	1	Initial release

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