Scheduling Divisible Workloads from Multiple Sources in Network-on-chip Plan

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Abstract

This paper is about multiple sources workloads scheduling in Network-on-chip.

Keywords: Divisible Load Theory, Processor equivalence, Voronoi Diagram, Optimal Mass Transport, Network-on-chip, Monte Carlo Method, Manhattan Distance

1. Introduction

Processor Equivalence[1] [2]
There are some properties about the NOC.

- Each unit core has 4 ports.
- Each unit core's computation ability and communication ability is the same.

There has some variable situation need to be considered.

1. Each unit core has front-end or not.
2. The number of sources.
3. The source position,for example, corner,edge or inner grid position.
4. The load fraction of each sources. They are even or not.
5. Computation and Communication schema
   - Simultaneously computing after receiving the first bit.
   - Computing after receiving the whole fraction.

2. Processor Equivalence

2.1. Load From Corner

- 2*2 regular mesh 1
- 2*3 regular mesh 2
- 2*n regular mesh 3
- m*n regular mesh 4
- Sensitivity Analysis 5 6

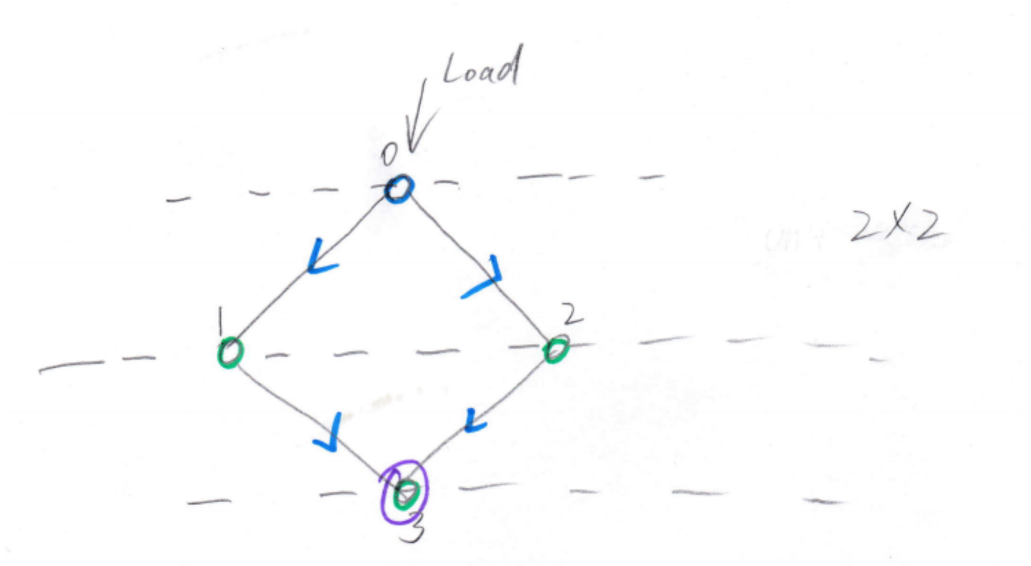

Figure 1: 2*2 regular mesh

2.2. Processor Equivalence Formula

- Simultaneously computing after receiving the first bit.7
- Computing after receiving the whole fraction.8

2.3. Load From Edge

- Load from edge grid point. 9

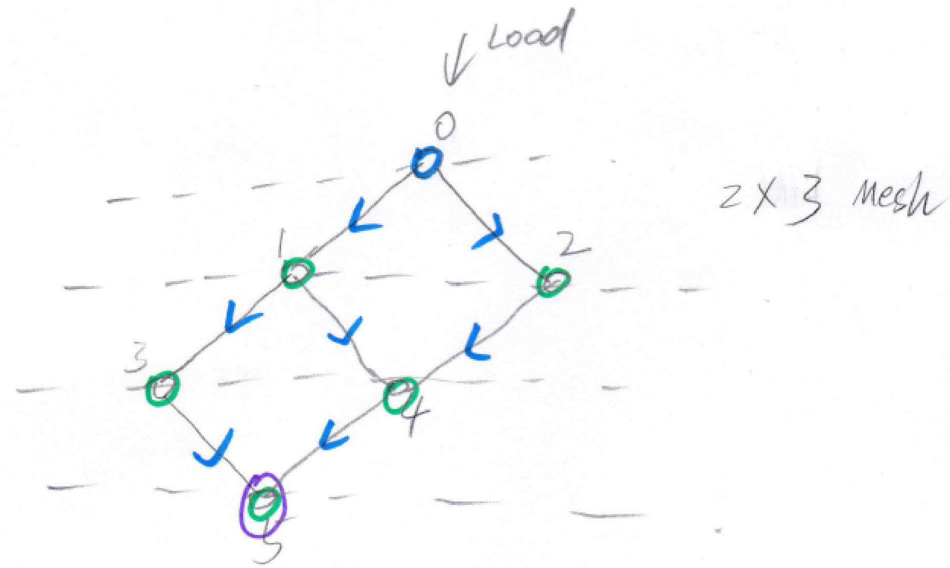

Figure 2: 2*3 regular mesh

2.4. Load From Inner Grid Point

- Load from inner grid position. 9

3. Calculate the source subgraph

- the sources consist of a whole larger source node.11
- the load fraction are even.We can calculate the Manhattan Voronoi diagram 12 directly under the definition of Manhattan distance.13
- the source load fraction are not even. 14
  - Calculate the Manhattan Voronoi Diagram.
  - Calculate the processor equivalence ability.
  - If the ability of each subgraph equals to the corresponding load fraction, then stop.
  - Otherwise, merge the furthest level leaves to other source node voronoi area.(I can explain with you on Tuesday discussion.) 14

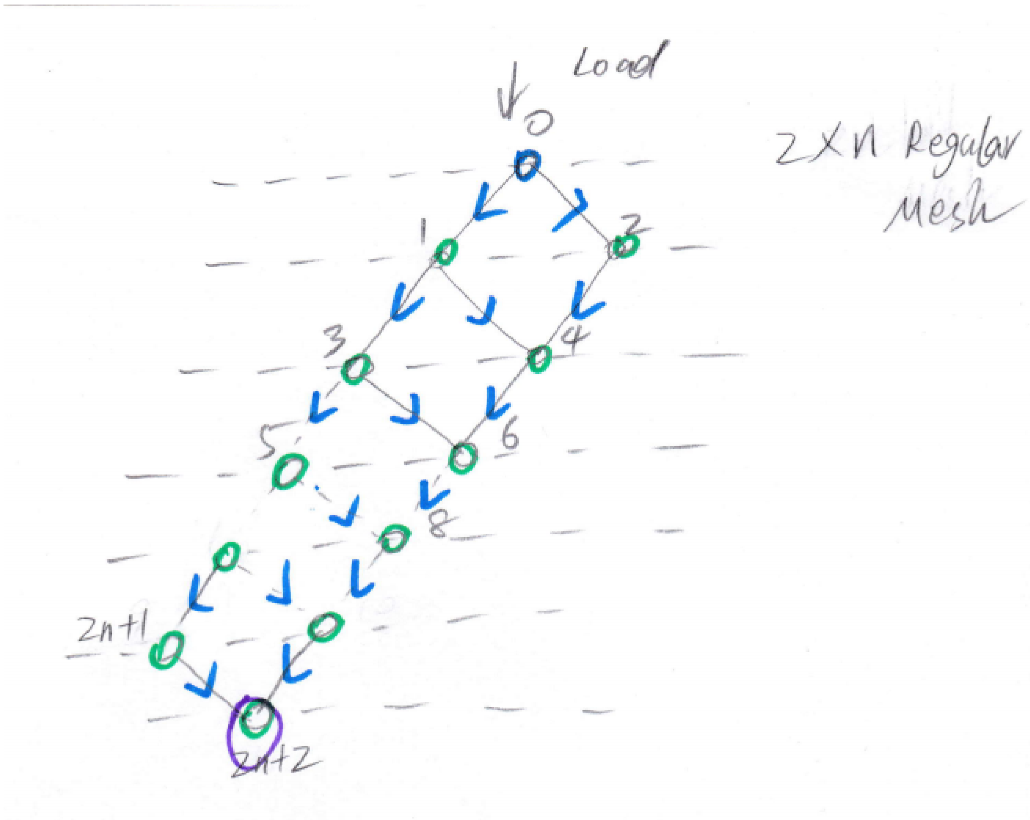

Figure 3: 2*n regular mesh

4. Optimal Mass Transport

- If we know the number of source
- If we know the load fraction of each source
- To decide the location of each base.

The main assumption is here.

- All the unit core are the same.
- The number of core is approximate with the ability with the power of corresponding subgraph.
- The number of core is approximate with the area of each subgraph.

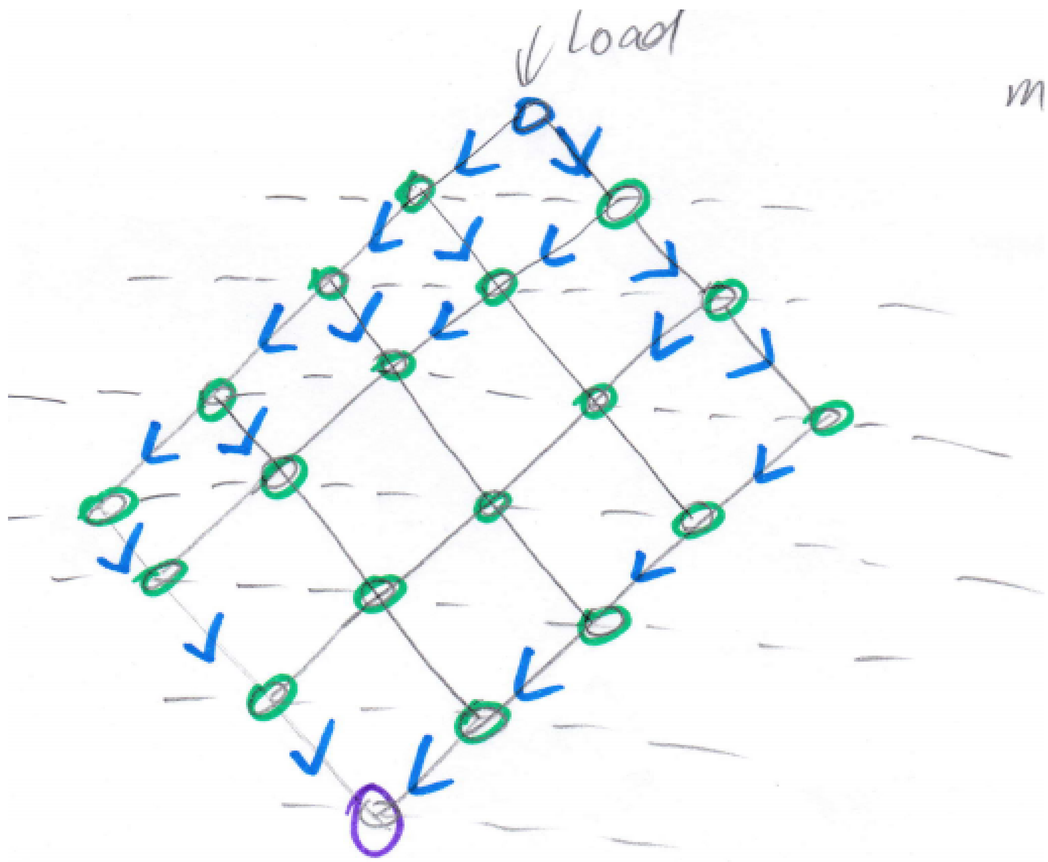

Figure 4: m*n regular mesh

So the problem transfer a work load fraction to a problem which is divide the whole graph to a target area(measure).

If the target workload are equal, we also can choose the Centroidal Voronoi tessellation.

5. Experiment

- PDE simulation
- Superposition
- Processor Equivalence simulation.

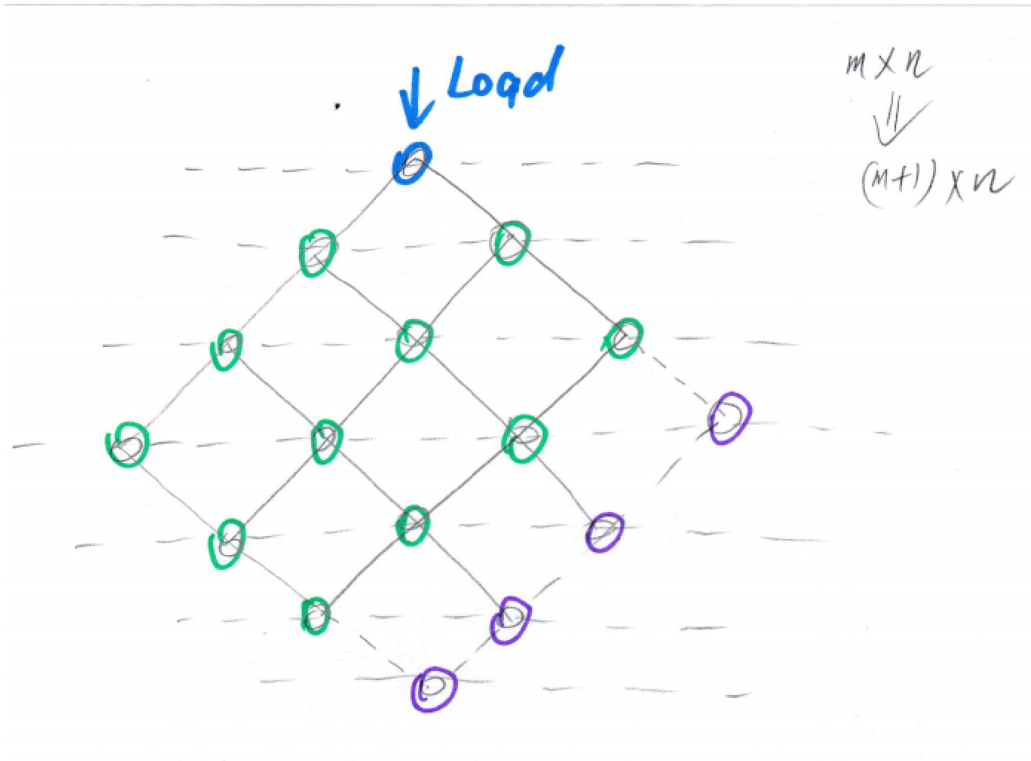

Figure 5: Add one column

6. Conclusion

[1] T. G. Robertazzi, Processor equivalence for daisy chain load sharing processors, IEEE Transactions on Aerospace and Electronic Systems 29 (1993) 1216–1221.

[2] J. Jia, B. Veeravalli, J. Weissman, Scheduling multisource divisible loads on arbitrary networks, IEEE Transactions on Parallel and Distributed Systems 21 (2010) 520–531.

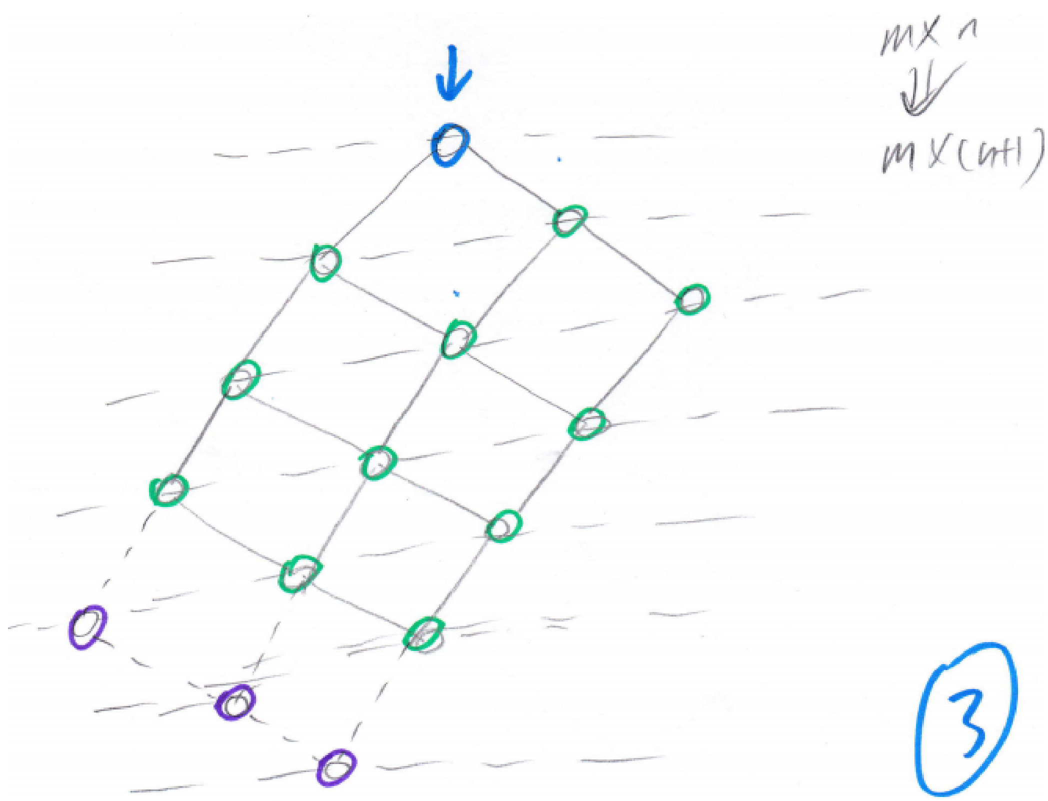

Figure 6: Add one row

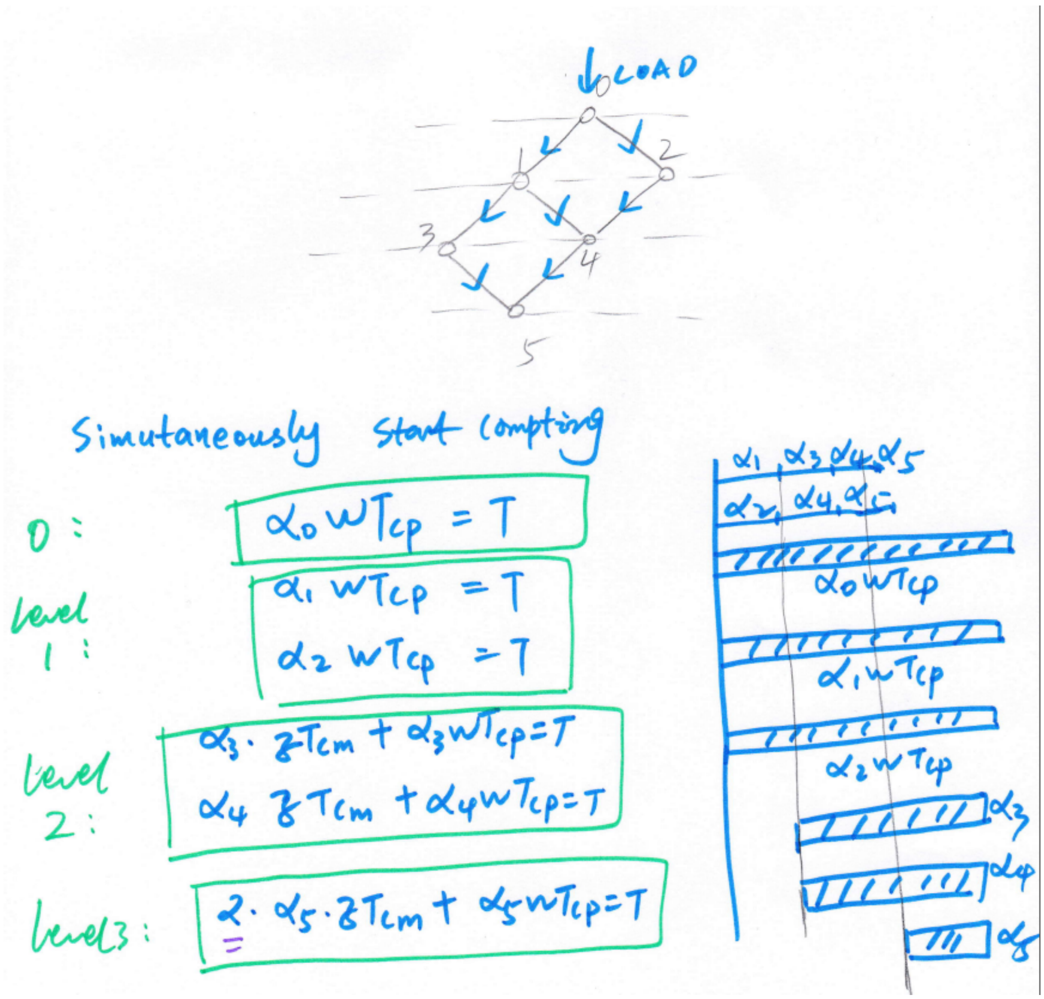

Figure 7: Simultaneously computing after receiving the first bit

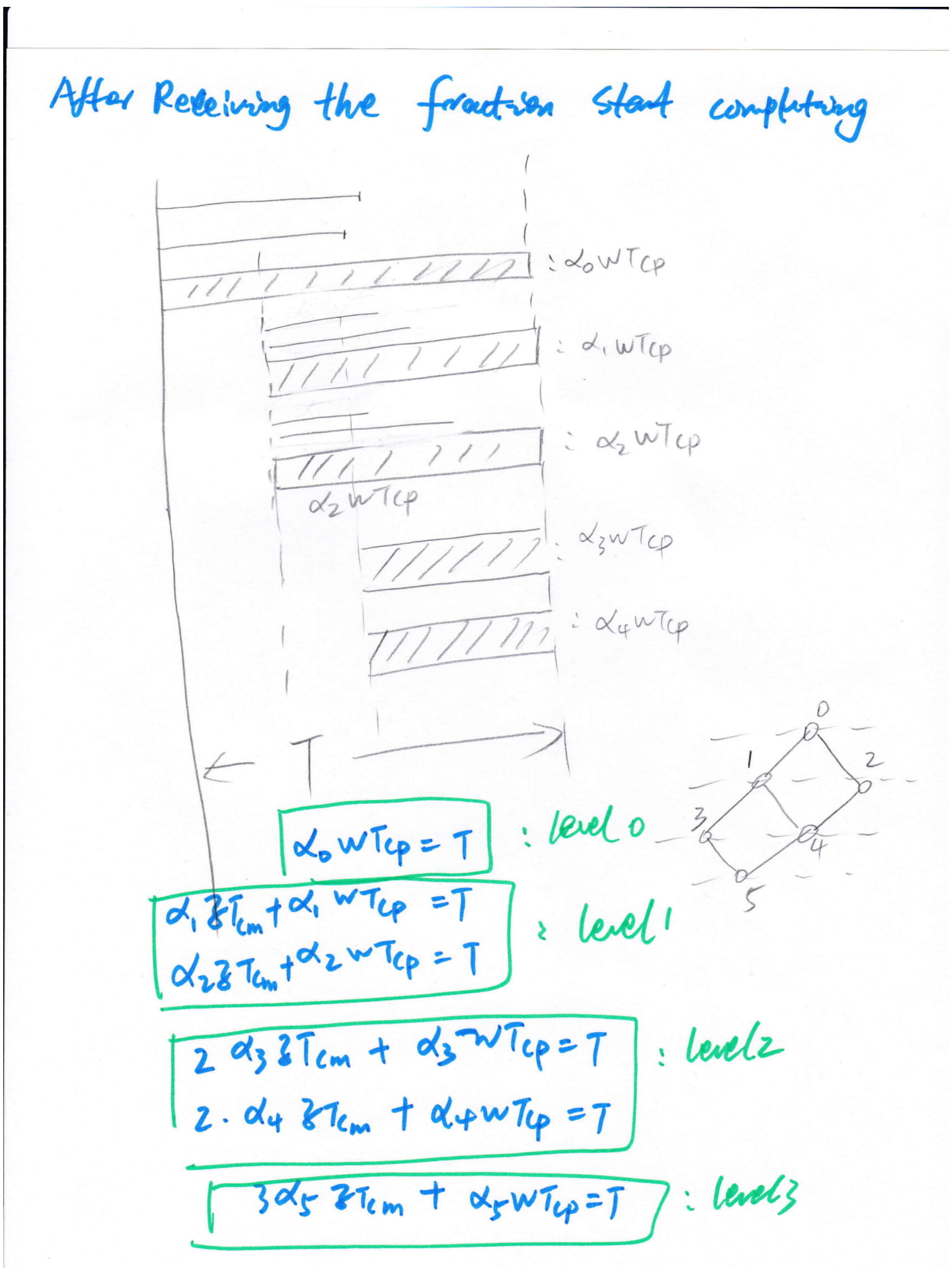

Figure 8: Computing after receiving the whole fraction

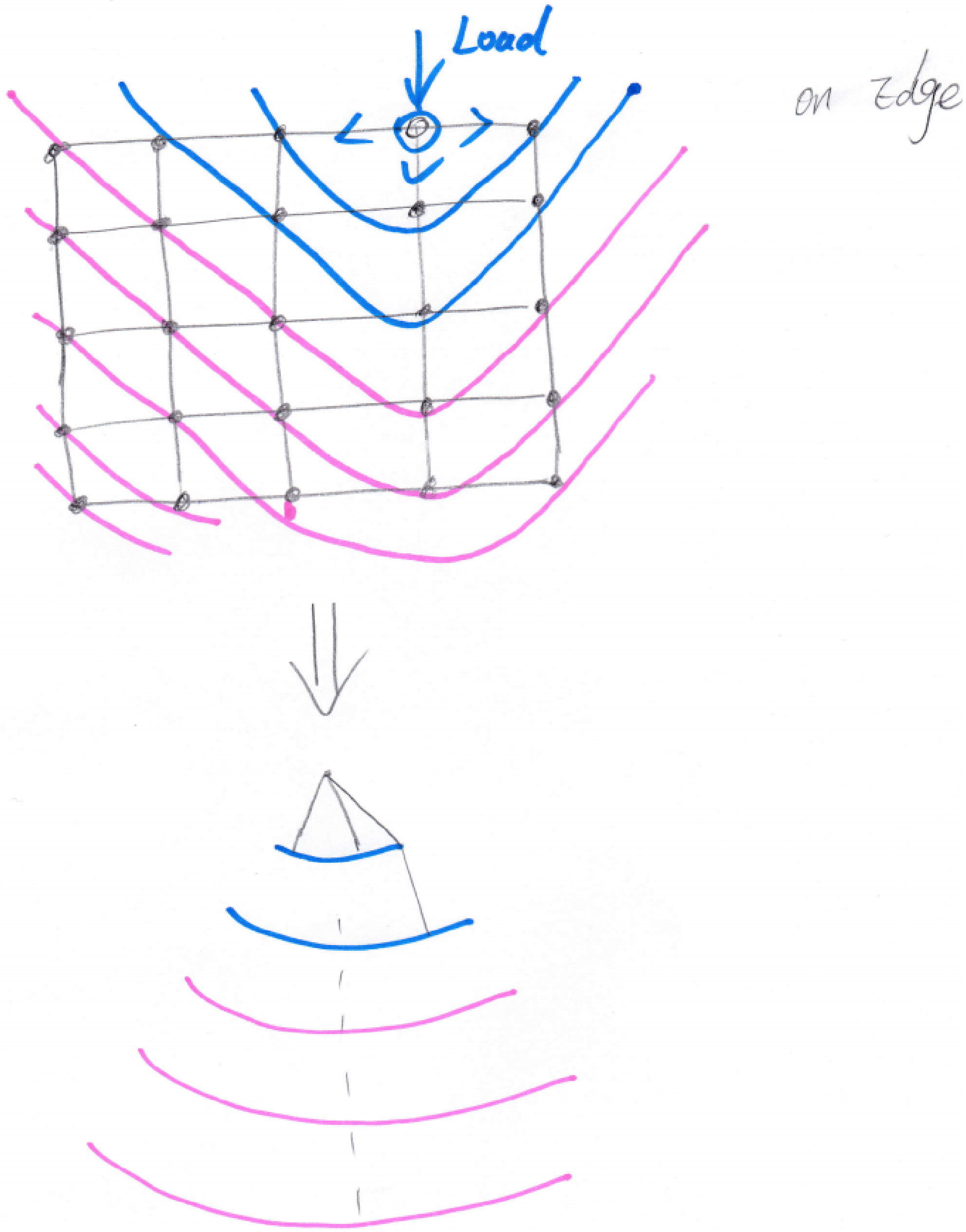

Figure 9: Load from edge grid and the contour line

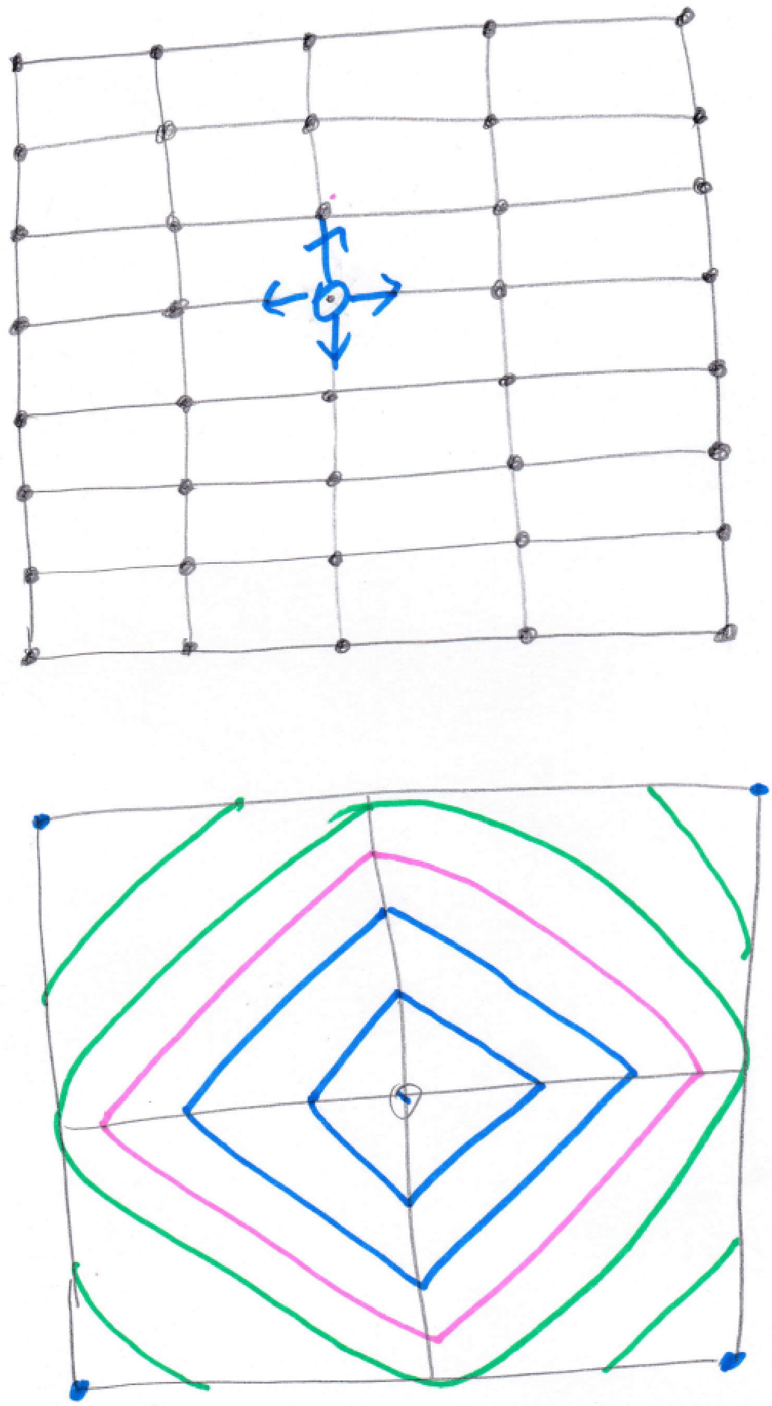

Figure 10: Load from inner grid and it's contour line

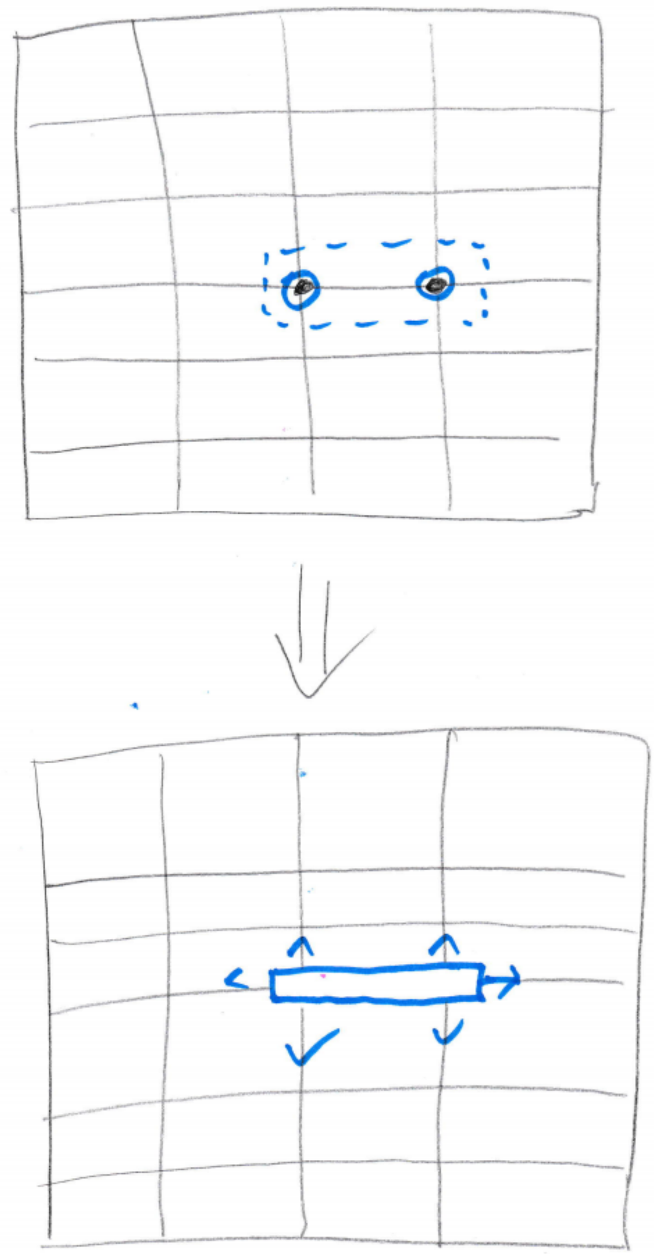

Figure 11: Two source node consists of a whole source node.

Figure 12: Two source node consists of a whole source node.

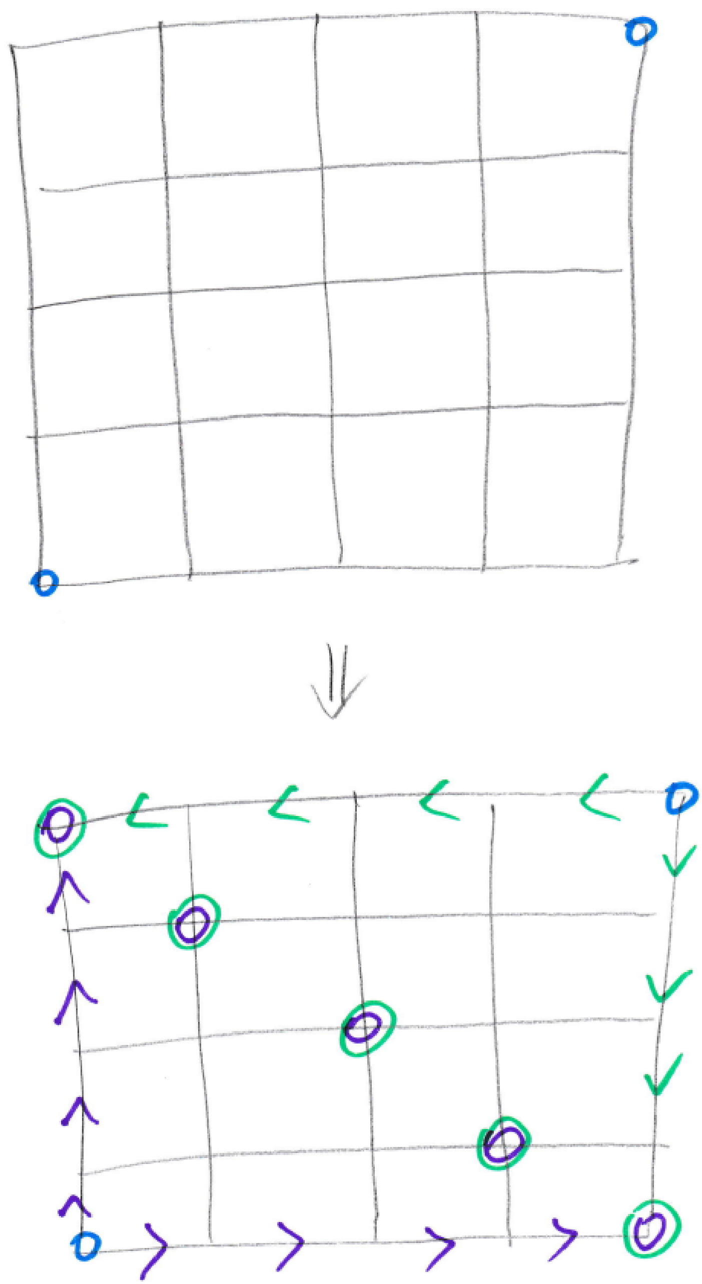

Figure 13: Calculate the Manhattan voronoi

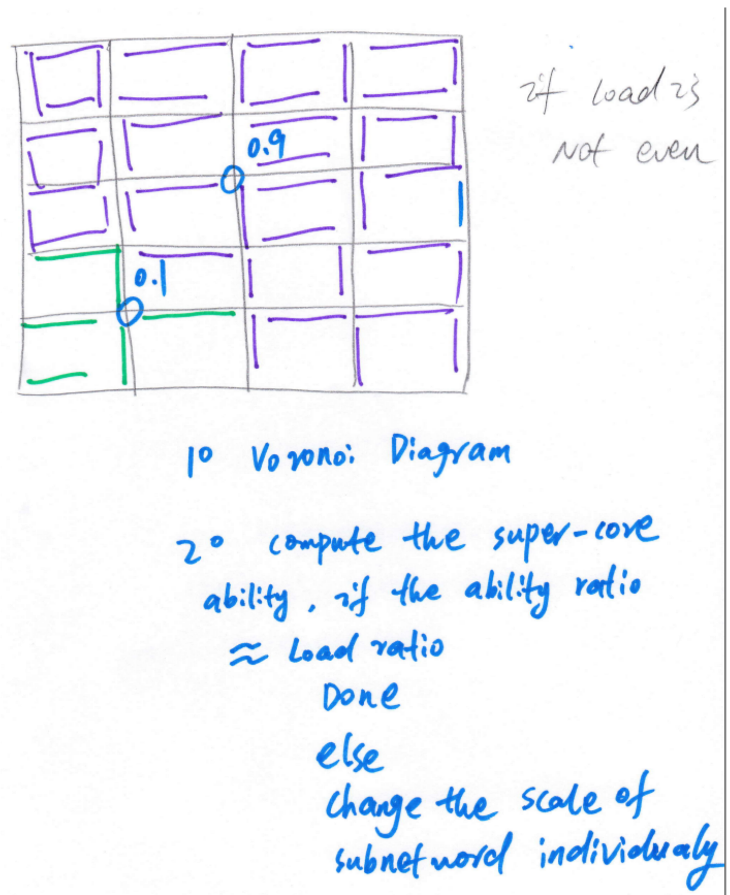

Figure 14: Load balance based on the load fraction