

Scalable Hybrid Wireless Network-on-Chip Architectures for Multicore Systems

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Abstract—Multicore platforms are emerging trends in the design of System-on-Chips (SoCs). Interconnect fabrics for these multicore SoCs play a crucial role in achieving the target performance. The Network-on-Chip (NoC) paradigm has been proposed as a promising solution for designing the interconnect fabric of multicore SoCs. But the performance requirements of NoC infrastructures in future technology nodes cannot be met by relying only on material innovation with traditional scaling. The continuing demand for low-power and high-speed interconnects with technology scaling necessitates looking beyond the conventional planar metal/dielectric-based interconnect infrastructures. Among different possible alternatives, the on-chip wireless communication network is envisioned as a revolutionary methodology, capable of bringing significant performance gains for multicore SoCs. Wireless NoCs (WiNoCs) can be designed by using miniaturized on-chip antennas as an enabling technology. In this paper, we present design methodologies and technology requirements for scalable WiNoC architectures and evaluate their performance. It is demonstrated that WiNoCs outperform their wired counterparts in terms of network throughput and latency, and that energy dissipation improves by orders of magnitude. The performance of the proposed WiNoC is evaluated in presence of various traffic patterns and also compared with other emerging alternative NoCs.

Index Terms—Network-on-chip, multicore, wireless communication, on-chip antenna, small-world network.



1 INTRODUCTION

THE Network-on-Chip (NoC) paradigm has emerged as a communication backbone to enable a high degree of integration in multicore System-on-Chips (SoCs) [1]. Despite their advantages, an important performance limitation in traditional NoCs arises from planar metal interconnect-based multihop communications, wherein the data transfer between two distant blocks causes high latency and power consumption. To alleviate this problem, insertion of long-range links in a standard mesh network using conventional metal wires has been proposed [2]. Another effort to improve the performance of multihop NoC was undertaken by introducing ultralow-latency and low-power express channels between communicating nodes [3], [4]. But these communication channels are also basically metal wires, though they are significantly more power and delay-efficient compared to their more conventional counterparts. According to the International Technology Roadmap for Semiconductors (ITRS) [5] for the longer term, improvements in metal wire characteristics will no longer satisfy

performance requirements and new interconnect paradigms are needed. Different approaches have been explored already, such as 3D and photonic NoCs and NoC architectures with multiband RF interconnect [6], [7], [8]. Though all these emerging methodologies are capable of improving the power and latency characteristics of the traditional NoC, they need further and more extensive investigation to determine their suitability for replacing and/or augmenting existing metal/dielectric-based planar multihop NoC architectures. Consequently, it is important to explore further alternative strategies to address the limitations of planar metal interconnect-based NoCs.

Here, we propose an innovative and novel approach, which addresses simultaneously the latency, power consumption, and interconnect routing problems: replacing multihop wired paths in a NoC by high-bandwidth single-hop long-range wireless links.

Over the last few years, there have been considerable efforts in the design and fabrication of miniature antennas operating in the range of tens of gigahertz to hundreds of terahertz, opening up the possibility of designing on-chip wireless links [9], [10], [11]. It is also predicted that the intrachip communication bandwidth achievable with conventional CMOS-based RF technology is not going to be sufficient [12]. Hence, the need to explore alternative technologies arises. Recent research has uncovered excellent emission and absorption characteristics leading to dipole-like radiation behavior in carbon nanotubes (CNTs), making them promising for use as antennas for on-chip wireless communication [11]. In this paper, the design principles of Wireless Network-on-Chip (WiNoC) architectures are presented. The performance benefits of these WiNoCs due to the utilization of high-speed wireless links are evaluated through cycle accurate simulations. On-chip wireless links

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enable one-hop data transfers between distant nodes and hence reduce the hop counts in intercore communication. In addition to reducing interconnect delay, eliminating multi-hop long-distance wired communication reduces energy dissipation as well. In future, the number of cores in an SoC is expected to increase manifold. Consequently, it is imperative to have a scalable communication infrastructure without affecting system performance significantly. Our work proposes a scalable WiNoC architecture and evaluates its performance with respect to conventional wired NoCs. It is demonstrated that by utilizing the wireless medium efficiently, it is possible to minimize the effects of scaling up the system size on the performance of the WiNoCs. It is possible to create various configurations for the WiNoC depending on the number of available wireless channels and their placement in the network. All the different WiNoC architectures, considered in this paper, are shown to dissipate significantly less energy and to achieve notable improvements in throughput and latency compared to traditional wired NoCs.

2 RELATED WORK

Conventional NoCs use multihop packet switched communication. At each hop, the data packet goes through a complex router/switch, which contributes considerable power, throughput, and latency overhead. To improve performance, the concept of express virtual channels is introduced in [3]. It is shown that by using virtual express lanes to connect distant cores in the network, it is possible to avoid the router overhead at intermediate nodes, and thereby greatly improve NoC performance in terms of power, latency, and throughput. Performance is further improved by incorporating ultralow-latency, multidrop on-chip global lines (G-lines) for flow-control signals [4]. In [2], performance of NoCs has been shown to improve by insertion of long-range wired links following principles of small-world graphs [13]. Despite significant performance gains, the schemes in [2], [3], [4] still require laying out long wires across the chip and hence performance improvements beyond a certain limit may not be achievable.

The performance improvements due to NoC architectural advantages will be significantly enhanced if 3D integration is adopted as the basic fabrication methodology. The amalgamation of two emerging paradigms, namely NoCs and 3D ICs, allows for the creation of new structures that enable significant performance enhancements over traditional solutions [6], [14], [15]. Despite these benefits, 3D architectures pose new technology challenges such as thinning of the wafers, interdevice layer alignment, bonding, and interlayer contact patterning [16]. Additionally, the heat dissipation in 3D structures is a serious concern due to increased power density [16], [17] on a smaller footprint. There have been some efforts to achieve near speed-of-light communications through on-chip wires [18], [19]. Though these techniques achieve very low delay in data exchange along long wires, they suffer from significant power and area overheads from the signal conditioning circuitry. Moreover, the speed of communication is actually about a factor of one-half the speed of light in silicon dioxide. By contrast, on-chip data links at the true velocity of light can be designed using recent

advances in silicon photonics [20], [21]. The design principles of a photonic NoC are elaborated in [6] and [21]. The components of a complete photonic NoC, e.g., dense waveguides, switches, optical modulators, and detectors, are now viable for integration on a single silicon chip. It is estimated that a photonic NoC will dissipate an order of magnitude less power than an electronic planar NoC. Although the optical interconnect option has many advantages, some aspects of this new paradigm need more extensive investigation. The speed of light in the transmitting medium, losses in the optical waveguides, and the signal noise due to coupling between waveguides are the important issues that need more careful investigation. Another alternative is NoCs with multiband RF interconnects [22]. Various implementation issues of this approach are discussed in [8]. In this particular NoC, instead of depending on the charging/discharging of wires for sending data, electromagnetic (EM) waves are guided along on-chip transmission lines created by multiple layers of metal and dielectric stack [22]. As the EM waves travel at the effective speed of light, low-latency and high-bandwidth communication can be achieved. This type of NoC too, is predicted to dissipate an order of magnitude less power than the traditional planar NoC with significantly reduced latency.

On-chip wireless interconnects were demonstrated first in [23] for distributing clock signals. Recently, the design of a wireless NoC based on CMOS Ultra-Wideband (UWB) technology was proposed [24]. The particular antennas used in [24] achieve a transmission range of 1 mm with a length of 2.98 mm. Consequently, for a NoC spreading typically over a die area of 20 mm \times 20 mm, this architecture essentially requires multihop communication through the on-chip wireless channels. Moreover, the overheads of a wireless link may not be justifiable for 1 mm range of on-chip communication compared to a wired channel. We therefore propose to use relatively long-range on-chip wireless communication data links to achieve energy-efficient and low-latency wireless NoC architectures.

3 WIRELESS NOC ARCHITECTURE

In a generic wired NoC, the constituent embedded cores communicate via multiple switches and wired links. This multihop communication results in data transfers with high energy dissipation and latency. To alleviate this problem, we propose long-distance high-bandwidth wireless links between distant cores in the chip. In the following sections, we will explain the design of a scalable architecture for WiNoCs of various system sizes.

3.1 Topology

Modern complex network theory [25] provides us with a powerful method to analyze network topologies and their properties. Between a regular, locally interconnected mesh network and a completely random Erdős-Rényi topology, there are other classes of graphs [25], such as small-world and scale-free graphs. Networks with the small-world property have a very short average path length, which is commonly measured as the number of hops between any pair of nodes. The average shortest path length of small-world graphs is bounded by a polynomial in $\log(N)$, where

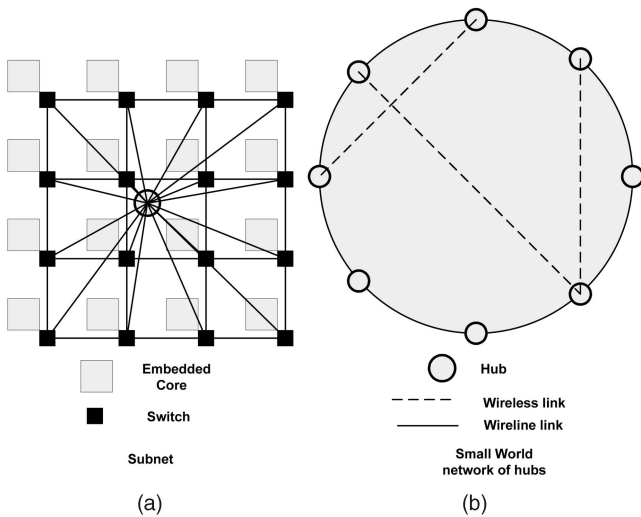


Fig. 1. (a) Mesh topology of subnet with a hub connected to all switches in the subnet. (b) Network topology of hubs connected by a small-world graph with both wired and wireless links.

N is the number of nodes, which makes them particularly interesting for efficient communication with minimal resources [26], [27]. This feature of small-world graphs makes them particularly attractive for constructing scalable WiNoCs. Most complex networks, such as social networks, the Internet, as well as certain parts of the brain exhibit the small-world property. A small-world topology can be constructed from a locally connected network by rewiring connections randomly to any other node, which creates shortcuts in the network [28]. These random long-range links between nodes can also be established following probability distributions depending on the distance separating the nodes [29]. It has been shown that such “shortcuts” in NoCs can significantly improve the performance compared to locally interconnected mesh-like networks [2], [27] with fewer resources than a fully connected system.

Our goal here is to use the “small-world” approach to build a highly efficient NoC based on both wired and wireless links. Thus, for our purpose, we first divide the whole system into multiple small clusters of neighboring cores and call these smaller networks *subnets*. As subnets are smaller networks, *intrasubnet* communication will have a shorter average path length than a single NoC spanning the whole system. Fig. 1a shows a subnet with mesh topology. This mesh subnet has NoC switches and links as in a standard mesh-based NoC. The cores are connected to a centrally located hub through direct links and the hubs from all subnets are connected in a second-level network forming a hierarchical network. This upper level of the hierarchy is designed to have characteristics of small-world graphs. Due to a limited number of possible wireless links, as discussed in later sections, neighboring hubs are connected by traditional wired links forming a bidirectional ring and a few wireless links are distributed between hubs separated by relatively long distances. Reducing long-distance multihop wired communication is essential in order to achieve the full benefit of on-chip wireless networks for multicore systems. As the links are initially established probabilistically, the network performance

might not be optimal. Hence, after the initial placement of the wireless links the network is further optimized for performance by using Simulated Annealing (SA) [30]. The particular probability distribution and the heuristics followed in establishing the network links are described in the next section. Key to our approach is establishing optimal overall network topology under given resource constraints, i.e., a limited number of wireless links. Fig. 1b shows a possible interconnection topology with eight hubs and three wireless links. Instead of the ring used in this example, the hubs can be connected in any other possible interconnect architecture. The size and number of subnets are chosen such that neither the subnets nor the upper level of the hierarchy become too large. This is because if either level of the hierarchy becomes too large then it causes a performance bottleneck by limiting the data throughput in that level. However, since the architecture of the two levels can be different causing their traffic characteristics to differ from each other, the exact hierarchical division can be obtained by performing system-level simulations as shown in Section 4.3.

We propose a hybrid wired/wireless NoC architecture. The hubs are interconnected via both wireless and wired links while the subnets are wired only. The hubs with wireless links are equipped with wireless base stations (WBs) that transmit and receive data packets over the wireless channels. When a packet needs to be sent to a core in a different subnet it travels from the source to its respective hub and reaches the hub of the destination subnet via the small-world network consisting of both wireless and wired links, where it is then routed to the final destination core. For intersubnet and intrasubnet data transmission, wormhole routing is adopted. Data packets are broken down into smaller parts called flow-control units or *flits* [31]. The header flit holds the routing and control information. It establishes a path, and subsequent payload or body flits follow that path. The routing protocol is described in Section 3.4.

3.2 Wireless Link Insertion and Optimization

As mentioned above, the overall interconnect infrastructure of the WiNoC is formed by connecting the cores in the subnets with each other and to the central hub through traditional metal wires. The hubs are then connected by wires and wireless links such that the second level of the network has the small-world property. The placement of the wireless links between a particular pair of source and destination hubs is important as this is responsible for establishing high-speed, low-energy interconnects on the network, which will eventually result in performance gains. Initially, the links are placed probabilistically; i.e., between each pair of source and destination hubs, i and j , respectively, the probability P_{ij} of having a wireless link is proportional to the distance measured in number of hops along the ring, h_{ij} , as shown in (1).

$$P_{ij} = \frac{h_{ij}}{\sum_{i,j} h_{ij}}. \quad (1)$$

The probabilities are normalized such that their sum is equal to one. Such a distribution is chosen because in the presence of a wireless link, the distance between the pair

becomes a single hop and hence it reduces the original distance between the communicating hubs through the ring. Depending on the number of available wireless links, they are inserted between randomly chosen pairs of hubs, which are chosen following the probability distribution mentioned above.

Once the network is initialized, an optimization by means of SA heuristics is performed. Since the subnet architectures are independent of the top-level network, the optimization can be done only on the top-level network of hubs and hence the subnets can be decoupled from this step. The optimization step is necessary as the random initialization might not produce the optimal network topology. SA offers a simple, well established, and scalable approach for the optimization process as opposed to a brute-force search.

If there are N hubs in the network and n wireless links to distribute, the size of the search space S is given by

$$|S| = \binom{\binom{N}{2} - N}{n}. \quad (2)$$

Thus, with increasing N , it becomes increasingly difficult to find the best solution by exhaustive search. In order to perform SA, a metric has been established, which is closely related to the connectivity of the network. The metric to be optimized is the average distance, measured in number of hops, between all source and destination hubs. To compute this metric, the shortest distances between all hub pairs are computed following the routing strategy outlined in Section 3.4. In each iteration of the SA process, a new network is created by randomly rewiring a wireless link in the current network. The metric for this new network is calculated and compared to the metric of the current network. The new network is always chosen as the current optimal solution if the metric is lower. However, even if the metric is higher, we choose the new network probabilistically. This reduces the probability of getting stuck in a local optimum, which could happen if the SA process were to never choose a worse solution. The exponential probability shown in (3) is used to determine whether or not a worse solution is chosen as the current optimal:

$$P(h, h', T) = \exp[(h - h')/T]. \quad (3)$$

The optimization metrics for the current and new networks are h and h' , respectively. T is a temperature parameter, which decreases with the number of optimization iterations according to an *annealing schedule*. In this work, we have used Cauchy scheduling, where the temperature varies inversely with the number of iterations [30]. The algorithm used to optimize the network is shown in Fig. 2.

Here, we assume a uniform spatial traffic distribution where a packet originating from any core is equally likely to have any other core on the die as its destination. However, with other kinds of spatial traffic distributions, where the network loads are localized in different clusters, the metric for optimization has to be changed accordingly to account for the nonuniform traffic patterns as discussed later in Section 4.6.

An important component in the design of the WiNoCs is the on-chip antenna for the wireless links. In the next section, we describe various alternative on-chip antenna choices and their pros and cons.

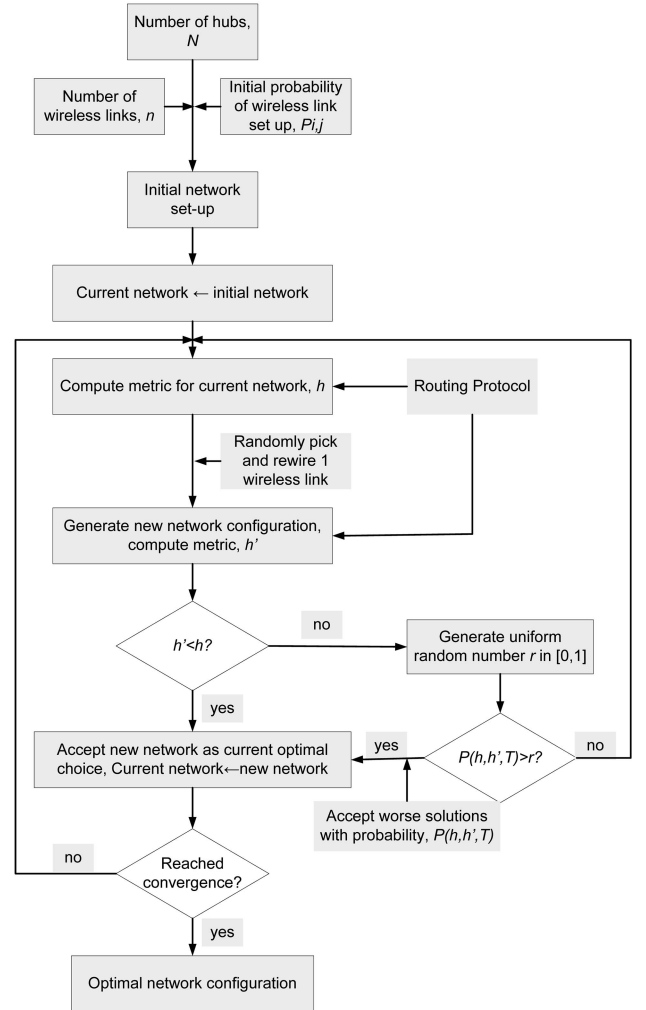


Fig. 2. Flow diagram for the simulated-annealing-based optimization of WiNoC architectures.

3.3 On-Chip Antennas

Suitable on-chip antennas are necessary to establish wireless links for WiNoCs. In [9], the authors demonstrated the performance of silicon integrated on-chip antennas for intra- and interchip communication. They have primarily used metal zigzag antennas operating in the range of tens of GHz. Design of an ultra-wideband antenna for inter- and intrachip communication is elaborated in [32]. This particular antenna was used in the design of a wireless NoC [24] mentioned earlier in Section 2. The above-mentioned antennas principally operate in the millimeter wave (tens of GHz) range and consequently their sizes are on the order of a few millimeters.

If the transmission frequencies can be increased to THz/optical range, then the corresponding antenna sizes decrease, occupying much less chip real estate. Characteristics of metal antennas operating in the optical and near-infrared region of the spectrum of up to 750 THz have been studied [33]. Antenna characteristics of CNTs in the THz/optical frequency range have also been investigated both theoretically and experimentally [10], [11]. Bundles of CNTs are predicted to enhance performance of antenna modules by up to 40 dB in radiation efficiency and provide excellent directional properties in far-field patterns [34]. Moreover, these antennas can

achieve a bandwidth of around 500 GHz, whereas the antennas operating in the millimeter wave range achieve bandwidths of tens of GHz [34]. Thus, antennas operating in the THz/optical frequency range can support much higher data rates. CNTs have numerous characteristics that make them suitable as on-chip antenna elements for optical frequencies. Given wavelengths of hundreds of nanometers to several micrometers, there is a need for virtually one-dimensional antenna structures for efficient transmission and reception. With diameters of a few nanometers and any length up to a few millimeters possible, CNTs are the perfect candidate. Such thin structures are almost impossible to achieve with traditional microfabrication techniques for metals. Virtually defect-free CNT structures do not suffer from power loss due to surface roughness and edge imperfections found in traditional metallic antennas. In CNTs, ballistic electron transport leads to quantum conductance, resulting in reduced resistive loss, which allows extremely high current densities in CNTs, namely 4-5 orders of magnitude higher than copper. This enables high transmitted powers from nanotube antennas, which is crucial for long-range communications. By shining an external laser source on the CNT, radiation characteristics of multiwalled carbon nanotube (MWCNT) antennas are observed to be in excellent quantitative agreement with traditional radio antenna theory [11], although at much higher frequencies of hundreds of THz. Using various lengths of the antenna elements corresponding to different multiples of the wavelengths of the external lasers, scattering and radiation patterns are shown to be improved. Such nanotube antennas are good candidates for establishing on-chip wireless communications links and are henceforth considered in this work.

Chemical vapor deposition (CVD) is the traditional method for growing nanotubes in specific locations by using lithographically patterned catalyst islands. The application of an electric field during growth or the direction of gas flow during CVD can help align nanotubes. However, the high-temperature CVD could potentially damage some of the preexisting CMOS layers. To alleviate this, localized heaters in the CMOS fabrication process to enable localized CVD of nanotubes without exposing the entire chip to high temperatures are used [35].

As mentioned above, the NoC is divided into multiple subnets. Hence, the WBs in the subnets need to be equipped with transmitting and receiving antennas, which will be excited using external laser sources. As mentioned in [7], the laser sources can be located off-chip or bonded to the silicon die. Hence, their power dissipation does not contribute to the chip power density. The requirements of using external sources to excite the antennas can be eliminated if the electroluminescence phenomenon from a CNT is utilized to design linearly polarized dipole radiation sources [36]. But further investigation is necessary to establish such devices as successful transceivers for on-chip wireless communication.

To achieve line of sight communication between WBs using CNT antennas at optical frequencies, the chip packaging material has to be elevated from the substrate surface to create a vacuum for transmission of the high-frequency EM waves. Techniques for creating such vacuum packaging are already utilized for MEMS applications [37], and can be adopted to make creation of line of sight communication

between CNT antennas viable. In classical antenna theory, it is known that the received power degrades inversely with the fourth power of the separation between source and destination due to ground reflections beyond a certain distance. This threshold separation, r_0 between source and destination antennas assuming a perfectly reflecting surface, is given by (4).

$$r_0 = \frac{2\pi H^2}{\lambda}. \quad (4)$$

Here, H is the height of the antenna above the reflecting surface and λ is the wavelength of the carrier. Thus, if the antenna elements are at a distance of H from the reflective surfaces like the packaging walls and the top of the die substrate, the received power degrades inversely with the square of the distance until it is r_0 . Thus, H can be adjusted to make the maximum possible separation smaller than the threshold separation r_0 for a particular frequency of radiation used. Considering the optical frequency ranges of CNT antennas, depending on the separation between the source and destination pairs in a single chip, the required elevation is a few tens of microns only.

3.4 Routing and Communication Protocols

In the proposed WiNoC, intrasubnet data routing depends on the topology of the subnets. For example, if the cores within a subnet are connected in a mesh, then data routing within the subnet follows dimension order (e-cube) routing. Intersubnet data are routed through the hubs, along the shortest path between the source and destination subnets in terms of number of links traversed. The hubs in all the subnets are equipped with a prerouting block to determine this path through a search across all potential paths between the hubs of the source and destination subnets. In the current work, paths involving only a single wireless link and none or any number of wired links on the ring are considered. All such paths as well as the completely wired path on the ring are compared and the one with the minimum number of link traversals is chosen for data transfer. For a data packet requiring intersubnet routing, this computation is done only once for the header flit at the hub of the originating subnet. The header flit needs to have a field containing the address of the intermediate hub with a WB that will be used in the path. Only this information is sufficient as the header follows the default wireline path along the ring to that hub with the WB from its source, which is also the shortest path along the ring. Since each WB has a single, unique destination, the header reaches that destination and is then again routed via the wireline path to its final destination hub using normal ring routing. The rest of the flits follow the header, as wormhole routing is adopted in this paper. Considering only those paths that have a single wireless link reduces computational overheads in the WB routers as it limits the search space. As the wireless links are placed as long-distance shortcuts, they are always comparable in length to the diameter of the ring. Hence, the probability that a path with multiple wireless links between any source/destination pair will be shorter than paths with a single wireless link is extremely low. So, in order to achieve the best trade-off between the router complexity and network performance, only paths with single wireless link are considered. Also, if two alternatives

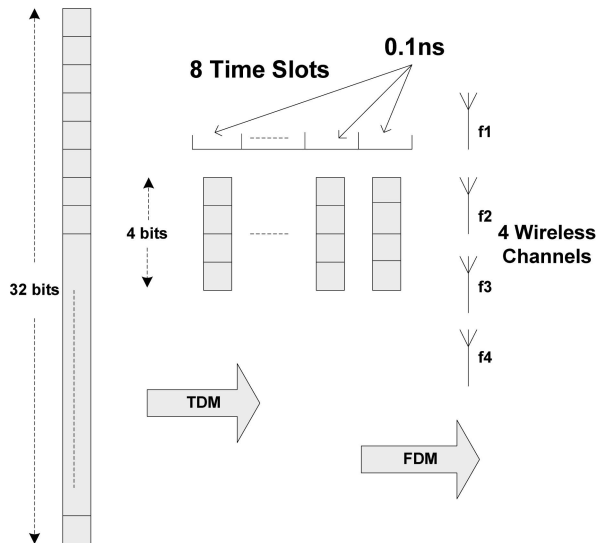


Fig. 3. Adopted communication protocol for the wireless channel.

have the same number of hops, the one with the wireless link is chosen, as this will have less energy dissipation. In this routing scheme, the path is predetermined at the source hub and hence no cycles are possible. Consequently, there is no possibility of a deadlock or livelock.

An alternative routing approach is to avoid the one-time evaluation of the shortest path at the original source hub and adopt a distributed routing mechanism. In this scenario, the path is determined at each node by checking for the existence of a wireless link at that node, which if taken will shorten the path length to the final destination. If this wireless link does not exist or shorten the path in comparison to the wireline path from that node, then the default routing mechanism along the ring is followed to the next node. This mechanism performs a check at every node by computing and comparing the path lengths by using the default wireline routing or the wireless link. The adopted centralized routing performs all the checks at the original source hub, which includes all the wireless links and the wireline path from the source to the destination. We will present the comparative performance evaluation of these two schemes later in Section 4.3.

By using multiband laser sources to excite CNT antennas, different frequency channels can be assigned to pairs of communicating subnets. This will require using antenna elements tuned to different frequencies for each pair, thus creating a form of frequency division multiplexing (FDM) creating dedicated channels between a source and destination pair. This is possible by using CNTs of different lengths, which are multiples of the wavelengths of the respective carrier frequencies. High directional gains of these antennas, demonstrated in [11], [34], aid in creating directed channels between source and destination pairs. In [38], 24 continuous wave laser sources of different frequencies are used. Thus, these 24 different frequencies can be assigned to multiple wireless links in the WiNoC in such a way that a single-frequency channel is used only once to avoid signal interference on the same frequencies. This enables concurrent use of multiband channels over the chip. The number of wireless links in the network can therefore

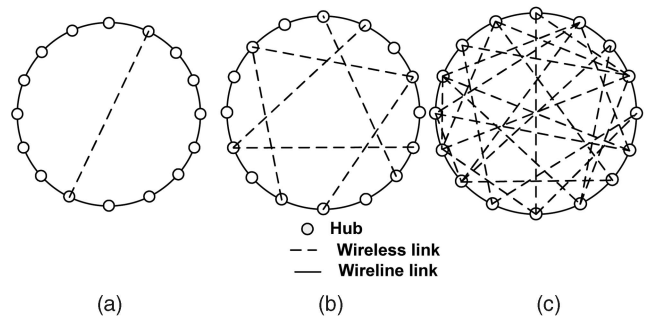


Fig. 4. The optimal wireless link arrangement for (a) 1, (b) 6, and (c) 24 wireless links among 16 hubs. Note that symmetrical solutions with the same performance are possible.

vary from 24 links, each with a single-frequency channel, to a single link with all 24 channels. Assigning multiple channels per link increases the link bandwidth. Currently, high-speed silicon integrated Mach-Zehnder optical modulators and demodulators, which convert electrical signals to optical signals and vice versa are commercially available [39]. The optical modulators can provide 10 Gbps data rate per channel on these links. At the receiver, a low-noise amplifier (LNA) can be used to boost the power of the received electrical signal, which will then be routed into the destination subnet. As noted in [38], this data rate is expected to increase manifold with future technology scaling. The modulation scheme adopted is noncoherent on-off keying (OOK), and therefore does not require complex clock recovery and synchronization circuits. Due to limitations in the number of distinct frequency channels that can be created through the CNT antennas, the flit width in NoCs is generally higher than the number of possible channels per link. Thus, to send a whole flit through the wireless link using a limited number of distinct frequencies, a proper channelization scheme needs to be adopted. In this work, we assume a flit width of 32 bits. Hence, to send the whole flit using the distinct frequency channels, time division multiplexing (TDM) is adopted. The various components of the wireless channel, viz., the electro-optic modulators, the TDM modulator/demodulator, the LNA, and the router for routing data on the network of hubs are implemented as a part of the WB. Fig. 3 illustrates the adopted communication mechanism for the intersubnet data transfer. In this WiNoC example, we use a wireless link with four frequency channels. In this case, one flit is divided into eight four-bit nibbles, and each nibble is assigned a 0.1 ns timeslot, corresponding to a bit rate of 10 Gbps. The bits in each nibble are transmitted simultaneously over four different carrier frequencies. The routing mechanism, discussed in this section, is easily extendable to incorporate other addressing techniques like multicasting. Performance of traditional NoC architectures incorporating multicasting have been already investigated [40] and it can be similarly used to enhance the performance of the WiNoC developed in this work. For example, let us consider a subnet in a 16-subnet system (as in Fig. 4), which tries to send packets to three other subnets such that one of them is diagonally opposite to the source subnet and the other two are on either side of it. In absence of long-range wireless links, using multicasting the zero load latency for the delivery of a single flit is nine cycles whereas without multicasting the same flit will need 11 cycles to be delivered

to the respective destinations. Here, the communication takes place only along the ring. However, if a wireless link exists along the diagonal from the source to the middle destination subnet then with multicasting the flit can be transferred in five cycles if there are eight distinct channels in the link. Four cycles are needed to transfer a 32-bit flit to the diagonally opposite hub via the wireless links and one more hop along the ring to the final destinations on either side. The efficiency of using multicasting varies with number of channels in the link as it governs the bandwidth of the wireless link.

4 EXPERIMENTAL RESULTS

In this section, we analyze the characteristics of the proposed WiNoC architectures and study trends in their performance with scaling of system size. For our experiments, we have considered three different system sizes, namely 128, 256, and 512 cores on a die of size 20 mm × 20 mm. We observe results of scaling up the system size by increasing both the number of subnets as well as the number of cores per subnet. Hence, in one scenario, we have considered a fixed number of cores per subnet to be 16 and varied the number of subnets between 8, 16, and 32. In the other case, we have kept the number of subnets fixed at 16 and varied the size of the subnets from 8 to 32 cores. These system configurations are chosen based on the experiments explained later in Section 4.3. Establishment of wireless links using simulated annealing, however, depends only on the number of hubs on the second level of the network.

4.1 Establishment of Wireless Links

Initially, the hubs are connected in a ring through normal wires and the wireless links are established between randomly chosen hubs following the probability distribution given by (1). We then use simulated annealing to achieve an optimal configuration by finding the positions of the wireless links which minimize the average distance between all source and destination pairs in the network. Fig. 4 shows the location of 1, 6, and 24 wireless links with 24, 4, and 1 channels, respectively, in a network of 16 hubs. We followed the same optimization methodology for all the other networks. The corresponding average distances for the

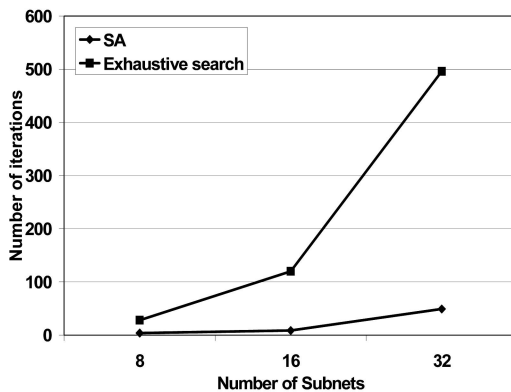
TABLE 1
Average Distance for Optimized WiNoCs

No. of subnets (N)	Avg distance (hops)		
	1 Wire-less Link	6 Wireless Links	24 Wireless Links
8	1.7188	1.3125	1.1250 *
16	3.2891	2.1875	1.5625
32	6.3301	3.8789	2.6309

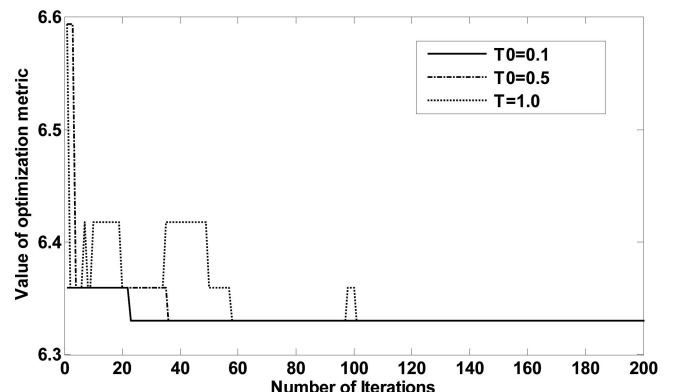
*In case of 8 subnets only 12 wireless links are used with 2 channels per link.

optimized networks with different system sizes are shown in Table 1. It should be noted that the particular placement of wireless links to obtain the optimal network configuration is not unique because of symmetric considerations in our setup, i.e., there are multiple configurations with the same optimal performance.

In order to establish the performance of the SA algorithm used, we compared the resultant optimization metric with the metric obtained through exhaustive search for the optimized network configuration for various system sizes. The SA algorithm produces network configurations with total average hop count exactly equal to that generated by the exhaustive search technique for the system configurations considered in this paper. However, the obtained WiNoC configuration in terms of topology is nonunique as different configurations can have the same average hop count. Fig. 5a shows the number of iterations required to arrive at the optimal solution with SA and exhaustive search algorithms. Clearly, the SA algorithm converges to the optimal configuration much faster than the exhaustive search technique. This advantage will increase for larger system sizes. Fig. 5b shows the convergence of the metric for different values of the initial temperature to illustrate that the SA approach converges robustly to the optimal value of the average hopcount with numerical variation in the temperature. This simulation was performed for a system with 32 subnets with one wireless link. With higher values of the initial temperature, it can take longer to converge. Naturally, for large enough values of the initial temperature,



(a)



(b)

Fig. 5. (a) Number of iterations required to reach optimal solution by the SA and exhaustive search methods, (b) Convergence with different temperatures.

the metric does not converge. On the other hand, lower values of the initial temperature make the system converge faster but at the risk of getting stuck in a local optimum. Using the network configurations developed in this section, we will now evaluate the performance of the WiNoC based on well-established performance metrics.

4.2 Performance Metrics

To characterize the performance of the proposed WiNoC architectures, we consider three network parameters: latency, throughput, and energy dissipation. Latency refers to the number of clock cycles between the injection of a message header flit at the source node and the reception of the tail flit at the destination. Throughput is defined as the average number of flits successfully received per embedded core per clock cycle. Energy dissipation per packet is the average energy dissipated by a single packet when routed from the source to destination node; both the wired subnets and the wireless channels contribute to this. For the subnets, the sources of energy dissipation are the interswitch wires and the switch blocks. For the wireless channels, the main contribution comes from the WBs, which include antennas, transceiver circuits, and other communication modules like the TDM block and the LNA. Energy dissipation per packet, E_{pkt} , can be calculated according to (5) below:

$$E_{pkt} = \frac{N_{intrasubnet}E_{subnet,hop}h_{subnet} + N_{intersubnet}E_{sw}h_{sw}}{(N_{intrasubnet} + N_{intersubnet})}. \quad (5)$$

In (5), $N_{intrasubnet}$ and $N_{intersubnet}$ are the total number of packets routed within the subnet and between subnets, respectively. $E_{subnet,hop}$ is the energy dissipated by a packet traversing a single hop on the wired subnet including a wired link and switch, and E_{sw} is the energy dissipated by a packet traversing a single hop on the second network level of the WiNoC, which has the small-world properties. E_{sw} also includes the energy dissipation in the core to hub links. In (5), h_{subnet} and h_{sw} are the average number of hops per packet in the subnet and the small-world network.

4.3 Performance Evaluation

The network architectures, developed earlier in this section, are simulated using a cycle accurate simulator which models the progress of data flits accurately per clock cycle accounting for flits that reach destination as well as those that are dropped. One hundred thousand iterations were performed to reach stable results in each experiment, eliminating the effect of transients in the first few thousand cycles.

The mesh subnet architecture considered is shown in Fig. 1a. The width of all wired links is considered to be same as the flit size, which is 32 in this paper. The particular NoC switch architecture, adopted from [41] for the switches in the subnets, has three functional stages, namely, input arbitration, routing/switch traversal, and output arbitration. The input and output ports including the ones on the wireless links have four virtual channels per port, each having a buffer depth of 2 flits [41]. Each packet consists of 64 flits. Similar to the intrasubnet communication, we have adopted wormhole routing in the wireless channel too. Consequently, the hubs have similar architectures as the NoC switches in the subnets. Hence, each port of the hub has same input and output arbiters, and equal number of virtual channels with same

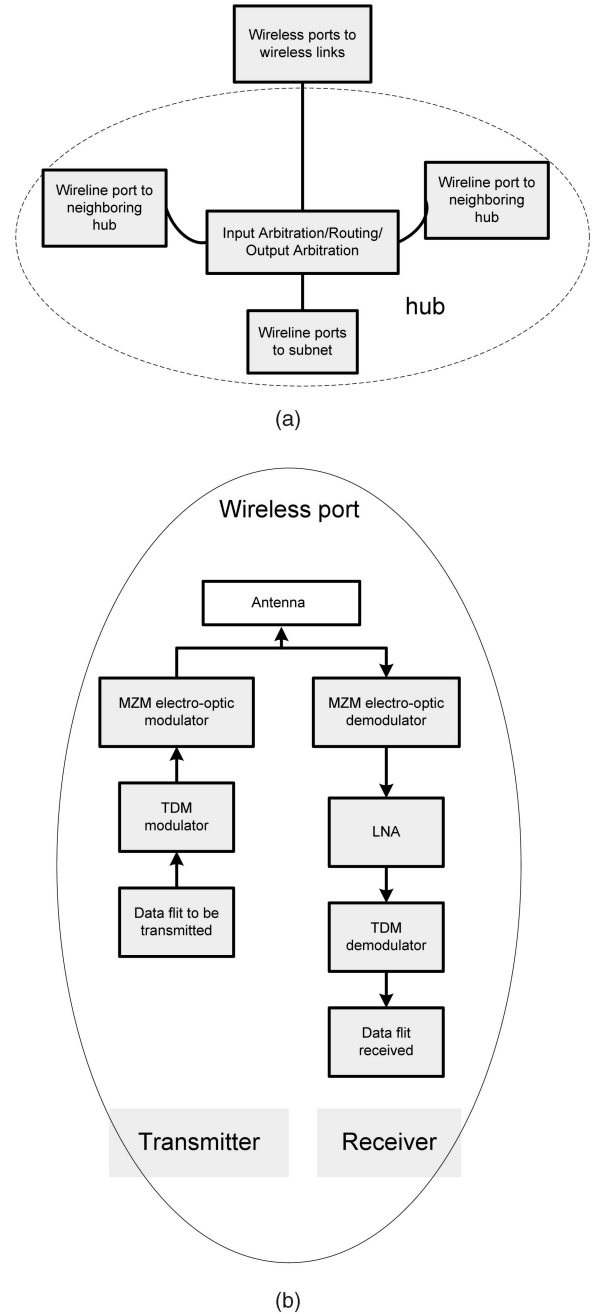


Fig. 6. (a) The components of a WB with multiple wired and wireless ports at input and output. (b) A wireless port.

buffer depths as the subnet switches. The number of ports in a hub depends on the number of links connected to it. The hubs also have three functional stages, but as the number of cores increases in a subnet the delays in arbitration and switching for some cases are more than a clock cycle. Depending on the subnet sizes, traversal through these stages need multiple cycles and this has been taken into consideration while evaluating overall latency of the WiNoC. The wireless ports of the WBs are assumed to be equipped with antennas, TDM modules, and electro-optic modulators and demodulators. The various components of a WB are shown in Fig. 6. A hub consisting of only ports to wired links is also highlighted in the figure to emphasize that a WB has

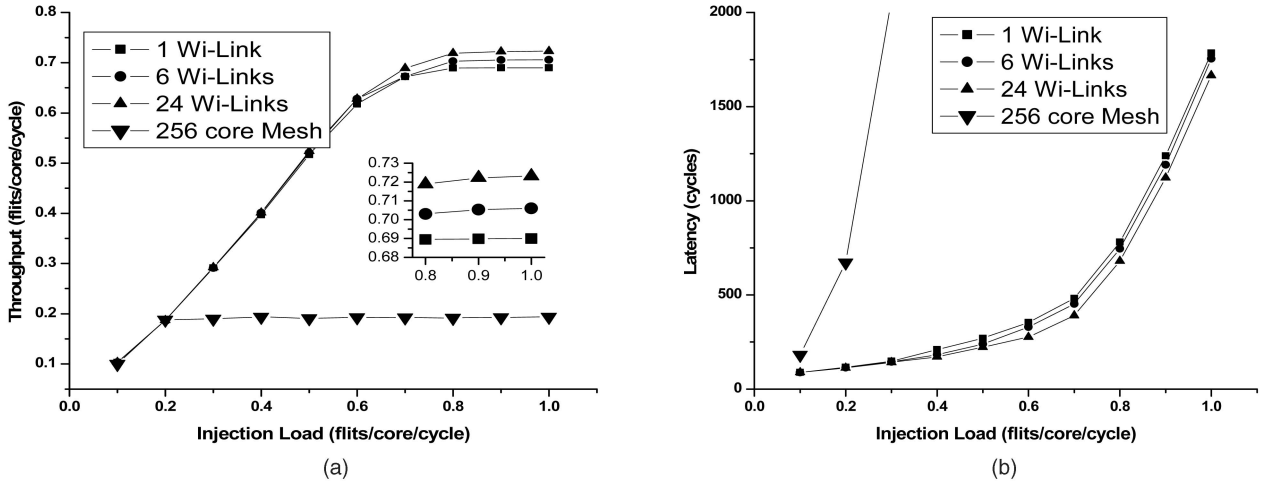


Fig. 7. (a) Throughput and (b) latency of 256-core WiNoCs with different numbers of wireless links.

additional components compared to a hub. A simple flow-control mechanism is adopted uniformly for wireless links in which, the sender WB stops transmitting flits only when a *full* signal is asserted from the receiver WB. This full signal is embedded in a control flit sent from the receiver to the sender only when the receiver buffer is filled above a predefined threshold. When the full signal is asserted, flits do not move and are blocked spanning multiple switches or hubs. This, in turn, can block other messages in the network as in wormhole routing. In case all buffers are full, the new injected packets from the cores are dropped until new buffer space is available. A more advanced flow-control mechanism could be incorporated to improve WiNoC performance further [4]. The NoC switches, the hubs, and the wired links are driven with a clock of frequency 2.5 GHz.

Fig. 7 shows throughput and latency plots as a function of injection load for a system with 256 cores divided into 16 subnets, each with 16 cores. The delays incurred by the wired links from the cores to the hub for varying number of cores in the subnets for different system sizes are shown in Table 2. The delays in the interhub wires for varying number of subnets are also shown. As can be seen, these delays are all less than the clock period of 400 ps and it maybe noted that the lengths of both core-to-hub and interhub wireline links will reduce with increase in the number of subnets as then each subnet becomes smaller in area and the subnets also come closer to each other. The

delays incurred by the electro-optic signal conversions with the MZM devices are 20 ps. When computing the overall system latency and throughput of the WiNoCs, the delays of these individual components are taken into account. This particular hierarchical topology was selected as it provided optimum system performance. Fig. 8 shows the saturation throughputs for alternative ways of dividing the 256-core WiNoC into different numbers of subnets with a single wireless link. As can be seen from the plot, all alternative configurations achieve worse saturation throughput. The same trend is observed if we vary the number of wireless links. Using the same method, the suitable hierarchical division that achieves best performance is determined for all the other system sizes. For system sizes of 128 and 512, the hierarchical divisions considered here achieved much better performance compared to the other possible divisions with either lower or higher number of subnets.

By varying the number of channels in the wireless links, various WiNoC configurations are created. We have considered WiNoCs with 1, 6, and 24 wireless links in our

TABLE 2
Delays on Wired Links in the WiNoCs

System Size	No. of subnets	Subnet size	Core-hub link delay (ps)	Inter-hub link delay (ps)
128	8	16	96	181/86*
	16	8	60	86
256	16	16	60	86
512	16	32	60	86
	32	16	48	86/43*

*for 8 and 32 subnets, the intersubnet distances are different along the two planar directions.

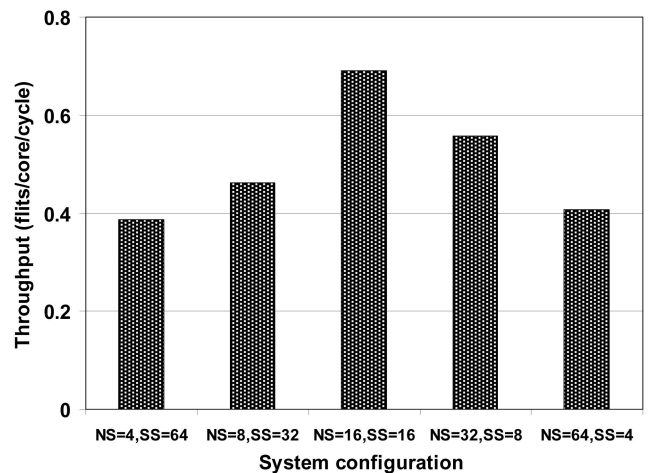


Fig. 8. Throughput of 256-core WiNoC for various hierarchical configurations. **NS = number of subnets, SS = subnet size.

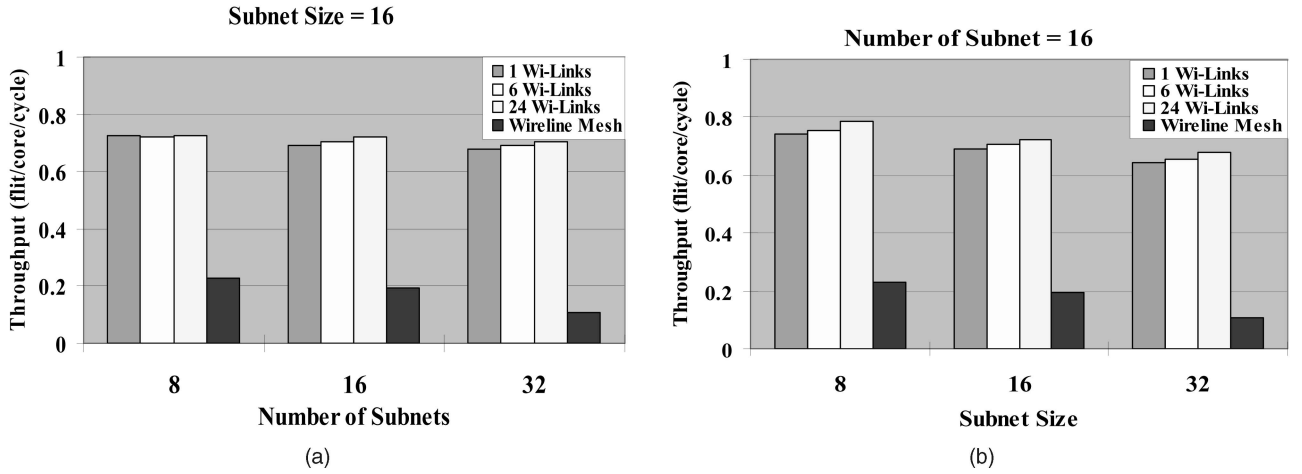


Fig. 9. Saturation throughput with varying (a) number of subnets and (b) size of each subnet.

experiments. Since the total number of frequencies considered in this work is 24, the number of channels per link is 24, 4, and 1, respectively. As can be seen from Fig. 7, the WiNoCs with different possible configurations outperform the single-wired monolithic flat mesh architecture. It can also be observed that with increasing number of wireless links, throughput improves slightly. It should be noted that even though increasing the number of links does increase the number of concurrent wireless communication links, the bandwidth on each link decreases as the total number of channels is fixed by the number of off-chip laser sources. This causes the total bandwidth over all the wireless channels to remain the same. The only difference is in the degree of distribution across the network. Consequently, network throughput increases only slightly with increasing number of wireless links. However, the hardware cost increases with increasing numbers of links as discussed in Section 4.7. Thus, depending upon whether the demand on performance is critical the designer can choose to trade off the area overhead of deploying the maximum number of wireless links possible. However, if the constraints on area overhead are really stringent then one can choose to employ only one wireless link and consequently provide more bandwidth per link and have only a little negative effect on performance.

In order to observe trends among various WiNoC configurations, we performed further analysis. Fig. 9a shows the throughput at network saturation for various system sizes while keeping the subnet size fixed for different numbers of wireless links. Fig. 9b shows the variation in throughput at saturation for different system sizes for a fixed number of subnets. For comparison, the throughput at network saturation for a single traditional wired mesh NoC of each system size is also shown in both of the plots. As in Fig. 7, it may be noted from Fig. 9 that for a WiNoC of any given size, number of subnets and subnet size, the throughput increases with increase in number of wireless links deployed.

As can be observed from the plots, the maximum achievable throughput in WiNoCs degrades with increasing system size for both cases. However, by scaling up the number of subnets, the degradation in throughput is smaller

compared to when the subnet size is scaled up. By increasing the subnet size, we are increasing congestion in the wired subnets and load on the hubs and not fully using the capacity of the high-speed wireless links in the upper level of the network. When the number of subnets scales up, traffic congestion in the subnets does not get worse and the optimal placement of the wireless links makes the top-level network very efficient for data transfer. The effect on throughput with increasing system size is therefore marginal.

To determine the energy dissipation characteristics of the WiNoCs, we first estimated the energy dissipated by the antenna elements. As noted in [11], the directional gain of MWCNT antennas we propose to use is very high. The ratio of emitted power to incident power is around -5 dB along the direction of maximum gain. Assuming an ideal line of sight channel over a few millimeters, transmitted power degrades with distance following the inverse square law. Therefore, the received power P_R can be related to the transmitted power P_T as

$$P_R = \frac{G_T A_R}{4\pi R^2} P_T. \quad (6)$$

In (6), G_T is the transmitter antenna gain, which can be assumed to be -5 dB [11]. A_R is the area of the receiving antenna and R is the distance between the transmitter and receiver. The energy dissipation of the transmitting antennas therefore depends on the range of communication. The area of the receiving antenna can be found by using the antenna configuration used in [11]. It uses a MWCNT of diameter 200 nm and length 7λ , where λ is the optical wavelength. The length 7λ was chosen as it was shown to produce the highest directional gain, G_T , at the transmitter. In one of the setups in [11], the wavelength of the laser used was 543.5 nm, and hence the length of the antenna is around $3.8 \mu\text{m}$. Using these dimensions, the area of the receiving antenna, A_T can be calculated.

The noise floor of the LNA [42] is -101 dBm. Considering the MZM, demodulators cause an additional loss of up to 3 dB over the the operational bandwidth, the receiver sensitivity turns out to be -98 dBm in the worst case. The length of the longest possible wireless link considered among all WiNoC configurations is 23 mm. For this length and receiver sensitivity, a transmitted power of 1.3 mW is required.

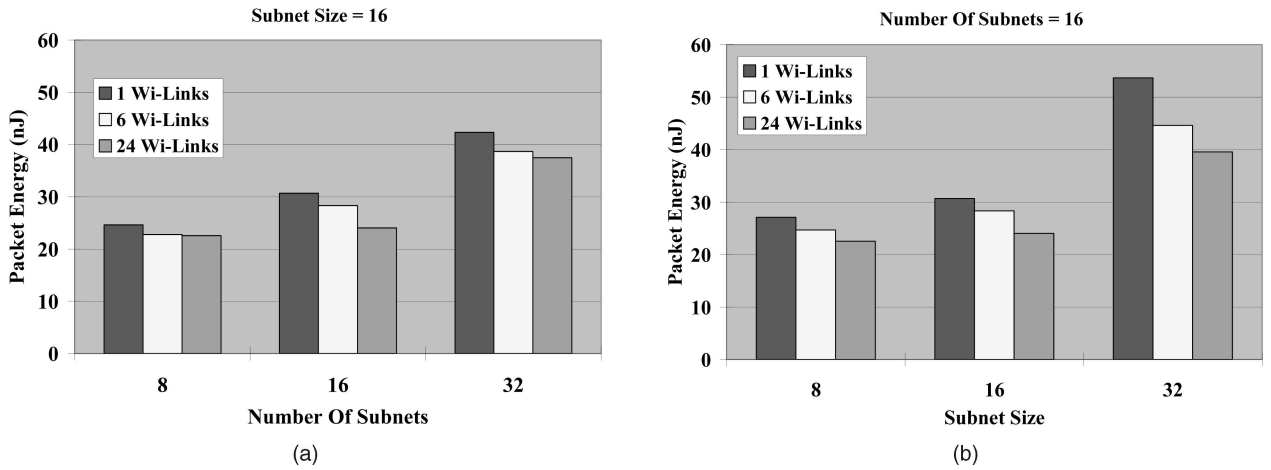


Fig. 10. Packet energy dissipation with varying (a) number of subnets and (b) size of each subnet.

Considering the energy dissipation at the transmitting and receiving antennas, and the components of the transmitter and receiver circuitry such as the MZM, TDM block, and the LNA, the energy dissipation of the longest possible wireless link on the chip is 0.33 pJ/bit. The energy dissipation of a wireless link, E_{Link} is given as

$$E_{Link} = \sum_{i=1}^m (E_{antenna,i} + E_{transceiver,i}), \quad (7)$$

where m is the number of frequency channels in the link and $E_{antenna,i}$ and $E_{transceiver,i}$ are the energy dissipations of the antenna element and transceiver circuits for the i th frequency in the link.

The network switches and hubs are synthesized from a RTL level design using 65 nm standard cell libraries from CMP [43], using Synopsys Design Vision and assuming a clock frequency of 2.5 GHz. A large set of data patterns were fed into the gate-level netlists of the network switches and hubs, and by running Synopsys Prime Power, their energy dissipation was obtained.

The energy dissipation of the wired links depends on their lengths. The lengths of the interswitch wires in the subnets can be found by using the formula

$$l_M = \frac{l_{edge}}{M-1}. \quad (8)$$

Here, M is number of cores along a particular edge of the subnet and l_{edge} is the length of that edge. A 20 mm × 20 mm die size is considered for all system sizes in our simulations. The interhub wire lengths are also computed similarly as these are assumed to be connected by wires parallel to the edges of the die in rectangular dimensions only. Hence, to compute interhub distances along the ring, parallel to a particular edge of the die, (8) is modified by changing M to the number of hubs along that edge and l_{edge} to the length of that particular edge. In each subnet, the lengths of the links connecting the switches to the hub depend on the position of the switches as shown in Fig. 1a. The capacitances of each wired link, and subsequently their energy dissipation, were obtained through HSPICE simulations taking into account the specific layout for the subnets and the second level of the ring network.

Figs. 10a and 10b show the packet energy dissipation for each of the network configurations considered in this work. The packet energy for the flat wired mesh architecture is not shown as it is higher than that of the WiNoCs by orders of magnitude, and hence cannot be shown on the same scale. The comparison with the wired case is shown in Table 3 in the next section along with another hierarchical wired architecture.

From the plots, it is clear that the packet energy dissipation increases with increasing system size. However, scaling up the number of subnets has a lower impact on the average packet energy. The reason for this is that the throughput does not degrade much and the average latency per packet also does not change significantly. Hence, the data packets occupy the network resources for less duration, causing only a small increase in packet energy. However, with an increase in subnet size, the throughput degrades noticeably, and so does latency. In this case, the packet energy increases significantly as each packet occupies network resources for a longer period of time. With an increase in the number of wireless links while keeping the number of subnets and subnet size constant, the packet energy decreases. This is because higher connectivity of the network results in higher throughput (or lower latency), which means that packets get routed faster, occupy network resources for less time, and consume less energy during the transmission. Since the wireline subnets pose the major bottleneck as is made evident by the trends in the

TABLE 3
Packet Energy Dissipation for Flat Wired Mesh, WiNoC, and Hierarchical G-Line NoC Architectures

System Size	Sub-net Size	No. of Sub-nets	Flat Mesh (nJ)	WiNoC (nJ)	NoC with G-Line (nJ)
128	16	8	1319	22.57	490.3
256	16	16	2936	24.02	734.5
512	16	32	4992	37.48	1012.8

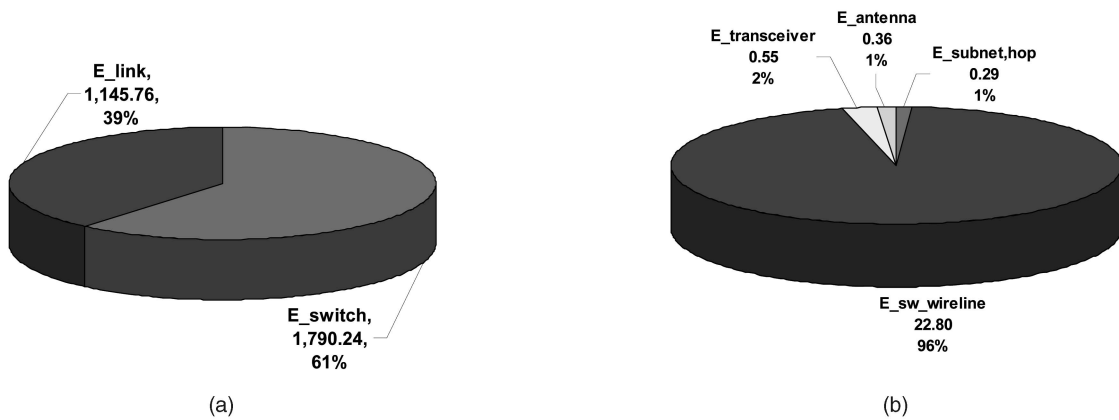


Fig. 11. Components of packet energy dissipation for a (a) flat mesh and (b) WiNoC. Values of energy dissipation are labeled in nJ units.

plots of Figs. 9 and 10 their size should be optimized. In other words, smaller subnets imply better performance and lower packet energies. Hence, as a designer one should target to limit the size of the subnets as long as the size of the upper level of the network does not impact the performance of the overall system negatively. The exact optimal solution also depends on the architecture of the upper level of the network, which need not be restricted to the ring topology chosen in this work as an example.

The adopted centralized routing strategy is compared with the distributed routing discussed in Section 3.4 for a WiNoC of size 256 cores split into 16 subnets with 16 cores in each. Twenty four wireless links were deployed in the exact same topology for both cases. With distributed routing, the throughput was 0.67 flits/core/cycle whereas with centralized routing it was 0.72 flits/core/cycle as already noted in Fig. 7, which is 7.5 percent higher. Centralized routing results in a better throughput as it finds the shortest path whereas the distributed routing uses nonoptimal paths in some cases. Hence, the distributed routing has lower throughput. The distributed routing dissipates a packet energy of 31.2 nJ compared to 30.8 nJ with centralized routing. This is because on an average the number of path length computation with the distributed routing is more per packet, as this computation occurs at every intermediate WB. However, with centralized routing each hub has additional hardware overhead to compute the shortest path by comparing all the paths using the wireless links. This hardware area cost is discussed in Section 4.7.

4.4 Comparison with Wired NoCs

We evaluated the performance of the WiNoCs in terms of energy dissipation compared to different wired NoC architectures. As demonstrated in the last section, with increase in system size, increasing the number of subnets while keeping the subnet size fixed is a better scaling strategy; hence, we followed that in the following analysis.

The first wired architecture considered was the conventional flat mesh architecture. Table 3 quantifies the energy dissipation per packet of the WiNoC and the wired architectures for various system sizes. The WiNoC configuration with 24 wireless links was chosen because it has the lowest packet energy dissipation among all the possible hybrid wired/wireless configurations. It is evident that the WiNoC consumes orders of magnitude less energy compared

to the flat wired mesh network. Fig. 11 shows the contributions of the various components of the packet energy dissipation for the WiNoC with 24 wireless links and the flat mesh architecture for a system size of 256 cores. The contributions of the antenna and the transceiver, which constitute the wireless link energy, are shown separately from the wireline links of the upper level small-world network. The largest contribution to packet energy in WiNoC is from the wireless and wireline link traversals combined in the upper level small-world network. This is because on an average a large portion of the packets travel through the upper level of the WiNoC to reach other subnets. However, as this level has very small average path length due to its small-world nature and due to the low-power wireless channels the absolute value of this energy dissipation is very small.

The performance of the flat mesh NoC architectures can be improved by incorporating express virtual channels (EVCs), which connect the distant cores in the network by bypassing intermediate switches/routers. It is demonstrated that the switch/router energy dissipation of the baseline mesh architecture is improved by about 25-38 percent depending on the system size by using dynamic EVCs. The energy dissipation profile is improved by another eight percent over the EVC scheme by using low-swing, multidrop, ultralow-latency global interconnect (G-Lines) for the flow-control signals [4]. Recently, a number of papers have shown the possibility of communicating near speed of light across several millimeters on a silicon substrate. Among them, low-swing, long-range, and ultralow-latency communication wires as proposed in [44] achieve higher bandwidth at lower power consumption [4]. G-lines use a capacitive preemphasis transmitter that increases the bandwidth and decreases the voltage swing without the need of an additional power supply. To avoid cross talk, differential interconnects are implemented with a pair of twisted wires. A decision feedback equalizer is employed at the receiver to further increase the achievable data rate. It is evident that though introduction of EVCs improves the energy dissipation profile of a flat wired mesh NoC, the achievable performance gain is still limited compared to the gains achieved by the WiNoCs. This is because the basic architecture is still a flat mesh and the savings in energy principally arises from bypassing the intermediate NoC switches.

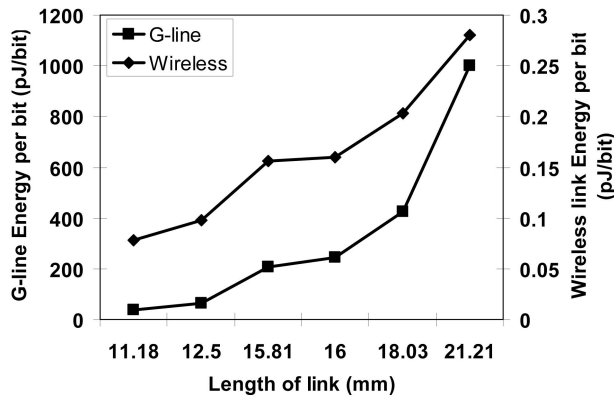


Fig. 12. Energy dissipation per bit on G-line and wireless links with varying link lengths.

As a next step, we undertook a study where we compared the energy dissipation profile of the proposed hybrid NoC architecture using wireless links to that of the same hierarchical network using G-Lines as long-range communication links. To do so, we replaced the wireless links of the WiNoCs by the G-Lines while maintaining the same hierarchical topology with shortcuts in the upper level. Here, each G-line link is designed such that it has the same bandwidth as the wireless link it replaces. Thus, the overall throughput and end-to-end latency of the hierarchical NoC with G-line links is the same as that of the WiNoC. We performed simulations in 65 nm technology. The lumped wire resistance is 20 ohms/mm, and the capacitance is 400 fF/mm. The simulated power dissipation is found to be 0.6 mW/transmitter and 0.4 mW/receiver. In order to achieve the same bandwidth as the wireless links in our experiments, multiple G-line links are used in place of a single wireless channel between a pair of source and destination hubs. For example, a single G-line can sustain a bandwidth of around 2.5 Gbps for a wire length of 11 mm, whereas each wireless channel can sustain a bandwidth of 10 Gbps. Therefore, to maintain the same data rate as provided by a single wireless channel, we need four G-lines between a source and destination pair separated by 11 mm. Moreover, since each G-line works on differential signals, we will need eight wires to replace a single wireless link in this case.

The packet energy dissipation for a WiNoC and hierarchical NoC with G-line links are also shown in Table 3 for various system sizes. The WiNoC's energy per packet consumption is one order of magnitude less compared to the hierarchical NoC with G-line links of the same bandwidth as the wireless channels. This experiment was conducted to highlight the savings in energy dissipation due to two factors, viz., the architectural innovation proposed here and the use of on-chip wireless links in place of highly optimized wired connections. The difference in energy dissipation between the flat wired mesh NoC and the hybrid NoC with G-Lines arises primarily due to the architecture proposed here. The difference in energy dissipation between the WiNoCs and the hybrid NoC with G-lines is solely due to the use of wireless channels. Fig. 12 shows the energy dissipation of a wireless link considered in this paper and that of the G-line link as a function of communication distance between source and destination WBs considered here. This shows how high

TABLE 4
Percentage of Packet Energy Dissipation on Long-Range Links

No. of links	1	6	24
Wireless	0.5	2.8	3.4
G-Line	47.3	95.8	98.5

the energy dissipation of a G-line link of the same bandwidth as the wireless link is. The impact of this is reflected in the packet energy dissipation profiles shown in Table 3, which is obtained after full system simulation using these links. Table 4 shows the percentage of total packet energy dissipated on the wired and wireless links for a WiNoC with 128 cores divided into 16 subnets. The percentage of packet energy dissipated on the G-line links replacing the wireless links are also shown to signify the trade-off in energy dissipation as more wireline (G-Line) links are replaced with the wireless links for a single-network configuration. As shown in Tables 3 and 4, the hierarchical NoC with G-line links dissipate higher packet energy than the WiNoC and the long-distance G-line links dissipate a considerably larger proportion of that high packet energy.

Another wireline architecture developed in [2] uses long-range wired shortcuts to design a small-world network over a basic mesh topology. We considered a system size of 128 cores and eight wireline shortcuts were optimally deployed on a basic wireline mesh following the scaling trend outlined in [2]. The chosen WiNoC configuration was 16 subnets with eight cores in each with eight wireless links. The throughput of the wireline small-world NoC proposed in [2] was 0.26 flits/core/cycle, which is 18.7 percent more than that of a flat mesh NoC. In comparison, the WiNoC had a throughput of 0.75 flits/core/cycle. This huge gain was due to the hierarchical division of the whole NoC as well as the high-bandwidth wireless links used in creating the shortcuts. The packet energy dissipation for the NoC proposed in [2] for the configuration mentioned above is 984 nJ. This energy dissipation is about 25 percent less than the packet energy dissipation in a flat mesh. However, even this packet energy is an order of magnitude higher than that of the WiNoC for the same size of 128 cores as shown in Table 3.

From the above analysis, it is clear that the proposed WiNoC architectures outperform their corresponding wired counterparts significantly in terms of all the relevant network parameters. Moreover, the WiNoC is much more energy-efficient compared to an exactly equivalent hierarchical wired architecture implemented with the recently proposed high-bandwidth low-latency G-lines as the long-range communication links.

4.5 Comparative Analysis with Other Emerging NoC Paradigms

There are several emerging paradigms which enhance the performance of NoCs using nontraditional technology such as three-dimensional integration, photonic interconnects, RF interconnect (RF-I), and on-chip wireless communication using UWB links. In this section, we perform a comparative analysis to establish the relative performance benefits achieved by using these alternative techniques with specific system parameters. We consider a system with 128 cores and

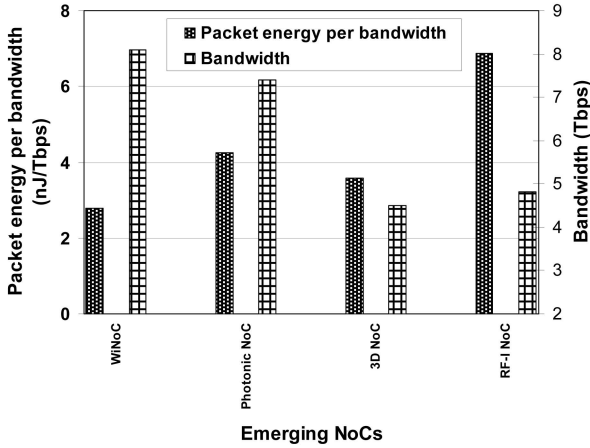


Fig. 13. Packet energy dissipation per bandwidth and achievable NoC bandwidth for various types of emerging NoC paradigms for system size of 128 cores.

packet size of 64 flits. We map this to a 3D mesh-based NoC with four layers as in [14]. The photonic NoC architecture was adopted from [7]. For the RF-I NoC, we followed the architecture of [8] with eight sectors. For the UWB NoC, we followed the design shown in [24]. Fig. 13 shows the achievable overall network bandwidth and the packet energy dissipation per unit bandwidth for all the different NoCs using alternative interconnect technologies. We considered the packet energy dissipation per unit bandwidth as the various NoCs are capable of achieving different network throughputs. The WiNoC considered in this comparison had 16 subnets. Due to the multihop nature of communication, relatively higher transceiver energy, and lower achievable bandwidth, the UWB NoC dissipates 432.9 nJ/Tbps, which is orders of magnitude more compared to all the other alternative solutions. That's why UWB NoC energy is not shown in the same plot. The achievable bandwidth of this architecture is 1.04 Tbps which is also lower than that of the other emerging alternatives considered here.

It can be observed that among all the emerging NoC architectures, the hybrid WiNoC, proposed in this paper, has the lowest packet energy dissipation per unit bandwidth and it also has the highest peak bandwidth. This is because in the WiNoC, each of the 24 wireless channels can sustain a data rate of 10 Gbps. WiNoC reduces the average hop count compared to both the 3D and RF-I NoCs. The photonic NoC considered in the comparative evaluation requires an electrical control network to configure photonic switching elements which uses a flat wireline mesh NoC. This causes overheads and hence limits its performance. However, this overhead can be reduced for longer packets. The lower bandwidth of the RF-I NoC compared to the WiNoC is due to the fact that it is essentially a flat wireline architecture as it uses a waveguide overlayed on an existing wireline mesh. The drop points to the RF-I become hotspots limiting the performance of the RF-I NoC. However, an alternative photonic NoC architecture, Corona, demonstrated in [45] employs an optical network amalgated onto a 3D chip. This particular architecture achieves a higher bandwidth than the WiNoC as it takes advantage of both photonic links and 3D integration simultaneously. For a

uniform traffic distribution, Corona with 256 cores is shown to achieve a bandwidth of 4.5 TBps. In comparison, a 256-core WiNoC segmented into 16 subnets with 24 wireless links can achieve a peak bandwidth of 1.8 TBps for the same traffic pattern. A more detailed performance benchmarking across all emerging NoC paradigms for various system parameters is the subject of a future investigation.

4.6 Traffic-Dependent Wireless Link Insertion

So far, we assumed a uniformly random spatial distribution of traffic between the hubs. We also principally considered the distance between the hubs to be the deciding factor for choosing the positions of the wireless links. However, in reality, there could be nonuniform traffic distributions with a particular pair of hubs communicating more frequently between themselves than with the others. In order to optimize our network for such nonuniform traffic scenarios, we modify (1) and also the optimization metric, which was based only on distances between cores earlier. Equation (1) is modified as shown below in (9).

$$P_{ij} = \frac{h_{ij}f_{ij}}{\sum_{i,j} h_{ij}f_{ij}}. \quad (9)$$

In (9), f_{ij} is the frequency of communication between the i th source and j th destination. This frequency is expressed as the percentage of traffic generated from i that is addressed to j . This frequency distribution is based on the particular application mapped to the overall NoC and is hence set prior to wireless link insertion. Therefore, the a priori knowledge of the traffic pattern is used to optimize the WiNoC. This optimization approach establishes a correlation between traffic distribution across the NoC and network configuration as in [46]. The optimization metric, which was just the sum of distances between all possible source and destination pairs of hubs in the previous experiments, needs to be modified to factor in the effect of nonuniform traffic:

$$\mu = \sum_{i,j} h_{ij}f_{ij}, \quad (10)$$

where, μ is the optimization metric. In this particular case, equal weight is attached to distance as well as frequency of communication in the metric. Using this modified metric, the simulated annealing algorithm is used to insert the wireless links for optimized performance. To represent nonuniform traffic patterns, we considered both synthetic and application-specific traffic patterns.

We considered two types of synthetic traffic to evaluate the performance of the proposed WiNoC architecture. First, a *transpose* traffic pattern [2] was considered where a certain number of hubs were considered to communicate more frequently with each other. We considered 1, 3, and 5 such pairs and called them *transpose1*, *transpose3*, and *transpose5*, respectively. The system size considered was 128 with 16 subnets and four wireless links. Fifty percent of packets generated from one of these hubs were targeted toward the other in the pair. The other synthetic traffic pattern considered was the *hotspot* [2], where each hub communicates with a certain number of hubs more frequently than with the others. We have considered three such hotspot locations to

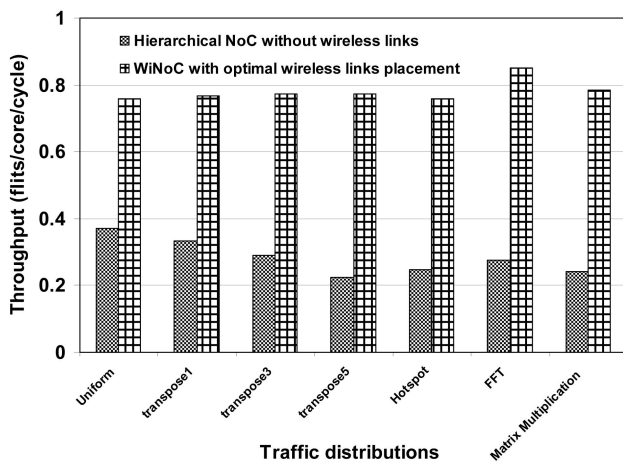


Fig. 14. Throughput of 128-core WiNoC with various traffic patterns.

which all other hubs send 50 percent of the packets that originate from them. To represent application-based traffic patterns, two scientific applications were mapped onto the 128-core NoC considered here. First, a 256-point fast Fourier transform (FFT) application was considered, wherein each core performs a two-point radix-2 FFT computation. Second, the traffic pattern generated in performing multiplication of two 128×128 matrices was considered.

For all the above nonuniform traffic distributions, the SA algorithm achieves the optimal configuration faster than the exhaustive search, though it takes more iterations than the case with uniform traffic distribution.

Fig. 14 shows the maximum throughput at network saturation for nonuniform traffic distributions with and without wireless links. For the transpose traffic, the pairs of nodes are chosen along the diagonals of the ring topology of the upper level of the network to incorporate the worst-case effect on the throughput due to nonuniform traffic. Without any long-range wireless links, the throughput of the network decreases with increase in the number of transpose pairs. As these pairs are placed along the diagonals of the ring the amount of multihop communication increases and that affects the throughput. But by inserting the wireless links between these highly communicating hubs, the throughput increases significantly. It is evident from Fig. 14 that with increase in the number of highly communicating pairs, insertion of the wireless links brings significantly more performance gain. When the traffic is uniform, insertion of the wireless links improves the performance by around 104 percent. In the case of nonuniform traffic distribution with 5 transpose pairs, the performance improvement is 243 percent. The optimization of the network configuration for hotspot traffic also yields similar results where the gain in throughput becomes 209 percent. For the FFT and the matrix multiplication applications, the percentage improvements in throughput are 209 and 226 percent, respectively. In case of the application-specific nonuniform traffic patterns, the wireless links are inserted depending on the mutual interactions among various cores of the system giving a preference to more frequently communicating subnets. For each application-specific traffic pattern, the wireless link insertion process finds a corresponding

TABLE 5
Total Area Overhead of Wireless Ports

Number of Wire-less links	Total area of wireless ports (μm^2)
1	151
6	5343
24	85443

optimum network configuration. Due to this inherent correlation between the optimization of the network configuration and the traffic pattern, the gains in throughput with nonuniform traffic are larger than that with uniform traffic.

4.7 Area Overheads

In this section, we present a detailed analysis of the area overhead involved in overall wireless deployment in the hierarchical WiNoC. A key advantage of CNT antennas is that they are nanoscale structures with diameters of only a few hundreds of nanometers. The length of the nanotubes required for the WiNoCs vary in the range of a few microns. Hence, the areas of the antenna elements themselves are very small. The area of the transceiver circuits required per wireless port is the total area required for the TDM modulator/demodulator, the MZM modulator/demodulator, and the LNAs. The area overhead for a link varies depending upon the number of channels per link as the TDM modulator/demodulator complexity changes with number of channels per link. Table 5 summarizes the area overheads required for different number of wireless links. The area complexity increases with increase in the number of wireless links deployed in the WiNoC but is significantly less than the silicon area of the hubs.

The arbitration, data routing and storage components of the hubs have area cost depending upon the number of ports per hub. The number of wireline ports, in turn, varies with the number of cores in the subnets. The number of wireline ports is equal to two more than the number of cores in each subnet due to two neighboring hubs that each hub is connected with, in addition to the cores in the subnet. This area cost is independent of the deployment of the wireless links as the wireless links are just extra ports deployed to the hubs whose area is already quantified. Fig. 15 shows the total area cost of WiNoCs of various system sizes with different numbers of subnets. Since flat mesh switches still exist in the WiNoCs, the total area is the sum of the areas of the flat mesh switches and the hubs. The additional silicon area overhead due to the hubs is at the most 25 percent for the system configurations considered in this work. This area cost analysis is done for hubs which implement the centralized routing strategy adopted throughout the paper. However, due to the higher complexity of the routers in this strategy compared to that in the distributed routing strategy, the area of each hub is up to 10 percent higher with the centralized routing than with distributed routing.

The core-hub and the interhub wireline links are additional wiring overheads, which depend on the number and size of subnets. Fig. 16 shows the total wiring requirements of various lengths for a $20 \text{ mm} \times 20 \text{ mm}$ die for the various system configurations considered in this

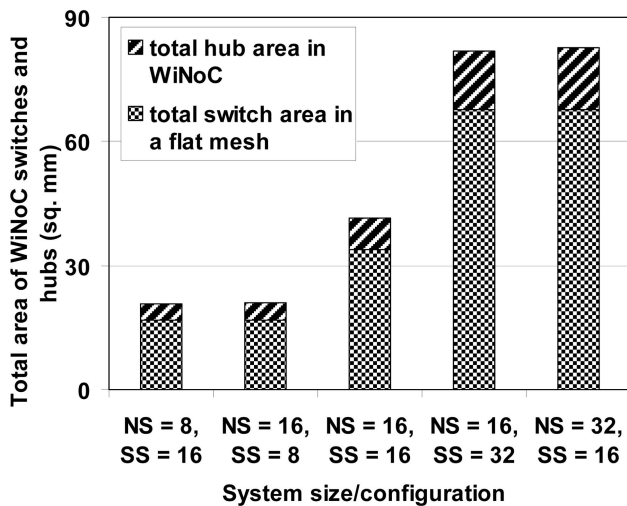


Fig. 15. Total silicon area in WiNoC hubs and switches. **NS = number of subnets, SS = subnet size.

work. The wiring requirements for a flat mesh architecture are shown for comparison. There are only a very few 10 mm long links in the 128-core WiNoC and hence is not apparent in the figure. It may be noted that in the WiNoC, there are no intersubnet direct core to core links as intersubnet communication occurs through the hubs. Hence, WiNoCs eliminate a number of wireline links along the subnet boundaries which are present in the flat mesh topology.

5 CONCLUSIONS AND FUTURE WORK

In this work, we propose and evaluate the performance of the WiNoC architectures used as communication backbones for multicore systems. By establishing long-range wireless links between distant cores and incorporating small-world network architectures, the WiNoCs are capable of outperforming their more traditional wired counterparts in terms of network throughput, latency, and energy dissipation. With increase in system size, increasing the number of subnets provides an efficient scaling technique without significantly degrading system performance. The architectural innovations proposed in this work are made possible by the use of low-power and high-speed wireless links capable of communicating directly between distant parts of the chip in a single hop. The gains in network performance metrics are in part due to the architecture and the rest is due to the adopted high-bandwidth, energy-efficient wireless links. Optimum placement of the wireless links based on nonuniform traffic distribution improves the performance of the WiNoC significantly more compared to a uniform traffic scenario.

As a part of this work, we evaluated performance of the WiNoC with respect to other emerging NoC architectures for a specific system configuration. In ongoing and future investigations, we intend to establish a detailed benchmarking methodology to compare and contrast the performance of WiNoCs with the other alternatives by varying system size, packet length, traffic patterns, and other relevant parameters. More efficient and scalable techniques will also be developed for optimizing the WiNoC architectures, specifically in presence of complex transient workloads. It

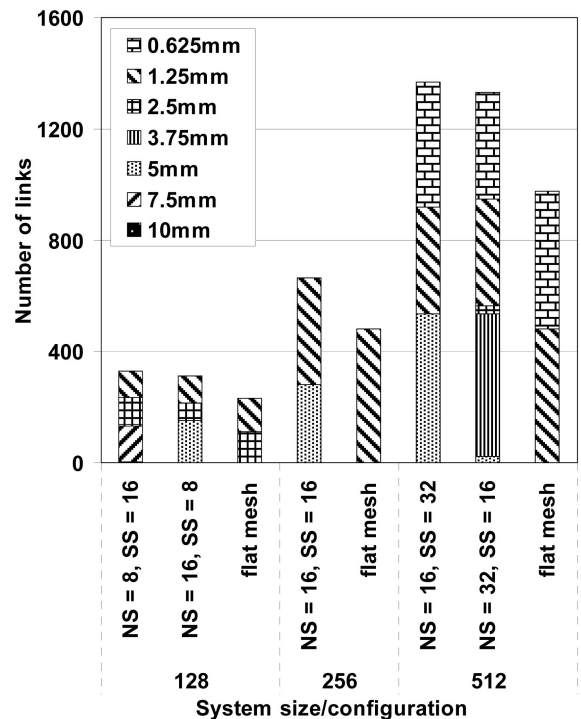


Fig. 16. Wiring requirement of WiNoC. **NS = number of subnets, SS = subnet size of WiNoC.

is well known that manufacturing processes of CNTs are defect-prone and hence in order to make WiNoCs with CNT antennas a reality appropriate fault-tolerant mechanism need to be incorporated to fully leverage the high-bandwidth and low-power wireless links. In the future, a hybrid NoC with wired as well as wireless links can deliver the target performance of multicore chips by utilizing the benefits of both.

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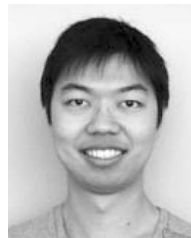
REFERENCES

- [1] L. Benini and G.D. Micheli, "Networks on Chips: A New SoC Paradigm," *Computer*, vol. 35, no. 1, pp. 70-78, Jan. 2002.
- [2] U.Y. Ogras and R. Marculescu, "It's a Small World After All: NoC Performance Optimization via Long-Range Link Insertion," *IEEE Trans. Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 7, pp. 693-706, July 2006.
- [3] A. Kumar et al., "Toward Ideal On-Chip Communication Using Express Virtual Channels," *IEEE Micro*, vol. 28, no. 1, pp. 80-90, Jan.-Feb. 2008.
- [4] T. Krishna et al., "NoC with Near-Ideal Express Virtual Channels Using Global-Line Communication," *Proc. IEEE Symp. High Performance Interconnects (HOTI)*, pp. 11-20, Aug. 2008.
- [5] ITRS, <http://www.itrs.net/Links/2007ITRS/Home2007.htm>, 2007.
- [6] V.F. Pavlidis and E.G. Friedman, "3D Topologies for Networks-on-Chip," *IEEE Trans. Very Large Scale Integration (VLSI) Systems*, vol. 15, no. 10, pp. 1081-1090, Oct. 2007.

- [7] A. Shacham et al., "Photonic Network-on-Chip for Future Generations of Chip Multi-Processors," *IEEE Trans. Computers*, vol. 57, no. 9, pp. 1246-1260, 2008.
- [8] M.F. Chang et al., "CMP Network-on-Chip Overlaid with Multi-Band RF-Interconnect," *Proc. IEEE Int'l Symp. High-Performance Computer Architecture (HPCA)*, pp. 191-202, Feb. 2008.
- [9] J. Lin et al., "Communication Using Antennas Fabricated in Silicon Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1678-1687, Aug. 2007.
- [10] P.J. Burke et al., "Quantitative Theory of Nanowire and Nanotube Antenna Performance," *IEEE Trans. Nanotechnology*, vol. 5, no. 4, pp. 314-334, July 2006.
- [11] K. Kempa et al., "Carbon Nanotubes as Optical Antennae," *Advanced Materials*, vol. 19, pp. 421-426, 2007.
- [12] K.K. O et al., "The Feasibility of On-Chip Interconnection Using Antennas," *Proc. IEEE/ACM Int'l Conf. Computer-Aided Design (ICCAD '05)*, pp. 979-984, 2005.
- [13] D.J. Watts, *Small Worlds: The Dynamics of Networks between Order and Randomness*, Princeton Univ. Press, 1999.
- [14] B. Feero and P.P. Pande, "Networks-on-Chip in a Three-Dimensional Environment: A Performance Evaluation," *IEEE Trans. Computers*, vol. 58, no. 1, pp. 32-45, Jan. 2009.
- [15] D. Park et al., "MIRA: A Multi-Layered On-Chip Interconnect Router Architecture," *IEEE Int'l Symp. Computer Architecture (ISCA)*, pp. 251-261, June 2008.
- [16] W.R. Davis et al., "Demystifying 3D ICs: The Pros and Cons of Going Vertical," *IEEE Design and Test of Computers*, vol. 22, no. 6, pp. 498-510, Nov.-Dec. 2005.
- [17] A.W. Topol et al., "Three-Dimensional Integrated Circuits," *IBM J. Research & Development*, vol. 50, nos. 4/5, pp. 491-506, July/Sept. 2006.
- [18] A.P. Jose et al., "Pulsed Current-Mode Signaling for Nearly Speed-of-Light Intrachip Communication," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 772-780, Apr. 2006.
- [19] R.T. Chang et al., "Near Speed-of-Light Signaling over On-Chip Electrical Interconnects," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 834-838, May 2003.
- [20] I. O'Connor et al., "Systematic Simulation-Based Predictive Synthesis of Integrated Optical Interconnect," *IEEE Trans. Very Large Scale Integration (VLSI) Systems*, vol. 15, no. 8, pp. 927-940, Aug. 2007.
- [21] M. Briere et al., "System Level Assessment of an Optical NoC in an MPSoC Platform," *Proc. IEEE Design, Automation and Test in Europe Conf. and Exhibition*, pp. 1084-1089, Apr. 2007.
- [22] M.F. Chang et al., "RF Interconnects for Communications On-Chip," *Proc. Int'l Symp. Physical Design*, pp. 78-83, Apr. 2008.
- [23] B.A. Floyd et al., "Intra-Chip Wireless Interconnect for Clock Distribution Implemented with Integrated Antennas, Receivers, and Transmitters," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 543-552, May 2002.
- [24] D. Zhao and Y. Wang, "SD-MAC: Design and Synthesis of a Hardware-Efficient Collision-Free QoS-Aware MAC Protocol for Wireless Network-on-Chip," *IEEE Trans. Computers*, vol. 57, no. 9, pp. 1230-1245, Sept. 2008.
- [25] R. Albert and A.-L. Barabasi, "Statistical Mechanics of Complex Networks," *Rev. of Modern Physics*, vol. 74, pp. 47-97, Jan. 2002.
- [26] M. Buchanan, *Nexus: Small Worlds and the Groundbreaking Theory of Networks*, Norton, W. W. & Company, 2003.
- [27] C. Teuscher, "Nature-Inspired Interconnects for Self-Assembled Large-Scale Network-on-Chip Designs," *Chaos*, vol. 17, no. 2, 2007.
- [28] D.J. Watts and S.H. Strogatz, "Collective Dynamics of 'Small-World' Networks," *Nature*, vol. 393, pp. 440-442, 1998.
- [29] T. Petermann and P. De Los Rios, "Physical Realizability of Small-World Networks," *Physical Rev. E*, vol. 73, 2006.
- [30] S. Kirkpatrick et al., "Optimization by Simulated Annealing," *Science*, vol. 220, pp. 671-680, 1983.
- [31] J. Duato et al., *Interconnection Networks—An Engineering Approach*, Morgan Kaufmann Publishers, 2002.
- [32] M. Fukuda et al., "A 0.18 μm CMOS Impulse Radio Based UWB Transmitter for Global Wireless Interconnections of 3D Stacked-Chip System," *Proc. Int'l Conf. Solid State Devices and Materials*, pp. 72-73, Sept. 2006.
- [33] G.W. Hanson, "On the Applicability of the Surface Impedance Integral Equation for Optical and Near Infrared Copper Dipole Antennas," *IEEE Trans. Antennas and Propagation*, vol. 54, no. 12, pp. 3677-3685, Dec. 2006.
- [34] Y. Huang et al., "Performance Prediction of Carbon Nanotube Bundle Dipole Antennas," *IEEE Trans. Nanotechnology*, vol. 7, no. 3, pp. 331-337, May 2008.
- [35] Y. Zhou et al., "Design and Fabrication of Microheaters for Localized Carbon Nanotube Growth," *Proc. IEEE Conf. Nanotechnology*, pp. 452-455, 2008.
- [36] M. Freitag et al., "Hot Carrier Electroluminescence from a Single Carbon Nanotube," *Nano Letters*, vol. 4, no. 6, pp. 1063-1066, 2004.
- [37] T.S. Marinis et al., "Wafer Level Vacuum Packaging of MEMS Sensors," *Proc. Electronic Components and Technology Conf.*, vol. 2, pp. 1081-1088, May-June 2005.
- [38] B.G. Lee et al., "Ultrahigh-Bandwidth Silicon Photonic Nanowire Waveguides for On-Chip Networks," *IEEE Photonics Technology Letters*, vol. 20, no. 6, pp. 398-400, Mar. 2008.
- [39] W.M.J. Green et al., "Ultra-Compact, Low RF Power, 10Gb/s Silicon Mach-Zehnder Modulator," *Optics Express*, vol. 15, no. 25, pp. 17106-17113, 2007.
- [40] Z. Lu et al., "Connection-Oriented Multicasting in Wormhole-Switched Networks on Chip," *Proc. IEEE CS Ann. Symp. VLSI: Emerging VLSI Technologies and Architectures*, pp. 205-210, 2006.
- [41] P.P. Pande et al., "Performance Evaluation and Design Trade-Offs for Network-on-Chip Interconnect Architectures," *IEEE Trans. Computers*, vol. 54, no. 8, pp. 1025-1040, Aug. 2005.
- [42] A. Ismail and A. Abidi, "A 3 to 10 GHz LNA Using a Wideband LC-Ladder Matching Network," *Proc. IEEE Int'l Solid-State Circuits Conf.*, pp. 384-534, Feb. 2004.
- [43] Circuits Multi-Projects, <http://cmp.imag.fr>, 2010.
- [44] E. Mensink et al., "A 0.28pf/b 2gb/s/ch Transceiver in 90 nm CMOS for 10 mm On-Chip Interconnects," *Proc. IEEE Solid-State Circuits Conf.*, pp. 412-413, Feb. 2007.
- [45] D. Vantrease et al., "Corona: System Implications of Emerging Nanophotonic Technology," *Proc. IEEE Int'l Symp. Computer Architecture (ISCA)*, pp. 153-164, June 2008.
- [46] P. Bogdan and R. Marculescu, "Quantum-Like Effects in Network-on-Chip Buffers Behavior," *Proc. IEEE Design Automation Conf. (DAC)*, pp. 266-267, June 2007.



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