

# **Data Distribution Equivalence for Data Intensive Interconnection Networks**

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Abstract of the Dissertation

# **Data Distribution Equivalence for Data Intensive Interconnection Networks**

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This thesis considers two problems. One problem is closed-form solutions for equivalence computation of divisible workload in mesh and toroidal networks and the other problem is scheduling divisible workloads from multiple sources in mesh and toroidal networks of processors.

We propose a flow matrix closed-form equation to present the equivalence, which allows a characterization of the nature of minimal time solution and a simple method to determine when and how much load to distribute for processors. Also, we propose the use of a reduced Manhattan distance Voronoi diagram algorithm (RMDVDA) to minimize the overall processing time of these workloads by taking advantage of the processor equivalence technique. Three case studies with 10 sources of workloads are presented to illustrate the

general approach for multiple sources of workloads. In the first phase, a Manhattan distance Voronoi diagram is used to obtain a network cluster division. In the second phase, we propose an efficient algorithm to obtain near-optimal load distribution among processors represented by equivalent processors. The algorithm minimizes the number of processors utilized. Experimental evaluation through simulations demonstrates that a task can be finished in the same suboptimal time and yet save over 30% of processor resources.

*Key Words : Divisible Load Theory, Voronoi Diagram, Multi-source, Network On Chip (NOC)*

*To my Parents and all loving ones*

# Table of Contents

<b>List of Figures</b> . . . . .	<b>xiii</b>
<b>List of Tables</b> . . . . .	<b>xiv</b>
<b>Acknowledgements</b> . . . . .	<b>xv</b>
<b>1 Introduction</b> . . . . .	<b>1</b>
<b>2 Problem Description</b> . . . . .	<b>4</b>
2.1 Problem Background . . . . .	4
2.2 Definitions and Assumption . . . . .	6
2.2.1 Notions . . . . .	7
<b>3 Mesh Network</b> . . . . .	<b>9</b>
3.1 Virtual Cut-through Switching Scenario . . . . .	9
3.1.1 Data Injection on The Corner Processor . . . . .	9
3.1.2 Data Injection On The Boundary Processor . . . . .	27
3.1.3 Data Injection On The Inner Grid Processor . . . . .	32
3.1.4 Sensitivity Analysis Virtual Cut-through Switching Scenario . . . . .	38
3.1.5 Multi-source Uniform Data Fraction . . . . .	44
3.1.6 Improve the Bottleneck Voronoi Division Equivalence Computation . . . . .	65

3.1.7	Multi-source Non-uniform Data Injection . . . . .	69
3.2	Store and Forward Switching Scenario . . . . .	72
3.2.1	Data Injection on The Corner Processor . . . . .	72
3.2.2	Data Injection on The Boundary Processor . . . . .	84
3.2.3	Data Injection on The Inner Grid Processor . . . . .	87
3.2.4	Sensitivity Analysis Store and Forward Scenario . . . . .	89
3.2.5	Multi-source Uniform Data Fraction . . . . .	95
3.2.6	Multi-source Non-uniform Data Injection . . . . .	104
<b>4</b>	<b>Toroidal Rectangle Network . . . . .</b>	<b>105</b>
4.1	Toroidal Rectangle Network Notions . . . . .	105
4.2	Virtual Cut-through Switching Scenario . . . . .	107
4.2.1	Data Injection On The Grid Processor . . . . .	107
4.2.2	Sensitivity Analysis of Toroidal Rectangle Network . .	110
4.2.3	Multi-source Uniform Data Fraction . . . . .	113
4.2.4	Multi-source Non-uniform Data Injection . . . . .	131
4.3	Store and Forward Switching Scenario . . . . .	132
4.3.1	Data Injection On The Grid Processor . . . . .	132
4.3.2	Sensitivity Analysis of Toroidal Rectangle Network . .	134
4.3.3	Multi-source Uniform Data Injection . . . . .	136
4.3.4	Multi-source Non-uniform Data Injection . . . . .	136
4.4	Comparison Result . . . . .	136
4.4.1	Comparison Result Between Mesh Network and Toroidal With Same Number of Processors . . . . .	136
4.4.2	Comparison Result With Corner Processor and Inner Grid Processor . . . . .	137
4.4.3	Comparison Result Between Virtual Cut-through Switch- ing Scenario and Store and Forward Scenario . . . . .	139

<b>5</b>	<b>Hypercube Network and General Network . . . . .</b>	<b>146</b>
5.1	Hypercube Network Virtual Cut-through Switching Scenario . .	146
5.1.1	Data Injection On The Grid Processor . . . . .	147
5.2	General Case Virtual Cut-through Switching Scenario . . . .	149
5.3	Hypercube Network Store and Forward Switching Scenario . .	150
5.4	General Case Store and Forward Switching Scenario . . . .	151
<b>6</b>	<b>Conclusion and Future work . . . . .</b>	<b>153</b>
6.1	Conclusion . . . . .	153
6.2	Future Work . . . . .	154
	<b>Bibliography . . . . .</b>	<b>155</b>

## List of Figures

2.1	A m*n mesh network(m = 5, n = 5) . . . . .	5
2.2	A toroidal rectangle network with grid unit cores . . . . .	5
3.1	The 2*2 mesh network and the root processor is $P_0$ . . . . .	10
3.2	The timing diagram for 2*2 mesh network and the root processor is $P_0$ . . . . .	11
3.3	2*2 mesh network. $\alpha_0, \alpha_1, \alpha_2, \alpha_3$ value curve . . . . .	13
3.4	The 2*3 mesh network and the data injection happens on corner processor $P_0$ . . . . .	15
3.5	The timing diagram for a 2*3 mesh network and the data injection happens on processor $P_0$ . . . . .	16
3.6	2*3 mesh network. $\alpha_0, \alpha_1, \alpha_3, \alpha_5$ value curve. . . . .	19
3.7	2*n (n = 10) mesh network and the workload happens on $P_0$ . .	20
3.8	The timing diagram for 2*10 mesh network and the data injection happens on $P_0$ . . . . .	21
3.9	3*8 mesh network. The data injection position is $P_0$ . . . . .	26
3.10	The 3*3 mesh network and the root processor is $P_0$ . . . . .	28
3.11	The timing diagram for 3*3 mesh network and the data injection occurs on $P_0$ . . . . .	29
3.12	The data fraction simulation result of 3*3 mesh network and the data injection happens on the boundary $P_0$ . . . . .	32

3.13	$3 \times 3$ mesh network. The data injection position is inner grid point $P_0$	33
3.14	The timing diagram for $3 \times 3$ mesh network and the data injection is inner grid $P_0$	34
3.15	$3 \times 3$ mesh network. The data injection position is inner grid point $P_0$	36
3.16	Sensitivity analysis result of $2 \times n$ mesh network (where $n = 1 \dots 10$ )	38
3.17	Speedup curves of $2 \times n$ mesh network (where $n = 1 \dots 10$ )	39
3.18	Sensitivity analysis result of $3 \times n$ mesh network and the injection position on boundary processor $P_2$ (where $n = 1 \dots 8$ )	40
3.19	Speedup curve of $3 \times n$ mesh network (where $n = 1 \dots 8$ )	41
3.20	Sensitivity analysis result of $5 \times n$ mesh network and the injection position on inner processor $P_{12}$ (where $n = 1 \dots 5$ )	42
3.21	Speedup curves of $5 \times n$ mesh network Fig. 2.1 (where $n = 1 \dots 5$ )	43
3.22	Data injection consists of a connected subgraph of $G$	45
3.23	Data injection consists of a connected subgraph of $G$	45
3.24	Connected subgraph Fig. 3.22 speedup vs $\sigma$	47
3.25	Connected subgraph Fig. 3.22's processor data fraction vs $\sigma$	48
3.26	Connected subgraph Fig. 3.23 speedup vs $\sigma$	49
3.27	Connected subgraph Fig. 3.23's processor data fraction vs $\sigma$	50
3.28	10 Manhattan distance Voronoi Cells	53
3.29	10 Manhattan distance Voronoi Cells speedup curves	54
3.30	10 reduced Voronoi cells	56
3.31	10 reduced Voronoi cells's speedup curves	57
3.32	Reduced Voronoi division algorithm average saved processors' percentage	58
3.33	Connected subgraphs and individual data injections on mesh network	61

3.34	Speedup curves for Situation III . . . . .	62
3.35	Reduced constrained Voronoi diagram for connected subgraphs and individual data injections on mesh network . . . . .	63
3.36	Speedup curves of connected subgraphs and individual data in- jection on mesh network . . . . .	64
3.37	The timing diagram for $2*2$ mesh network store and forward sce- nario . . . . .	72
3.38	Data fraction curves of mesh network $2 * 2$ vs $\sigma$ . . . . .	74
3.39	The timing diagram for store and forward switching $2*3$ mesh network. . . . .	75
3.40	Data fraction curves of mesh network $2 * 3$ vs $\sigma$ . . . . .	77
3.41	The timing diagram for $3*3$ boundary data injection on $P_0$ . . .	84
3.42	The fraction curve for $3*3$ boundary data injection on $P_0$ . . .	86
3.43	The timing diagram for $3*3$ inner grid injection $P_0$ . . . . .	88
3.44	Sensitivity analysis result of $2*n$ mesh network result ( $n = 1 \dots 10$ )	89
3.45	Speedup curve of $2*n$ mesh network result ( $n = 1 \dots 10$ ) . . .	90
3.46	Sensitivity analysis result of $3*n$ mesh network result ( $n = 1 \dots 8$ )	91
3.47	Speedup curve of $3*n$ mesh network result ( $n = 1 \dots 8$ ) . . .	92
3.48	Sensitivity analysis result of data injection position on inner grid processor of $5 * 5$ mesh network . . . . .	93
3.49	Speedup curve of $5 * n$ mesh network result ( $n = 1 \dots 5$ ) . . .	94
3.50	Connected subgraph Fig. 3.22 speedup vs $\sigma$ . . . . .	95
3.51	Connected subgraph Fig. 3.22's data injection processor workload fraction vs $\sigma$ . . . . .	96
3.52	Connected subgraph Fig. 3.23 speedup vs $\sigma$ . . . . .	97
3.53	Connected subgraph Fig. 3.23's data injection processor workload fraction vs $\sigma$ . . . . .	98
3.54	10 Manhattan distance Voronoi Cells . . . . .	99

3.55	10 Manhattan distance Voronoi cells store and forward switching speedup curves . . . . .	100
3.56	10 reduced Manhattan distance store and forward switching Voronoi cells . . . . .	101
3.57	10 reduced Voronoi cells' store and forward switching speedup curves . . . . .	102
4.1	The rectangular toroidal network . . . . .	106
4.2	The rectangular toroidal network . . . . .	106
4.3	The $m^*n$ toroidal rectangle network and the data injection is $P_{4,2}$	107
4.4	Data fraction curve of toroidal rectangle network Fig. 4.3 . . .	109
4.5	Sensitivity analysis of $5^*n$ torus network (where $n = 1 \dots 5$ ) . .	111
4.6	Data fraction curves of a $5^*n$ torus network (where $n = 1 \dots 5$ ) vs $\sigma$ . . . . .	112
4.7	Toroidal mesh network subgraph data injection . . . . .	114
4.8	Data fraction curves of connected subgraph Fig. 4.7 . . . . .	115
4.9	Toroidal mesh network subgraph data injection . . . . .	116
4.10	Data fraction on different type processors for Fig. 4.9 . . . . .	117
4.11	How to calculate torus Voronoi Diagram . . . . .	118
4.12	Initial Manhattan distance Voronoi Diagram . . . . .	119
4.13	Torus Manhattan distance Voronoi diagram . . . . .	120
4.14	Voronoi diagram casting to the torus . . . . .	121
4.15	Toroidal Voronoi cells' speedup curves . . . . .	122
4.16	Torus reduced Voronoi diagram . . . . .	123
4.17	Torus reduced Voronoi diagram casting to a toroidal rectangle network . . . . .	124
4.18	Torus reduced Voronoi diagram speedup curves . . . . .	125
4.19	Torus reduced Voronoi diagram average saved processors . . . .	126
4.20	Subgraph and individual data injection division on torus network	127

4.21	Subgraph and individual data injection constrained Voronoi dia- gram division on torus network . . . . .	128
4.22	Subgraph and individual data injection speedup curves on torus network . . . . .	129
4.23	Subgraph and individual data injection constrained Voronoi dia- gram division speedup curves on torus network . . . . .	130
4.24	The data fraction curve of $6 * 6$ torus network Fig. 4.3 . . . . .	133
4.25	Sensitivity analysis result of $5 * n$ torus network ( $n = 1 \dots 5$ ) . .	135
4.26	Speedup difference between corner injection and inner grid injec- tion $5 * n$ network ( $n = 1 \dots 5$ ) . . . . .	137
4.27	Comparing result between virtual cut-through switching and store and forward switching in $2 * 2$ mesh network . . . . .	140
4.28	Comparing result between virtual cut-through switching and store and forward switching in $2 * 3$ mesh network . . . . .	141
4.29	Comparing result between virtual cut-through switching scenario and store and forward switching scenario. The data injection is boundary processor of a $3 * 3$ mesh network. . . . .	142
4.30	The comparing result between virtual cut-through switching pro- cessor with without virtual cut-through switching processor in $3 * 3$ mesh network injection on inner grid processor . . . . .	143
4.31	Speedup difference between store and forward switching and vir- tual cut-through switching in $5 * n$ mesh network ( $n = 1 \dots 5$ ) .	145
5.1	Hypercube in 0, 1, 2, 3 dimension. [1] . . . . .	146
5.2	A hypercube network . . . . .	147

## List of Tables

4.1	$D_i$ vs Number . . . . .	108
4.2	$D_i$ vs Number of processor on each $D_i$ . . . . .	110
4.3	$D_i$ vs Number of processor on $D_i$ . . . . .	134

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# **Chapter 1**

## **Introduction**

During the past decade, divisible load scheduling and distribution techniques have been widely studied forming the divisible load theory (DLT). The load is defined to be divisible for computation and communication if it can be partitioned arbitrarily among processors. The divisible load model is a good approximation of tasks that require large number of identical, low-granularity computations, thus has been proposed for a wide range of scientific and engineering data processing, such as image processing, matrix multiplication, fast-Fourier-transformation (FFT), video encoding/decoding, stereo matching, etc [2] [3] [4] [5] [6]. A various constrains on different interconnection topologies [7] [8] [9] scheduling problems have been studied by the researchers.

Also, Networks on Chip (NOC) have become important and even essential to today's and future's electronic technology. This paradigm has emerged as a communication backbone to enable a high degree of integration in multi-core System-on-chip (SOC) [10] [11] [12]. To aid our discussion we will consider in detail the most popular and the most basic structured interconnection network for on-chip networking: the mesh and toroidal network. It is basically a chessboard (Manhattan streets) patterns of interconnection. Intellectual property (IP) are connected to their north, south, east and west neighbors through a network interface (NI). More specifically each network interface connects

through a link to a nearby “router”. Internally, each router consists of at most a  $5 \times 5$  cross-bar interconnection network (for up to four neighbors and a local connection), buffers, control logic and registers. Switching on a packet basis can either be done using *store and forward* [13] or *virtual cut-through* [14] switching approaches.

Further, Voronoi diagram is comprehensively utilized in network optimization application [15] [16] [17]. Nonetheless, most DLT researches mainly focused on the single source load distribution because of the complexity of optimal scheduling increase exponentially with the increase of load sources. Jia [18] propose a general method to address the multi-source scheduling problem. Yet, the algorithm has three perspective need more attention. First, his algorithm need to discard the part of previous computation result and do the global re-distribution. Then, his method didn’t give a quantitative model to represent the data fraction on each processor. Third, the algorithm doesn’t propose a general equivalence computation power, which is very useful for user to estimate the makespan and help me to allocate the data source workload.

The concept of processor equivalence was first proposed in [19]. This inspires us to adopt this model to tackle multi-source workload scheduling problems. We propose a flow matrix closed-form equation to present the equivalence, which allows a characterization of the nature of minimal time solution and a simple method to determine when and how much load to distribute for processors.

Also, we propose the use of a reduced Manhattan distance Voronoi diagram algorithm (RMDVDA) to minimize the overall processing time of these workloads by taking advantage of the processor equivalence technique. Three case studies with 10 sources of workloads are presented to illustrate the general approach for multiple sources of workloads. Experimental evaluation through simulations demonstrates that a task can be finished in the same suboptimal

time and yet save over 30% of processor resources.

Four chapters are organized as follows :

- A problem introduction, notation and definitions are shown in Chapter II.
- Chapter III considers mesh network. We solve the processor equivalence problem with virtual cut-through scenario and store and forward situation. Sensitivity analysis is another topic. In considering the multi-source workload assignment problem, we propose a reduced Manhattan distance Voronoi diagram algorithm. We propose two objective functions. First, we finish the load in the same makespan, yet utilizing less processors. Another one is changing the cluster partitioning to increasing the bottleneck's capacity to increase the whole cluster's equivalence computation.
- Chapter IV investigates the toroidal network situation. The virtual cut-through switching and store and forward switching assumption are discussed. Sensitivity analysis is examined and the multi-source assignment in torus network environment is also discussed. Two objective function, finishing the load with less sources and increasing the total equivalence computation, of torus network are also implemented in this chapter.
- Chapter V mentioned some general case for example, hypercube network and general network. We give two equivalence computation flow matrix in virtual cut-through switching and store and forward switching.
- Chapter VI discuss the conclusion and future work.

## Chapter 2

### Problem Description

#### 2.1 Problem Background

In large-scale data intensive problems with geographically distributed resources, load is generated from multiple sources [20] for a class of problems. It is assumed that the problem representation can be arbitrarily divided amongst the processors. Thus the problem representation is said to be “divisible”. The processing of massive amounts of data on distributed and parallel networks is becoming more and more common. The problem of minimizing the processing time of extensive loads originating from a multiplicity of sources and being processed on a multiplicity of nodes presents a challenge.

In this chapter, the closed-form processor equivalence [19] [21] problem in the grid networks of mesh network and toroidal rectangle network is discussed. Also, the multi-source workload assignment is also taken into account.

In this thesis, we investigate two problems. One is the processor equivalence problem. The other one is scheduling divisible workloads from multiple sources in mesh networks Fig. 2.1, toroidal rectangle networks Fig. 2.2.

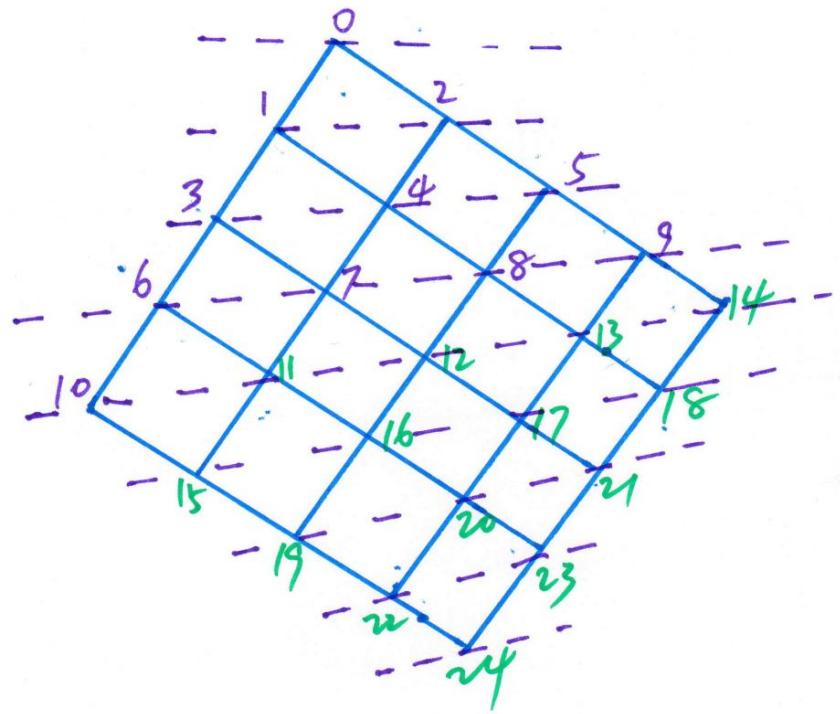


Figure 2.1: A  $m^*n$  mesh network( $m = 5$ ,  $n = 5$ )

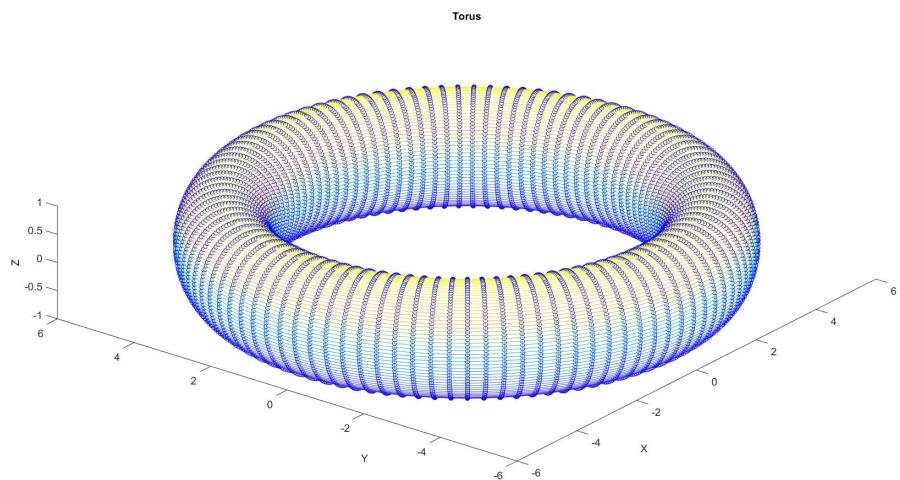


Figure 2.2: A toroidal rectangle network with grid unit cores

## 2.2 Definitions and Assumption

### Definition 2.2.1. *Equivalence Computation*

*Equivalence computation is a technique, which considers combining a cluster of processors as one whole processor to process a unit 1 workload.*

The following assumptions are used throughout the paper:

- Virtual cut-through [14] switching and store and forward switching is used to transmit the assigned workload between processors.
  - Under virtual cut-through switching, a node can relay the beginning bit of a message (packet) before the entire message is received.
  - Under store and forward switching, a message must be completely received by a node before it can be relayed to the next node along their transmission path.
- For simplicity, return communication is not considered.
- The communication delays are taken into consideration.
- The time costs of computation and communication are assumed to be linear function of the data size.
- The network environment is homogeneous, that is, all the processors have the same computation capacity. The link speeds between any two unit cores are identical.
- The number of outgoing ports in each processor is limited. In NOC (network on chip), the port number is fixed 4 or 5.
- The general graph's grid node's in-degree and out-degree is 5, .

The optimization objective functions are as follows :

- Equivalence computation : the problem's objective function is how to partition and schedule the workloads amongst the processors to obtain the minimum makespan (finish time).
- Multi-source assignment : how all processors can finish processing a unit 1 workload at the same time utilizing fewer processors.

To achieve the minimum time solution is obtained by forcing the processors over a network to stop processing simultaneously. Intuitively, this is because the solution could be improved by transfer load from some busy processors to idle ones [22] [23].

### 2.2.1 Notions

The following notations and definitions are utilized:

- $P_i$ : The  $i$ th processor.  $0 \leq i \leq m * n - 1$ .
- $L_i$ : The  $i$ th work load.  $1 \leq i \leq k$ .
- $D_i$ : The minimum number of hops from the processor  $P_i$  to the data load injection site  $L$ .
- $level_i$ : The processors have  $i$  minimum Manhattan distance to the data injection node.
- $\alpha_0$ : The load fraction assigned to the root processor.
- $\alpha_i$ : The load fraction assigned to the  $i$ th processor.
- $\omega_i$ : The inverse computing speed on the  $i$ th processor.
- $\omega_{eq}$ : The inverse computing speed on an equivalent node collapsed from a cluster of processors.

- $z_i$ : The inverse link speed on the  $i$ th link.
- $T_{cp}$ : Computing intensity constant. The entire load is processed in time  $\omega_i T_{cp}$  seconds on the  $i$ th processor.
- $T_{cm}$ : Communication intensity constant. The entire load is transmitted in time  $z_i T_{cm}$  seconds over the  $i$ th link.
- $T_{f,n}$ : The finish time of the whole processor network. Here  $T_{f,n}$  is equal to  $\omega_{eq} T_{cp}$ .
- $T_{f,0}$ : The finish time for the entire divisible load solved on the root processor. Here  $T_{f,0}$  is equal to  $1 \times \omega_0 T_{cp}$ , that is  $\omega_0 T_{cp}$ .
- $\sigma = \frac{z_i T_{cm}}{\omega_i T_{cp}}$ : The ratio between the communication speed to the computation speed,  $0 < \sigma < 1$  [22] [24].
- In multi-source situation,  $\sum_{i=1}^k L_i = 1$
- $\sum_{i=0}^{m*n-1} \alpha_i = 1$
- $Speedup = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega_0 T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0}$

## Chapter 3

### Mesh Network

#### 3.1 Virtual Cut-through Switching Scenario

In the virtual cut-through environment, a node can begin relaying the first part of a message (packet) along a transmission path as soon as it starts to arrive at the node , that is, it doesn't have to wait to receive the entire message before it can begin forwarding the message.

First we consider about the  $2*2$  mesh network,  $2*n$  mesh network. After, we analyze a more general case  $m*n$  mesh network and obtain a general closed-form matrix presentation. Finally, we give a key principle to address this type of question. In addition, different data injection position, such as the corner, boundary and inner grid are also discussed.

##### 3.1.1 Data Injection on The Corner Processor

###### **$2*2$ Mesh Network**

The  $L$  is assigned on the corner processor  $P_0$  Fig. 3.1. The whole task is tackled by four processors  $P_0, P_1, P_2, P_3$  together.

The processor  $P_0, P_1$  and  $P_2$  start to process its respective fraction at the same time. The processor  $P_3$  starts to work when the  $\alpha_1$  and  $\alpha_2$  are completed

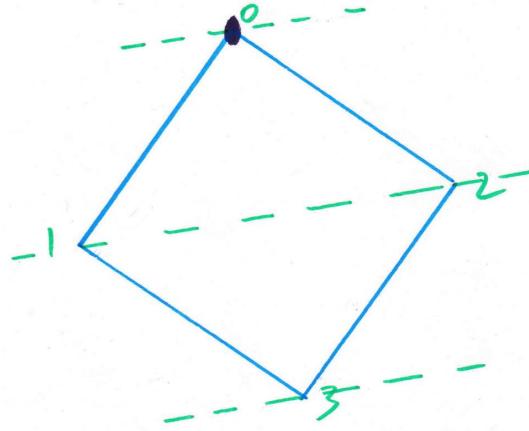


Figure 3.1: The  $2 \times 2$  mesh network and the root processor is  $P_0$

transmission. That is, the link  $0 - 1$  and  $0 - 2$  are occupied transmitting load to processor 1 and 2, respectively and only transmission to 3 when that is finished.

According to the divisible load theory [25], we obtain the timing diagram Fig. 3.2.

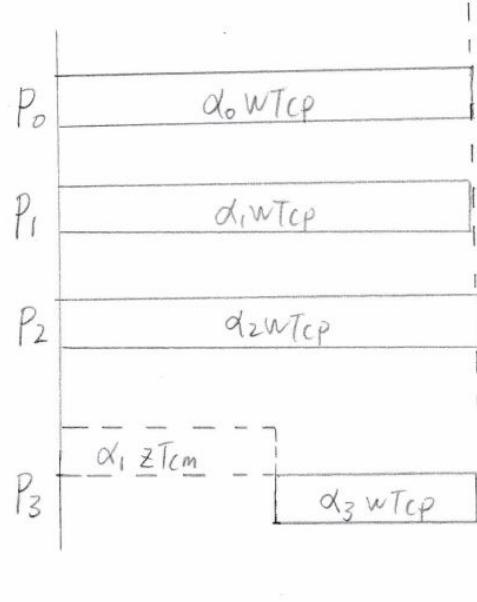


Figure 3.2: The timing diagram for  $2 \times 2$  mesh network and the root processor is  $P_0$

Here in the Gantt-like timing diagram communication appears above each axis and computations appears below the each axis. Let's assume that all processors stop computing at the same time in order to minimize the makespan [23].

Based on the timing diagram, we obtain a group of linear equations to find the fraction workload assigned to each processor  $\alpha_i$  :

$$\left\{ \begin{array}{l} \alpha_0 \omega T_{cp} = T_{f,m} \\ \alpha_1 \omega T_{cp} = T_{f,m} \\ \alpha_2 \omega T_{cp} = T_{f,m} \\ \alpha_1 z T_{cm} + \alpha_3 \omega T_{cp} = T_{f,m} \\ \alpha_0 + \alpha_1 + \alpha_2 + \alpha_3 = 1 \\ \sigma = \frac{z T_{cm}}{\omega T_{cp}} \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1, \alpha_2, \alpha_3 < 1 \end{array} \right. \quad \begin{array}{l} (3.1) \\ (3.2) \\ (3.3) \\ (3.4) \\ (3.5) \\ (3.6) \\ (3.7) \\ (3.8) \\ (3.9) \end{array}$$

The group of equations are represented by the matrix form:

$$\begin{bmatrix} 1 & 2 & 1 \\ 1 & -1 & 0 \\ 0 & \sigma - 1 & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_3 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \quad (3.10)$$

The matrix is represented as  $A \times \alpha = b$ .  $A$  is named as the ***flow matrix***.

Finally, the explicit solution is:

$$\left\{ \begin{array}{l} \sigma = \frac{zT_{cm}}{\omega T_{cp}} \\ \alpha_0 = \frac{1}{4 - \sigma} \end{array} \right. \quad (3.11)$$

$$\left\{ \begin{array}{l} \alpha_1 = \frac{1}{4 - \sigma} \\ \alpha_3 = \frac{1 - \sigma}{4 - \sigma} \end{array} \right. \quad (3.12)$$

$$\left\{ \begin{array}{l} \alpha_2 = \frac{1 - \sigma}{4 - \sigma} \end{array} \right. \quad (3.13)$$

$$\left\{ \begin{array}{l} \alpha_3 = \frac{1 - \sigma}{4 - \sigma} \end{array} \right. \quad (3.14)$$

The simulation result is illustrated:

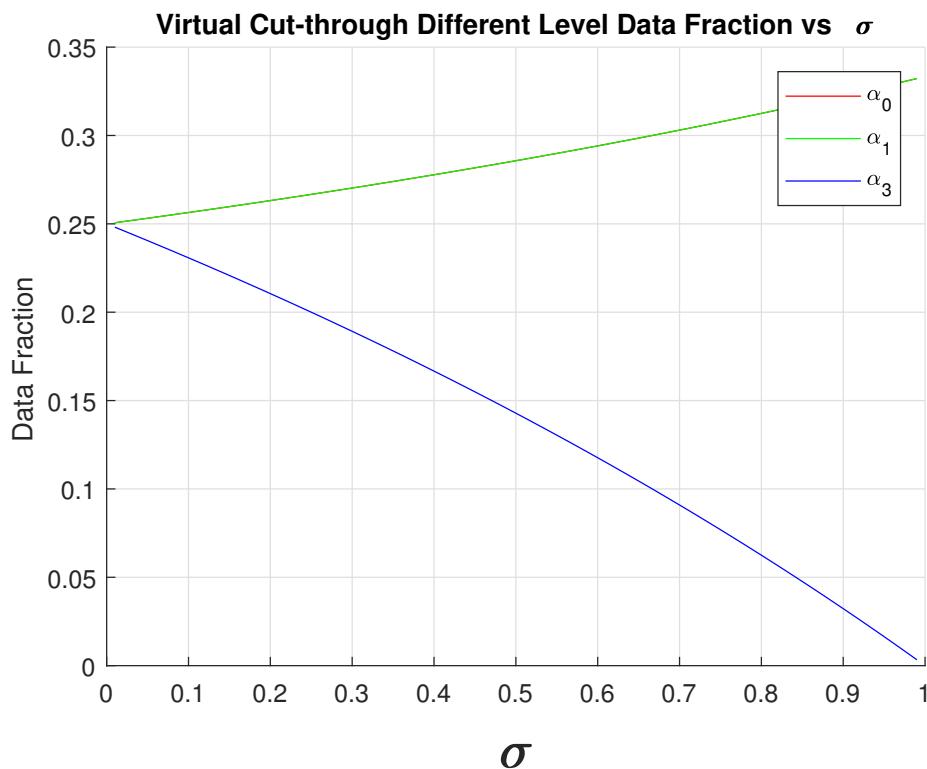


Figure 3.3: 2\*2 mesh network.  $\alpha_0, \alpha_1, \alpha_2, \alpha_3$  value curve

In Fig. 3.3, the three processors  $P_0, P_1, P_2$  three processors have the same data fraction workload, so the curve of  $\alpha_0$  and  $\alpha_1$  coincide.

Also from symmetry  $\alpha_1 = \alpha_2$ , the figure says that as  $\sigma$  grows, the value  $\alpha_3$  drops. In other words, as the communication capacity decreases, there is less data workload assigned to  $P_3$ . Further, it means it will be economical to keep the load local on  $P_0 P_1 P_2$  and not distribute it, to other processors.

The speedup is:

$$Speedup = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0} = 4 - \sigma$$

## 2\*3 Mesh Network

In Fig. 3.4 mesh network,  $L$  originates on processor  $P_0$ . There are 6 processors in this network.

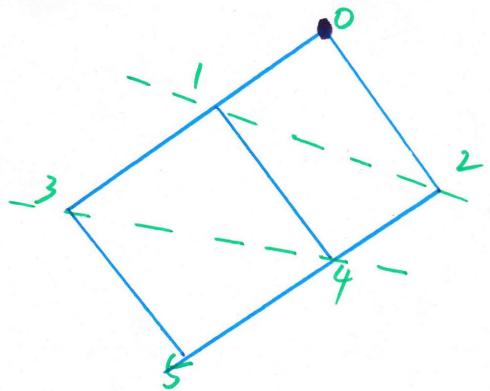


Figure 3.4: The 2\*3 mesh network and the data injection happens on corner processor  $P_0$

Here  $P_0$ ,  $P_1$  and  $P_2$  start processing at the same time. Processor  $P_3$  and  $P_4$  start to work when they receive the data from processor  $P_1$ ,  $P_2$ , after the  $0 - 1$  and  $0 - 2$  link become available to transfer load to  $P_3$  and  $P_4$ . The last processor  $P_5$  doesn't start to execute until the work load fraction  $\alpha_0, \alpha_1, \alpha_2, \alpha_3, \alpha_4$  are transmitted completed. According to the divisible load theory [25], we obtain the timing diagram Fig. 3.5.

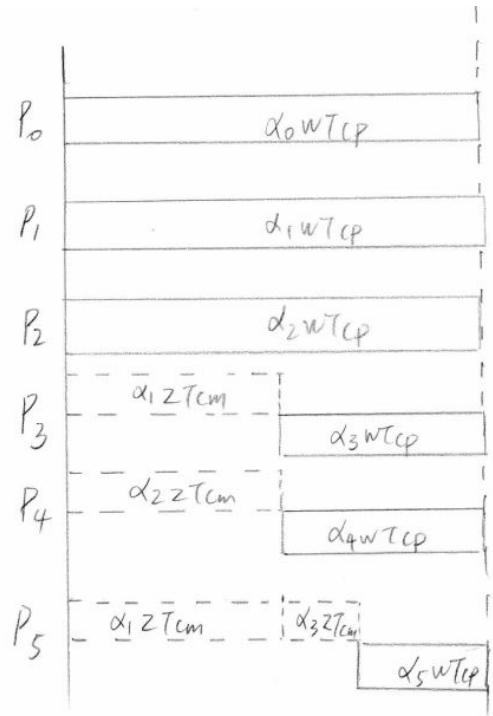


Figure 3.5: The timing diagram for a  $2 \times 3$  mesh network and the data injection happens on processor  $P_0$

The timing diagram equations as follows:

$$\left\{ \begin{array}{l} \alpha_0 \omega T_{cp} = T_{f,m} \\ \alpha_1 \omega T_{cp} = T_{f,m} \\ \alpha_2 \omega T_{cp} = T_{f,m} \\ \alpha_1 z T_{cm} + \alpha_3 \omega T_{cp} = T_{f,m} \\ \alpha_2 z T_{cm} + \alpha_4 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_3) z T_{cm} + \alpha_5 \omega T_{cp} = T_{f,m} \\ \alpha_0 + \alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 + \alpha_5 = 1 \\ \sigma = \frac{z T_{cm}}{\omega T_{cp}} \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5 < 1 \end{array} \right. \quad \begin{array}{l} (3.15) \\ (3.16) \\ (3.17) \\ (3.18) \\ (3.19) \\ (3.20) \\ (3.21) \\ (3.22) \\ (3.23) \\ (3.24) \\ (3.25) \end{array}$$

The flow matrix closed-form formula is:

$$\begin{bmatrix} 1 & 2 & 2 & 1 \\ 1 & -1 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 \\ 0 & \sigma - 1 & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_3 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.26)$$

The explicit solution is:

$$\left\{ \begin{array}{l} \sigma = \frac{zT_{cm}}{\omega T_{cp}} \end{array} \right. \quad (3.27)$$

$$\alpha_0 = \frac{1}{\sigma^2 - 4 \times \sigma + 6} \quad (3.28)$$

$$\alpha_1 = \frac{1}{\sigma^2 - 4 \times \sigma + 6} \quad (3.29)$$

$$\alpha_3 = \frac{1 - \sigma}{\sigma^2 - 4 \times \sigma + 6} \quad (3.30)$$

$$\alpha_5 = \frac{\sigma^2 - 2 \times \sigma + 1}{\sigma^2 - 4 \times \sigma + 6} \quad (3.31)$$

The  $\alpha$  calculation result are shown in Fig. 3.6.  $P_0, P_1$  have the same fraction so the curve of  $\alpha_0$  and  $\alpha_1$  coincide. Because of symmetry,  $\alpha_1 = \alpha_2$  and  $\alpha_3 = \alpha_4$ , if the communication time is zero, each of the six processors get like  $\frac{1}{6}$  of the load which shows in the figure. If the communication delay equals computation time  $\frac{1}{3}$  of the load goes to each of  $P_0, P_1$  and  $P_2$ .

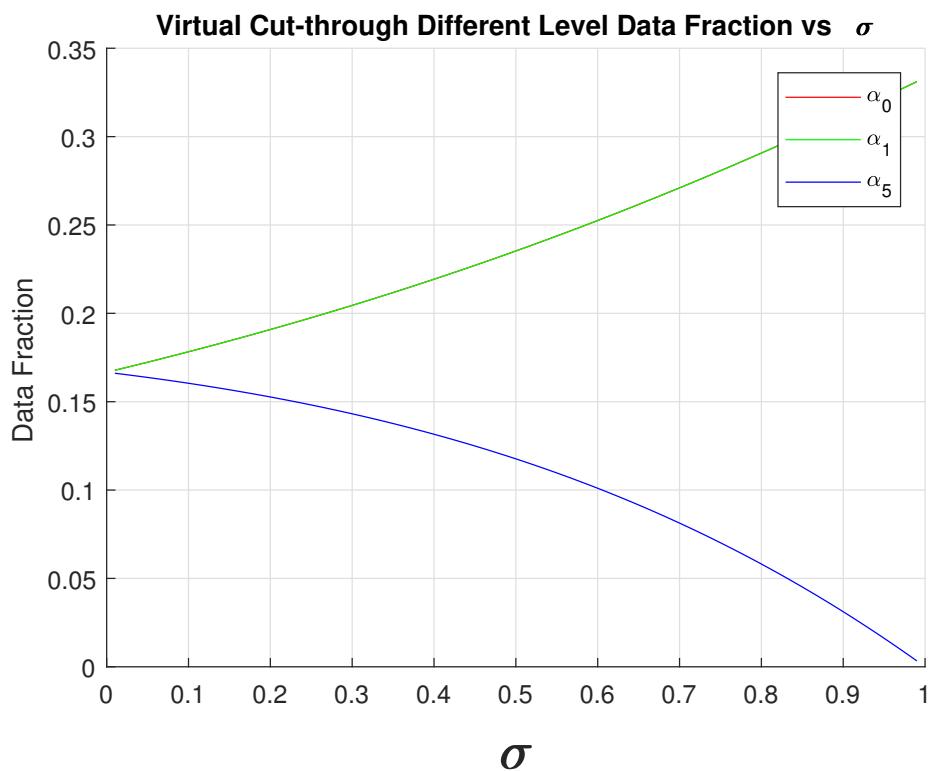


Figure 3.6:  $2^*3$  mesh network.  $\alpha_0$ ,  $\alpha_1$ ,  $\alpha_3$ ,  $\alpha_5$  value curve.

### 2\*N Mesh Network

The  $2 * n$  Fig. 3.7 homogeneous mesh network process load  $L$  and  $L$  originates  $P_0$ .

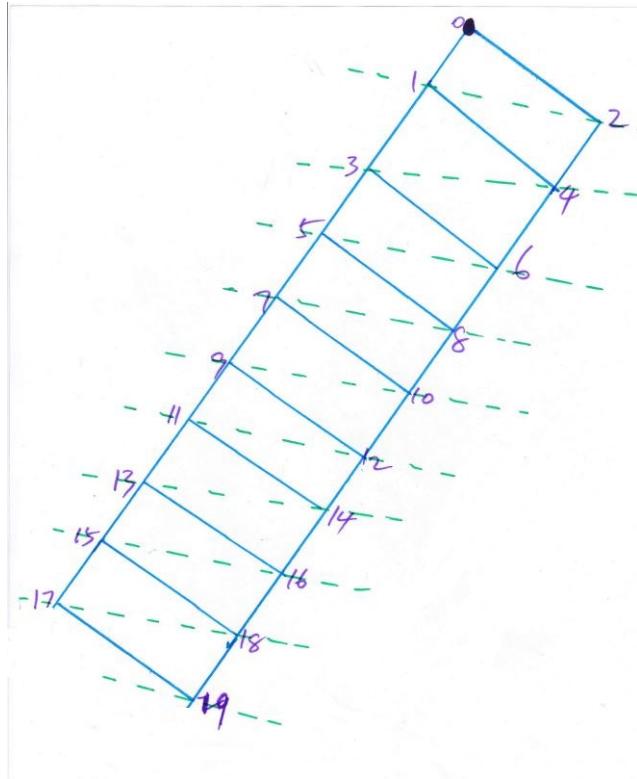


Figure 3.7:  $2^*n$  ( $n = 10$ ) mesh network and the workload happens on  $P_0$

Load a distribution from  $P_0$  to  $P_1$  and  $P_2$  via virtual cut-through. After  $P_1$  and  $P_2$  finish receiving load from link  $0 - 1$  and  $0 - 2$ , they will be used to forward load to  $P_3$  and  $P_4$  and so on.

Similarly to the analysis of Fig. 3.2 and Fig. 3.5, the timing diagram for Fig. 3.7 is shown in Fig. 3.8

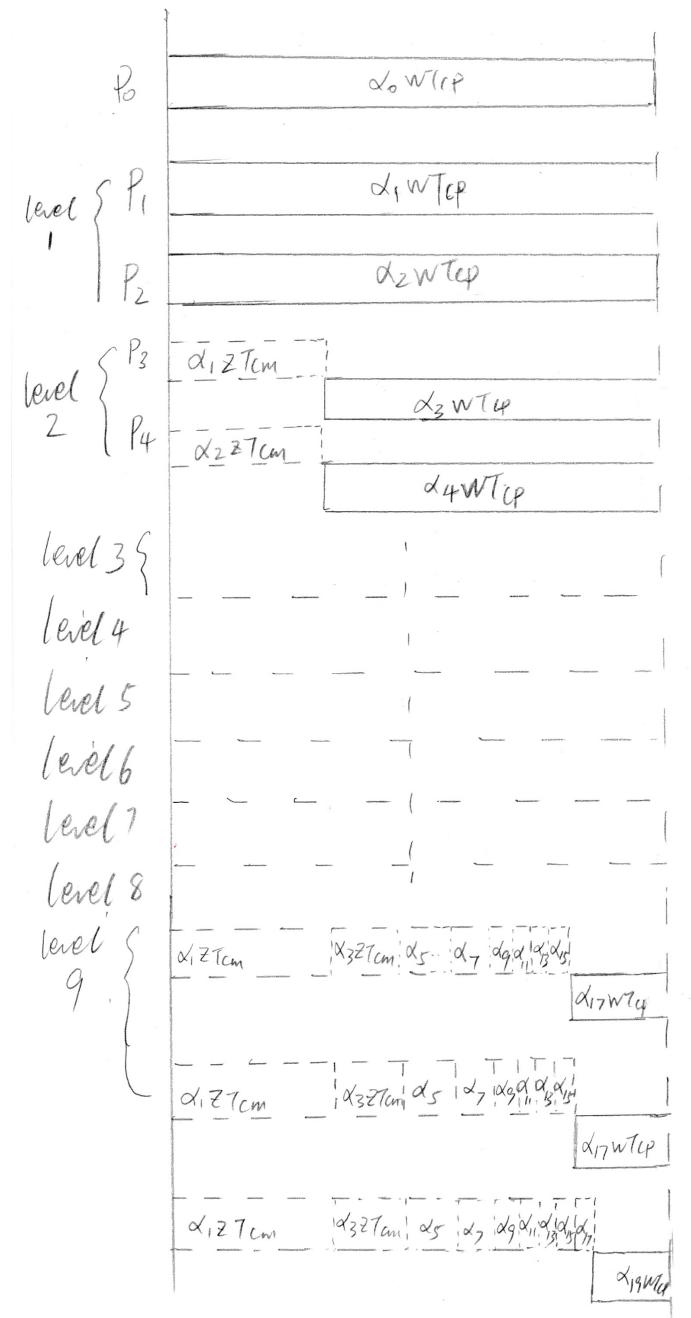


Figure 3.8: The timing diagram for  $2 \times 10$  mesh network and the data injection happens on  $P_0$

The equations are presented as:

$$\left\{ \begin{array}{l} \alpha_0 \omega T_{cp} = T_{f,m} \\ \alpha_1 \omega T_{cp} = T_{f,m} \\ \alpha_2 \omega T_{cp} = T_{f,m} \\ \alpha_1 z T_{cm} + \alpha_3 \omega T_{cp} = T_{f,m} \\ \alpha_2 z T_{cm} + \alpha_4 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_3) z T_{cm} + \alpha_5 \omega T_{cp} = T_{f,m} \\ \vdots \\ (\alpha_1 + \alpha_3 + \cdots + \alpha_{2 \times n-1}) z T_{cm} + \alpha_{2 \times n-1} \omega T_{cp} = T_{f,m} \\ \alpha_0 + \cdots + \alpha_{2 \times n-1} = 1 \\ \sigma = \frac{z T_{cm}}{\omega T_{cp}} \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1 \alpha_2 \cdots \alpha_{2 \times n-1} < 1 \end{array} \right. \quad \begin{array}{l} (3.32) \\ (3.33) \\ (3.34) \\ (3.35) \\ (3.36) \\ (3.37) \\ (3.38) \\ (3.39) \\ (3.40) \\ (3.41) \\ (3.42) \\ (3.43) \\ (3.44) \end{array}$$

The flow matrix closed-form is shown:

$$\left[ \begin{array}{ccccccc} 1 & 2 & 2 & \cdots & 2 & 2 & 1 \\ 1 & -1 & 0 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \\ 0 & \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{array} \right] \times \left[ \begin{array}{c} \alpha_0 \\ \alpha_1 \\ \alpha_3 \\ \alpha_5 \\ \vdots \\ \alpha_{2 \times n-3} \\ \alpha_{2 \times n-1} \end{array} \right] = \left[ \begin{array}{c} 1 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{array} \right] \quad (3.45)$$

According to the **Cramer's rule**, the explicit solution for the group of equations is:

$$\left\{ \alpha_i = \left| \frac{\det A_i^*}{\det A} \right| \right. \quad (3.46)$$

where  $A_i^*$  is the matrix formed by replacing the  $i$ -th column of  $A$  by the column vector  $b$ .

Especially,

$$A_0^* = \begin{bmatrix} 1 & 2 & 2 & \cdots & 2 & 2 & 1 \\ 0 & -1 & 0 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \ddots \\ 0 & \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{bmatrix} \quad (3.47)$$

$$\alpha_0 = \left| \frac{\det A_0^*}{\det A} \right|$$

$$\det A_0^* = -1$$

Finally, the speedup is:

$$Speedup = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0} = |-\det A|$$

Further, we prove the matrix  $\det A \neq 0$ .

$$C = \begin{bmatrix} -1 & 0 & \cdots & 0 & 0 & 0 \\ \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots \\ \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{bmatrix} \quad (3.48)$$

$C$  is a lower triangular matrix and the diagonal elements are not 0. So  $C$  is non-degenerate, that is, the matrix is column linear independence.

After a series of column reduction and row reduction actions, we get

$$A = \begin{bmatrix} 1 & 2 & 2 & \cdots & 2 & 2 & 1 \\ 1 & -1 & 0 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \\ 0 & \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{bmatrix} \xrightarrow{\text{Column Reduction}} \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 & 0 \\ 1 & -3 & -2 & \cdots & -2 & -2 & -1 \\ 0 & \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \\ 0 & \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{bmatrix}$$

$$\xrightarrow{\text{Row Reduction}} \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 & 0 \\ 0 & -3 & -2 & \cdots & -2 & -2 & -1 \\ 0 & \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \\ 0 & \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{bmatrix}$$

Considering the matrix  $\hat{C}$

$$\hat{C} = \begin{bmatrix} -3 & -2 & \cdots & -2 & -2 & -1 \\ \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots \\ \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{bmatrix} \quad (3.49)$$

, which is still column linear independence. Considering  $0 < \sigma < 1$ , the flow matrix is full rank. So  $\det A \neq 0$ .

After three user cases' investigation, we find a crucial methodology:

$$\forall D_i = D_j, \quad \text{then} \quad \alpha_i = \alpha_j, \quad 0 \leq i, j \leq m * n - 1$$

## $m*n$ Mesh Network

Considering a general  $m * n$  mesh network, such as Fig. 3.9 Fig. 2.1.

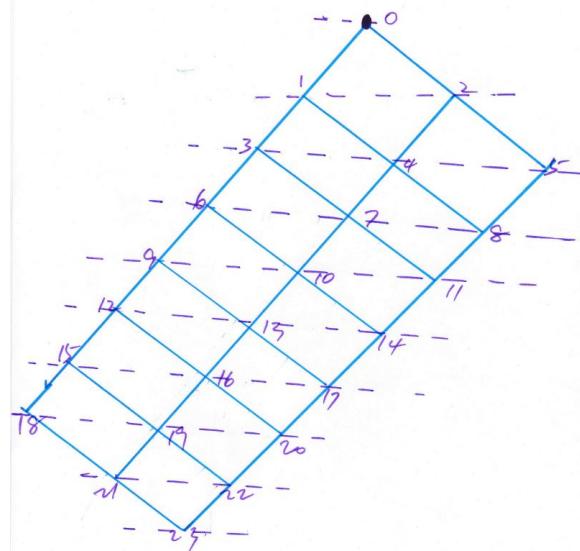


Figure 3.9:  $3*8$  mesh network. The data injection position is  $P_0$

Utilizing the previous methodology, we obtain the closed-form flow matrix equations for Fig. 3.9:

$$\begin{bmatrix}
 1 & 2 & 3 & 3 & 3 & 3 & 3 & 2 & 1 \\
 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & \sigma - 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & \sigma - 1 & \sigma & 1 & 0 & 0 & 0 & 0 & 0 \\
 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 & 0 & 0 \\
 0 & \sigma - 1 & \sigma & \sigma & \sigma & 1 & 0 & 0 & 0 \\
 0 & \sigma - 1 & \sigma & \sigma & \sigma & \sigma & 1 & 0 & 0 \\
 0 & \sigma - 1 & \sigma & \sigma & \sigma & \sigma & \sigma & 1 & 0 \\
 0 & \sigma - 1 & \sigma & \sigma & \sigma & \sigma & \sigma & \sigma & 1
 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_3 \\ \alpha_6 \\ \alpha_9 \\ \alpha_{12} \\ \alpha_{15} \\ \alpha_{18} \\ \alpha_{21} \\ \alpha_{23} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad (3.50)$$

Also, the flow matrix equations for Fig. 2.1:

$$\begin{bmatrix} 1 & 2 & 3 & 4 & 5 & 4 & 3 & 2 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & 1 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & \sigma & 1 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & \sigma & \sigma & 1 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & \sigma & \sigma & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_3 \\ \alpha_6 \\ \alpha_{10} \\ \alpha_{15} \\ \alpha_{19} \\ \alpha_{22} \\ \alpha_{24} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad (3.51)$$

We use the similar method to prove  $\det A \neq 0$ , so the speedup is:

$$Speedup = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0} = |-\det A|$$

### 3.1.2 Data Injection On The Boundary Processor

After the corner scenario, we extend the methodology to boundary processor load origination.

A single data injection root-node on the boundary processor, as shown in Fig. 3.10.

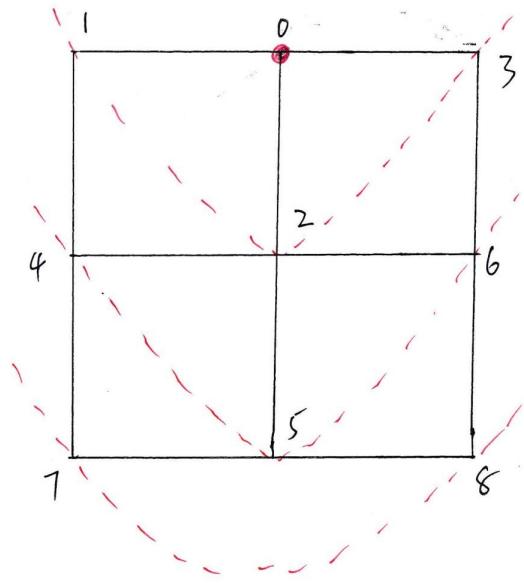


Figure 3.10: The  $3 \times 3$  mesh network and the root processor is  $P_0$

The timing diagram is Fig. 3.11:

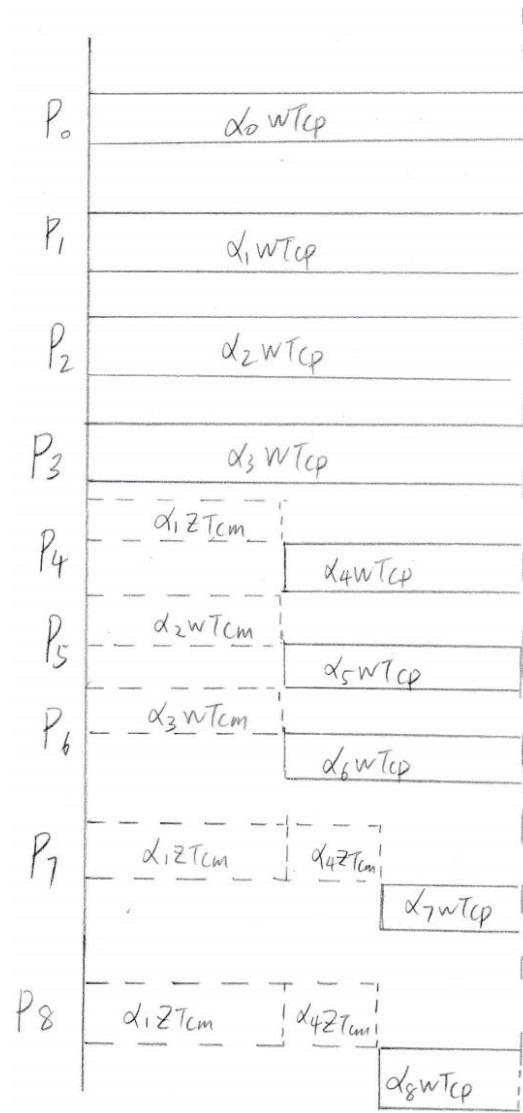


Figure 3.11: The timing diagram for  $3 \times 3$  mesh network and the data injection occurs on  $P_0$

$P_0$ ,  $P_1$ ,  $P_2$  and  $P_3$  commence processing at  $t = 0$  axis timing diagram.  $P_1$ ,  $P_2$  and  $P_3$  receive load in virtual cut-through mode from  $P_0$ . Once that is finished, link  $0 - 1$ ,  $0 - 2$  and  $0 - 3$  is used to forward load to nodes  $P_4$ ,  $P_5$  and  $P_6$  in virtual cut-through mode. Once that is finished, the link that have been

so far are used to forward load to  $P_7$  and  $P_8$  in virtual cut-through mode.

The equations are:

$$\left\{ \begin{array}{l} \alpha_0 \omega T_{cp} = T_{f,m} \\ \alpha_1 \omega T_{cp} = T_{f,m} \\ \alpha_2 \omega T_{cp} = T_{f,m} \\ \alpha_3 \omega T_{cp} = T_{f,m} \\ \alpha_1 z T_{cm} + \alpha_4 \omega T_{cp} = T_{f,m} \\ \alpha_2 z T_{cm} + \alpha_5 \omega T_{cp} = T_{f,m} \\ \alpha_3 z T_{cm} + \alpha_6 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_4) z T_{cm} + \alpha_7 \omega T_{cp} = T_{f,m} \\ (\alpha_2 + \alpha_5) z T_{cm} + \alpha_8 \omega T_{cp} = T_{f,m} \\ \alpha_0 + \dots + \alpha_8 = 1 \\ \sigma = \frac{z T_{cm}}{\omega T_{cp}} \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1 \alpha_2 \dots \alpha_8 < 1 \end{array} \right. \begin{array}{l} (3.52) \\ (3.53) \\ (3.54) \\ (3.55) \\ (3.56) \\ (3.57) \\ (3.58) \\ (3.59) \\ (3.60) \\ (3.61) \\ (3.62) \\ (3.63) \\ (3.64) \\ (3.65) \\ (3.66) \end{array}$$

And the flow matrix form is :

$$\begin{bmatrix} 1 & 3 & 3 & 2 \\ 1 & -1 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 \\ 0 & \sigma - 1 & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_4 \\ \alpha_7 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.67)$$

The explicit solution is:

$$\left\{ \begin{array}{l} \alpha_0 = \frac{1}{9 - 7 \times \sigma + 2 \times \sigma^2} \end{array} \right. \quad (3.68)$$

$$\left\{ \begin{array}{l} \alpha_1 = \frac{1}{9 - 7 \times \sigma + 2 \times \sigma^2} \end{array} \right. \quad (3.69)$$

$$\left\{ \begin{array}{l} \alpha_4 = \frac{1 - \sigma}{9 - 7 \times \sigma + 2 \times \sigma^2} \end{array} \right. \quad (3.70)$$

$$\left\{ \begin{array}{l} \alpha_7 = \frac{(1 - \sigma)^2}{9 - 7 \times \sigma + 2 \times \sigma^2} \end{array} \right. \quad (3.71)$$

$$\left\{ \begin{array}{l} \alpha_7 = \frac{(1 - \sigma)^2}{9 - 7 \times \sigma + 2 \times \sigma^2} \end{array} \right. \quad (3.72)$$

The simulation result is shown: The curve  $\alpha_0$  is identified to the curve for

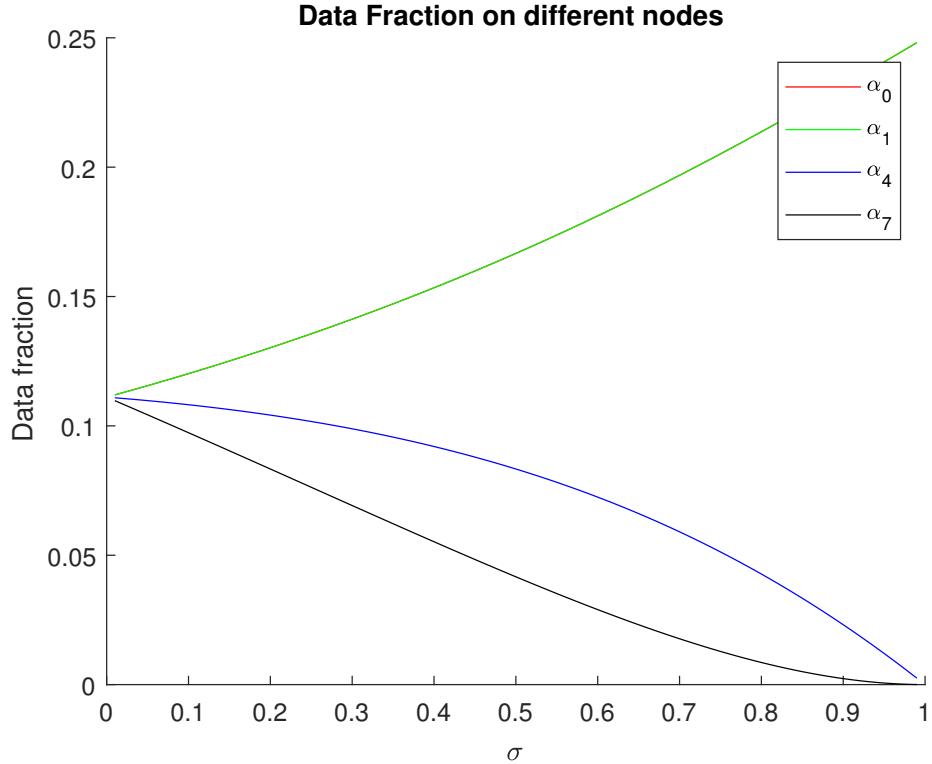


Figure 3.12: The data fraction simulation result of  $3 \times 3$  mesh network and the data injection happens on the boundary  $P_0$

$\alpha_1$ ,  $\alpha_2$  and  $\alpha_3$ . The curve  $\alpha_4$  is identified to the curves of  $\alpha_5$  and  $\alpha_6$ . The curve  $\alpha_7$  is identified to the curve for  $\alpha_8$ . If communication time is zero (extremely fast communication), each processor get  $\frac{1}{9}$  of the load. If communication time equals computation time, each of the four start stage nodes ( $P_0, P_1, P_2, P_3$ ) get  $\frac{1}{4}$  of the load fraction.

### 3.1.3 Data Injection On The Inner Grid Processor

Fig. 3.13 shows that  $L$  load on the inner grid processor  $P_0$ ,  $P_0$ ,  $P_1$ ,  $P_2$ ,  $P_3$  and  $P_4$  commence processing at time = 0 through virtual cut-through

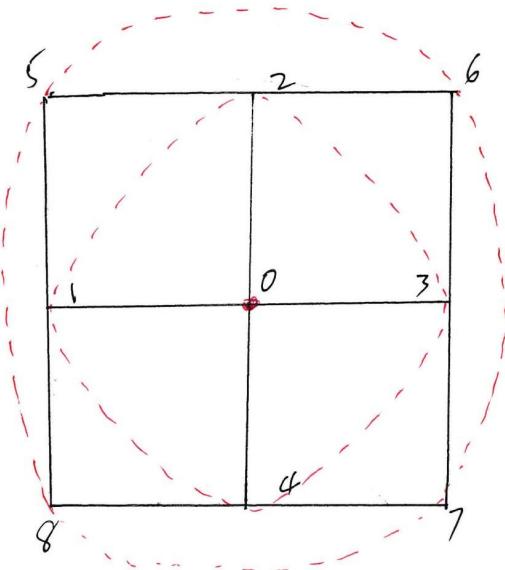


Figure 3.13:  $3 \times 3$  mesh network. The data injection position is inner grid point  $P_0$

switching. Once this is finished links  $0 - 1$ ,  $0 - 2$ ,  $0 - 3$  and  $0 - 4$  are released to forward load to  $P_5$ ,  $P_6$ ,  $P_7$  and  $P_8$  in virtual cut-through mode.

The timing diagram for this user case is illustrated as Fig. 3.14:

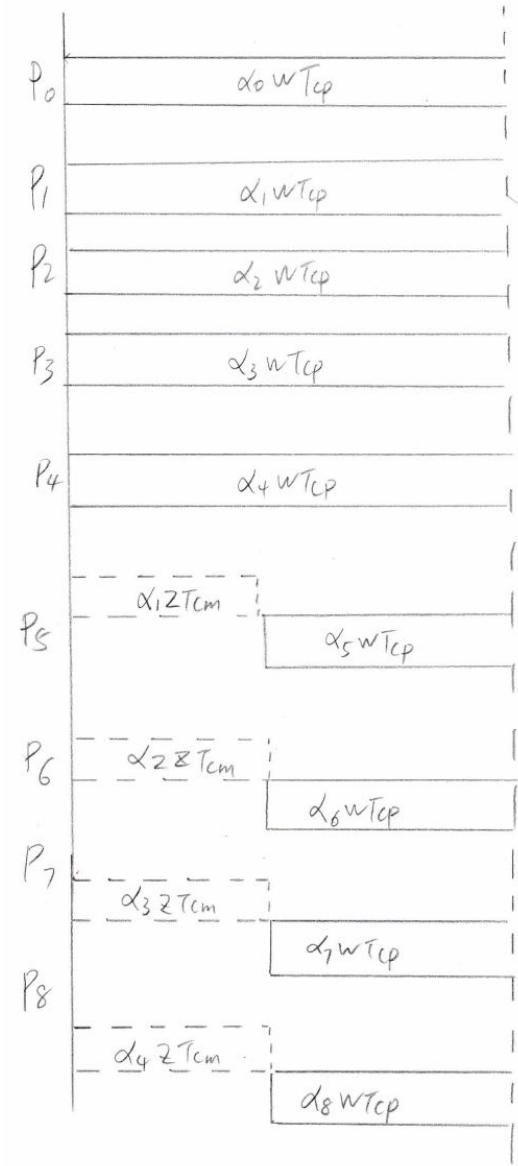


Figure 3.14: The timing diagram for  $3 \times 3$  mesh network and the data injection is inner grid  $P_0$

The group of equations are:

$$\left. \begin{array}{l} \alpha_0\omega T_{cp} = T_{f,m} \\ \alpha_1\omega T_{cp} = T_{f,m} \\ \alpha_2\omega T_{cp} = T_{f,m} \\ \alpha_3\omega T_{cp} = T_{f,m} \\ \alpha_4\omega T_{cp} = T_{f,m} \\ \alpha_1zT_{cm} + \alpha_5\omega T_{cp} = T_{f,m} \\ \alpha_1zT_{cm} + \alpha_6\omega T_{cp} = T_{f,m} \\ \alpha_1zT_{cm} + \alpha_7\omega T_{cp} = T_{f,m} \\ \alpha_1zT_{cm} + \alpha_8\omega T_{cp} = T_{f,m} \\ \sigma = \frac{zT_{cm}}{\omega T_{cp}} \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1 \quad \alpha_2 \quad \dots \quad \alpha_8 < 1 \end{array} \right\} \quad (3.73)$$

$$\alpha_1\omega T_{cp} = T_{f,m} \quad (3.74)$$

$$\alpha_2\omega T_{cp} = T_{f,m} \quad (3.75)$$

$$\alpha_3\omega T_{cp} = T_{f,m} \quad (3.76)$$

$$\alpha_4\omega T_{cp} = T_{f,m} \quad (3.77)$$

$$\alpha_1zT_{cm} + \alpha_5\omega T_{cp} = T_{f,m} \quad (3.78)$$

$$\alpha_1zT_{cm} + \alpha_6\omega T_{cp} = T_{f,m} \quad (3.79)$$

$$\alpha_1zT_{cm} + \alpha_7\omega T_{cp} = T_{f,m} \quad (3.80)$$

$$\alpha_1zT_{cm} + \alpha_8\omega T_{cp} = T_{f,m} \quad (3.81)$$

$$\sigma = \frac{zT_{cm}}{\omega T_{cp}} \quad (3.82)$$

$$0 < \sigma < 1 \quad (3.83)$$

$$0 < \alpha_0 \leq 1 \quad (3.84)$$

$$0 \leq \alpha_1 \quad \alpha_2 \quad \dots \quad \alpha_8 < 1 \quad (3.85)$$

The flow matrix form is :

$$\begin{bmatrix} 1 & 4 & 4 \\ 1 & -1 & 0 \\ 0 & \sigma - 1 & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \quad (3.86)$$

The simulation result is Fig. 3.15:  $P_0$  and  $P_1$  have the same  $\alpha$  value, so the curve of  $\alpha_0$  and  $\alpha_1$  coincide.

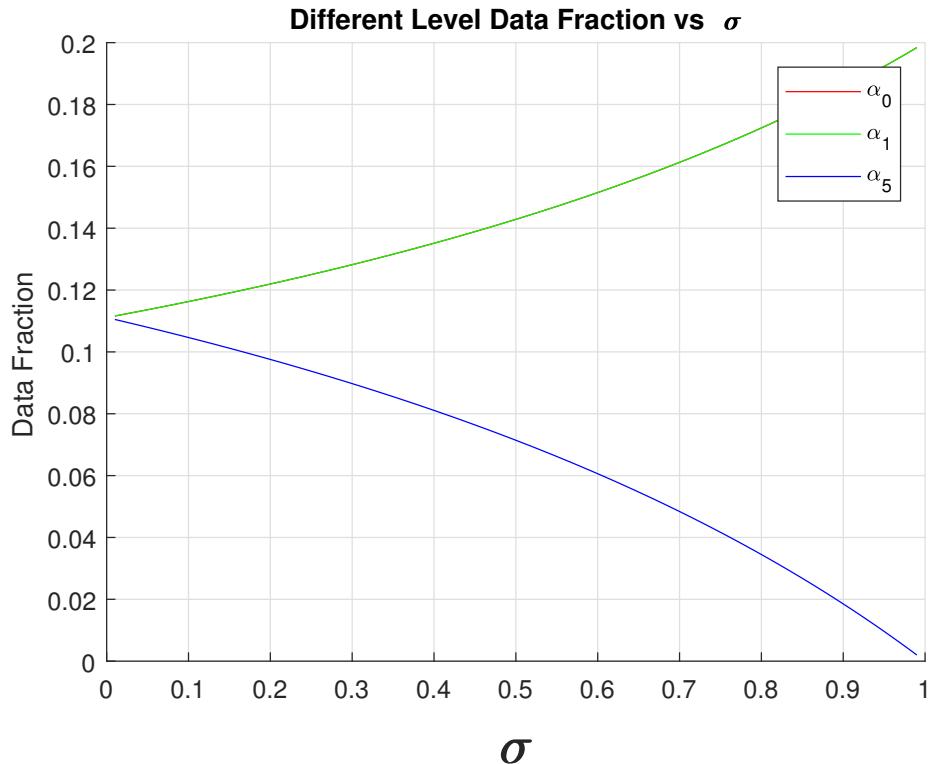


Figure 3.15: 3\*3 mesh network. The data injection position is inner grid point  $P_0$

The explicit solution is:

$$\left\{ \begin{array}{l} \alpha_0 = \frac{1}{9 - 4 \times \sigma} \\ \alpha_1 = \frac{1}{9 - 4 \times \sigma} \end{array} \right. \quad (3.87)$$

$$\left\{ \begin{array}{l} \alpha_5 = \frac{1 - \sigma}{9 - 4 \times \sigma} \end{array} \right. \quad (3.88)$$

$$\left\{ \begin{array}{l} \alpha_5 = \frac{1 - \sigma}{9 - 4 \times \sigma} \end{array} \right. \quad (3.89)$$

If the communication time is zero (very fast communication), each of nine

processors get  $\frac{1}{9}$  of the load. If communication time equals computation time, each of processors  $P_0$ ,  $P_1$ ,  $P_2$ ,  $P_3$  and  $P_4$  get  $\frac{1}{5}$  of the load.

### 3.1.4 Sensitivity Analysis Virtual Cut-through Switching Scenario

From Chapter 2, we know the speedup is :

$$\text{Speedup} = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0} = |-\det A|$$

#### Data Injection On The Corner Processor

The simulation result of sensitivity analysis of  $2*n$  mesh network Fig. 3.7 is as follows:

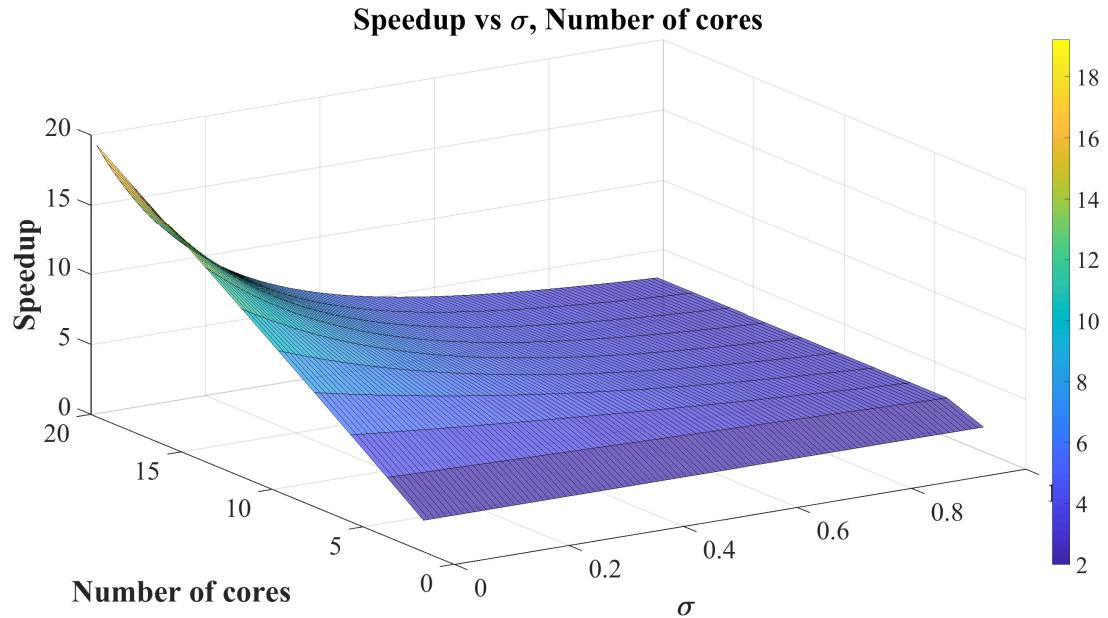


Figure 3.16: Sensitivity analysis result of  $2*n$  mesh network (where  $n = 1 \dots 10$ )

One can see speedup increases with an increasing number of core (i.e. processor) and also increases with decreasing  $\sigma$  (that is increasing communication speed relative to computation speed).

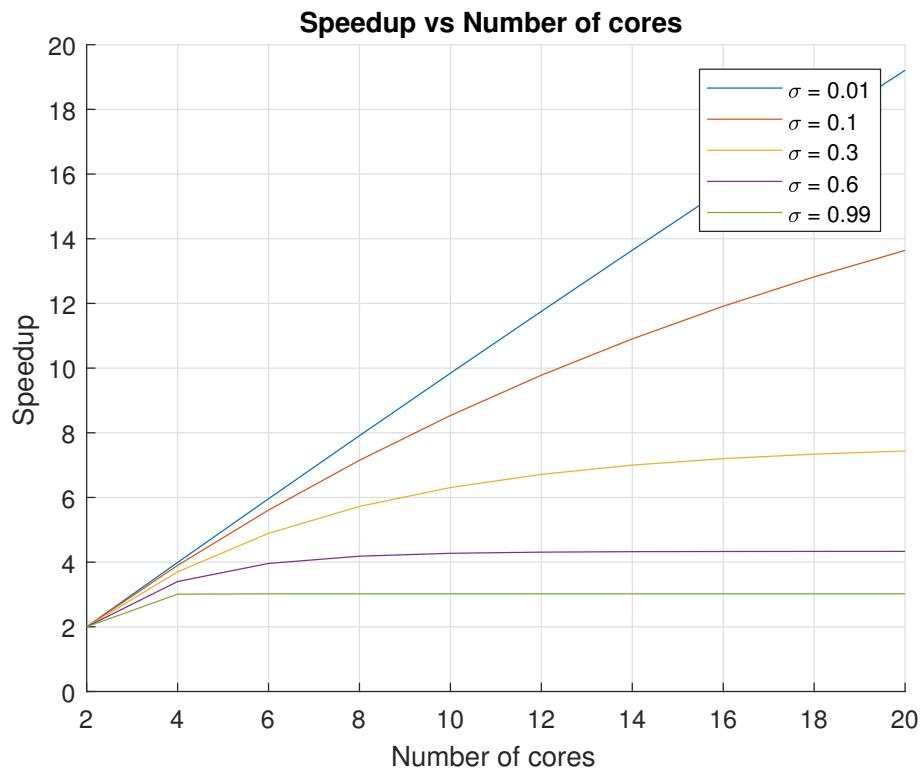


Figure 3.17: Speedup curves of  $2^*n$  mesh network (where  $n = 1 \cdots 10$ )

For a large number of cores and  $\sigma$  close to one, speedup is three times.  $P_0$  and two adjacent neighbor processor do most of the processing.

## Data Injection On The Boundary Processor

For a  $3*n$  mesh network Fig. 3.9, the data injection happens on boundary processor  $P_2$ .

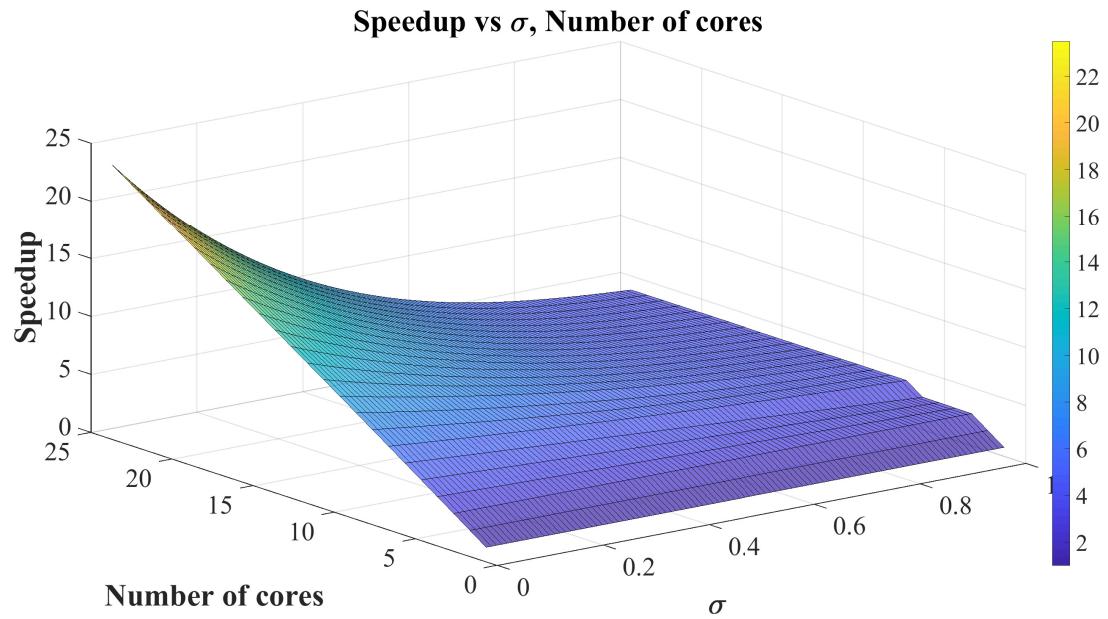


Figure 3.18: Sensitivity analysis result of  $3*n$  mesh network and the injection position on boundary processor  $P_2$  (where  $n = 1 \cdots 8$ )

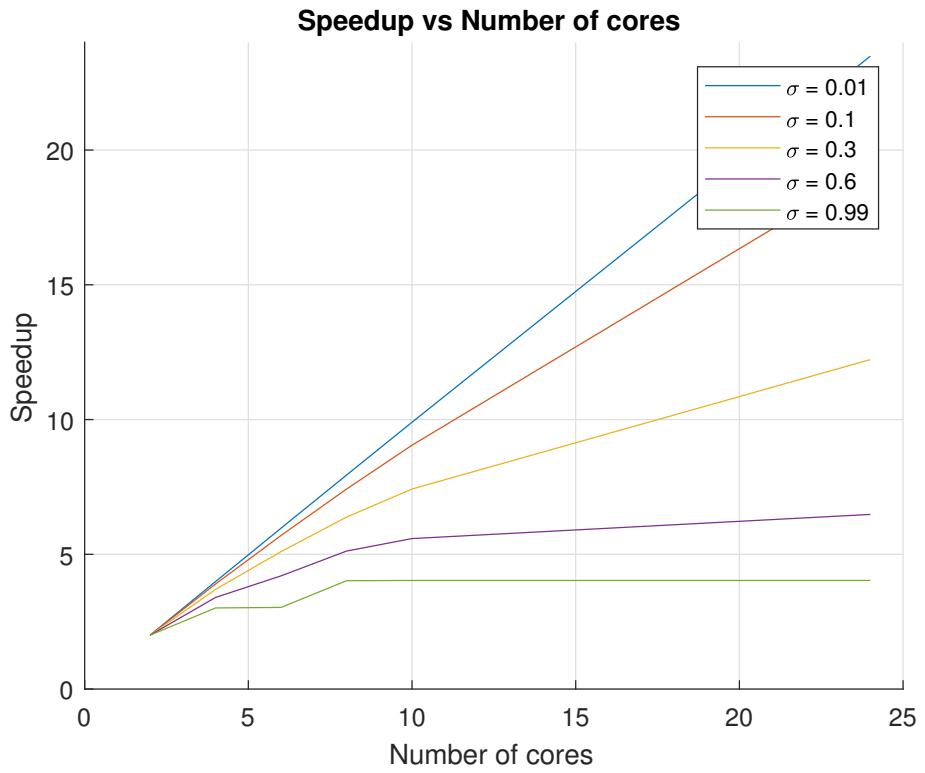


Figure 3.19: Speedup curve of  $3^*n$  mesh network (where  $n = 1 \cdots 8$ )

Fig. 3.18 and Fig. 3.19 show that if the value  $\sigma > 0.2$ , the speedup simulation effect increases rapidly. If the value  $\sigma < 0.1$ , the number of cores has linear impact on the speedup performance. If the number of cores is for  $\sigma$  close to one, the speedup is about four since only the three processors close to  $P_0$  and  $P_0$  do almost all the processing.

## Data Injection On The Inner Grid Processor

For a  $5 * n$  mesh network is in Fig. 2.1,  $L$  originate on the inner grid  $P_{12}$  and the simulation result says:

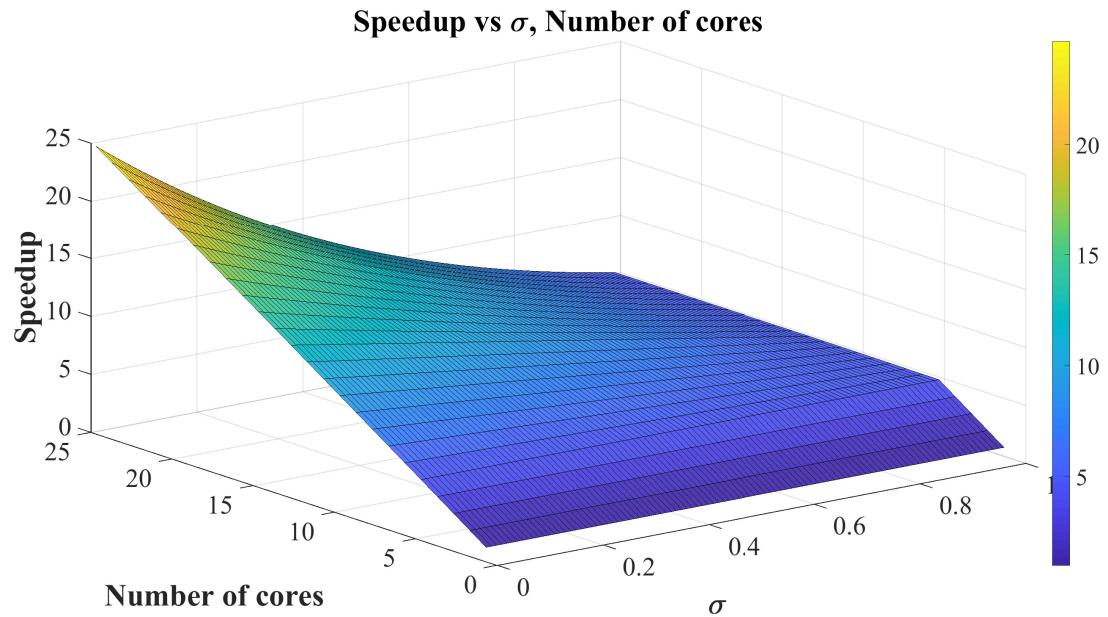


Figure 3.20: Sensitivity analysis result of  $5 * n$  mesh network and the injection position on inner processor  $P_{12}$  (where  $n = 1 \dots 5$ )

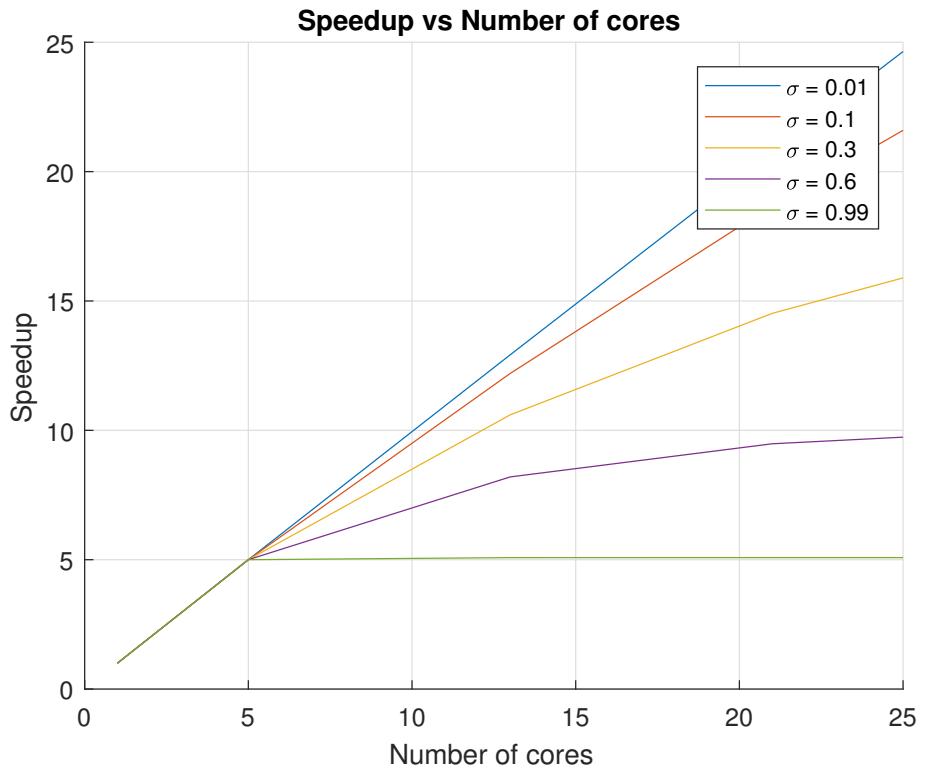


Figure 3.21: Speedup curves of  $5^*n$  mesh network Fig. 2.1 (where  $n = 1 \cdots 5$ )

If the number of processor  $> 5$ , the cluster equivalence computation ability is at least 5 time speedup. There are 5 processors in the first stage. For small  $\sigma$  speedup growth is linear. For large  $\sigma$  and a large number of cores, speedup is about five as only  $P_0$  and four adjacent processors do almost all the processing.

### 3.1.5 Multi-source Uniform Data Fraction

We extend the single source assignment to multi-source assignment problem [18] [21]. According to each processor, we concentrate on the processors' geographical location  $P_i$ , data fraction assigned  $\alpha_i$ .

Assume the data fraction is specially uniform. For example, the workload is unit 1 and there are  $k$  different data injection options. So each data injection is assigned  $\frac{1}{k}$  workload.

From the data injection position relationship we consider three different situations :

- Data injection positions consist of a connected subgraph  $G_L$  of  $G$ .
- Data injection processors don't connect with each other.
- Some data injection positions consist of some connected subgraphs and some are individual injection.

#### Situation I

If the data injection positions consist of a connected subgraph of  $G$ , we use  $G_L$  to present it.

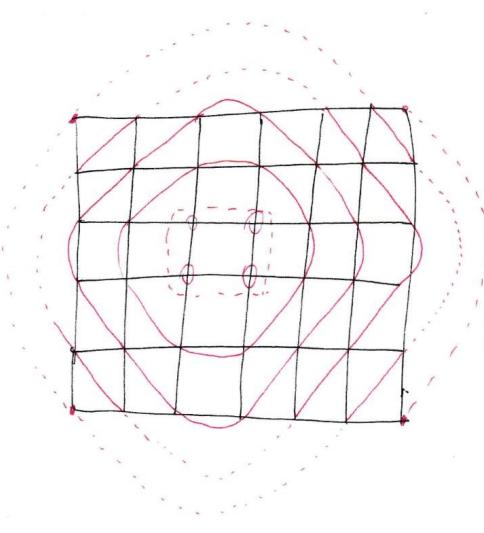


Figure 3.22: Data injection consists of a connected subgraph of  $G$

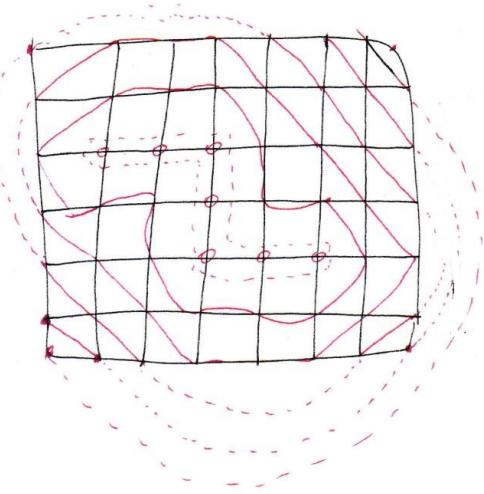


Figure 3.23: Data injection consists of a connected subgraph of  $G$

Connected subgraph Fig. 3.22 and connected subgraph Fig. 3.23 illustrate two examples that the data injections consist of connected subgraphs of  $G$ .

Our objective is to propose a general algorithm framework to tackle this situation and give quantitative model analysis. This algorithm is named as ***Equivalence Processor Scheduling Algorithm (EPSA)***.

---

**Algorithm 1** Equivalence Processor Scheduling Algorithm (EPSA)

---

**Input:**  $k$  data injection positions

**Output:**  $m * n$  processor data fractions  $\alpha_i$

Collapse the data injection processors into one “big” equivalent processor [19].

Calculate  $m * n$  processor’s  $D_i$ .

Obtain the flow matrix  $A$ .

Calculate  $m * n$  processors data fraction  $\alpha_i$ .

---

In term of the time complexity :

- The time complexity of calculating the determinant is  $O(r^3)$  with Gaussian elimination or LU decomposition.  $r$  is the rank of flow matrix and  $r$  is  $O(\max(m, n))$ .
- The time complexity of calculating the flow matrix  $A_i$  is  $O(k * m * n)$ .  
 $k$  is the number of data injection.
- The total time complexity is  $O(k * \max(m, n)^3)$ .

For example, connected subgraph Fig. 3.22's **flow matrix** is :

$$\begin{bmatrix} 4 & 8 & 12 & 10 & 6 & 2 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \alpha_4 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.90)$$

The simulation result illustrates as follows:

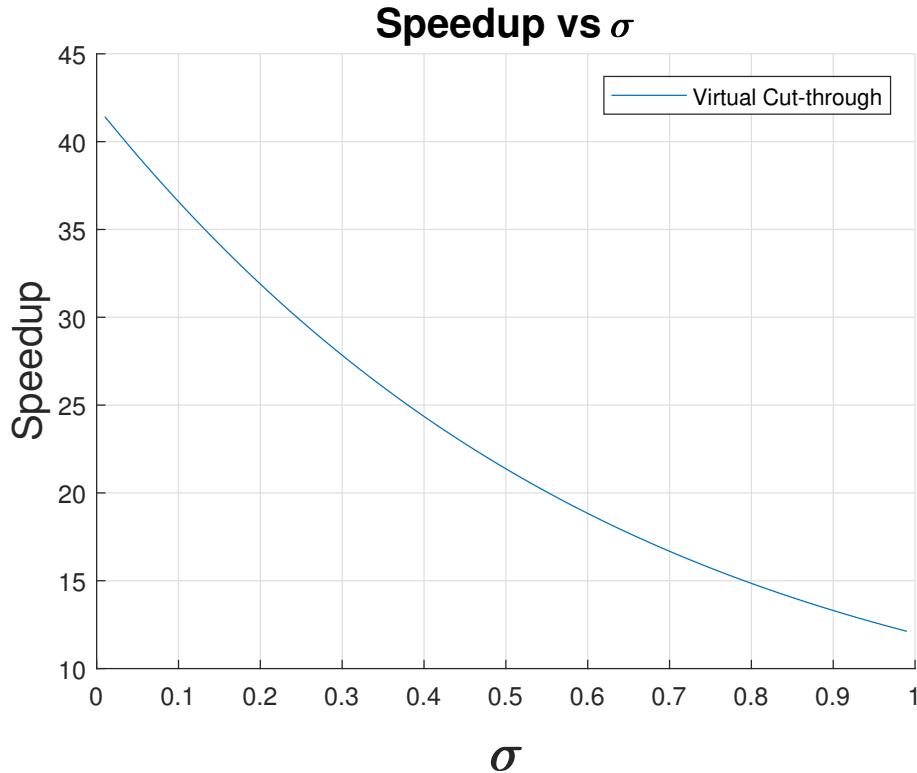


Figure 3.24: Connected subgraph Fig. 3.22 speedup vs  $\sigma$

This simulation says the best performance happens on value  $\sigma \leq 0.05$ , which hits about 42 times speedup as all 42 processors in the network are

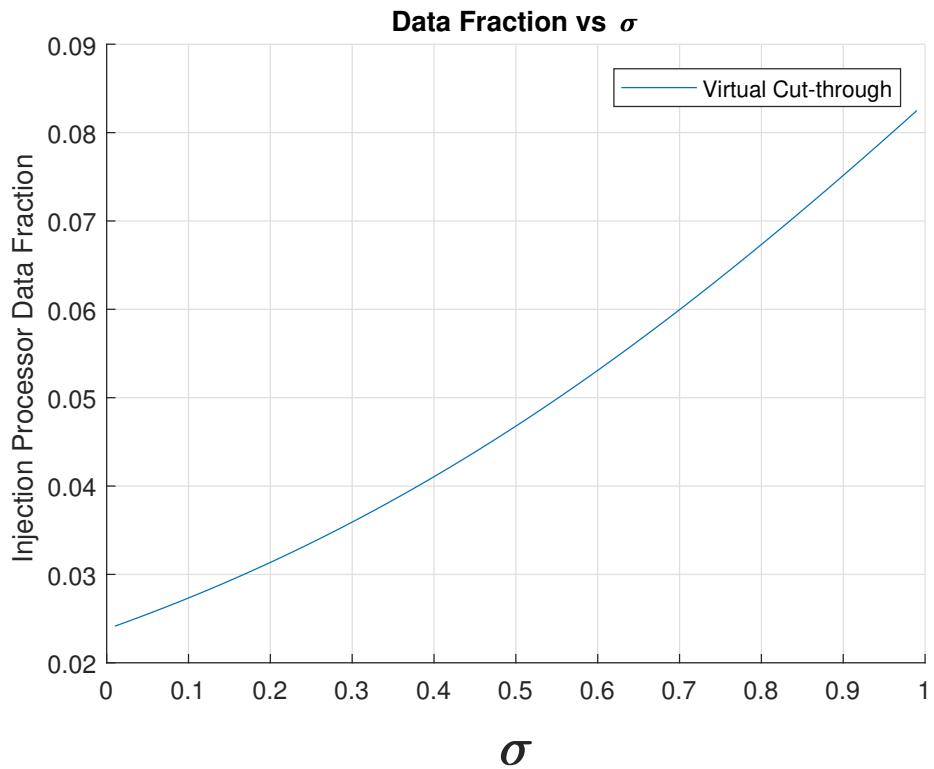


Figure 3.25: Connected subgraph Fig. 3.22's processor data fraction vs  $\sigma$

engaged in processing networks. There are 12 processors at the start stage. So if  $\sigma \approx 1$ , that is, communication time equals computation time, the network achieves about 12 times speedup performance, only those 12 processors do processing.

For example, connected subgraph Fig. 3.23's **flow matrix** is :

$$\begin{bmatrix} 7 & 14 & 15 & 10 & 6 & 3 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & 1 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \alpha_4 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.91)$$

The simulation result illustrates as follows:

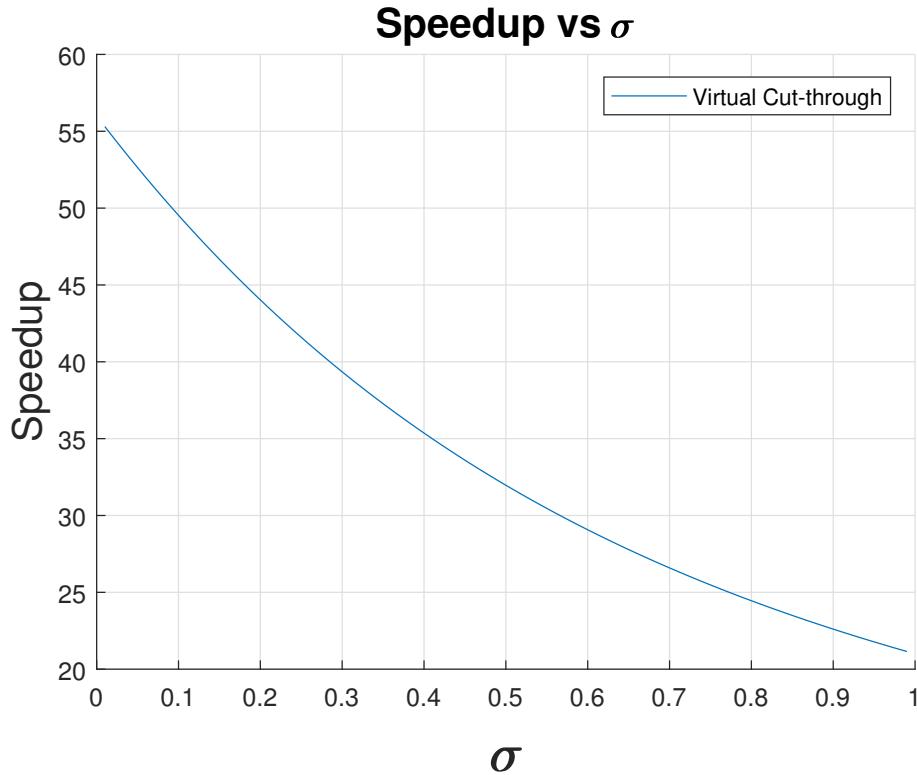


Figure 3.26: Connected subgraph Fig. 3.23 speedup vs  $\sigma$

This simulation says the best performance happens on value  $\sigma \leq 0.05$ ,

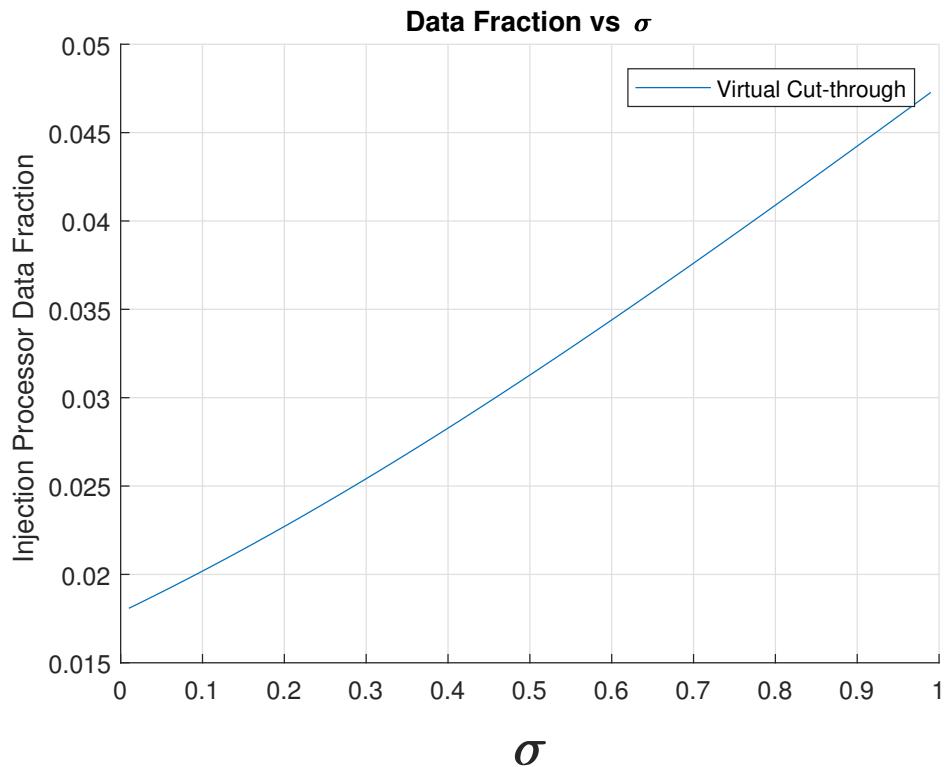


Figure 3.27: Connected subgraph Fig. 3.23's processor data fraction vs  $\sigma$

which hits about 56 times speedup as there are 56 processors engaged over the entire network. There are 21 processors in the start stage. So if  $\sigma \approx 1$ , the network achieves 21 times speedup performance as only those 21 processors do processing.

## Situation II

Now the data injections don't consist of a connected subgraph of  $G$ . Jia [26] proposes a genetic algorithm, which utilize a novel Graph Partitioning (GP) scheme to partition the network such that each source in the network gains a portion of network resources and then these sources cooperate to process their loads.

Relevant dividable load intricate applications include, for example, big file transmission, HPC scientific computation, like BlueGene [27] or Hadoop jobs.

Our objective is to propose a general algorithm framework to utilize less processors and achieve the same finish time. This is a critical issue for networks on chip (NOC) where the number of active processor is closely related to the chip power computation chip. Power computation is a limiting factor to scalability in such NOCs.

**Definition 3.1.1.** *Voronoi diagram [28]*

Let  $S$  denote a set of  $n$  points (called sites) in the plane. For two distinct sites  $p, q \in S$ , the dominance of  $p$  over  $q$  is defined as the subset of the plane being at least as close to  $p$  as to  $q$ . Formally,

$$dom(p, q) = \{x \in R^2 \mid \delta(x, p) \leq \delta(x, q)\}$$

for  $\delta$  denoting the euclidean distance function. Clearly,  $dom(p, q)$  is a closed half plane bounded by the perpendicular bisector of  $p$  and  $q$ .

This bisector separates all points of the plane closer to  $p$  from those closer to  $q$  and will be termed the separator of  $p$  and  $q$ . The region of a site  $p \in S$  is the portion of the plane lying in all of the dominances of  $p$  over the remaining sites in  $S$ . Formally,

$$reg(p) = \bigcap_{q \in S - p} dom(p, q)$$

For each seed there is a corresponding region consisting of all points closer to that seed than to any other.

**Definition 3.1.2.** *Manhattan distance Voronoi diagram* Unlike most Voronoi diagrams, which use the L2 (Euclidean distance) metric, **Manhattan distance Voronoi diagrams** use the L1 metric.

In this thesis, we utilize the Manhattan distance Voronoi diagram to implement the graph partitioning.

Manhattan distance Voronoi diagram division Fig. 3.28 shows 10 Voronoi cells division.

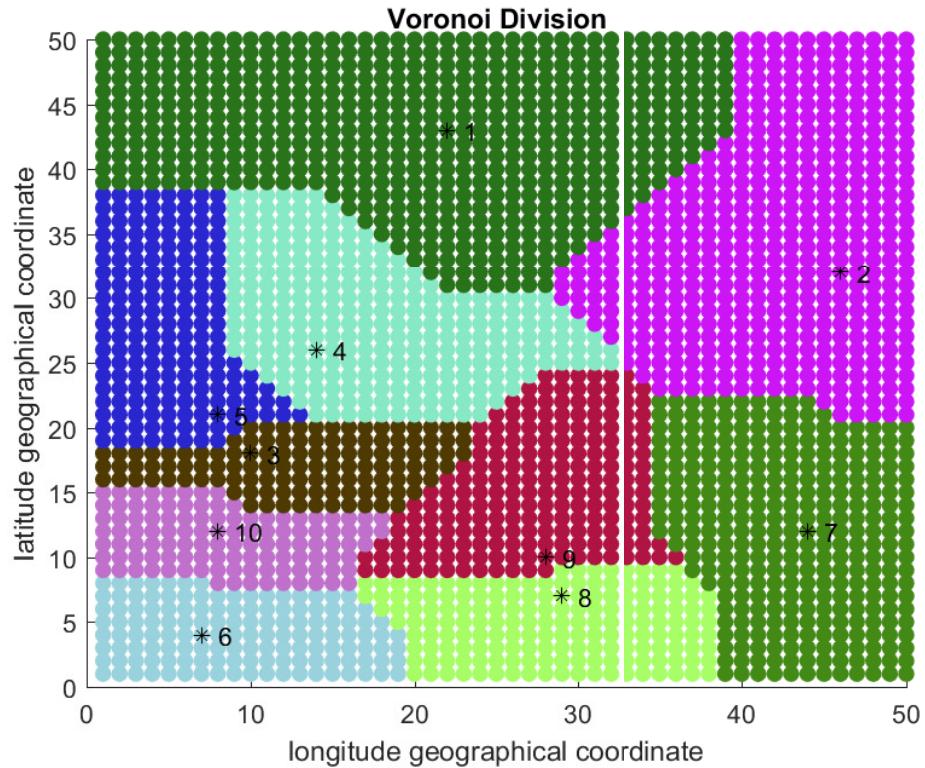


Figure 3.28: 10 Manhattan distance Voronoi Cells

Voronoi diagram division speedup curves Fig. 3.29 specifies the speedup of each cells.

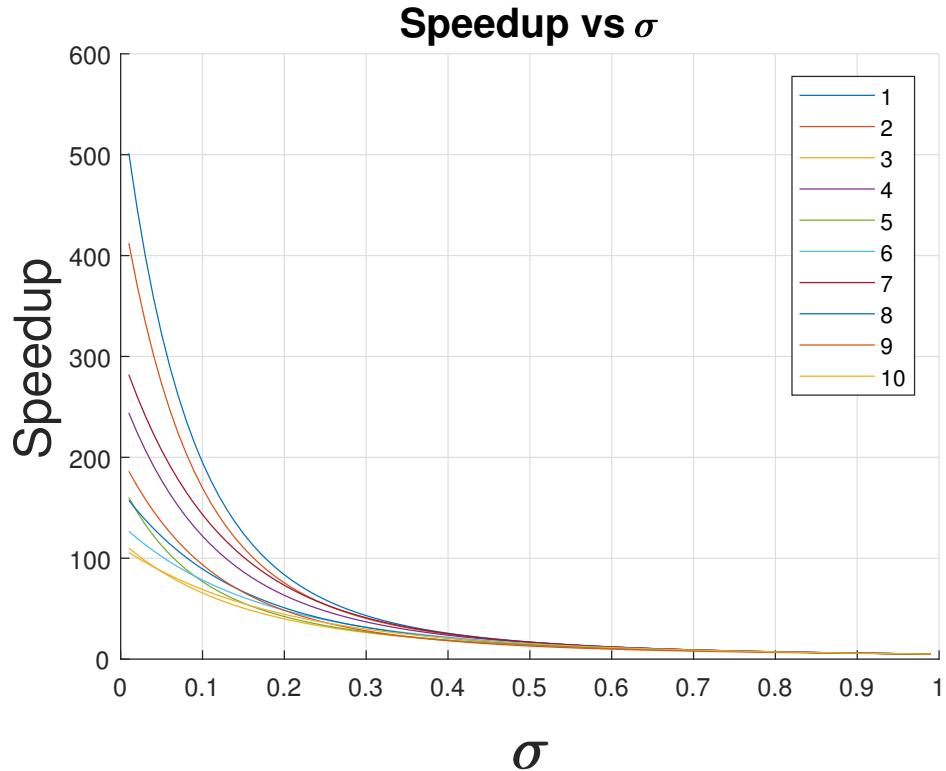


Figure 3.29: 10 Manhattan distance Voronoi Cells speedup curves

The heuristic algorithm is named as ***Reduced Manhattan distance Voronoi Diagram Algorithm***:

---

**Algorithm 2** Reduced Manhattan Distance Voronoi Diagram Algorithm (RMDVDA)

---

**Input:**  $k$  data injection positions

**Output:**  $m * n$  processor data fractions

Calculate  $k$  Voronoi cells with Manhattan distance.

Calculate  $k$  Voronoi cells' radius  $R_i$ .

Calculate  $k$  flow matrix  $A_i$ .

$depth_{min} = \min(Speedup_i)$ 's  $R_i$ .

Calculate the reduced Voronoi cells by setting the  $depth_i = depth_{min}$  in each Voronoi cell.

Calculate reduced Voronoi cell's flow matrix  $\hat{A}_i$ .

Display reduced Voronoi cells.

Illustrate reduced Voronoi cells' speedup curves.

---

In term of the time complexity :

- The time complexity of Manhattan distance Voronoi cells is  $O(k * m * n)$ ;
- The time complexity of flow matrix determinant is  $O(r^3)$ .  $r$  is the rank of flow matrix.
- So the total time complexity is  $O(k * \max(m, n)^3)$ .

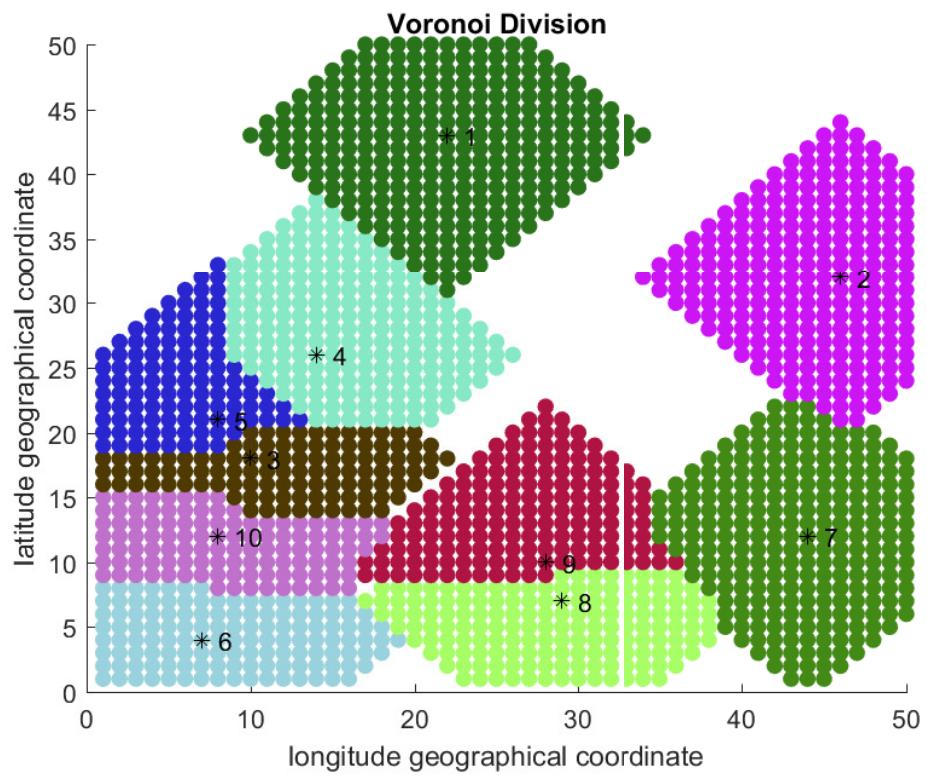


Figure 3.30: 10 reduced Voronoi cells

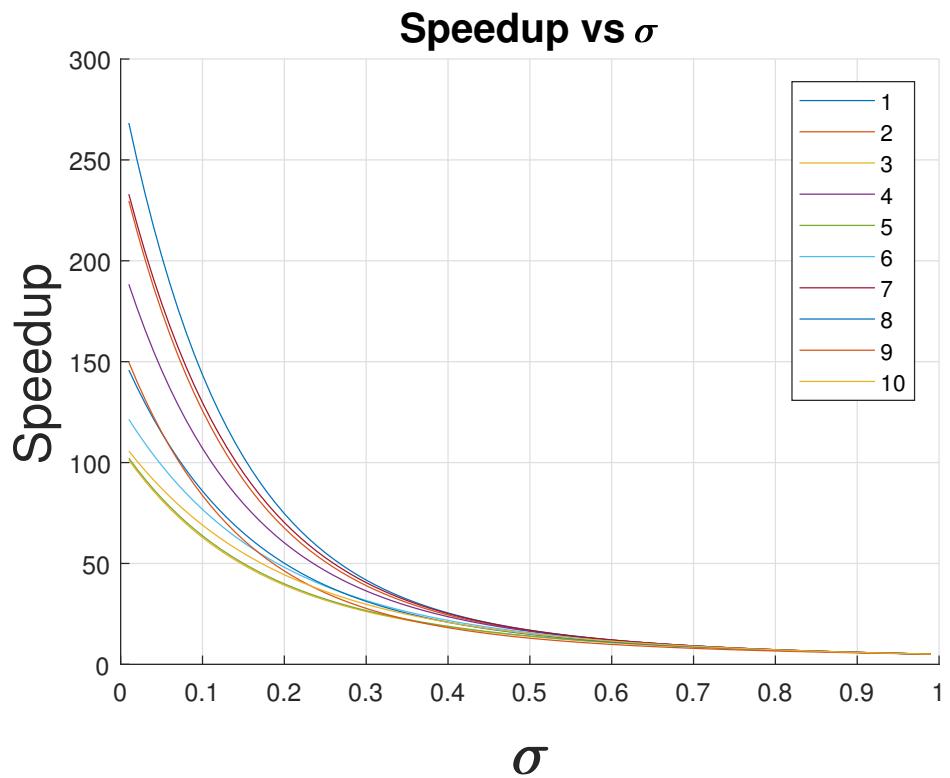


Figure 3.31: 10 reduced Voronoi cells's speedup curves

Reduced Voronoi cells Fig. 3.30 and reduced Voronoi speedup curves Fig. 3.31 show this algorithm obtains the same running time yet saves about 30% processors.

- Voronoi speedup curves Fig. 3.29 show that  $\sigma < 0.2$ , the ratio  $\max\left(\frac{\text{maxspeedup}}{\text{minspeedup}}\right) = \frac{500}{100} = 5$
- Reduced Voronoi speedup curves Fig. 3.31 show that  $\sigma < 0.2$ , the ratio is  $\max\left(\frac{\text{maxspeedup}}{\text{minspeedup}}\right) = \frac{270}{100} = 2.7$ .

It displays that 10 cell's equivalence computation is more balanced than the initial setting, and the whole cluster finishes processing load within the same time by less processors. After 1000 round random sampling experiments, we obtain the average saved processors ratio in Fig. 3.32.

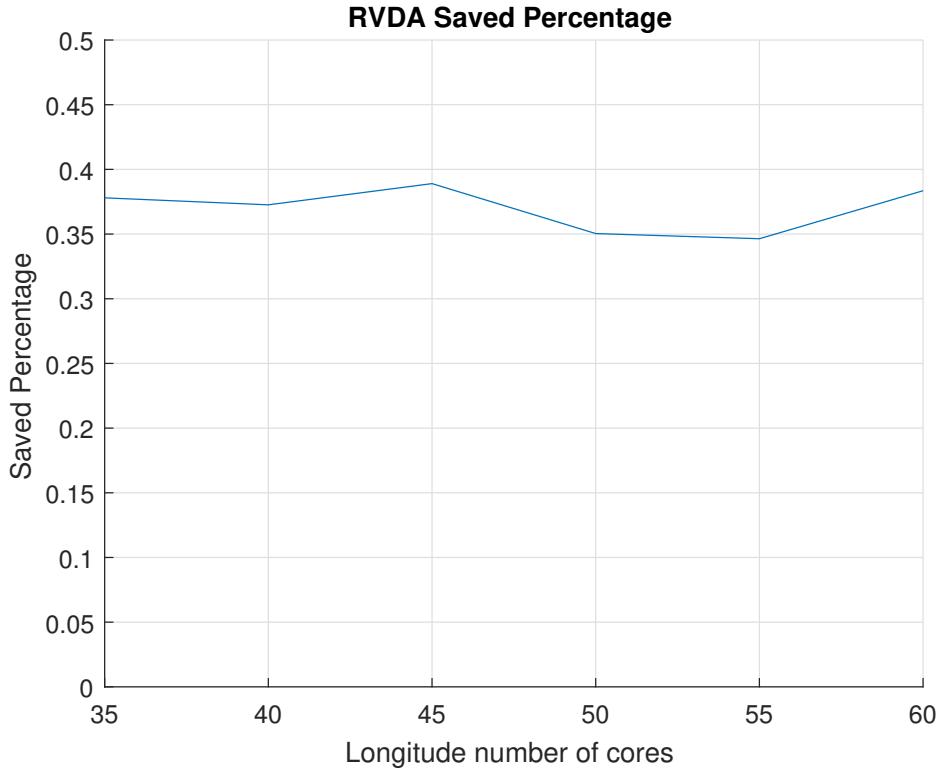


Figure 3.32: Reduced Voronoi division algorithm average saved processors' percentage

From the average saved processors ratio Fig. 3.32, it shows the average

percentage of saved processor is about 35%.

### Situation III

If there are some nodes consisting some connected subgraphs and there are some nodes individual processors, our objective to finish the load in the same time and save processors. We process an Reduced Constrained Manhattan Distance Voronoi Diagram Algorithm (RCMDVDA) to tackle this situation.

---

**Algorithm 3** Reduced Constrained Manhattan Distance Voronoi Diagram Algorithm (RCMDVDA)

---

**Input:**  $\hat{k}$  data injection positions

**Output:**  $m * n$  processor data fractions

Collapse the connected data injection processors into some “big” equivalent processors, individually.

Calculate  $k$  constrained Manhattan distance Voronoi cells [29].

Calculate  $k$  constrained Voronoi cells’ radius  $R_i$ .

Calculate  $k$  constrained Voronoi cells’ flow matrix  $A_i$ .

Calculate  $k$  constrained Voronoi cells’  $Speedup_i$ .

Set the  $depth_{min} = \min(Speedup_i)$ ’s radius.

Calculate  $k$  reduced constrained Voronoi cells by setting the  $depth_i = depth_{min}$  in each Voronoi cell.

Calculate Voronoi cell’s flow matrix  $\hat{A}_i$ .

Display reduced Voronoi cells.

Illustrate reduced Voronoi cells’ speedup curves

---

In term of the time complexity :

- The time complexity of Manhattan distance constrained Voronoi cells is  $O(k * m * n)$ .  $k$  is the number of data injection.

- The time complexity of flow matrix determinant is  $O(r^3)$ .  $r$  is the rank of flow matrix.
- So the total time complexity is  $O(k * \max(m, n)^3)$ .

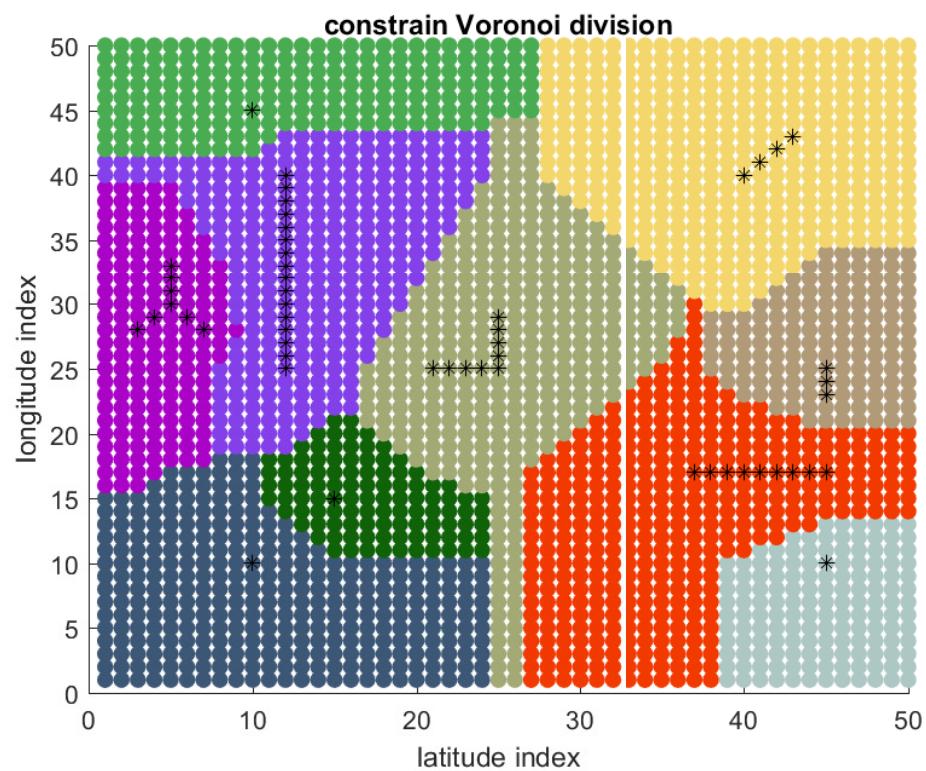


Figure 3.33: Connected subgraphs and individual data injections on mesh network

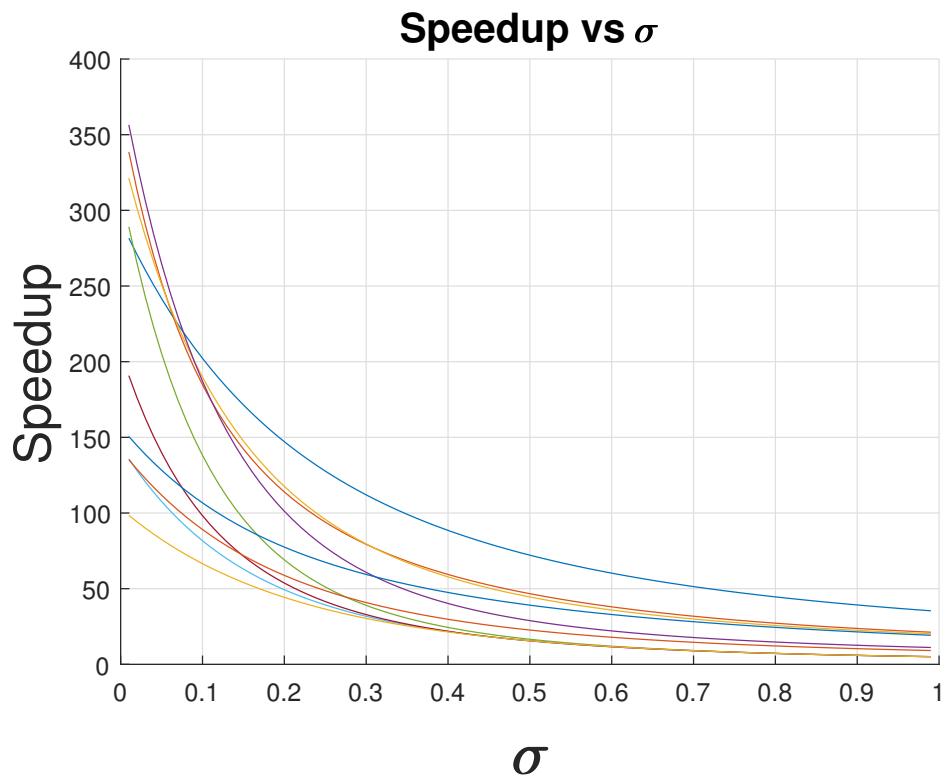


Figure 3.34: Speedup curves for Situation III

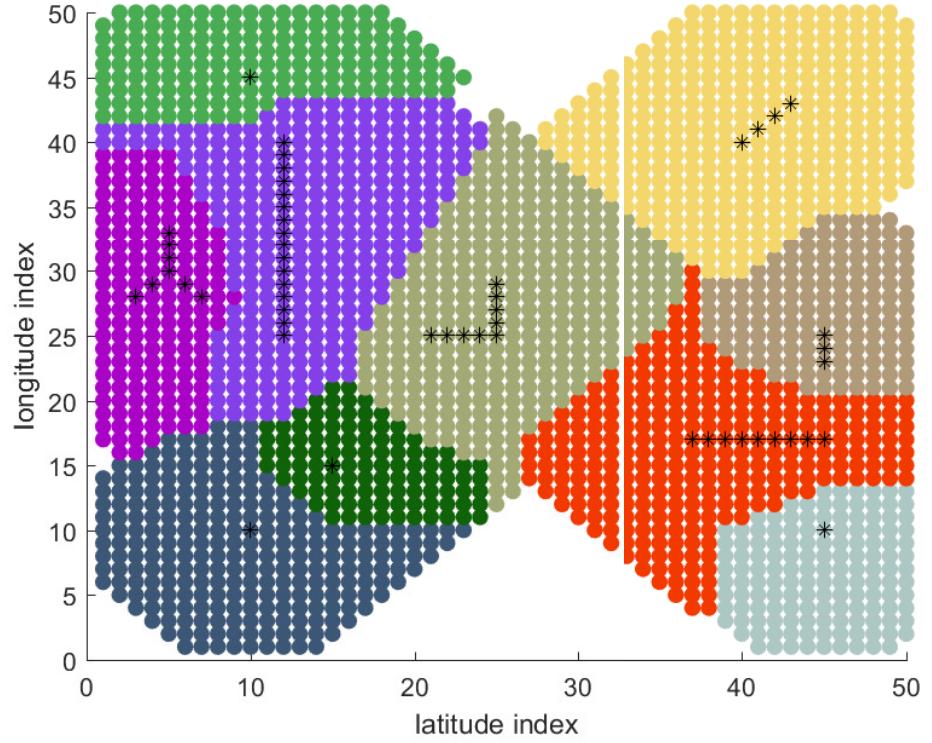


Figure 3.35: Reduced constrained Voronoi diagram for connected subgraphs and individual data injections on mesh network

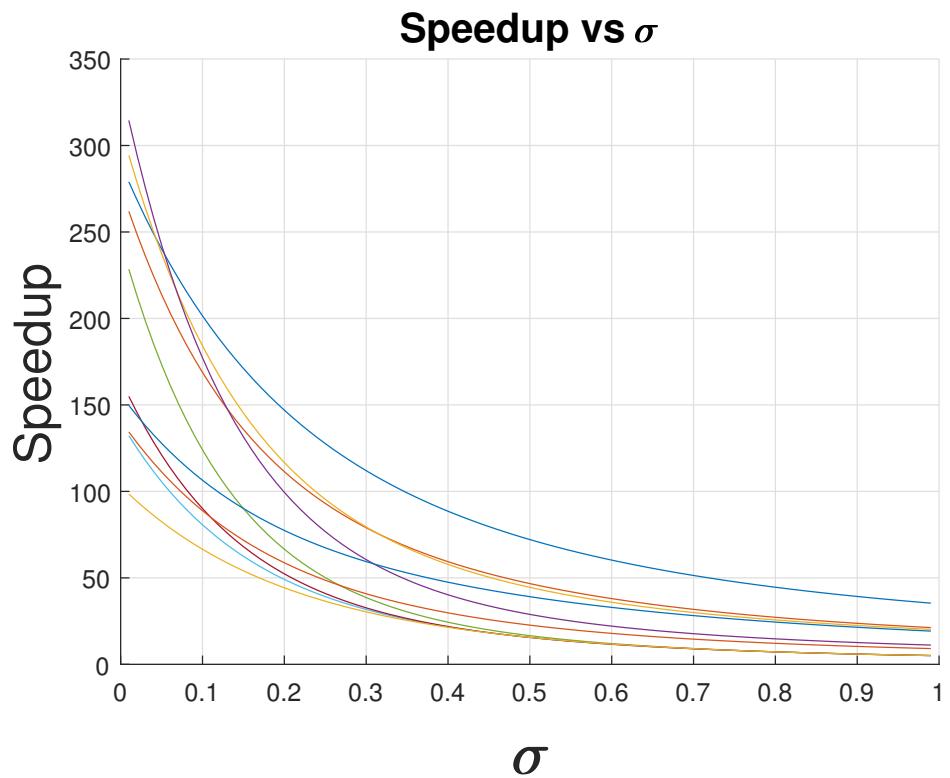


Figure 3.36: Speedup curves of connected subgraphs and individual data injection on mesh network

In this user case, we save about  $294/2500 \approx 11.7\%$  processors.

### **3.1.6 Improve the Bottleneck Voronoi Division Equivalence Computation**

From the data injection position relationship we consider two different situations :

- Data injection processors don't connect with each other.
- Some data injection positions consist of some connected subgraphs and some are individual injection.

#### **Situation I**

In order to reduce the makespan, we improve the reduced Manhattan distance Voronoi diagram algorithm to accelerate the bottleneck Voronoi division equivalence computation.

---

**Algorithm 4** Improve Bottleneck Voronoi Diagram Equivalence Computation Algorithm (IBVDECA)

---

**Input:**

- $k$  data injection positions
- $\sigma = \frac{zT_{cm}}{wT_{cp}}$
- processors and links' parameters
- $f_T$  : the requirement of finish time
- $r_{save}$  : the requirement of saved processor ratio
- $tmp_{save}$  : the ratio of saved processor in each iteration
- $Sp_i$  :  $i$  Voronoi cell's speedup ratio
- $Sp_{min} : \min(Sp_i) \quad i \in 1 \dots k$
- $i_{min}$  : the index of  $Sp_{min}$

**Output:**

- $m * n$  processor data fractions
- improved reduced Voronoi division

Calculate  $k$  Voronoi cells with Manhattan distance and  $k$  Voronoi cells' radius  $R_i$ .

Calculate  $k$  flow matrix  $A_i$  and set  $depth_{min} = \min(Sp_i)$ 's  $R_i$ .

Calculate the reduced Voronoi cells by setting the  $depth_i = depth_{min}$  in each Voronoi cell.

Calculate reduced Voronoi cell's flow matrix  $\hat{A}_i$  and  $Sp_i$  of each cell.

**while**  $\frac{1}{Sp_{min}} > f_T$  and  $tmp_{save} > r_{save}$  **do**

    merge processor to base  $i_{min}$  Voronoi cell one by one, according to  $D_i$  increasing order.

**end while**

Display reduced Voronoi cells.

Illustrate reduced Voronoi cells' speedup curves.

---

## **Situation II**

In order to reduce the makespan, we improve the reduced Manhattan distance Voronoi diagram algorithm to accelerate the bottleneck Voronoi division equivalence computation.

---

**Algorithm 5** Improve Bottleneck Voronoi Diagram Equivalence Computation

---

Algorithm 2 (IBVDECA2)

---

**Input:**

- $\hat{k}$  data injection positions
- $\sigma = \frac{zT_{cm}}{wT_{cp}}$
- processors and links' parameters
- $f_T$  : the requirement of finish time
- $r_{save}$  : the requirement of saved processor ratio
- $tmp_{save}$  : the ratio of saved processor in each iteration
- $Sp_i$  :  $i$  Voronoi cell's speedup ratio
- $Sp_{min} : \min(Sp_i) \quad i \in 1 \dots k$
- $i_{min}$  : the index of  $Sp_{min}$

**Output:**

- $m * n$  processor data fractions
- improved reduced Voronoi division

Collapse the connected data injection processors into some “big” equivalent processors, individually.

Calculate  $k$  Voronoi cells with Manhattan distance and  $k$  Voronoi cells' radius  $R_i$ .

Calculate  $k$  flow matrix  $A_i$  and set  $depth_{min} = \min(Sp_i)$ 's  $R_i$ .

Calculate the reduced Voronoi cells by setting the  $depth_i = depth_{min}$  in each Voronoi cell.

Calculate reduced Voronoi cell's flow matrix  $\hat{A}_i$  and  $Sp_i$  of each cell.

**while**  $\frac{1}{Sp_{min}} > f_T$  and  $tmp_{save} > r_{save}$  **do**

    merge processor to base  $i_{min}$  Voronoi cell one by one, according to  $D_i$  increasing order.

**end while**

Display reduced Voronoi cells.

Illustrate reduced Voronoi cells' speedup curves.

---

### 3.1.7 Multi-source Non-uniform Data Injection

From the data injection position relationship, we consider three different situations :

- Data injection positions consist of a subgraph  $G_L$  of  $G$ .
- Data injection processors don't connect with each other.
- Some data injection positions consist of some connected subgraphs and some are individual injection.

#### Situation I

We propose a suboptimal algorithm framework to address this kind of problem. The main idea is re-balancing the data fraction between the nodes in connected subgraph first. Then, run Equivalence Processor Scheduling Algorithm.

---

**Algorithm 6** Improved Equivalence Processor Scheduling Algorithm (IEPSA)

---

**Input:**  $k$  data injection positions

**Output:**  $m * n$  processor data fractions

$local_s$  :

Re-balance the connected subgraph  $G_L$  node's fraction distribution to be uniform.

$global_s$  :

Collapse the data injection processors into one “big” equivalent processor [19].

Calculate  $m * n$  processor's  $D_i$

Obtain the flow matrix  $A_i$ .

Calculate  $m * n$  processors data fraction  $\alpha_i$ .

Display reduced Voronoi cells.

Illustrate reduced Voronoi cells' speedup curves.

---

In  $local_s$  stage, our target is from a data fraction distribution to a uniform distribution and the minimum cost is called Earth Mover Distance [30].

- The time complexity of calculating Voronoi diagram is  $O(k * m * n)$ .  $k$  is the number of data injection.
- The time complexity of calculating determinant is  $O(r^3)$  with Gaussian elimination or LU decomposition.  $r$  is the rank of flow matrix.
- The total time complexity is  $O(k * \max(m, n)^3)$ .

## Situation II

We utilize the Reduced Manhattan Distance Voronoi Diagram Algorithm (RMDVDA) to address this problem.

## Situation III

---

**Algorithm 7** Improved Reduced Constrained Manhattan Distance Voronoi Diagram Algorithm (IRCMDVDA)

---

**Input:**  $\hat{k}$  data injection positions

**Output:**  $m * n$  processor data fractions

*local<sub>s</sub>* :

Collapse the connected data injection processors into some “big” equivalent processors, individually.

Redistribute the data fraction to uniform fraction within each connected subgraph processors.

*global<sub>s</sub>* :

Calculate  $k$  constrained Manhattan distance Voronoi cells [29].

Calculate  $k$  constrained Voronoi cells’ radius  $R_i$ .

Calculate  $k$  constrained Voronoi cells’ flow matrix  $A_i$ .

Calculate  $k$  constrained Voronoi cells’ *Speedup<sub>i</sub>*.

Set the  $depth_{min} = \min(Speedup_i)$ ’s radius.

Calculate the reduced constrained Voronoi cells by setting the  $depth_i = depth_{min}$  in each Voronoi cell.

Calculate Voronoi cell’s flow matrix  $\hat{A}_i$ .

Display each reduced Voronoi cells.

---

Illustrate each reduced Voronoi cells’ speedup curves

## 3.2 Store and Forward Switching Scenario

In the store and forward scenario, the processors solely start to process as soon as each processor receives its entire load assignment [31].

This subsection concerns the processors store and forward switching. Because of store and forward switching, the processors simultaneously receive the data and only start to process it as soon as each processor receives its entire load assignment.

### 3.2.1 Data Injection on The Corner Processor

#### 2\*2 Mesh Network

The timing diagram of Fig. 3.1 is shown:

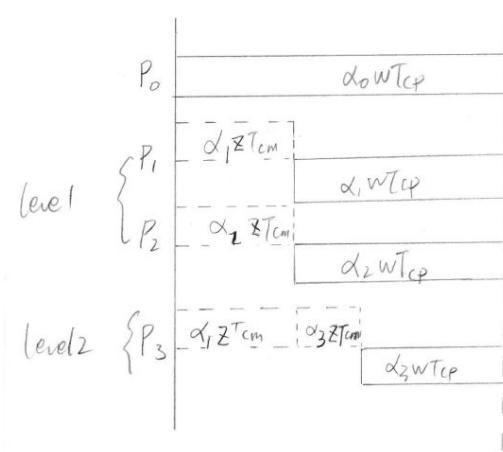


Figure 3.37: The timing diagram for 2\*2 mesh network store and forward scenario

The corresponding group of equations are as follows:

$$\left. \begin{array}{l} \alpha_0 \omega T_{cp} = T_{f,m} \\ \alpha_1 z T_{cm} + \alpha_1 \omega T_{cp} = T_{f,m} \\ \alpha_2 z T_{cm} + \alpha_2 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_3) z T_{cm} + \alpha_3 \omega T_{cp} = T_{f,m} \\ \sigma = \frac{z T_{cm}}{\omega T_{cp}} \\ \alpha_0 + \alpha_1 + \alpha_2 + \alpha_3 = 1 \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1, \alpha_2, \alpha_3 < 1 \end{array} \right\} \quad (3.92)$$

$$\alpha_1 z T_{cm} + \alpha_1 \omega T_{cp} = T_{f,m} \quad (3.93)$$

$$\alpha_2 z T_{cm} + \alpha_2 \omega T_{cp} = T_{f,m} \quad (3.94)$$

$$(\alpha_1 + \alpha_3) z T_{cm} + \alpha_3 \omega T_{cp} = T_{f,m} \quad (3.95)$$

$$\sigma = \frac{z T_{cm}}{\omega T_{cp}} \quad (3.96)$$

$$\alpha_0 + \alpha_1 + \alpha_2 + \alpha_3 = 1 \quad (3.97)$$

$$0 < \sigma < 1 \quad (3.98)$$

$$0 < \alpha_0 \leq 1 \quad (3.99)$$

$$0 \leq \alpha_1, \alpha_2, \alpha_3 < 1 \quad (3.100)$$

The matrix closed-form is presented as:

$$\begin{bmatrix} 1 & 2 & 1 \\ 1 & -(\sigma+1) & 0 \\ 1 & -\sigma & -(\sigma+1) \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_3 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \quad (3.101)$$

The explicit solution is:

$$\alpha_0 = \left( \frac{\sigma+1}{\sigma+2} \right)^2 \quad (3.102)$$

$$\alpha_1 = \frac{\sigma+1}{(\sigma+2)^2} \quad (3.103)$$

$$\alpha_3 = \frac{1}{(\sigma+2)^2} \quad (3.104)$$

The simulation result for Fig. 3.1 is provided in Fig. 3.38:

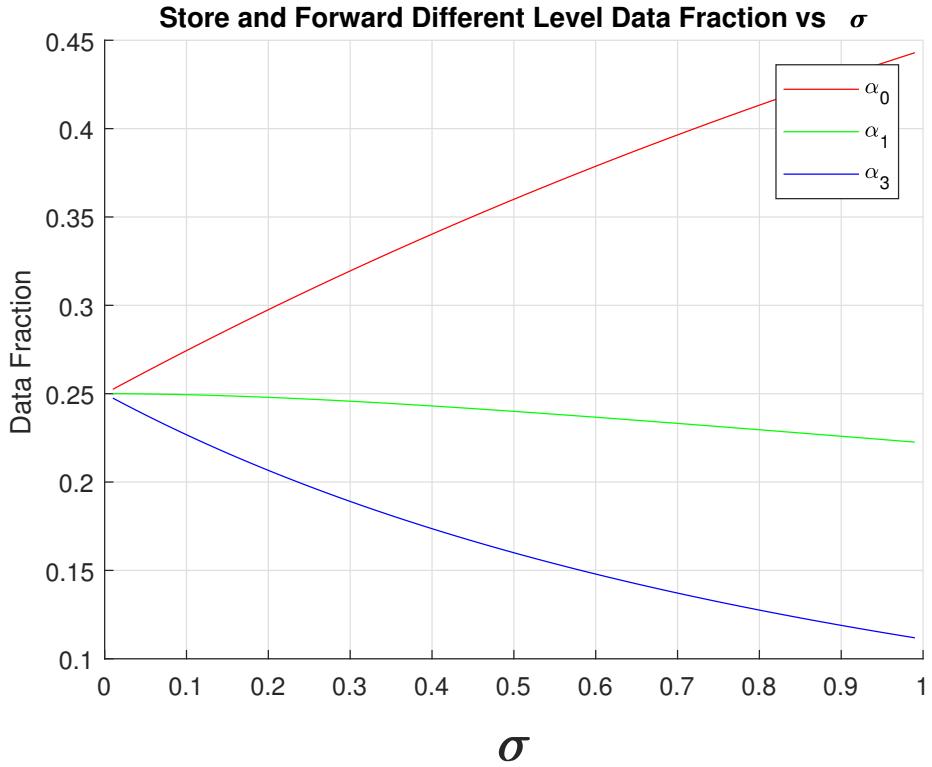


Figure 3.38: Data fraction curves of mesh network  $2 * 2$  vs  $\sigma$

A  $2*2$  mesh network Fig. 3.1's data fraction curves Fig. 3.38 explains that as the value  $\sigma$  increases, the fraction assigned to  $P_0$  increases, the fractions distributed to  $level_1$  and  $level_2$  reduces. In other words, if the communication capability decreases, there are more data processed locally, which is reasonable. If the ability of the link decreases, asymptotically equaling to the processor computation capacity, there is only 11% data is deployed to the  $level_2$ . In addition, if the  $\sigma > 1$ , it means that the transmitting time is greater than the processor's processing time. In this scenario, keeping the data locally is more economical than transmitting it. If  $\sigma$  is small (fast communication), all  $\sigma$  is equal, that is, all four processors are engaged in processing equally.

## 2\*3 Mesh Network

$P_0$  starts to process the assigned workload and it starts to transfer the data.  $P_1$  and  $P_2$  are idle until they get their data fraction from  $P_0$  through the link 0 – 1 and 0 – 2.

According to the  $level_2$ , the similar situation happens to  $P_3$  and  $P_4$ . They both start to transmit the  $\alpha_5$  after they totally receive the appropriate workload. In other words,  $P_5$  has to wait until the previous two layers processors obtain their own data.

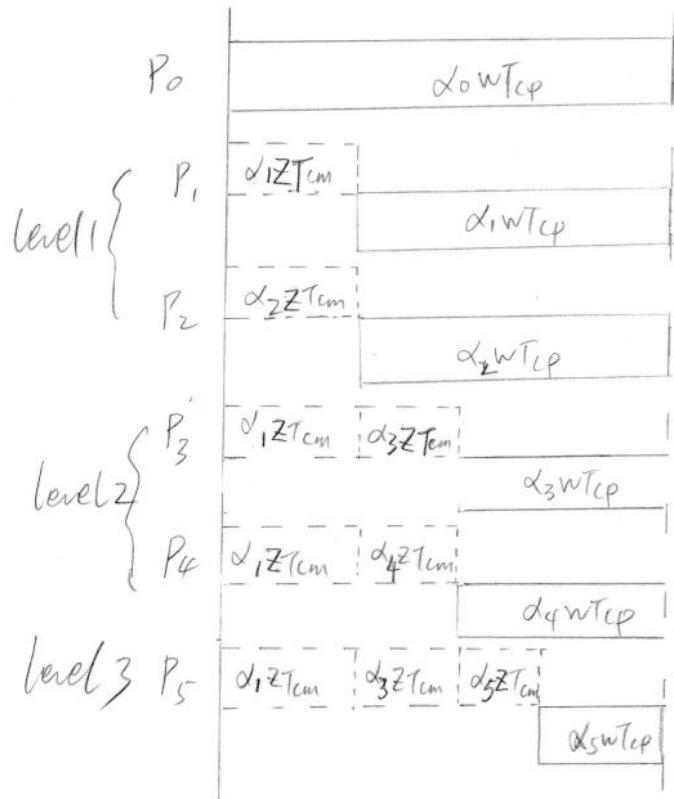


Figure 3.39: The timing diagram for store and forward switching 2\*3 mesh network.

In addition, the group of equations are as follows:

$$\left\{ \begin{array}{l} \alpha_0 \omega T_{cp} = T_{f,m} \\ \alpha_1 z T_{cm} + \alpha_1 \omega T_{cp} = T_{f,m} \\ \alpha_2 z T_{cm} + \alpha_2 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_3) z T_{cm} + \alpha_3 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_4) z T_{cm} + \alpha_4 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_3 + \alpha_5) z T_{cm} + \alpha_5 \omega T_{cp} = T_{f,m} \\ \sigma = \frac{z T_{cm}}{\omega T_{cp}} \\ \alpha_0 + \alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 + \alpha_5 = 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1 \quad \alpha_2 \quad \alpha_3 \quad \alpha_4 \quad \alpha_5 < 1 \end{array} \right. \begin{array}{l} (3.105) \\ (3.106) \\ (3.107) \\ (3.108) \\ (3.109) \\ (3.110) \\ (3.111) \\ (3.112) \\ (3.113) \\ (3.114) \end{array}$$

The flow matrix is :

$$\begin{bmatrix} 1 & 2 & 2 & 1 \\ 1 & -(\sigma + 1) & 0 & 0 \\ 1 & -\sigma & -(\sigma + 1) & 0 \\ 1 & -\sigma & -\sigma & -(\sigma + 1) \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_3 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.115)$$

The speedup is

$$Speedup = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0}$$

The explicit solution is:

$$\left\{ \begin{array}{l} \alpha_0 = \left( \frac{\sigma + 1}{\sigma + 2} \right)^3 \\ \alpha_1 = \frac{(\sigma + 1)^2}{(\sigma + 2)^3} \end{array} \right. \quad (3.116)$$

$$\left\{ \begin{array}{l} \alpha_3 = \frac{\sigma + 1}{(\sigma + 2)^3} \\ \alpha_5 = \frac{1}{(\sigma + 2)^3} \end{array} \right. \quad (3.117)$$

$$\left\{ \begin{array}{l} \alpha_3 = \frac{\sigma + 1}{(\sigma + 2)^3} \\ \alpha_5 = \frac{1}{(\sigma + 2)^3} \end{array} \right. \quad (3.118)$$

$$\left\{ \begin{array}{l} \alpha_3 = \frac{\sigma + 1}{(\sigma + 2)^3} \\ \alpha_5 = \frac{1}{(\sigma + 2)^3} \end{array} \right. \quad (3.119)$$

The simulation result is:

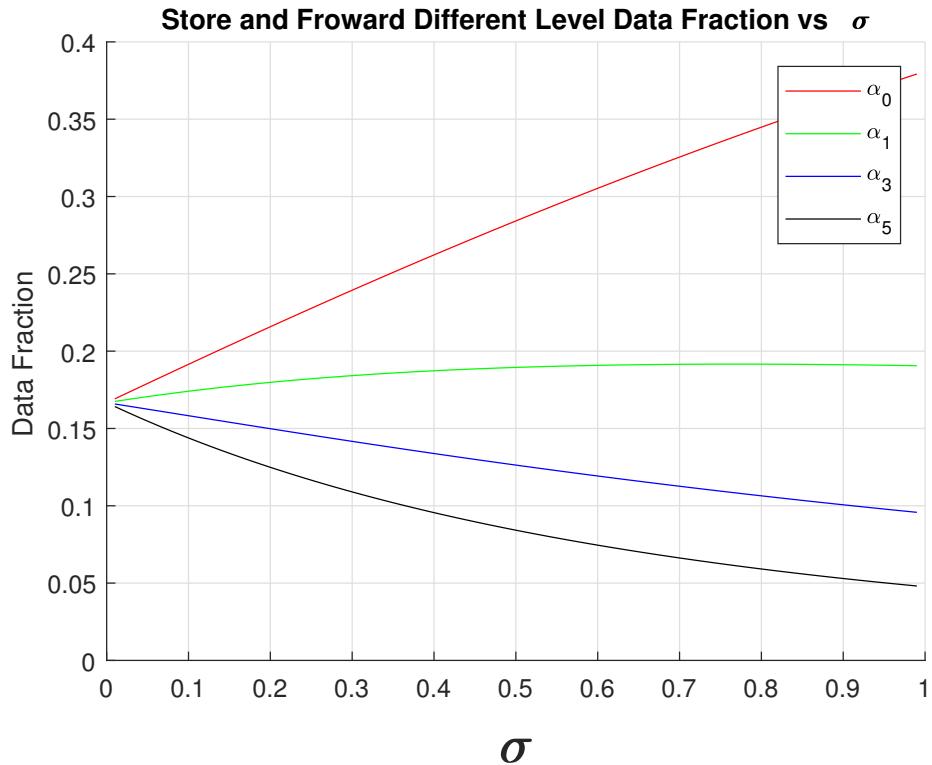


Figure 3.40: Data fraction curves of mesh network  $2 * 3$  vs  $\sigma$

If  $\sigma$  is small (fast communication), each of six processor gets  $\frac{1}{6}$  of the

load.

## 2\*n Mesh Network

Considering a  $2 * 10$  mesh network Fig. 3.7, the equations are demonstrated as follows:

$$\left\{ \begin{array}{l} \alpha_0 \omega T_{cp} = T_{f,m} \\ \alpha_1 z T_{cm} + \alpha_1 \omega T_{cp} = T_{f,m} \\ \alpha_2 z T_{cm} + \alpha_2 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_3) z T_{cm} + \alpha_3 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_4) z T_{cm} + \alpha_4 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_3 + \alpha_5) z T_{cm} + \alpha_5 \omega T_{cp} = T_{f,m} \\ \vdots \\ (\alpha_1 + \alpha_3 + \cdots + \alpha_{2 \times n-1}) z T_{cm} + \alpha_{2 \times n-1} \omega T_{cp} = T_{f,m} \\ \sigma = \frac{z T_{cm}}{\omega T_{cp}} \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1 \alpha_3 \cdots \alpha_{2 \times n-1} < 1 \end{array} \right. \begin{array}{l} (3.120) \\ (3.121) \\ (3.122) \\ (3.123) \\ (3.124) \\ (3.125) \\ (3.126) \\ (3.127) \\ (3.128) \\ (3.129) \\ (3.130) \\ (3.131) \end{array}$$

Utilize  $\sigma^*$  to present  $-(\sigma+1)$  and then the flow matrix form for the group of equations is :

$$\begin{bmatrix} 1 & 2 & 2 & \cdots & 2 & 2 & 1 \\ 1 & \sigma^* & 0 & \cdots & 0 & 0 & 0 \\ 1 & -\sigma & \sigma^* & \cdots & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & \sigma^* & 0 & \cdots & 0 \\ 1 & -\sigma & -\sigma & -\sigma & \sigma^* & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \\ 1 & -\sigma & -\sigma & \cdots & -\sigma & -\sigma & \sigma^* \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_3 \\ \alpha_5 \\ \vdots \\ \alpha_{2 \times n-3} \\ \alpha_{2 \times n-1} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad (3.132)$$

According to the **Cramer's rule**, the explicit solution for the group of equations is:

$$\left\{ \alpha_i = \left| \frac{\det A_i^*}{\det A} \right| \right. \quad (3.133)$$

where  $A_i^*$  is the matrix formed by replacing the  $i$ -th column of  $A$  by the column vector  $b$ .

We use  $-\sigma - 2 = \epsilon$  and  $\sigma^* - 2 = \beta$ .

After a series of column reduction and row reduction, the flow matrix changes as follows :

$$A = \begin{bmatrix} 1 & 2 & 2 & \cdots & 2 & 2 & 1 \\ 1 & \sigma^* & 0 & 0 & 0 & 0 & 0 \\ 1 & -\sigma & \sigma^* & 0 & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & \sigma^* & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma & \sigma^* & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* & 0 \\ 1 & -\sigma & -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* \end{bmatrix} \xrightarrow{\substack{\text{Column} \\ \text{Reduction}}} \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 & 0 \\ 1 & \beta & -2 & \cdots & -2 & -2 & -1 \\ 1 & \epsilon & \beta & \cdots & 0 & 0 & 0 \\ 1 & \epsilon & \epsilon & \beta & 0 & \cdots & 0 \\ 1 & \epsilon & \epsilon & \epsilon & \beta & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \ddots \\ 1 & \epsilon & \epsilon & \cdots & \epsilon & \epsilon & \beta \end{bmatrix}$$
  

$$\xrightarrow{\substack{\text{Row} \\ \text{Reduction}}} \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 & 0 \\ 0 & \beta & -2 & \cdots & -2 & -2 & -1 \\ 0 & \epsilon & \beta & \cdots & 0 & 0 & 0 \\ 0 & \epsilon & \epsilon & \beta & 0 & \cdots & 0 \\ 0 & \epsilon & \epsilon & \epsilon & \beta & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \ddots \\ 0 & \epsilon & \epsilon & \cdots & \epsilon & \epsilon & \beta \end{bmatrix}$$

We define

$$C = \begin{bmatrix} \sigma^* & 0 & 0 & 0 & 0 & 0 \\ -\sigma & \sigma^* & 0 & 0 & 0 & 0 \\ -\sigma & -\sigma & \sigma^* & 0 & 0 & 0 \\ -\sigma & -\sigma & -\sigma & \sigma^* & 0 & 0 \\ -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* & 0 \\ -\sigma & -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* \end{bmatrix}$$

$0 < \sigma < 1$ , then  $-2 < \sigma^* < -1$ , which means  $C$  is column linear

independent, after column and row reduction.

Further, we define

$$\hat{C} = \begin{bmatrix} \beta & -2 & \cdots & -2 & -2 & -1 \\ \epsilon & \beta & \cdots & 0 & 0 & 0 \\ \epsilon & \epsilon & \beta & 0 & \cdots & 0 \\ \epsilon & \epsilon & \epsilon & \beta & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots \\ \epsilon & \epsilon & \cdots & \epsilon & \epsilon & \beta \end{bmatrix}$$

$\hat{C}$  is also full rank.

So the flow matrix  $A$  is full rank, that is,  $\det A \neq 0$  and  $\det A^* \neq 0$ . The speedup is

$$Speedup = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0} = \frac{\det A}{\det A^*} = \left| \frac{\det A}{(\sigma^*)^{n-1}} \right|$$

## **m\*n Mesh Network**

Referring to a  $5 * 5$  mesh network Fig. 2.1, we utilize  $\sigma^*$  to present the  $-(\sigma + 1)$ .

The flow matrix closed-form is:

$$\begin{bmatrix} 1 & 2 & 3 & 4 & 5 & 4 & 3 & 2 & 1 \\ 1 & \sigma^* & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -\sigma & \sigma^* & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & \sigma^* & 0 & 0 & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma & \sigma^* & 0 & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* & 0 \\ 1 & -\sigma & \sigma^* \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_3 \\ \alpha_6 \\ \alpha_{10} \\ \alpha_{15} \\ \alpha_{19} \\ \alpha_{22} \\ \alpha_{24} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.134)$$

### 3.2.2 Data Injection on The Boundary Processor

A  $3 \times 3$  mesh network Fig. 3.10 shows an example of boundary processor  $P_0$  receiving  $L$ .

The timing diagram for Fig. 3.10 is Fig. 3.41.

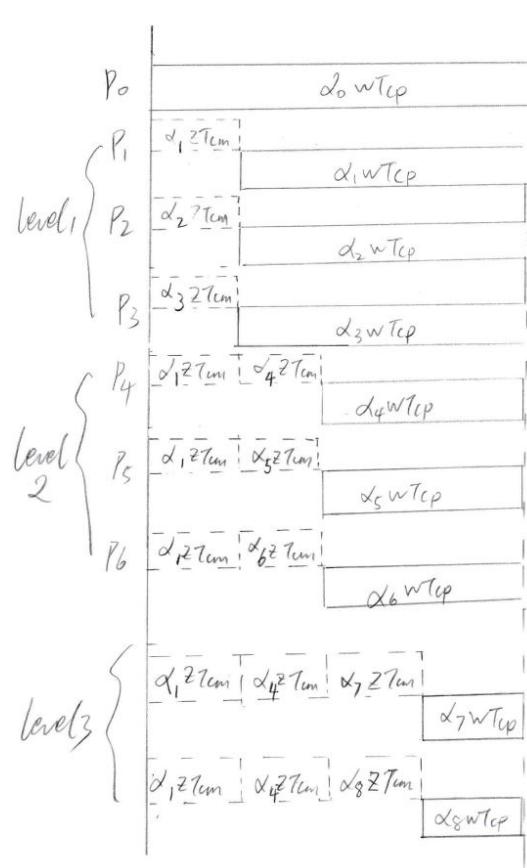


Figure 3.41: The timing diagram for  $3 \times 3$  boundary data injection on  $P_0$

The equations are:

$$\left\{ \begin{array}{l} \alpha_0 \omega T_{cp} = T_{f,m} \\ \alpha_1 z T_{cm} + \alpha_1 \omega T_{cp} = T_{f,m} \\ \alpha_2 z T_{cm} + \alpha_2 \omega T_{cp} = T_{f,m} \\ \alpha_3 z T_{cm} + \alpha_3 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_4) z T_{cm} + \alpha_4 \omega T_{cp} = T_{f,m} \\ (\alpha_2 + \alpha_5) z T_{cm} + \alpha_5 \omega T_{cp} = T_{f,m} \\ (\alpha_3 + \alpha_6) z T_{cm} + \alpha_6 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_4 + \alpha_7) z T_{cm} + \alpha_7 \omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_4 + \alpha_8) z T_{cm} + \alpha_8 \omega T_{cp} = T_{f,m} \\ \sigma = \frac{z T_{cm}}{\omega T_{cp}} \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1 \alpha_3 \alpha_4 \alpha_5 \alpha_6 \alpha_7 \alpha_8 < 1 \end{array} \right. \quad \begin{array}{l} (3.135) \\ (3.136) \\ (3.137) \\ (3.138) \\ (3.139) \\ (3.140) \\ (3.141) \\ (3.142) \\ (3.143) \\ (3.144) \\ (3.145) \\ (3.146) \\ (3.147) \end{array}$$

The flow matrix is :

$$\begin{bmatrix} 1 & 3 & 3 & 2 \\ 1 & -(\sigma + 1) & 0 & 0 \\ 1 & -\sigma & -(\sigma + 1) & 0 \\ 1 & -\sigma & -\sigma & -(\sigma + 1) \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_4 \\ \alpha_7 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.148)$$

The simulation result is shown in :

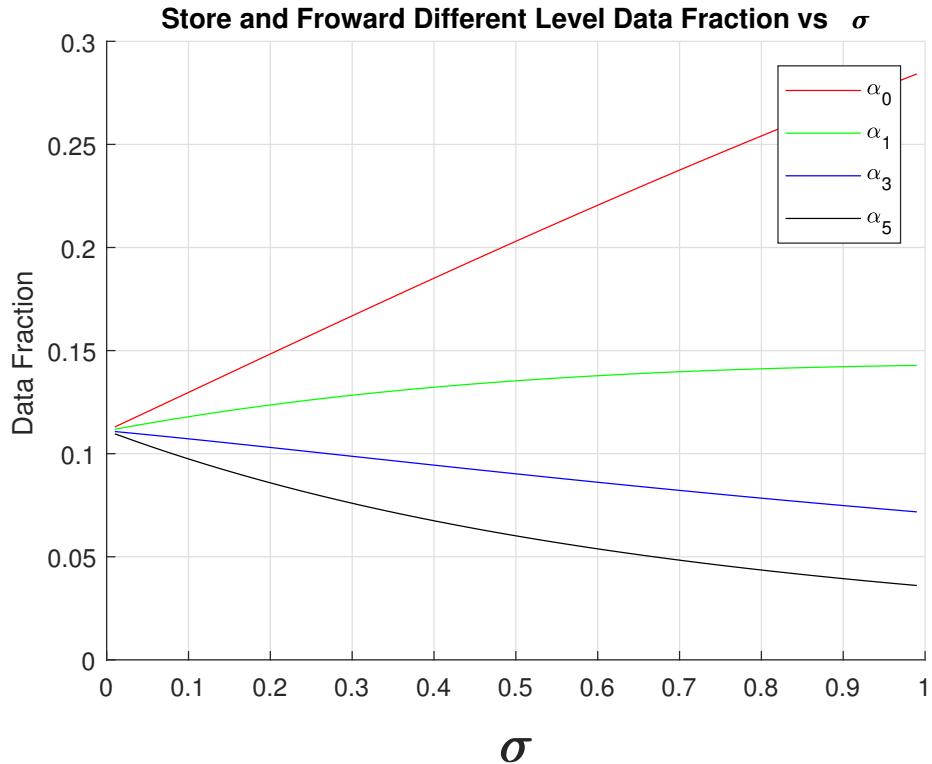


Figure 3.42: The fraction curve for  $3 \times 3$  boundary data injection on  $P_0$

A  $3 \times 3$  mesh network Fig. 3.10's data fraction curves Fig. 3.42 shows that as the value  $\sigma$  increases, the fraction assigned to  $P_0$  increases and the fractions distributed to  $level_2$  and  $level_3$  decreases. In other words, if the communication capability decreases, there are more data processed locally, which is reasonable.

If the ability of the link degrades, asymptotically equaling to the processor computation capacity, there is solely 4% data is deployed to the  $level_3$ . In addition, if the  $\sigma > 1$ , it means that the transmitting time is greater than the processor's processing time. In this scenario, keeping the data locally is more economical than transmitting it.

### 3.2.3 Data Injection on The Inner Grid Processor

The mesh network considered is  $3 * 3$ .

The equations are:

$$\left. \begin{array}{l} \alpha_0\omega T_{cp} = T_{f,m} \\ \alpha_1zT_{cm} + \alpha_1\omega T_{cp} = T_{f,m} \\ \alpha_2zT_{cm} + \alpha_2\omega T_{cp} = T_{f,m} \\ \alpha_3zT_{cm} + \alpha_3\omega T_{cp} = T_{f,m} \\ \alpha_4zT_{cm} + \alpha_4\omega T_{cp} = T_{f,m} \\ (\alpha_1 + \alpha_5)zT_{cm} + \alpha_5\omega T_{cp} = T_{f,m} \\ (\alpha_2 + \alpha_6)zT_{cm} + \alpha_6\omega T_{cp} = T_{f,m} \\ (\alpha_3 + \alpha_7)zT_{cm} + \alpha_7\omega T_{cp} = T_{f,m} \\ (\alpha_4 + \alpha_8)zT_{cm} + \alpha_8\omega T_{cp} = T_{f,m} \\ \sigma = \frac{zT_{cm}}{\omega T_{cp}} \\ 0 < \sigma < 1 \\ 0 < \alpha_0 \leq 1 \\ 0 \leq \alpha_1 \quad \alpha_3 \quad \alpha_4 \quad \alpha_5 \quad \alpha_6 \quad \alpha_7 \quad \alpha_8 < 1 \end{array} \right\} \quad (3.149)$$

$$\alpha_1zT_{cm} + \alpha_1\omega T_{cp} = T_{f,m} \quad (3.150)$$

$$\alpha_2zT_{cm} + \alpha_2\omega T_{cp} = T_{f,m} \quad (3.151)$$

$$\alpha_3zT_{cm} + \alpha_3\omega T_{cp} = T_{f,m} \quad (3.152)$$

$$\alpha_4zT_{cm} + \alpha_4\omega T_{cp} = T_{f,m} \quad (3.153)$$

$$(\alpha_1 + \alpha_5)zT_{cm} + \alpha_5\omega T_{cp} = T_{f,m} \quad (3.154)$$

$$(\alpha_2 + \alpha_6)zT_{cm} + \alpha_6\omega T_{cp} = T_{f,m} \quad (3.155)$$

$$(\alpha_3 + \alpha_7)zT_{cm} + \alpha_7\omega T_{cp} = T_{f,m} \quad (3.156)$$

$$(\alpha_4 + \alpha_8)zT_{cm} + \alpha_8\omega T_{cp} = T_{f,m} \quad (3.157)$$

$$\sigma = \frac{zT_{cm}}{\omega T_{cp}} \quad (3.158)$$

$$0 < \sigma < 1 \quad (3.159)$$

$$0 < \alpha_0 \leq 1 \quad (3.160)$$

$$0 \leq \alpha_1 \quad \alpha_3 \quad \alpha_4 \quad \alpha_5 \quad \alpha_6 \quad \alpha_7 \quad \alpha_8 < 1 \quad (3.161)$$

The flow matrix closed-form is:

$$\begin{bmatrix} 1 & 4 & 4 \\ 1 & -(\sigma + 1) & 0 \\ 1 & -\sigma & -(\sigma + 1) \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \quad (3.162)$$

The simulation result shows:

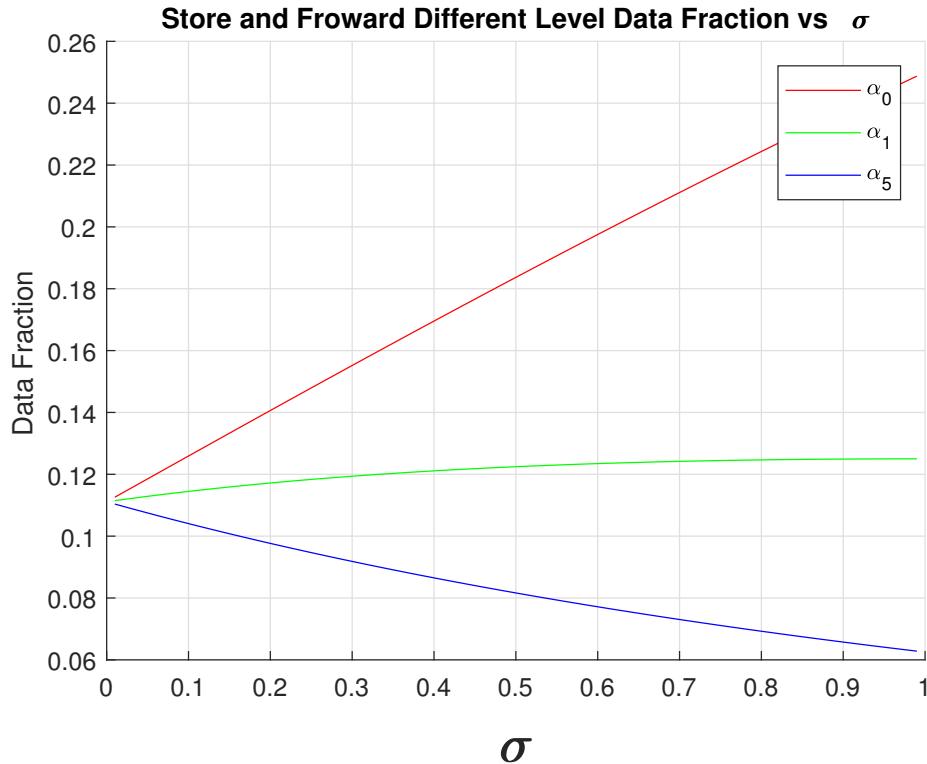


Figure 3.43: The timing diagram for  $3 \times 3$  inner grid injection  $P_0$

A  $3 \times 3$  mesh network Fig. 3.13's data fraction curves Fig. 3.43 illustrates that as the value  $\sigma$  increases, the fraction assigned to  $P_0$  increases and the fractions distributed to  $level_2$  reduces. In other words, if the communication capability decreases, there are more data processed locally, which is reasonable.

If the ability of the link degrades, asymptotically equaling to the processor computation capacity, there is only 6% data is deployed to the  $level_2$ .

If  $\sigma$  is very small (fast communication), each of nine processors process  $\frac{1}{9}$  of the load

### 3.2.4 Sensitivity Analysis Store and Forward Scenario

#### Data Injection on The Corner Processor

The simulation result of sensitivity analysis of  $2*n$  mesh network Fig. 3.7 is as follows:

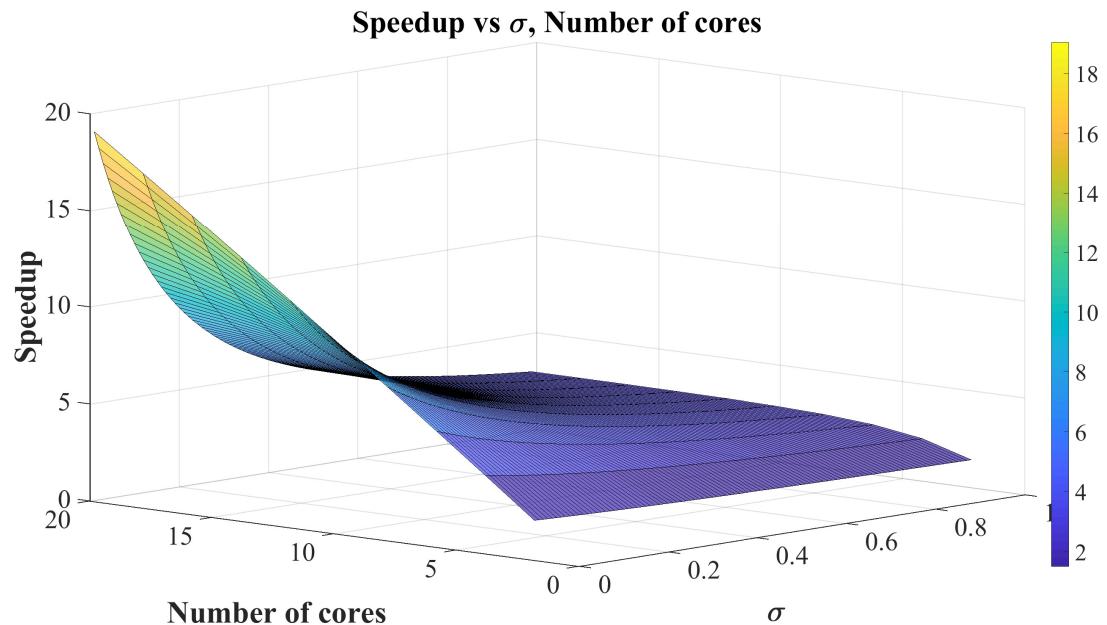


Figure 3.44: Sensitivity analysis result of  $2*n$  mesh network result ( $n = 1 \dots 10$ )

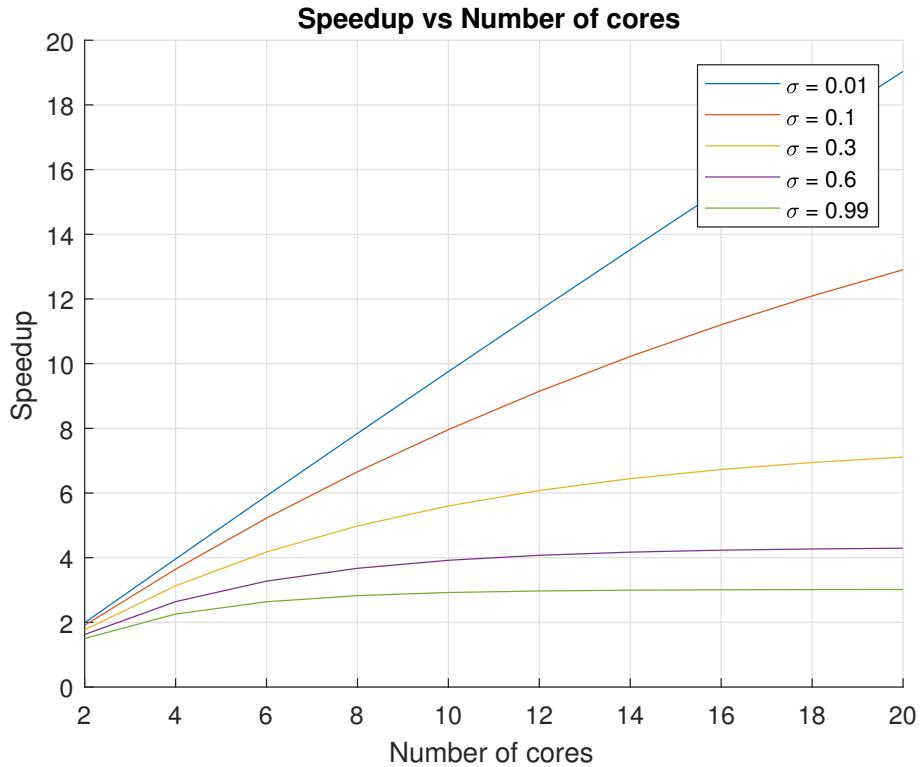


Figure 3.45: Speedup curve of  $2^*n$  mesh network result ( $n = 1 \cdots 10$ )

The figure illustrates that if  $\sigma < 0.1$ , the number of cores increases, the speedup efficiency is linear increasing. Alternatively speaking, if  $\sigma < 0.1$ , the factor core's number dominates the efficiency. If the  $\sigma > 0.3$ , the efficiency drops dramatically. That is, the  $\sigma$  value plays more critical role in the speedup simulation.

If  $\sigma$  is close to one (slow communication) and the number of cores is large, then speedup is three times since  $P_0$  and  $P_0$  two neighbors do almost all the processing.

## Data Injection on The Boundary Processor

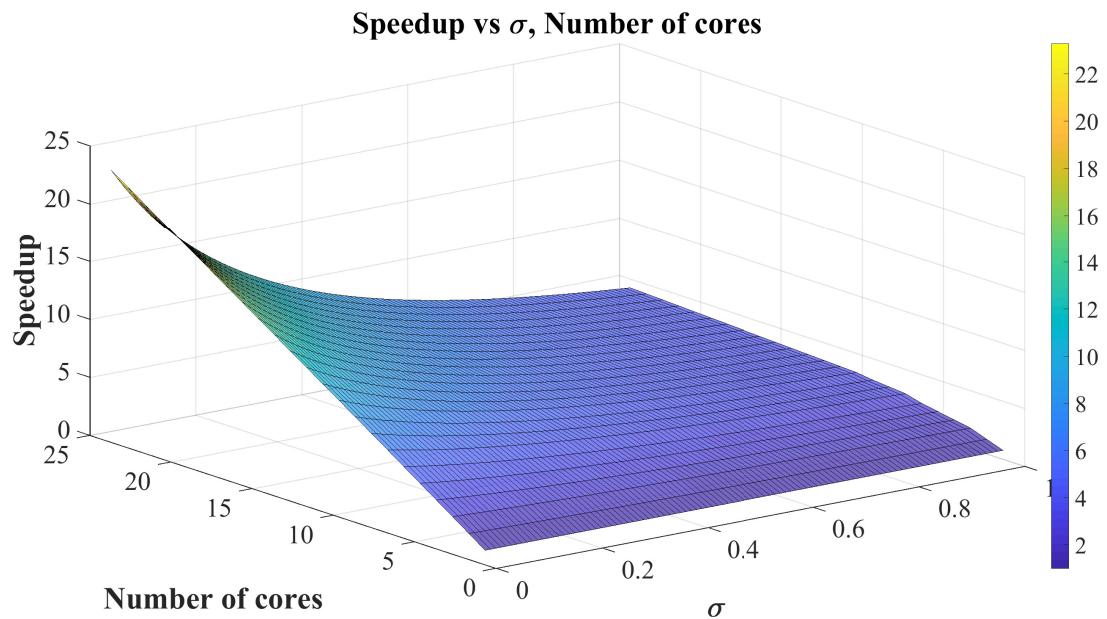


Figure 3.46: Sensitivity analysis result of  $3*n$  mesh network result ( $n = 1 \cdots 8$ )

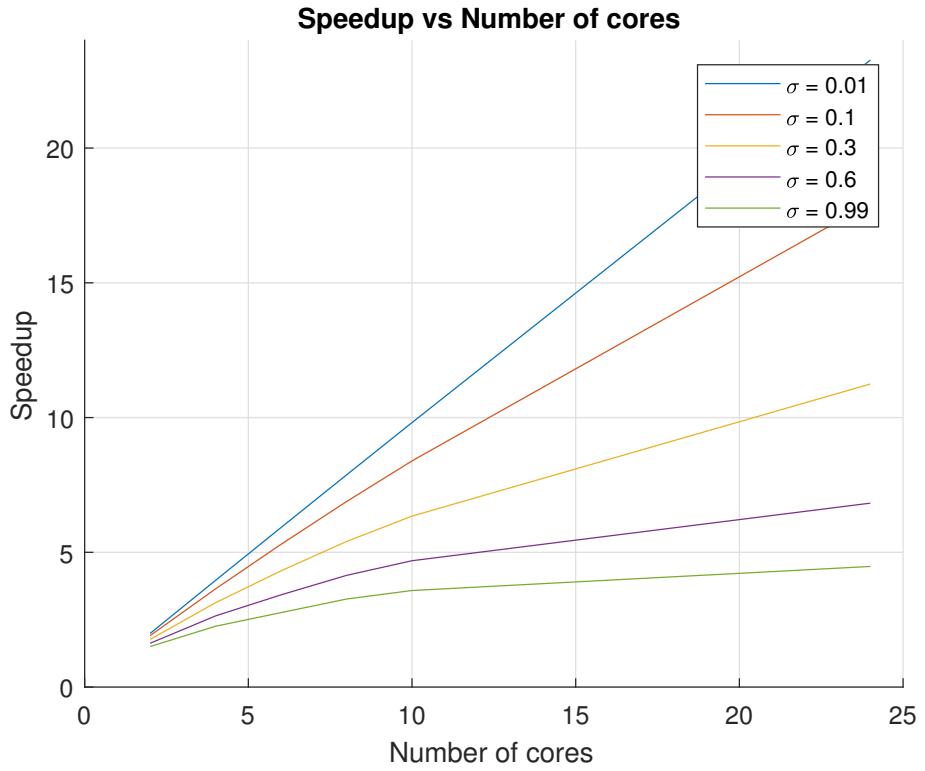


Figure 3.47: Speedup curve of  $3*n$  mesh network result ( $n = 1 \cdots 8$ )

Sensitivity analysis result Fig. 3.46 and speedup curve Fig. 3.47 tell the speedup efficiency for the data injection on the boundary scenario.

The figure illustrates that if  $\sigma < 0.1$  and the number of cores increases, the speedup efficiency is linear increasing. The maximum speedup is 24, the number of the cores in a  $3*8$  mesh network. Alternatively speaking, if  $\sigma < 0.1$ , the factor core's number dominates the efficiency. If the  $\sigma > 0.3$ , the efficiency drops dramatically. That is, the  $\sigma$  value plays more critical role in the speedup simulation.

## Data Injection on The Inner Grid Processor

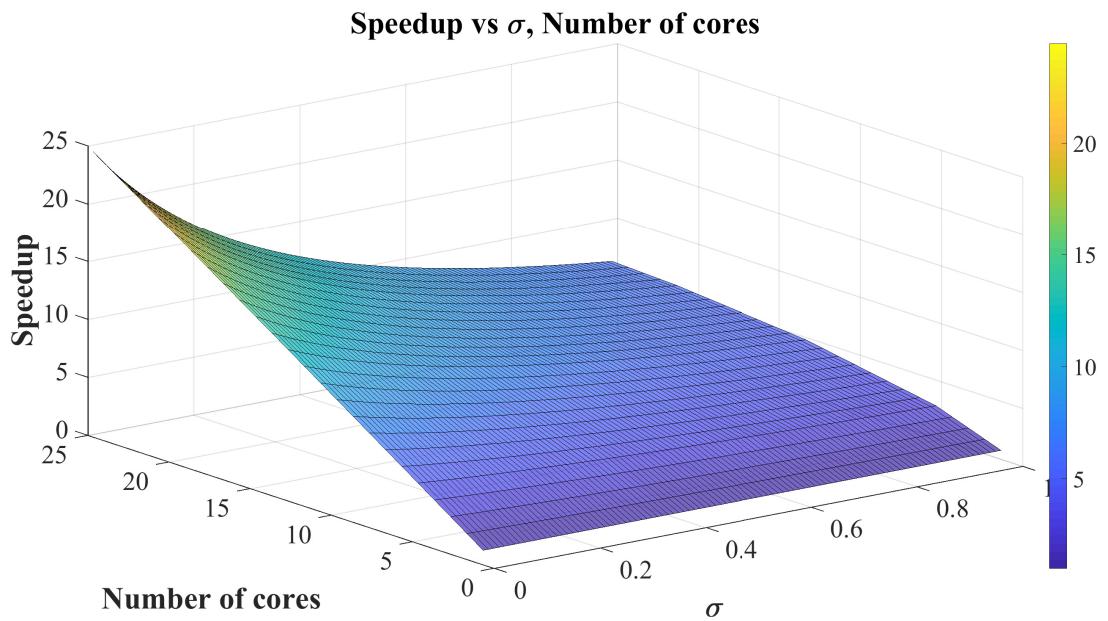


Figure 3.48: Sensitivity analysis result of data injection position on inner grid processor of  $5 * 5$  mesh network

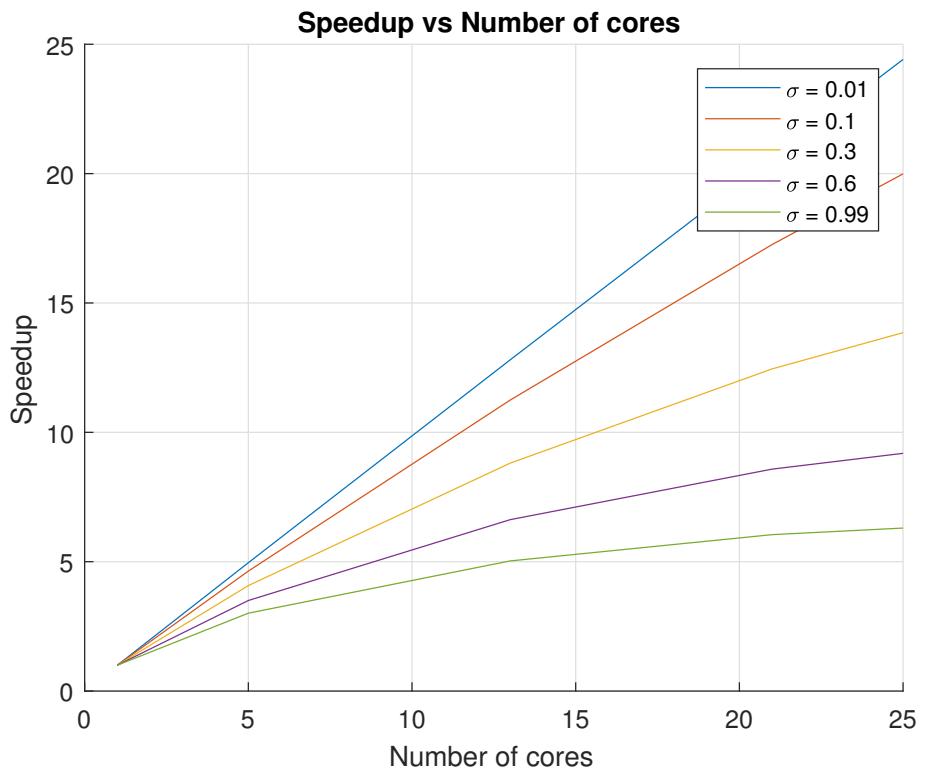


Figure 3.49: Speedup curve of  $5 * n$  mesh network result ( $n = 1 \cdots 5$ )

Sensitivity analysis Fig. 3.48 and speedup curves Fig. 3.49 display the simulation result for the data injection position  $P_{12}$ . If  $\sigma < 0.1$ , the speedup linearly increases and the maximum speedup is 24.

### 3.2.5 Multi-source Uniform Data Fraction

We utilize the similar methodology and algorithms and in virtual cut-through situation to deal with these problems. The critical point is that the flow matrix formula is different, which is replaced by the store and forward flow matrix formula.

#### Situation I

We utilize the Equivalence Processor Scheduling Algorithm to address this problem.

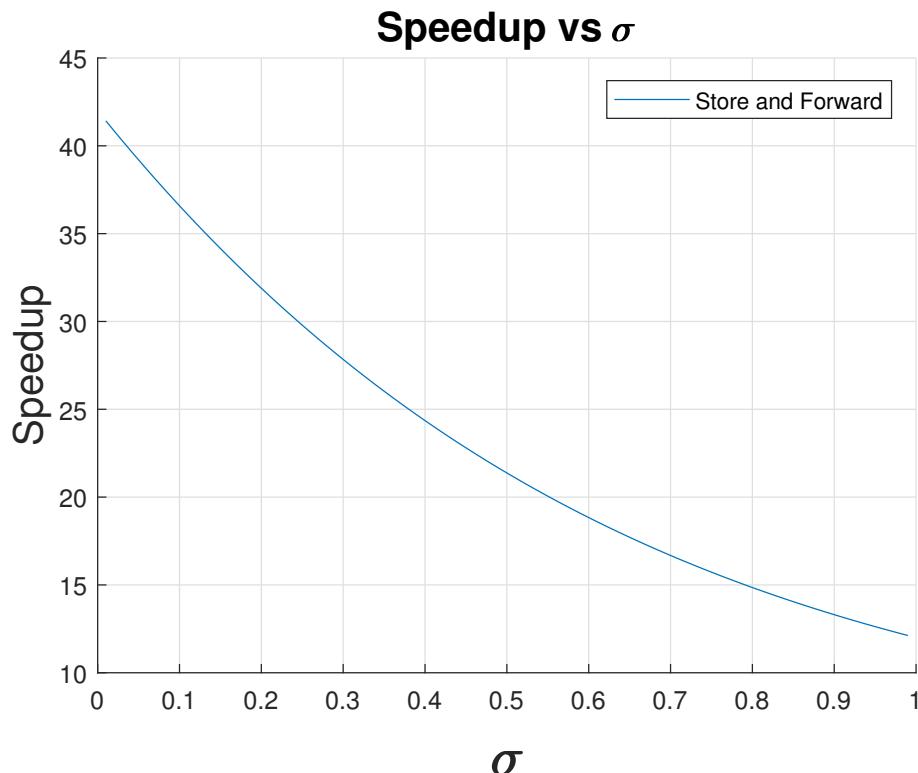


Figure 3.50: Connected subgraph Fig. 3.22 speedup vs  $\sigma$

For fast communication ( $\sigma \approx 0$ ), the maximum speedup is 42.

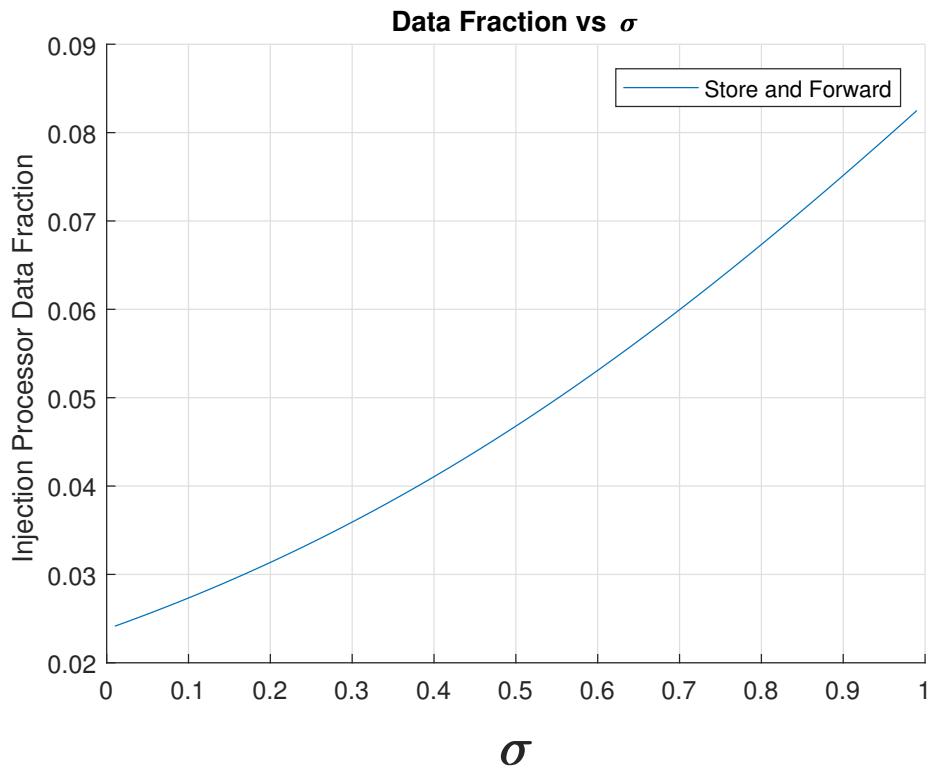


Figure 3.51: Connected subgraph Fig. 3.22's data injection processor workload fraction vs  $\sigma$

For fast communication ( $\sigma \approx 0$ ), each of 42 processors in Fig. 3.22 gets  $\frac{1}{42}$  of the load since they are all equals engaged in processing.

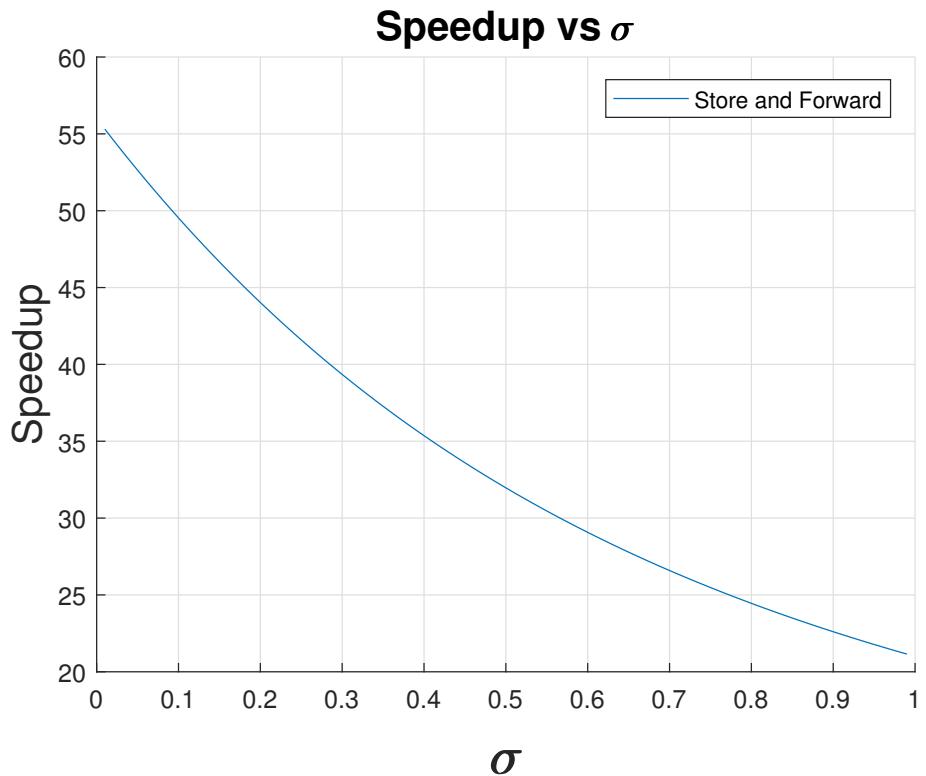


Figure 3.52: Connected subgraph Fig. 3.23 speedup vs  $\sigma$

For fast communication  $\sigma \approx 0$ , the maximum speedup is 56 (there are  $7 * 8 = 56$  processors in Fig. 3.23 ).

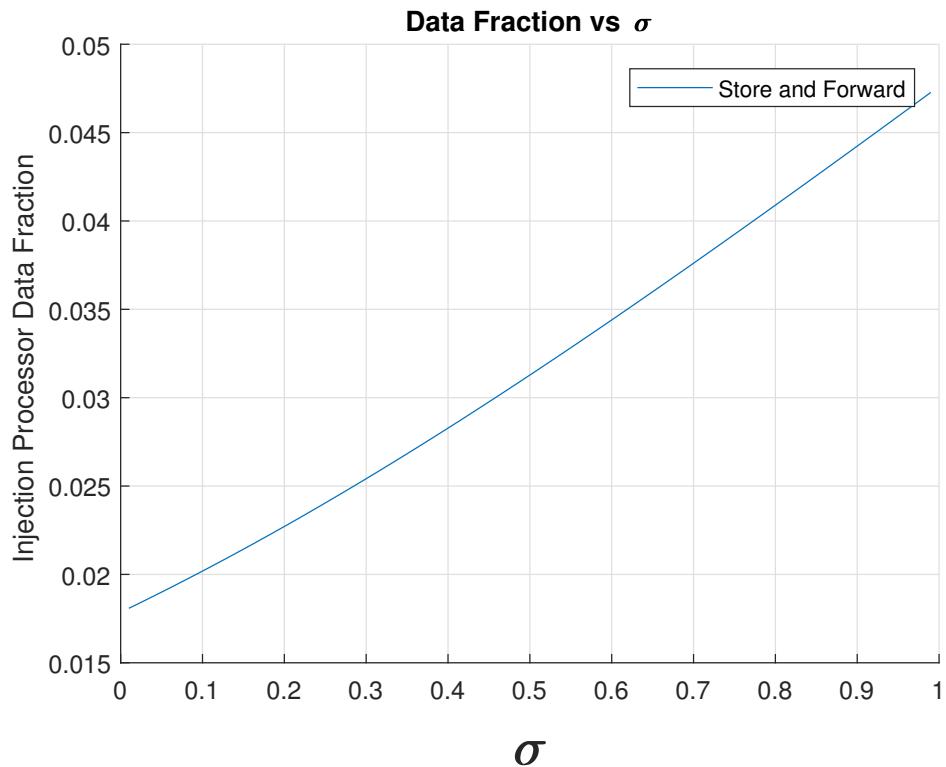


Figure 3.53: Connected subgraph Fig. 3.23's data injection processor workload fraction vs  $\sigma$

For fast communication ( $\sigma \approx 0$ ), each of 56 processors in Fig. 3.23 gets  $\frac{1}{56}$  of the load.

## Situation II

We utilize the Reduced Voronoi Diagram Algorithm to address this problem. The simulation result is as follows :

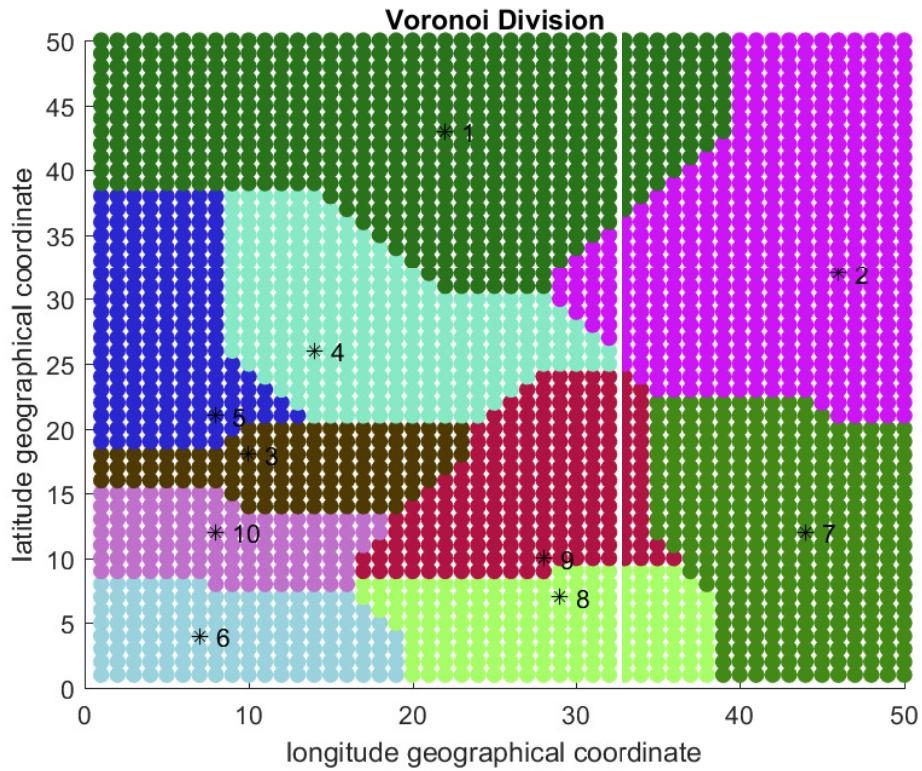


Figure 3.54: 10 Manhattan distance Voronoi Cells

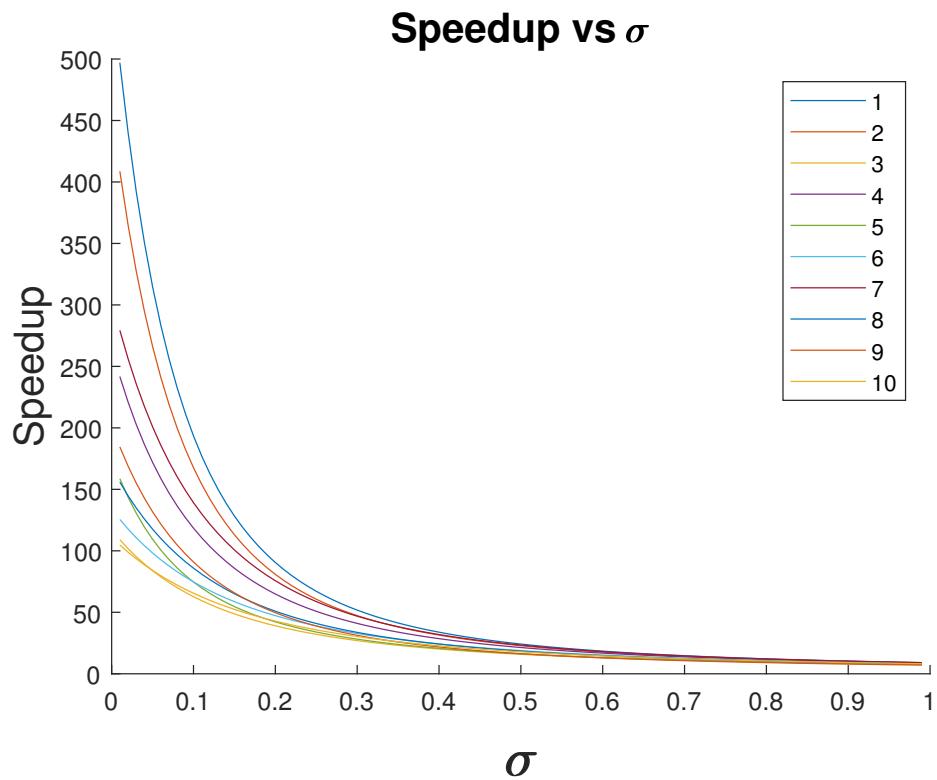


Figure 3.55: 10 Manhattan distance Voronoi cells store and forward switching speedup curves

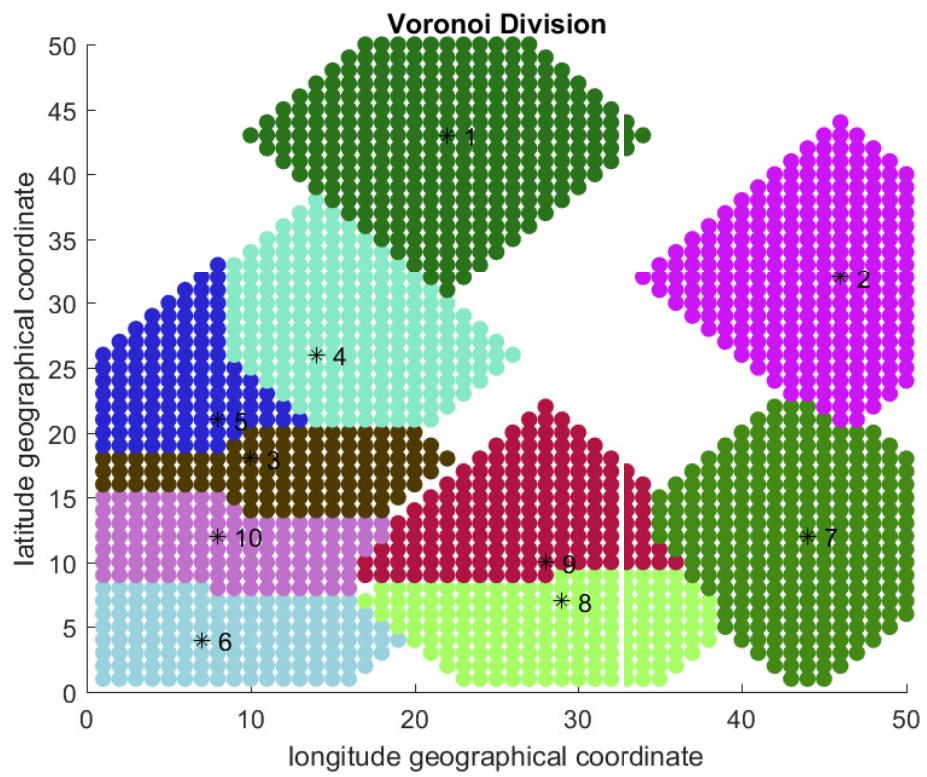


Figure 3.56: 10 reduced Manhattan distance store and forward switching Voronoi cells

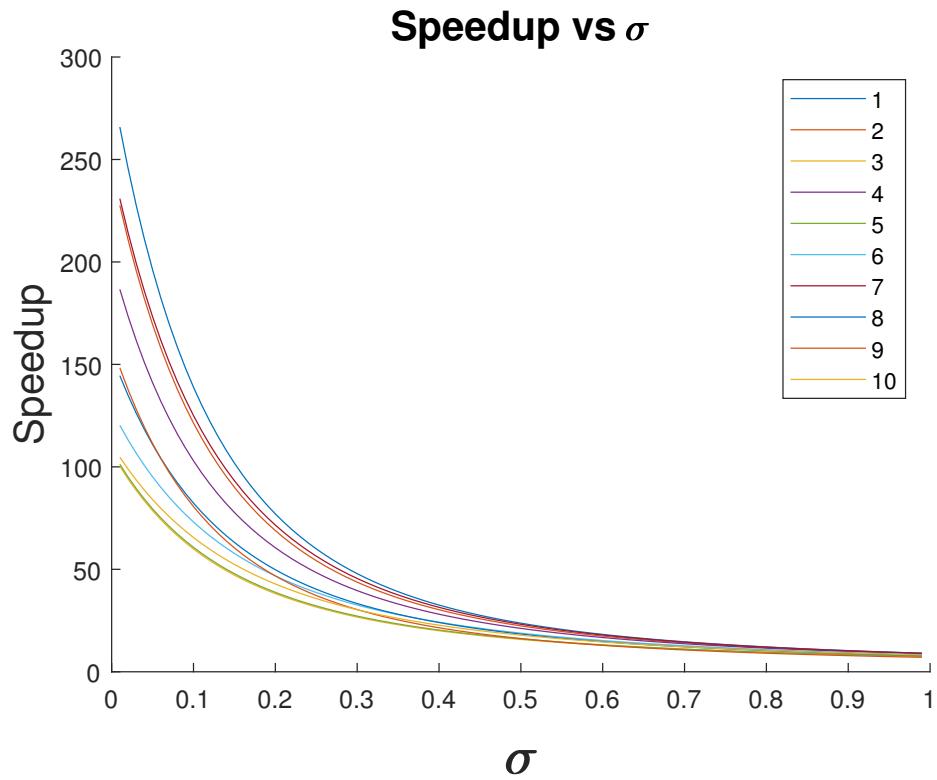


Figure 3.57: 10 reduced Voronoi cells' store and forward switching speedup curves

We save about 37% processors and finish the task within the same time.

### **Situation III**

We utilize the Reduced Constrained Voronoi Diagram Algorithm to address this problem.

### **3.2.6 Multi-source Non-uniform Data Injection**

We utilize the similar methodology and algorithms in virtual cut-through situation to deal with these problem.

## Chapter 4

### Toroidal Rectangle Network

#### 4.1 Toroidal Rectangle Network Notions

The toroidal network is a regular complex in that each polygonal face has the same number of links and each node is connected to the same number of links. According to the paper [32], there are three different torus mesh network. In this paper, our intent is not to propose one model to "fit all" problems but rather to indicate one normal case.

Considering the toroidal rectangle network Fig. 4.1 and Fig. 4.2.

- $m$  : There are  $m$  processors on the longitude.
- $n$  : There are  $n$  processors on the latitude.
- $L$  : The load injection site.
- $L_x$  : The  $L$ 's longitude coordinate.
- $L_y$  : The  $L$ 's latitude coordinate.
- $D_k$  :  $P_k$ 's shortest Manhattan distance to  $L$ .
- $D_{k,x}$  :  $P_k$ 's longitude shortest Manhattan distance to  $L$ .

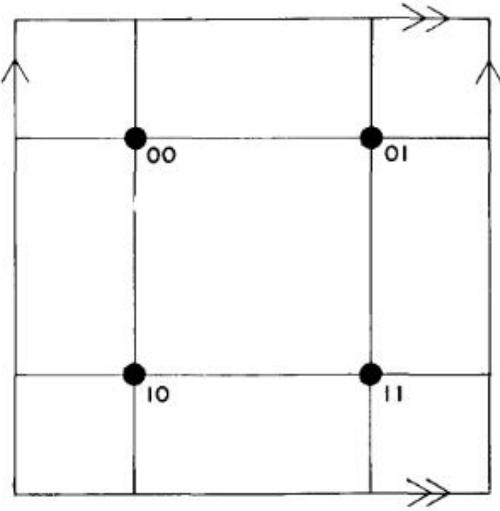


Figure 4.1: The rectangular toroidal network

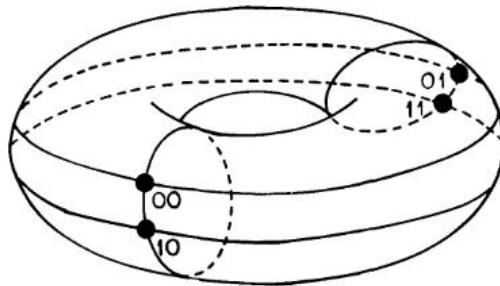


Figure 4.2: The rectangular toroidal network

- $D_{k,y}$  :  $P_k$ 's latitude shortest Manhattan distance to  $L$ .

$$D_k = D_{k,x} + D_{k,y} \quad (4.1)$$

$$D_{k,x} = \min\{\|D_{k,x} - L_x\|, m - \|D_{k,x} - L_x\|\} \quad (4.2)$$

$$D_{k,y} = \min\{\|D_{k,y} - L_y\|, n - \|D_{k,y} - L_y\|\} \quad (4.3)$$

## 4.2 Virtual Cut-through Switching Scenario

### 4.2.1 Data Injection On The Grid Processor

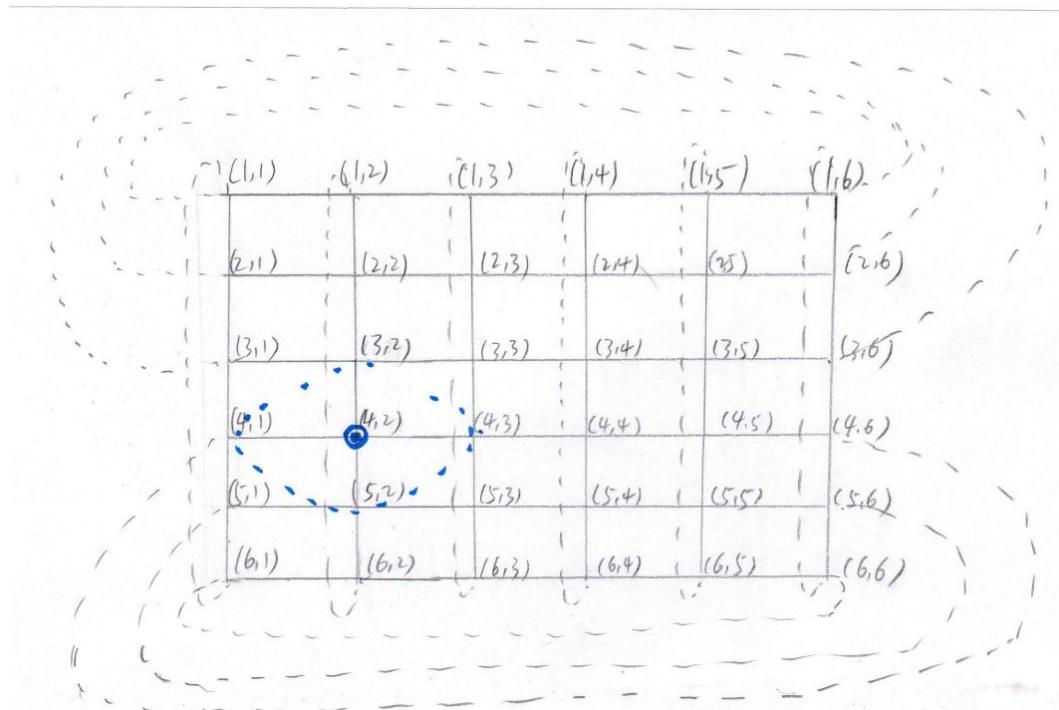


Figure 4.3: The  $m \times n$  toroidal rectangle network and the data injection is  $P_{4,2}$

In  $m \times n$  ( $m = 6, n = 6$ ) Fig. 4.3 toroidal rectangle network,  $L$  happens on grid position  $(4, 2)$ . We calculate the  $D_{k,i}$  table Table 4.1 by breadth first search(**BFS**) algorithm.

$D_i$	Number
0	1
1	4
2	8
3	10
4	8
5	4
6	1

Table 4.1:  $D_i$  vs Number

The flow matrix closed-form is :

$$\begin{bmatrix} 1 & 4 & 8 & 10 & 8 & 4 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & 1 & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & \sigma & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \alpha_4 \\ \alpha_5 \\ \alpha_6 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4.4)$$

The simulation result is :

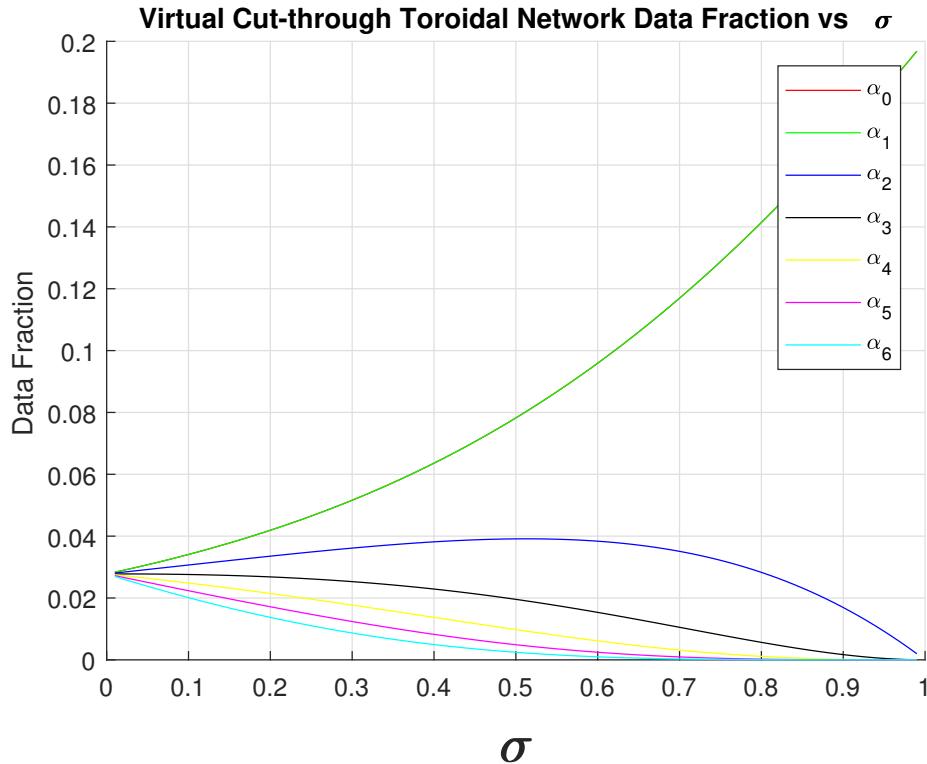


Figure 4.4: Data fraction curve of toroidal rectangle network Fig. 4.3

Here for fast communication ( $\sigma \approx 0$ ), each of 36 processors gets  $\frac{1}{36}$  of the load as all 36 processors receive a uniform amount of load. If communication is slow, each of  $P_0$  and four  $P_0$  neighbors receive  $\frac{1}{5}$  of the load (i.e. 0.2 of the load). The load sharing by these five processors is economical.

$D_i$	Number
0	1
1	4
2	8
3	8
4	4

Table 4.2:  $D_i$  vs Number of processor on each  $D_i$

#### 4.2.2 Sensitivity Analysis of Toroidal Rectangle Network

Considering a  $5 * 5$  toroidal rectangle network, the  $level_i$  table shows Table 4.2.

So the simulation result illustrates in Fig. 4.5

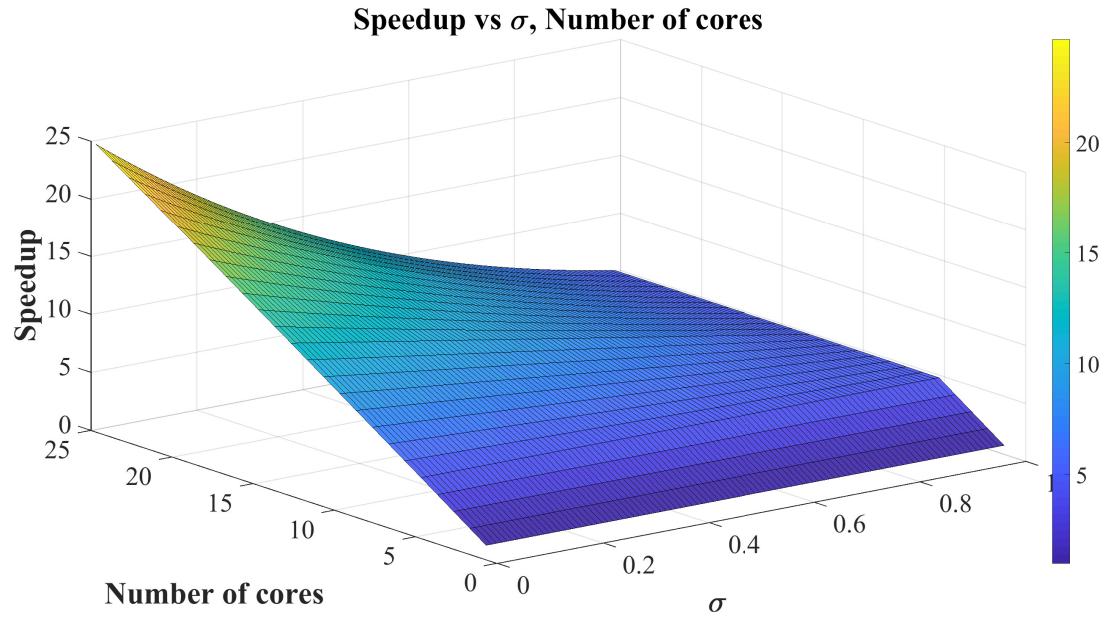


Figure 4.5: Sensitivity analysis of  $5*n$  torus network (where  $n = 1 \cdots 5$ )

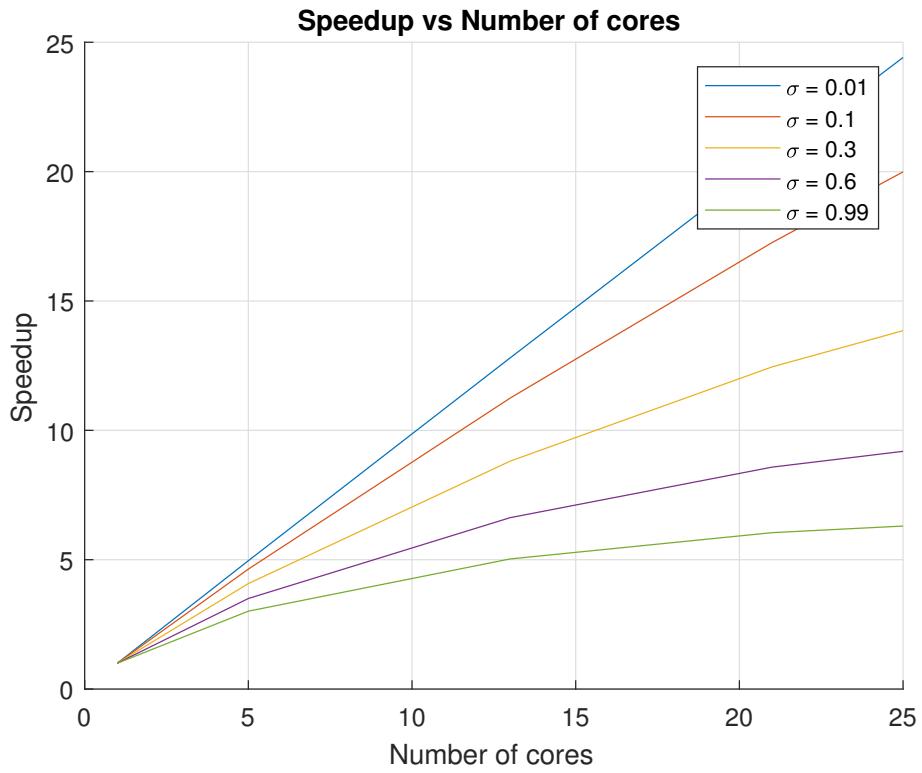


Figure 4.6: Data fraction curves of a  $5*n$  torus network (where  $n = 1 \cdots 5$ ) vs  $\sigma$

Fig. 4.6 illustrates that as the value  $\sigma$  decreases, the speedup efficiency increases. For fast communication ( $\sigma = 0.01$ ), the speedup is almost 25, as all 25 processors are uniformly engaged in processing. For slow communication ( $\sigma = 0.99$ ), the speedup is about 5 as there are  $P_0$  and its four neighbors are engaged into the processing load.

### 4.2.3 Multi-source Uniform Data Fraction

We extend the single source assignment to multi-source assignment problem [18] [21]. According to each processor, we concentrate on the processors' geographical location  $P_i$ , data fraction assigned  $\alpha_i$ .

Assuming the data fraction is even. For example, the workload is unit 1 and there are  $k$  different data injection options. So each data injection is assigned  $\frac{1}{k}$  workload.

From the data injection position relationship we consider three different situations :

- Data injection positions consist of a subgraph  $G_L$  of  $G$ .
- Data injection processor doesn't connect with each other.
- Data injection positions consist of some connected subgraphs and individual injection.

#### Situation I

We choose the Equivalence Processor Scheduling Algorithm to address the problem.

Torus connected subgraph data injection Fig. 4.7 Fig. 4.9 show a connected subgraph data injection situation.

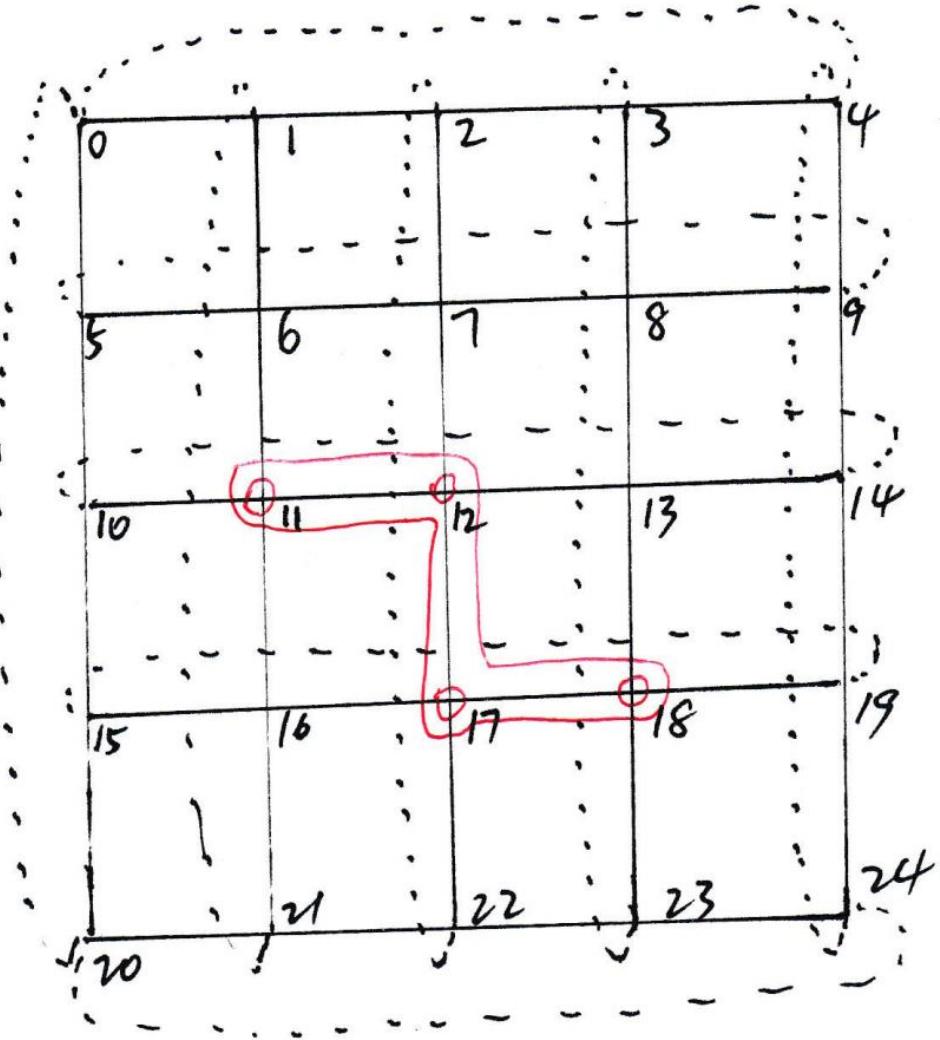


Figure 4.7: Toroidal mesh network subgraph data injection

A connected subgraph Fig. 4.7's flow matrix equation is

$$\begin{bmatrix} 4 & 8 & 9 & 4 \\ 1 & -1 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 \\ 0 & \sigma - 1 & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_2 \\ \alpha_3 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4.5)$$

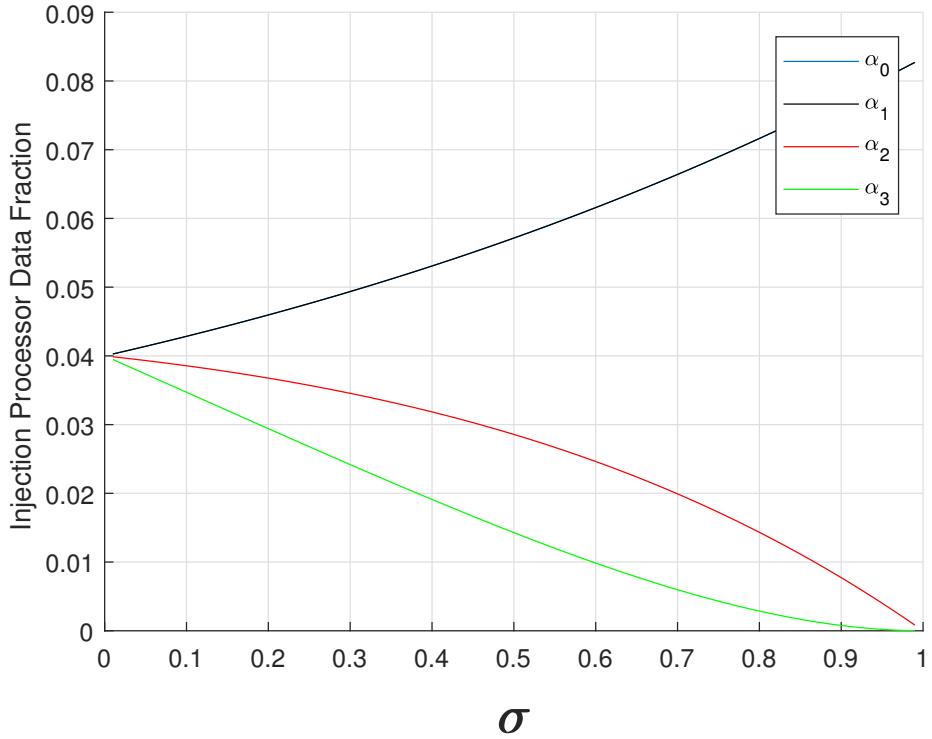


Figure 4.8: Data fraction curves of connected subgraph Fig. 4.7

The load fraction are 0.04 a small  $\sigma$  (fast communication) as all 25 processors are uniformly engaged processing. For slow communication, each of 12 processors (4 is the cluster and 8 is the adjacent neighbors) receives  $\frac{1}{12}$  of the load as it is not economical to distribute load beyond those 12 processors.

Fig. 4.9 shows another connected subgraph data injection example.

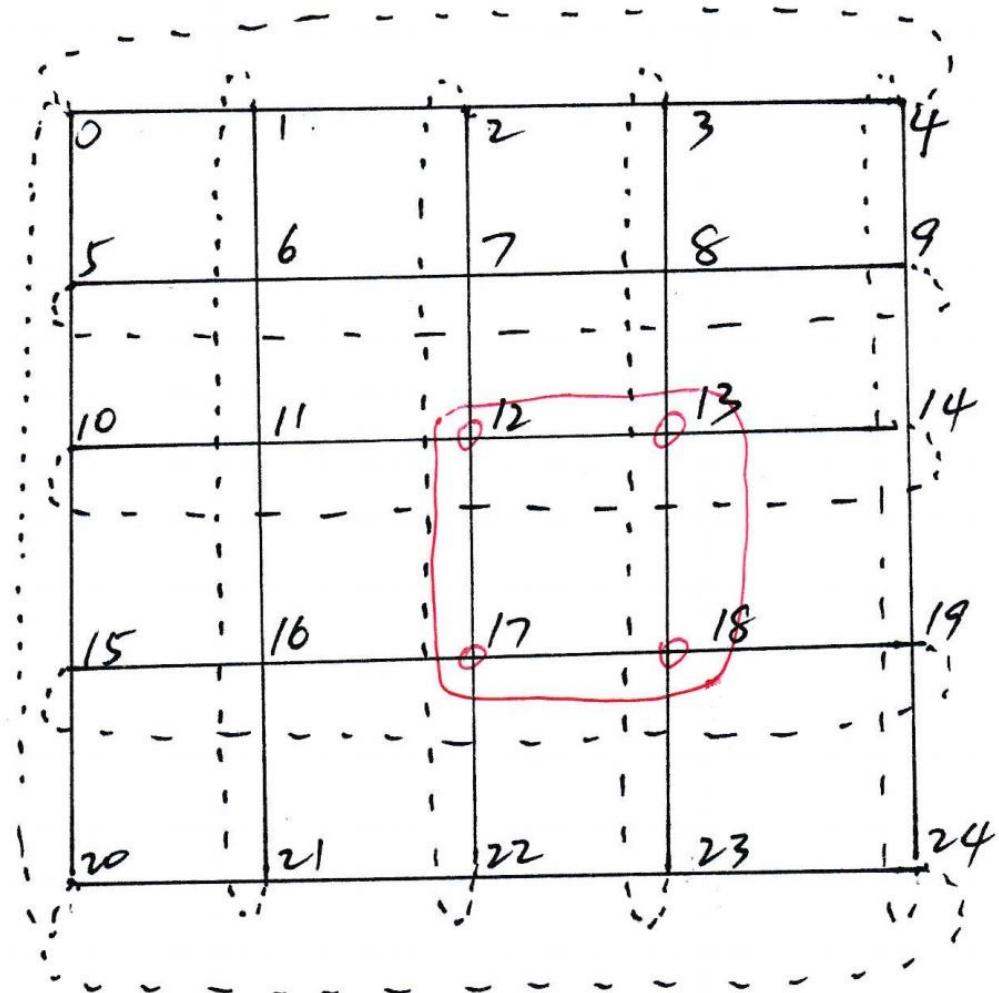


Figure 4.9: Toroidal mesh network subgraph data injection

Fig. 4.9's flow matrix equation is :

$$\begin{bmatrix} 4 & 8 & 9 & 4 \\ 1 & -1 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 \\ 0 & \sigma - 1 & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_2 \\ \alpha_3 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4.6)$$

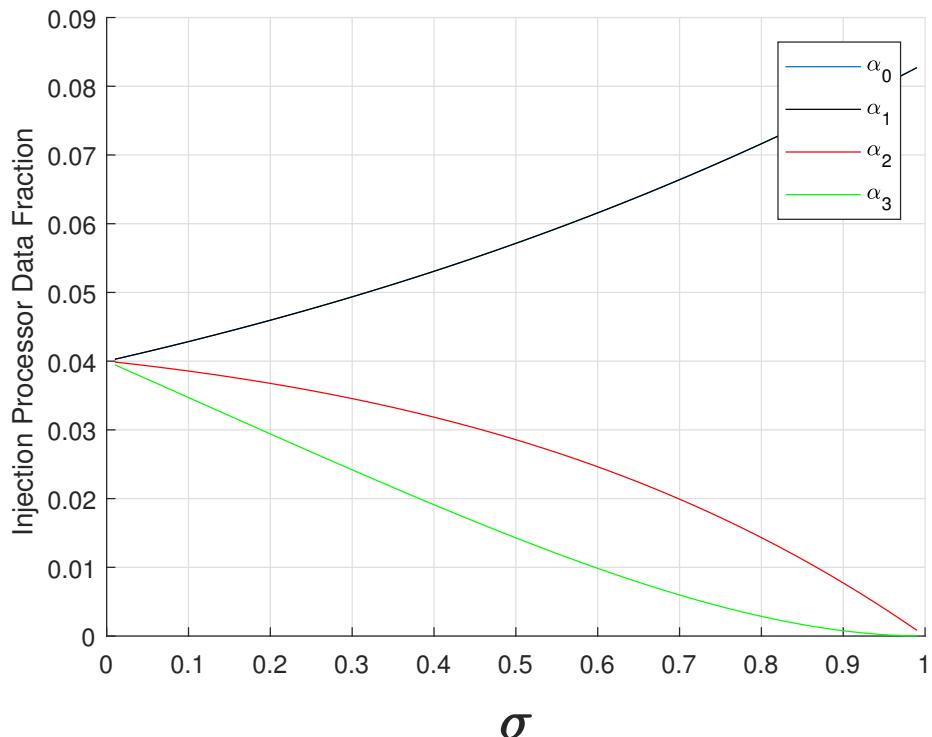


Figure 4.10: Data fraction on different type processors for Fig. 4.9

Since Fig. 4.10 also involves 25 total processors and 12 cluster processor and adjacent, it is identical to Fig. 4.7.

## Situation II

We choose the Reduced Voronoi Diagram Algorithm to address the problem.

Fig. 4.11 [33] provides a torus Voronoi method, which is used here. It extends the original domain to 8 copies and calculate the Voronoi Diagram as a planar algorithm [34]. Then the corner part is the torus Voronoi diagram.

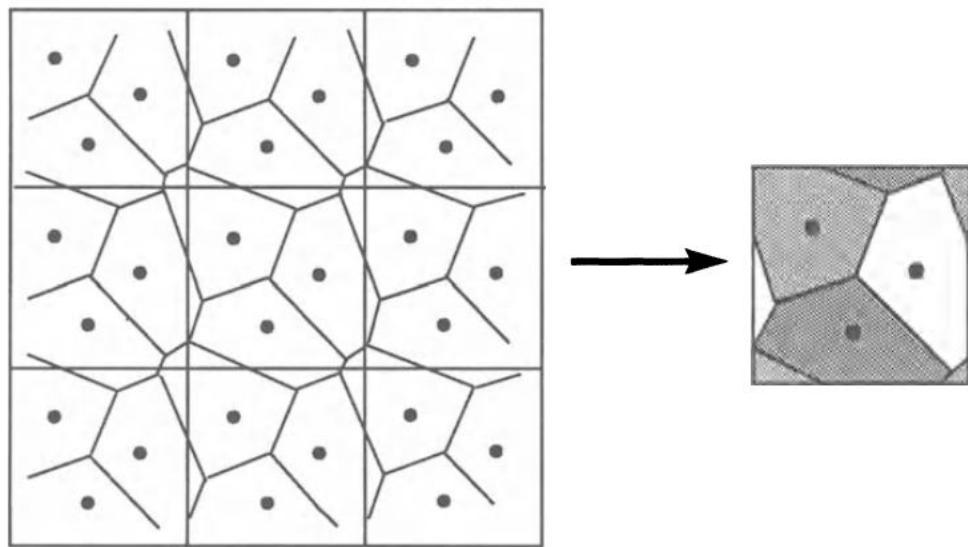


Figure 4.11: How to calculate torus Voronoi Diagram

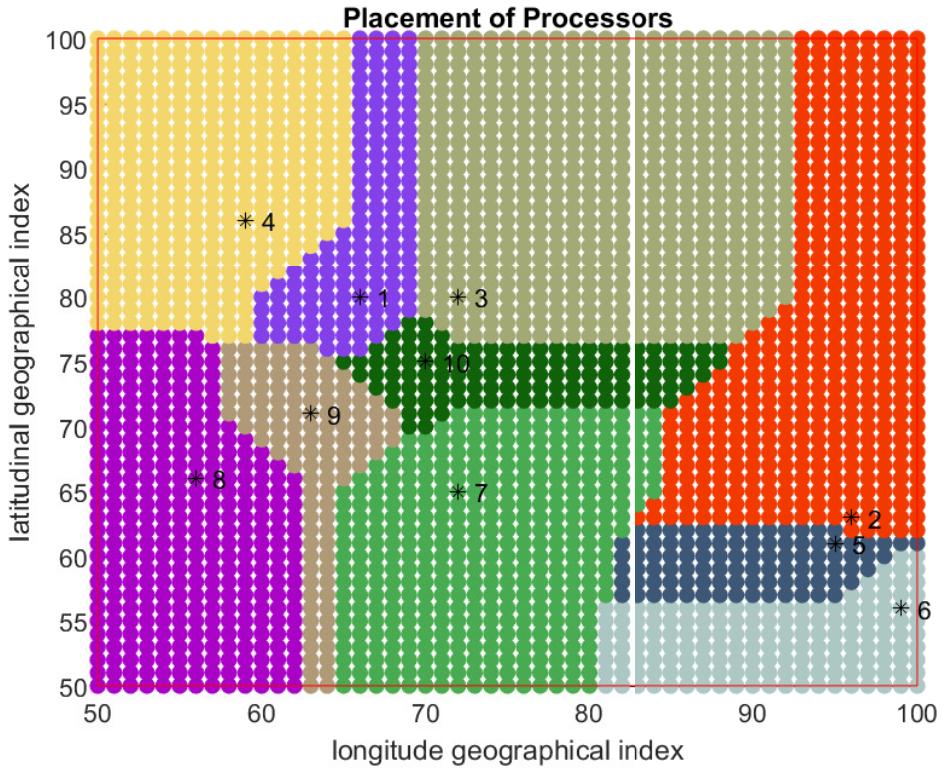


Figure 4.12: Initial Manhattan distance Voronoi Diagram

Fig. 4.12 says the initial Voronoi division of a  $50 \times 50$  mesh network. The base is the data injection and the processor Voronoi cell tackle base's workload together. The user case contains 10 data injections and each cell's speedup curve shows in Fig. 4.15.

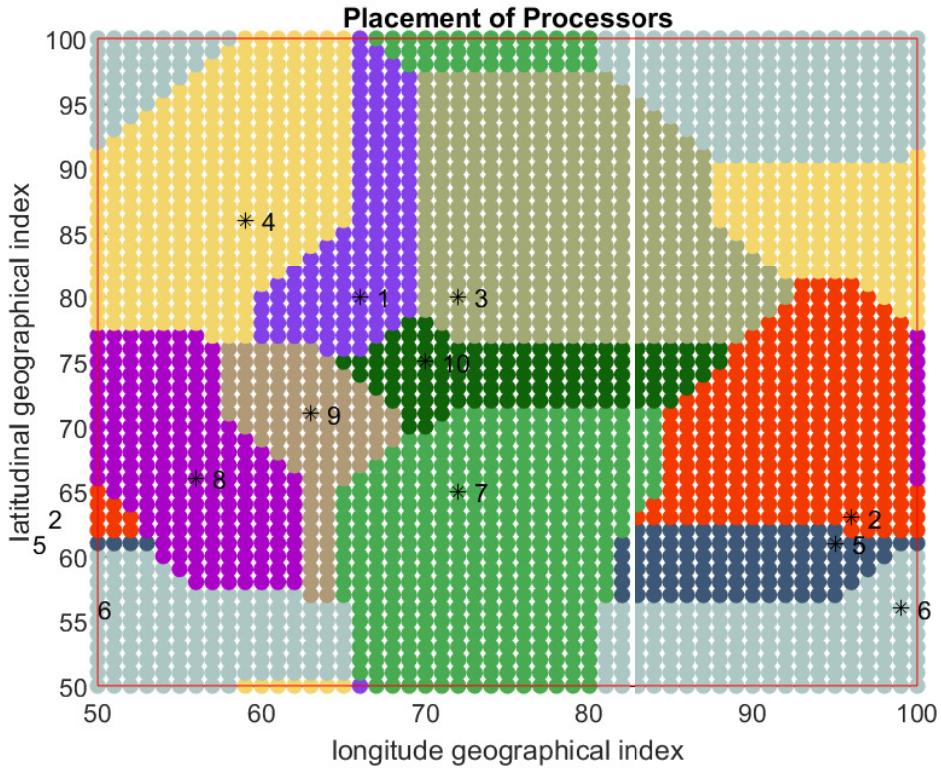


Figure 4.13: Torus Manhattan distance Voronoi diagram

Torus Manhattan distance Voronoi diagram Fig. 4.13 shows a toroidal Voronoi division result. The same color parts connect with each other and consist of a whole division in toroidal rectangle network. For example, the four gray corners consist of a whole area and the injection processor index is 6.

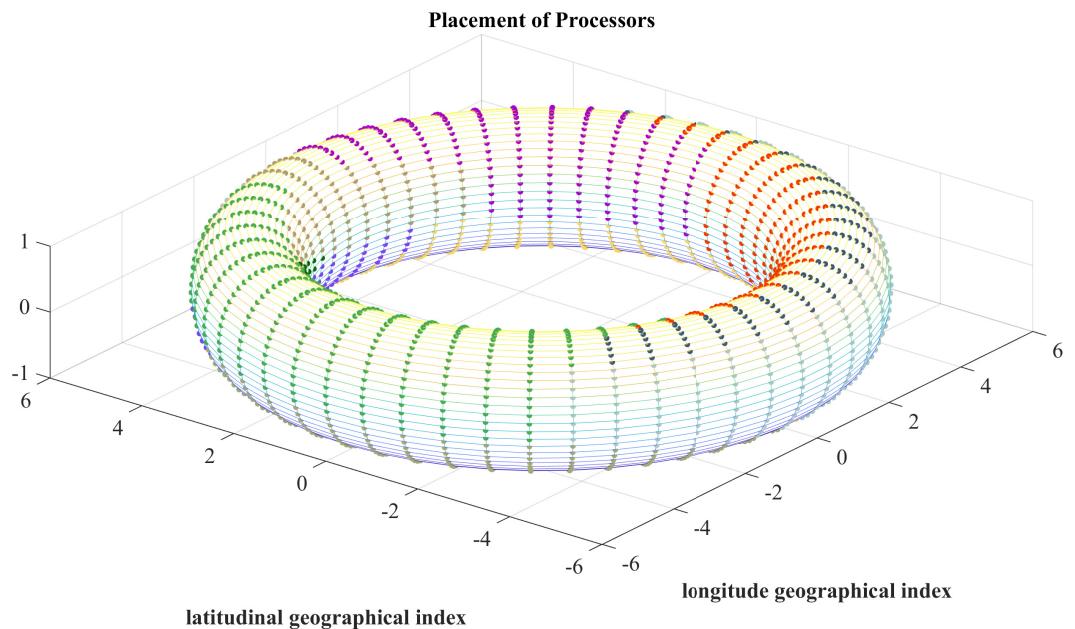


Figure 4.14: Voronoi diagram casting to the torus

Fig. 4.14 shows the Fig. 4.13 casts to the toroidal rectangle network result.

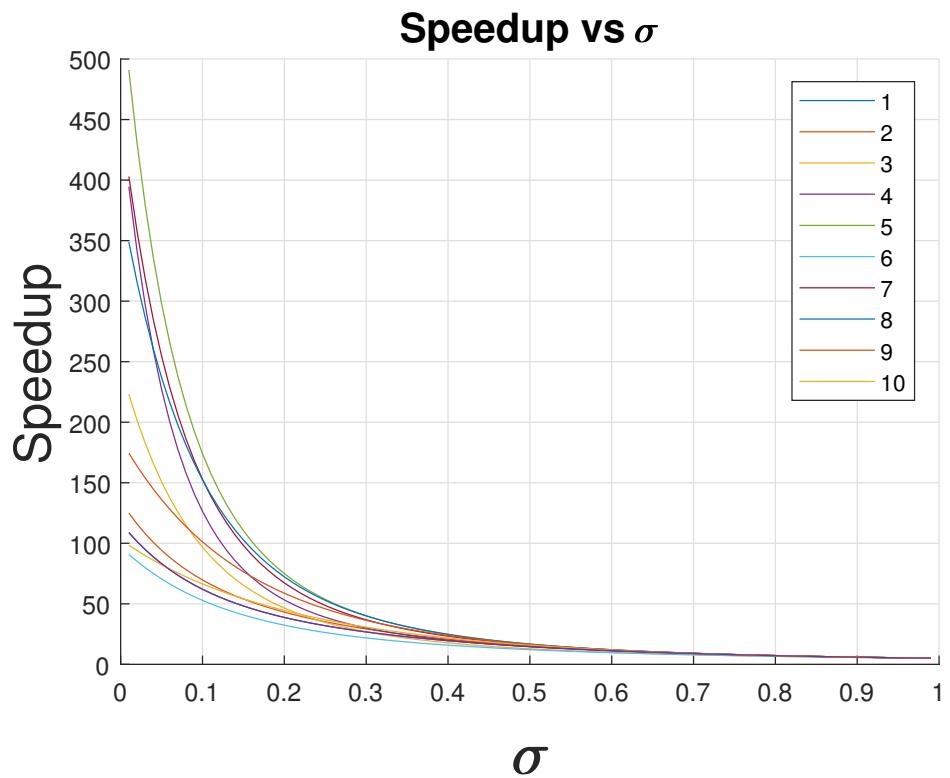


Figure 4.15: Toroidal Voronoi cells' speedup curves

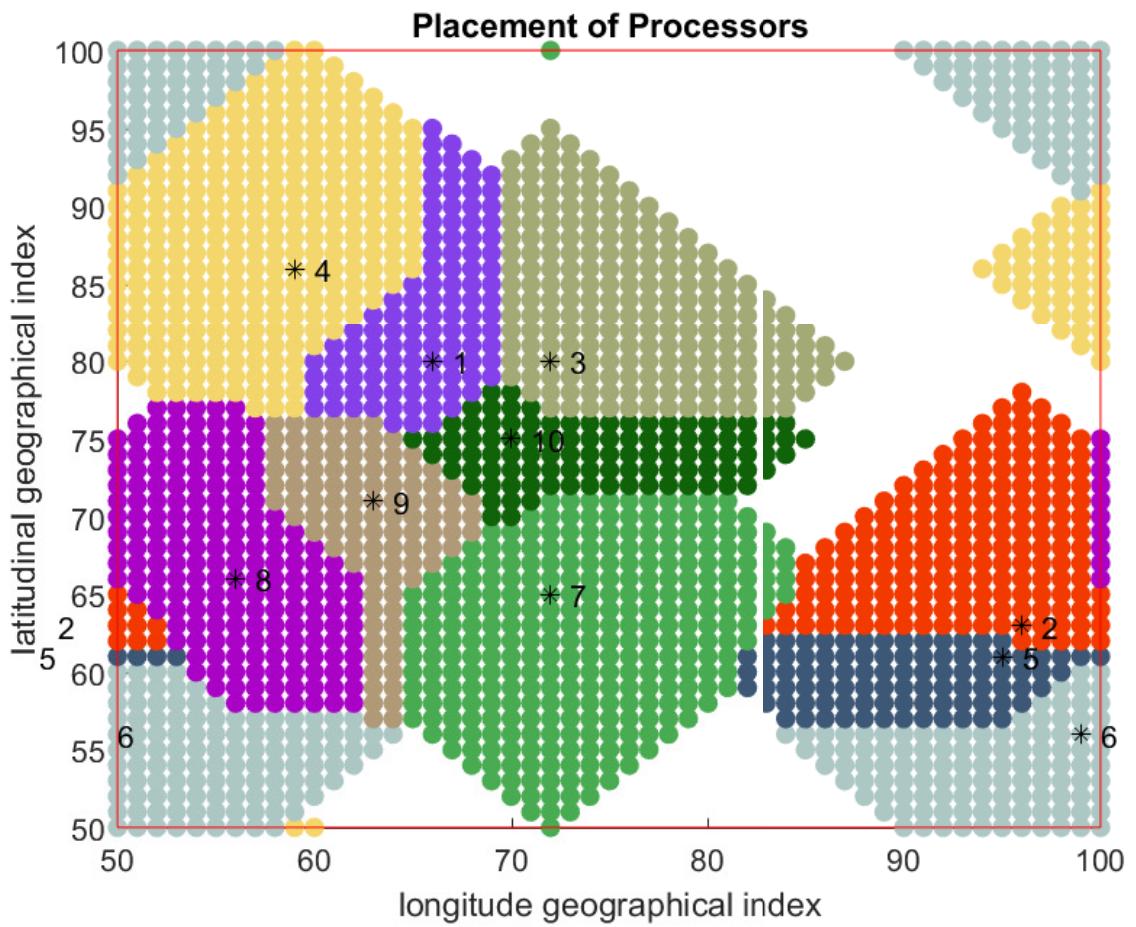


Figure 4.16: Torus reduced Voronoi diagram

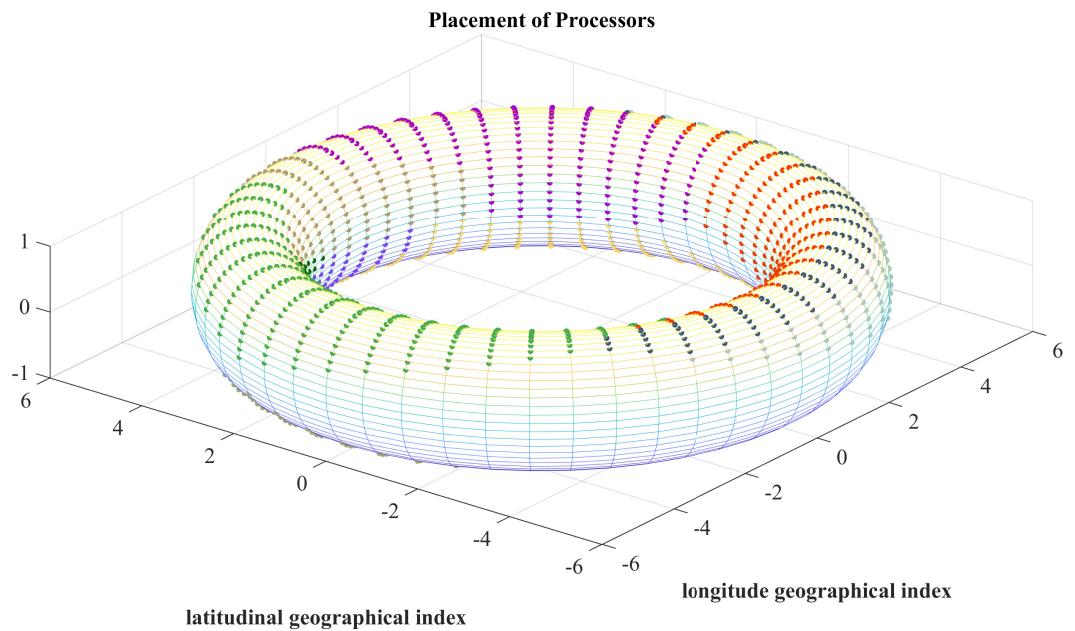


Figure 4.17: Torus reduced Voronoi diagram casting to a toroidal rectangle network

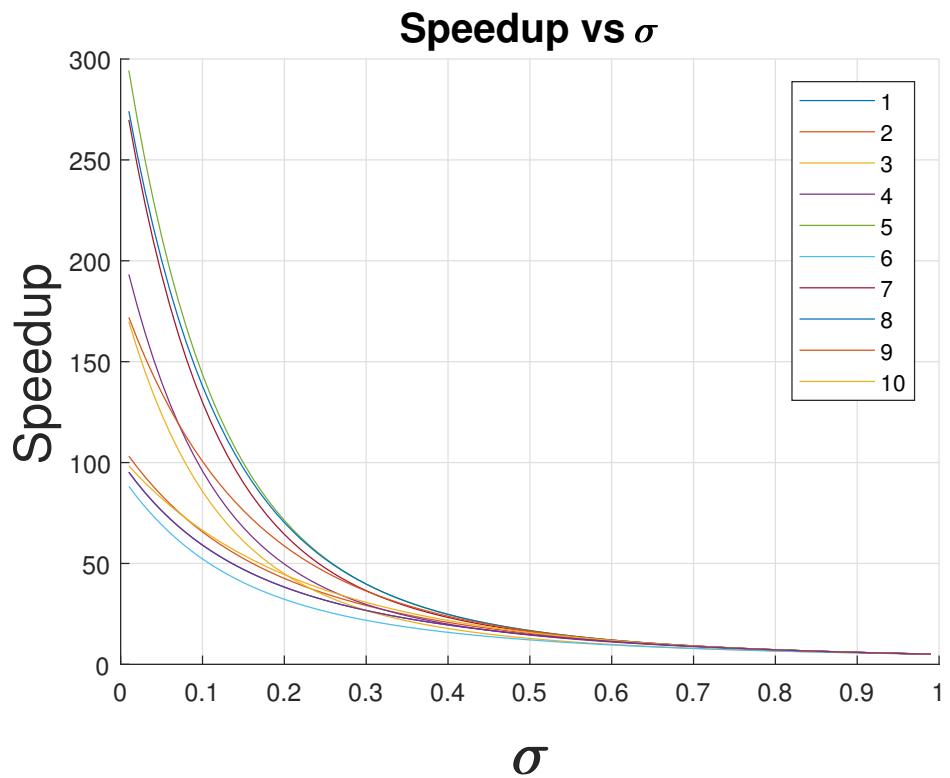


Figure 4.18: Torus reduced Voronoi diagram speedup curves

In the reduced model Fig. 4.17 and Fig. 4.18, reduced toroidal Voronoi diagram save 27% processors hit the same processing capacity.

The ratio speedup is about  $\frac{speedup_{max}}{speedup_{min}} = \frac{490}{98} = 5$ . After the reduced stage, the ratio is  $\frac{290}{98} \approx 2.96$ . That is the reduced heuristic algorithm obtaining more balanced computation capacity distribution.

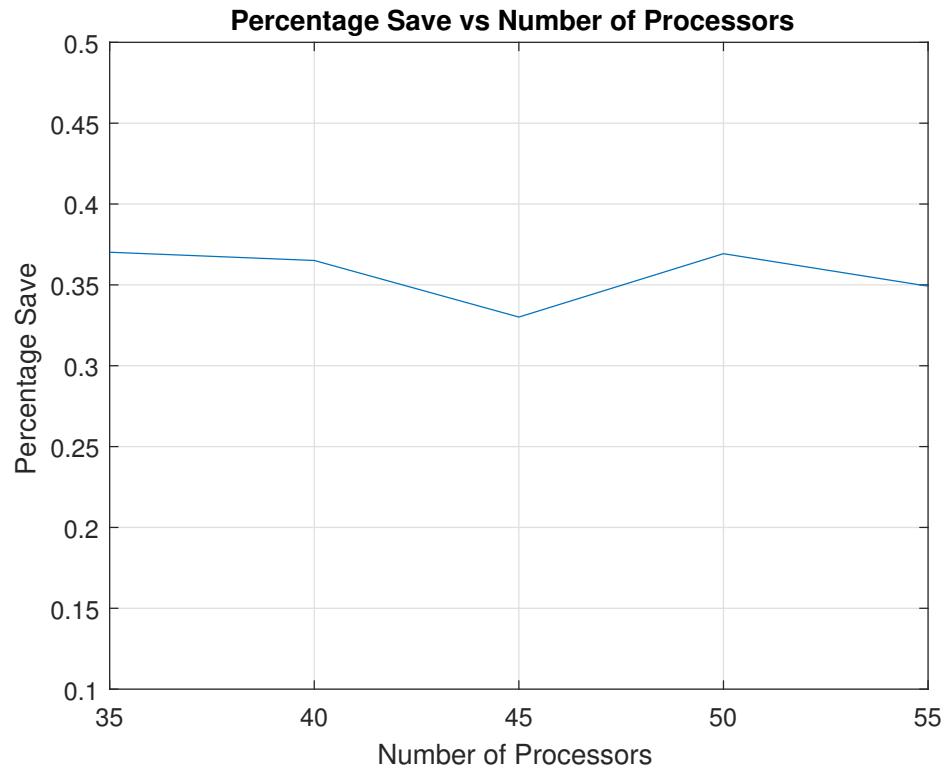


Figure 4.19: Torus reduced Voronoi diagram average saved processors

### Situation III

We utilize the Reduced Constrained Voronoi Diagram Algorithm to address this kind of question.

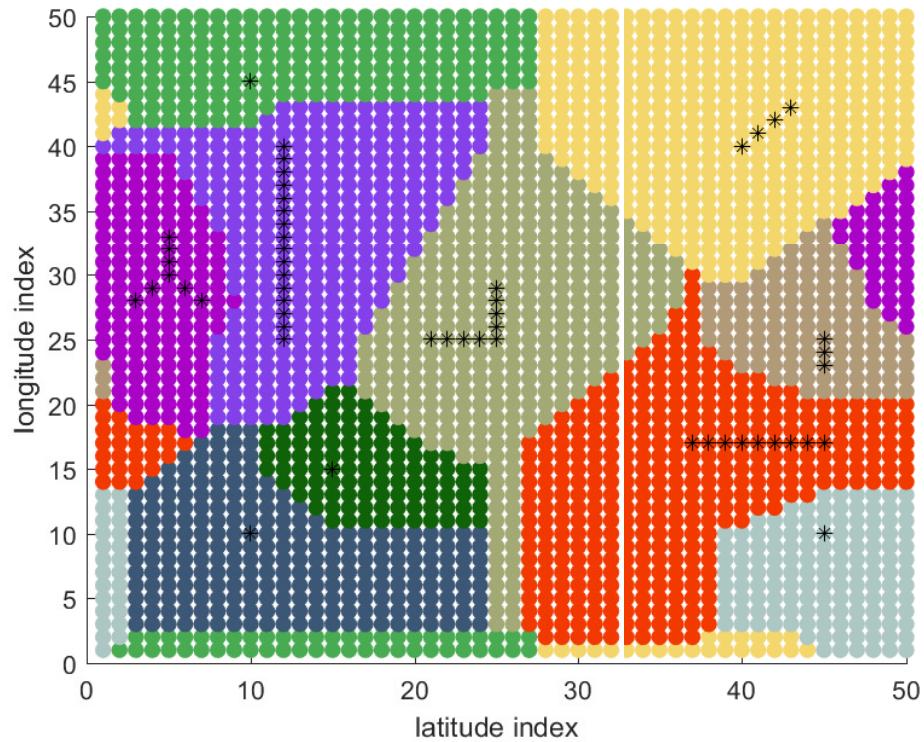


Figure 4.20: Subgraph and individual data injection division on torus network

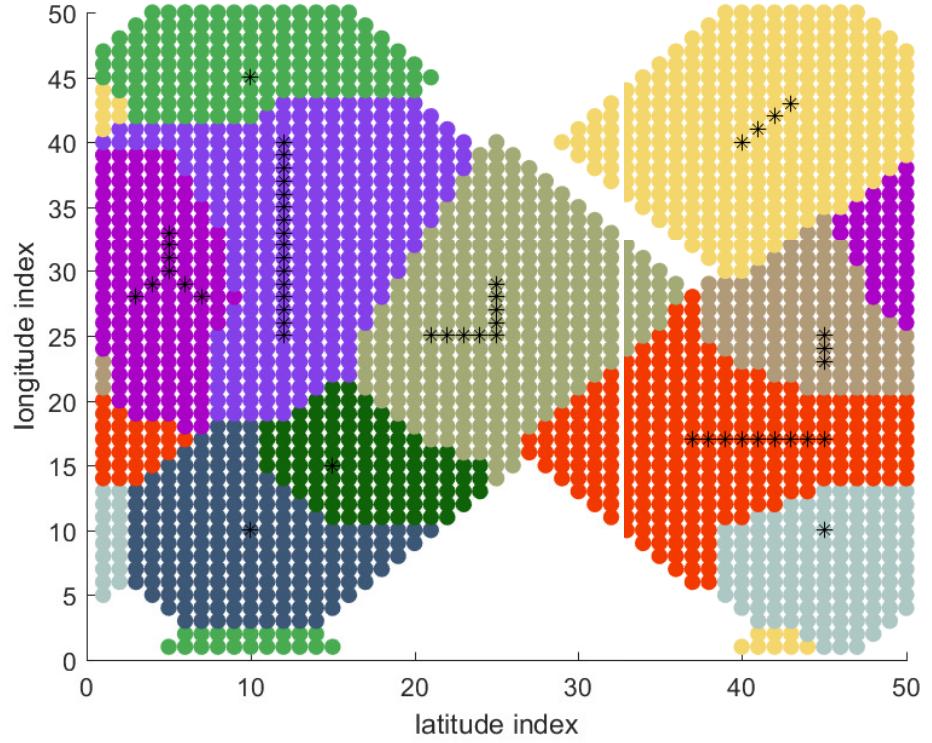


Figure 4.21: Subgraph and individual data injection constrained Voronoi diagram division on torus network

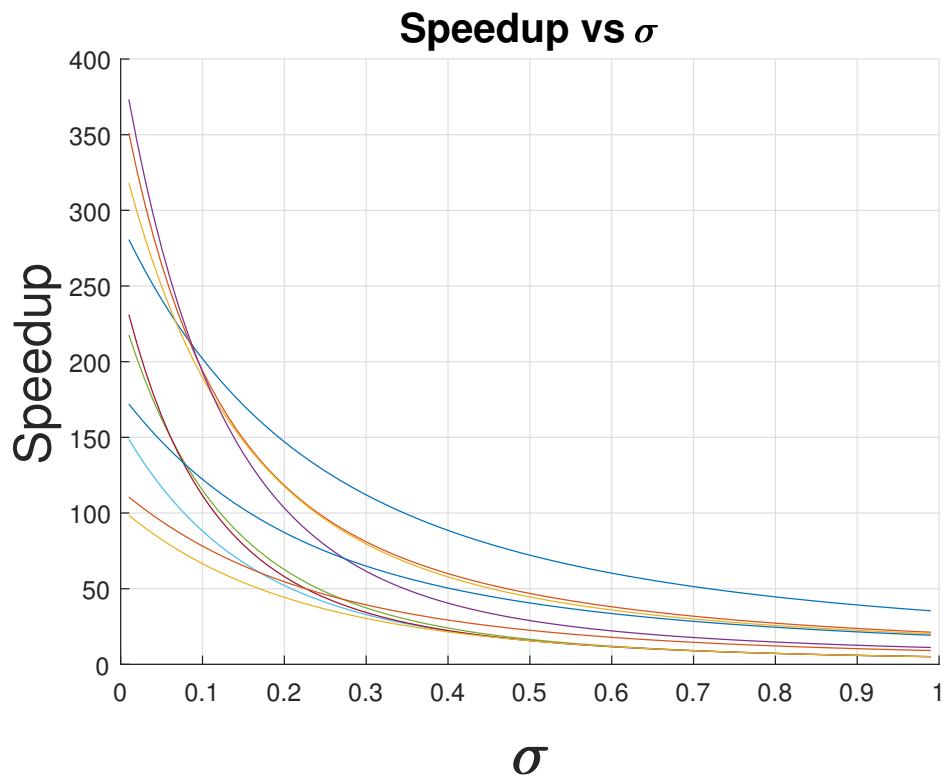


Figure 4.22: Subgraph and individual data injection speedup curves on torus network

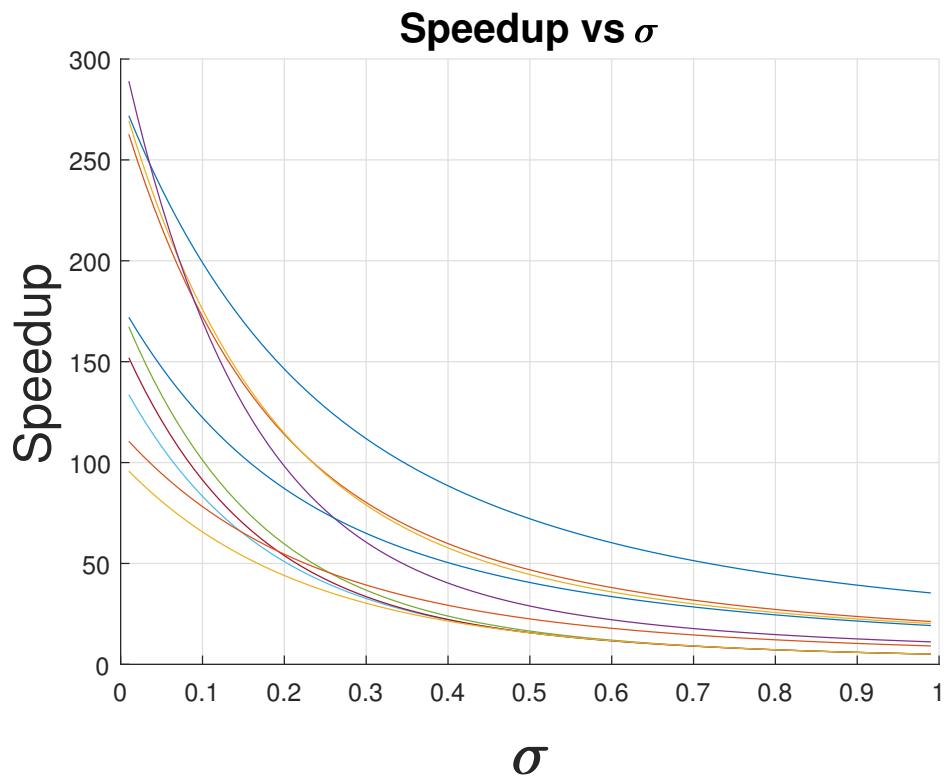


Figure 4.23: Subgraph and individual data injection constrained Voronoi diagram division speedup curves on torus network

Save about  $436/2500 \approx 17\%$  processors.

#### **4.2.4 Multi-source Non-uniform Data Injection**

We utilize the same methodology and algorithm used in the mesh network.

## 4.3 Store and Forward Switching Scenario

### 4.3.1 Data Injection On The Grid Processor

We utilize the  $\sigma^*$  to present  $-(\sigma + 1)$ . The flow matrix closed-form of Fig. 4.3 is:

$$\begin{bmatrix} 1 & 4 & 8 & 10 & 8 & 4 & 1 \\ 1 & \sigma^* & 0 & 0 & 0 & 0 & 0 \\ 1 & -\sigma & \sigma^* & 0 & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma^* & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma & \sigma^* & 0 & 0 \\ 1 & -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* & 0 \\ 1 & -\sigma & -\sigma & -\sigma & -\sigma & -\sigma & \sigma^* \end{bmatrix} \times \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \alpha_4 \\ \alpha_5 \\ \alpha_6 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4.7)$$

The fraction curve result is :

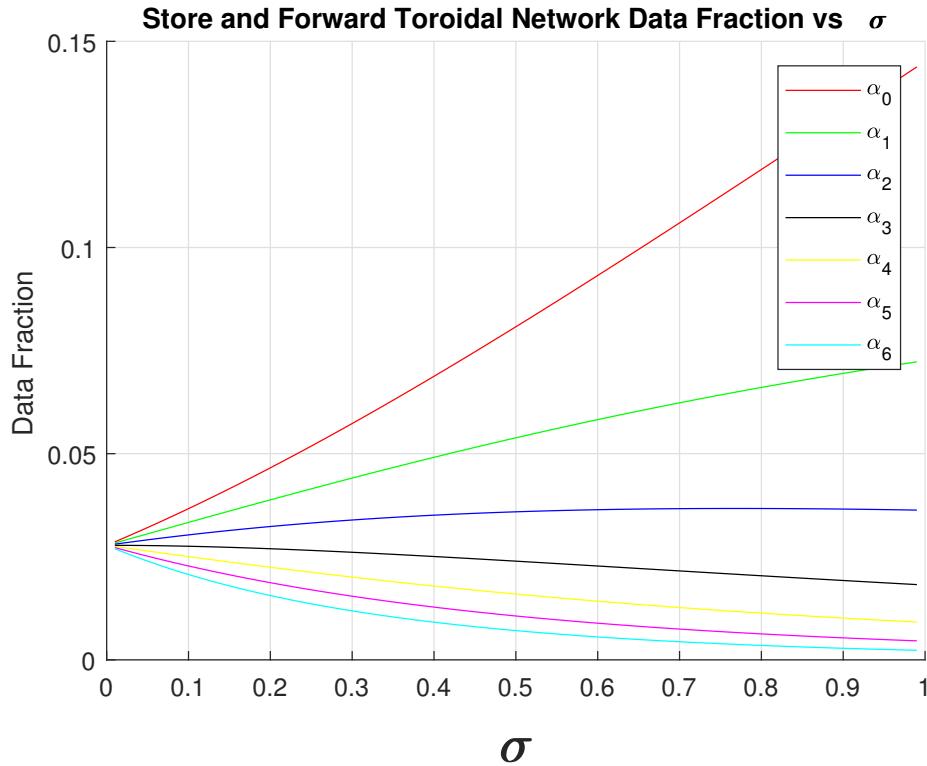


Figure 4.24: The data fraction curve of  $6 \times 6$  torus network Fig. 4.3

From Fig. 4.24, we see that as the value  $\sigma$  grows, more and more workload is assigned to the  $P_{4,2}$  and its one hop neighbors. Since there are 36 processors for  $\sigma \approx 0$  (fast communication),  $\frac{1}{36}$  of the load is assigned uniformly to each processor. That is, as the communication ability decades, the economical method is to locally process the job.

$D_i$	Number
0	1
1	4
2	8
3	8
4	4

Table 4.3:  $D_i$  vs Number of processor on  $D_i$

### 4.3.2 Sensitivity Analysis of Toroidal Rectangle Network

Considering a  $5 * n$  ( $n = 1 \dots 5$ ) toroidal rectangle network, the  $level_i$  table shows Table 4.3:

So the simulation result illustrates in Fig. 4.25

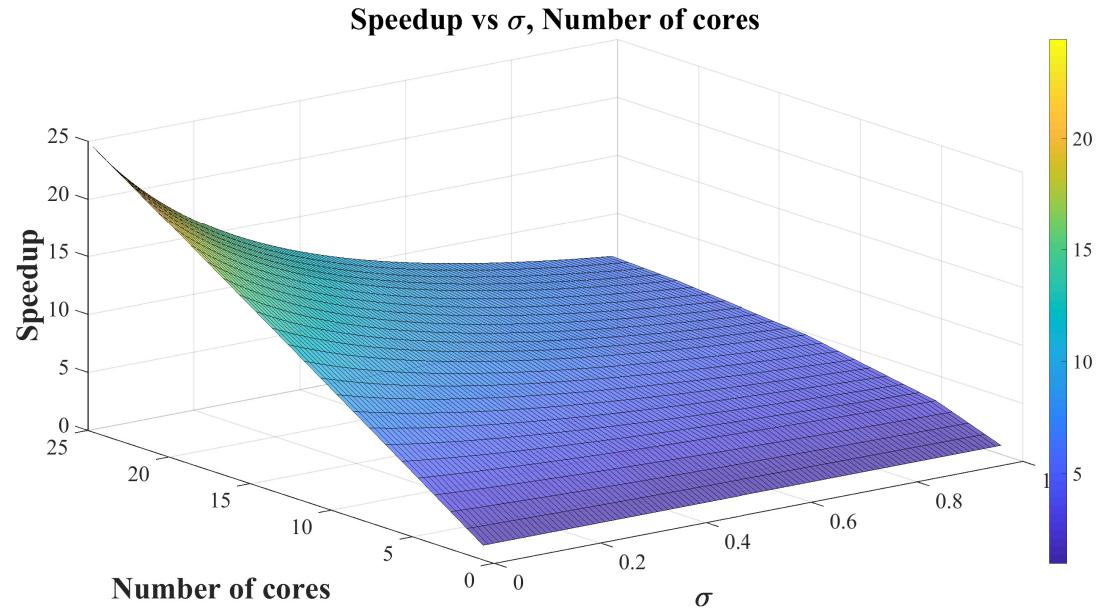


Figure 4.25: Sensitivity analysis result of  $5 * n$  torus network ( $n = 1 \cdots 5$ )

### **4.3.3 Multi-source Uniform Data Injection**

We choose the same algorithm in virtual cut-through scenario to deal with this problem.

### **4.3.4 Multi-source Non-uniform Data Injection**

We choose the same algorithm in virtual cut-through scenario to deal with this problem.

## **4.4 Comparison Result**

### **4.4.1 Comparison Result Between Mesh Network and Toroidal With Same Number of Processors**

Considering a  $5 * n$  ( $n = 1 \dots 5$ ) mesh network Fig. 2.1, the best position for data injection is  $P_{12}$ . Other positions, for example  $P_8, P_{13}$ , they don't have the same speedup efficiency. Yet, for a toroidal  $5 * 5$  regular mesh network, each position's efficiency is equal. Fig. 4.26 explores the comparison result between the toroidal and corner scenario difference.

#### 4.4.2 Comparison Result With Corner Processor and Inner Grid Processor

For a  $5 * n$  ( $n = 1 \dots 5$ ) mesh network, the inner grid position is  $P_{12}$  and the corner data injection position is  $P_0$ .

The comparing result is Fig. 4.26.

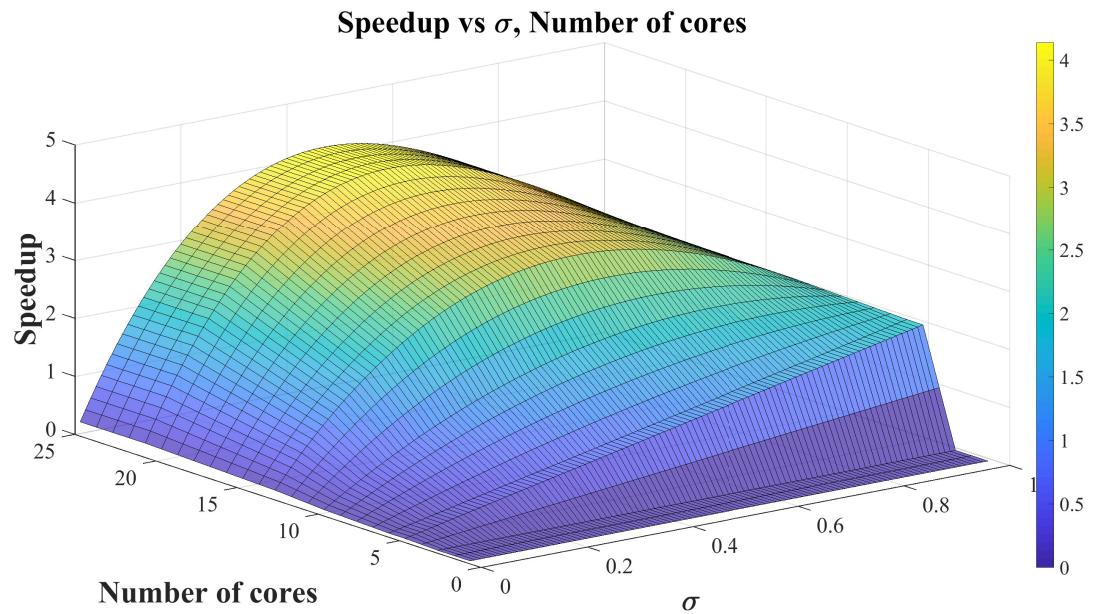


Figure 4.26: Speedup difference between corner injection and inner grid injection  $5 * n$  network ( $n = 1 \dots 5$ )

Generally speaking, Fig. 4.26 says the inner grid position scenario has better performance than the corner injection option. If the grid node is 25 and  $\sigma = 0.5$ , the speedup difference is largest, which is 4.

#### **4.4.3 Comparison Result Between Virtual Cut-through Switching Scenario and Store and Forward Scenario**

In the legend of figures, we use

- $VCT$  presents virtual cut-through switching.
- $SF$  presents store and forward switching.
- $VCT\alpha_0$  means the data fraction of  $P_0$  in virtual cut-through switching scenario.
- $SF\alpha_0$  means the data fraction of  $P_0$  in store and forward switching scenario.

#### **Data Injection On the Corner Processor**

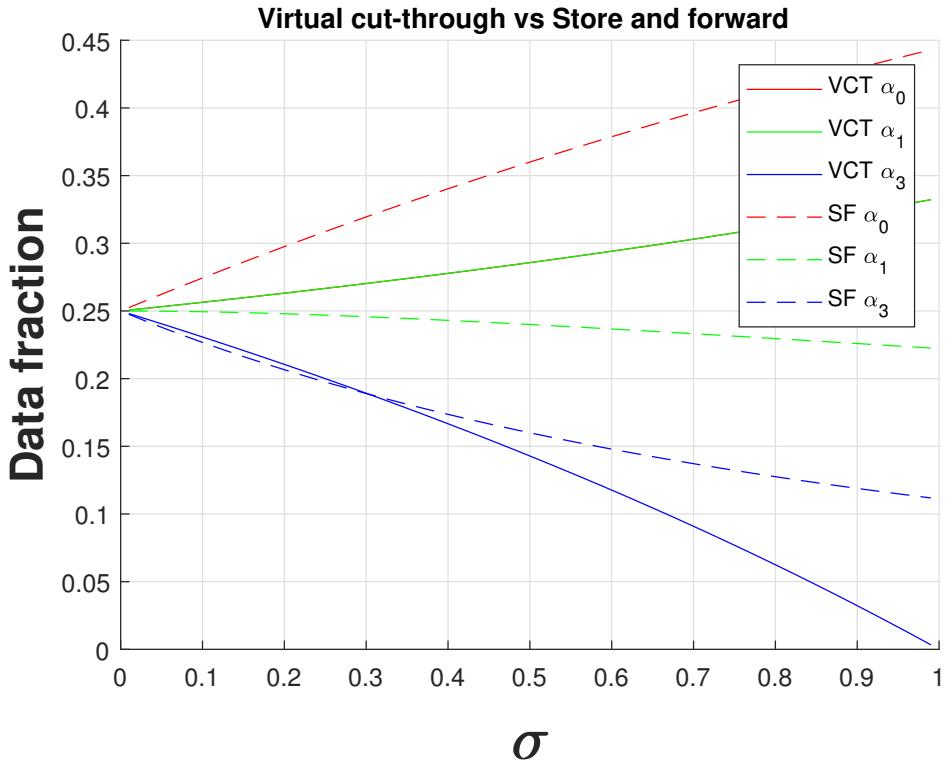


Figure 4.27: Comparing result between virtual cut-through switching and store and forward switching in  $2 \times 2$  mesh network

Fig. 4.27 says that  $P_0$  takes more of the assigned load in store and forward switching scenario than virtual cut-through switching situation. As the value of  $\sigma$  increases, the fractions that are deployed to the deeper layers decreases in both cases. In the limit condition, for example,  $\sigma = 1$ , there is no data transmitted to  $P_3$  in the virtual cut-through switching assumption, yet in the store and forward switching situation, there is still about 10% data fraction are communicated to  $P_3$ .

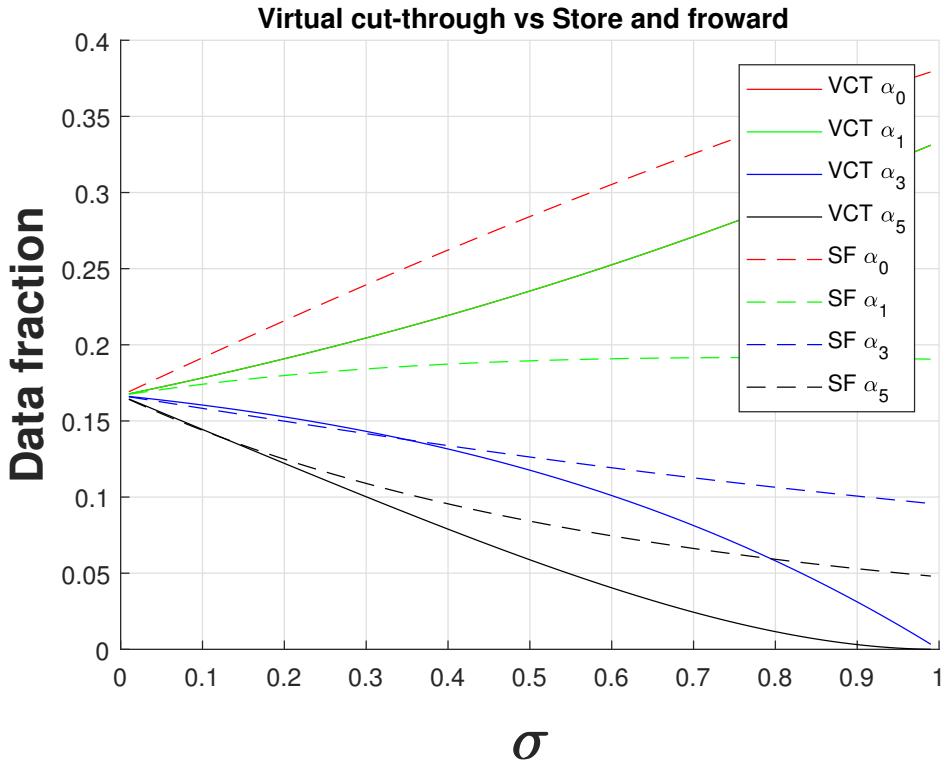


Figure 4.28: Comparing result between virtual cut-through switching and store and forward switching in  $2 * 3$  mesh network

Fig. 4.28 says that  $P_0$  takes more assigned task in store and forward switching scenario than virtual cut-through switching situation. As the value of  $\sigma$  increases, the fractions that are deployed to the deeper levels decreases. In the limit condition, for example,  $\sigma = 1$ , there is no data transmitted to  $level_3$ , that is,  $P_5$  in the virtual cut-through switching assumption. Yet in the store and forward switching situation, there is still about 5% data fraction is communicated to  $P_5$ .

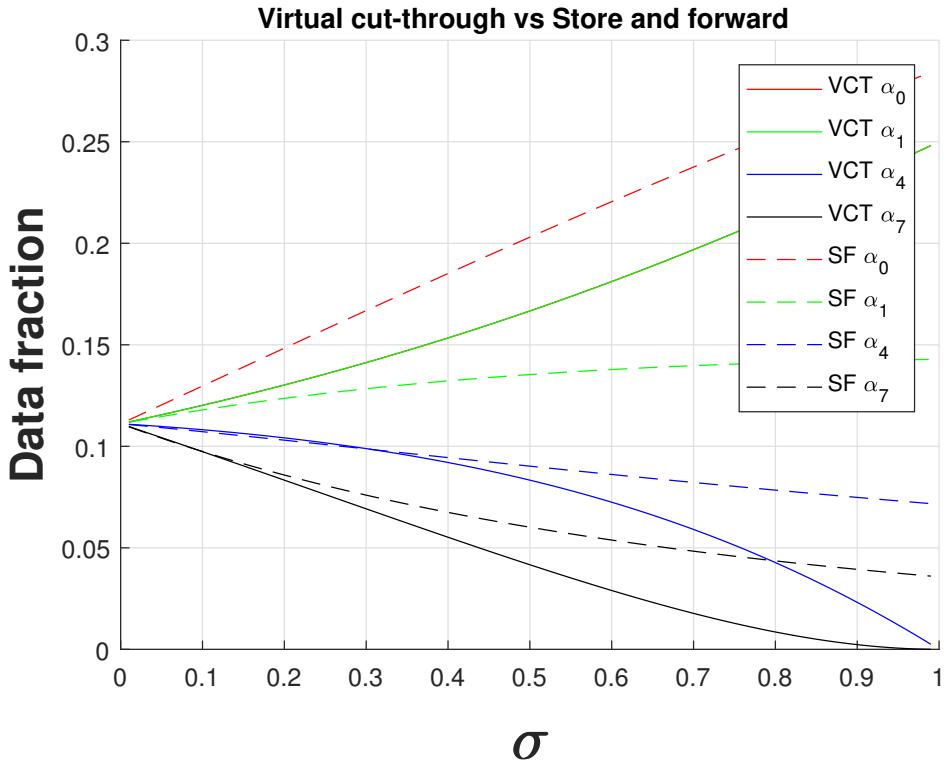


Figure 4.29: Comparing result between virtual cut-through switching scenario and store and forward switching scenario. The data injection is boundary processor of a  $3 * 3$  mesh network.

Fig. 4.29 says that  $P_0$  takes more assigned task in store and forward switching scenario than virtual cut-through switching situation. As the value of  $\sigma$  increases, the fractions that are deployed to the deeper levels decreases. In the limit condition, for example,  $\sigma = 1$ , there is no data transmitted to  $level_3$ , that is,  $P_7$  and  $P_8$  in the virtual cut-through switching assumption. Yet in the store and forward switching situation, there is still about 5% data fraction is communicated to  $P_7$  and  $P_8$ .

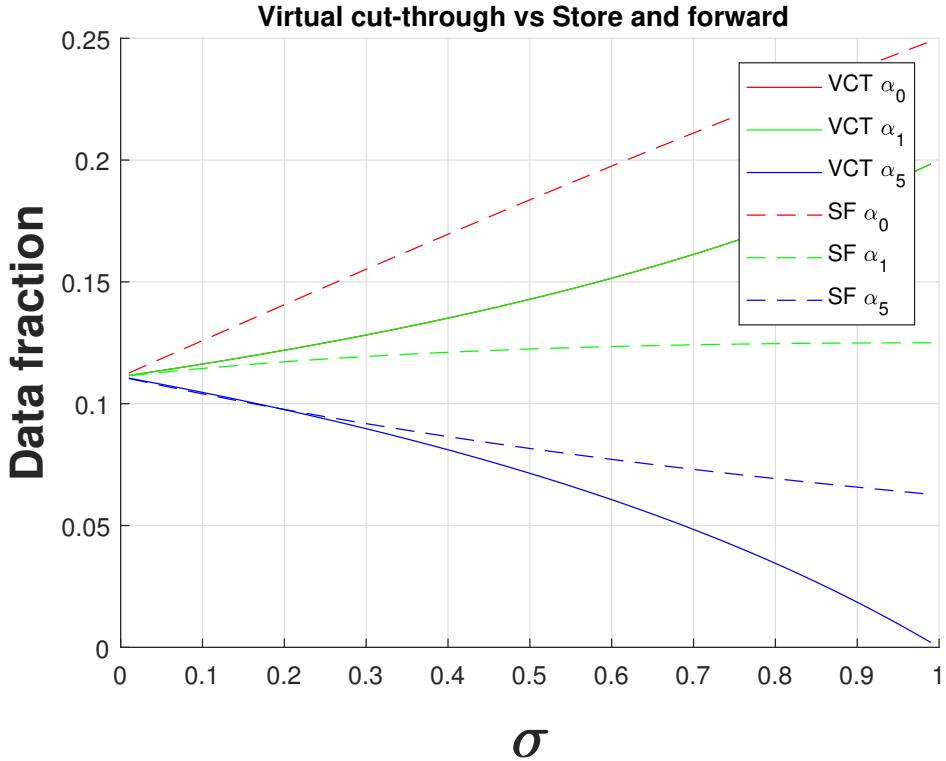


Figure 4.30: The comparing result between virtual cut-through switching processor with without virtual cut-through switching processor in  $3 \times 3$  mesh network injection on inner grid processor

Fig. 4.30 says that  $P_0$  takes more assigned task in store and forward switching scenario than virtual cut-through switching situation. As the value of  $\sigma$  increases, the fractions that are deployed to the deeper levels dropping down. In the limit condition, for example,  $\sigma = 1$ , there is no data transmitted to  $level_2$ , that is,  $P_5$ ,  $P_6$ ,  $P_7$  and  $P_8$  in the virtual cut-through switching assumption. Yet in the store and forward switching situation, there is still about 5% data fraction is communicated to  $P_5$ ,  $P_6$ ,  $P_7$  and  $P_8$ .

Comparing with Fig. 4.29,  $P_0$  takes less workload in inner grid position than boundary data injection. The reason is there are 4 neighbor processors

on the  $level_1$ , yet there is only three processors on  $level_1$  on the boundary.

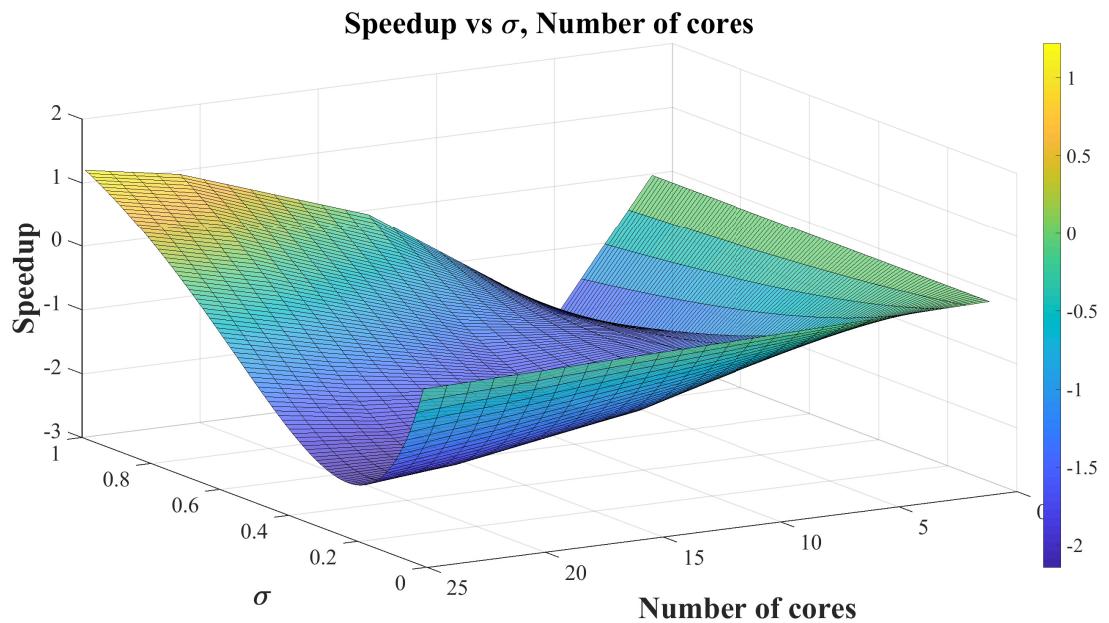


Figure 4.31: Speedup difference between store and forward switching and virtual cut-through switching in  $5 * n$  mesh network ( $n = 1 \cdots 5$ )

Fig. 4.31 shows the speedup difference between the virtual cut-through switching situation and store and forward switching scenario.

## Chapter 5

### Hypercube Network and General Network

#### 5.1 Hypercube Network Virtual Cut-through Switching Scenario

The hypercube topology has two nodes along each dimension and  $\log_2 n$  dimensions. The construction of a hypercube goes as follows, in general a  $d$ -dimensional hypercube is constructed by connecting corresponding nodes of two  $(d - 1)$  dimensional hypercubes Fig. 5.1.

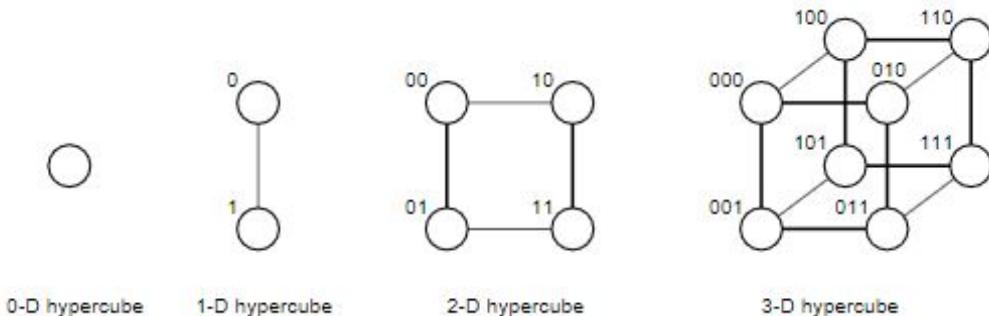


Figure 5.1: Hypercube in 0, 1, 2, 3 dimension. [1]

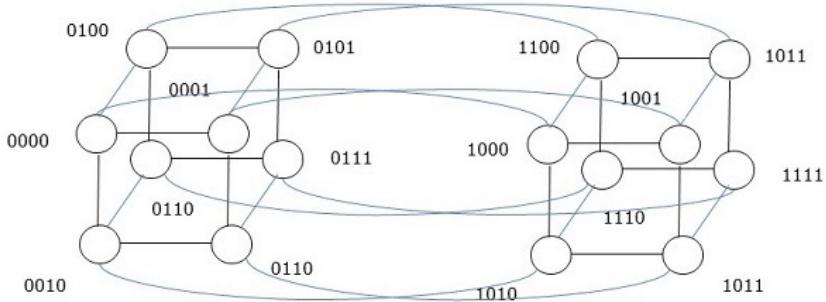


Figure 5.2: A hypercube network

### 5.1.1 Data Injection On The Grid Processor

For the hypercube of dimension  $d$  there are  $2^d$  processor in the system. Each of the processors has direct links to  $d$  neighbors. A method of naming the processors is to use label consisting of a binary string  $d-$  position long. Further, the label of a processor is a binary number from the interval  $[0, 2^d - 1]$

To address the qualitative model of computation, the critical problem is to calculate the number of processor on each  $D_i$ . Each node is connected by link and the hamming distance of their's label is 1. According to the lemma of [35],

**Lemma 5.1.1.** *In each layer  $i$  of  $d$ -dimensional hypercube, there are  $\binom{n}{i}$  processors each of which can be accessed through  $i$  communications links and is capable of transmitting to  $d - i$  still idle processors.*

According to a  $2 - D$  hypercube Fig. 3.1, the flow matrix is

$$A = \begin{bmatrix} \binom{2}{0} & \binom{2}{1} & \binom{2}{2} \\ 1 & -1 & 0 \\ 0 & \sigma - 1 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 2 & 1 \\ 1 & -1 & 0 \\ 0 & \sigma - 1 & 1 \end{bmatrix} \quad (5.1)$$

, which is investigated in Regular Network Chapter.

According to a  $3 - D$  hypercube, the flow matrix is

$$A = \begin{bmatrix} \binom{3}{0} & \binom{3}{1} & \binom{3}{2} & \binom{3}{3} \\ 1 & -1 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 \\ 0 & \sigma - 1 & \sigma & 1 \end{bmatrix} = \begin{bmatrix} 1 & 2 & 2 & 1 \\ 1 & -1 & 0 & 0 \\ 0 & \sigma - 1 & 1 & 0 \\ 0 & \sigma - 1 & \sigma & 1 \end{bmatrix} \quad (5.2)$$

The speedup is  $|- \det A|$ .

A general case,  $D$ -dimension network, the flow matrix is :

$$A = \begin{bmatrix} \binom{n}{0} & \binom{n}{1} & \binom{n}{2} & \cdots & \binom{n}{n-2} & \binom{n}{n-1} & \binom{n}{n} \\ 1 & -1 & 0 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{bmatrix}$$

## 5.2 General Case Virtual Cut-through Switching Scenario

$$\begin{bmatrix} 1 & m_1 & m_2 & \cdots & m_{n-2} & m_{n-1} & m_n \\ 1 & -1 & 0 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & 1 & \cdots & 0 & 0 & 0 \\ 0 & \sigma - 1 & \sigma & 1 & 0 & \cdots & 0 \\ 0 & \sigma - 1 & \sigma & \sigma & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & \sigma - 1 & \sigma & \cdots & \sigma & \sigma & 1 \end{bmatrix} \times \begin{bmatrix} \alpha_{l_0} \\ \alpha_{l_1} \\ \alpha_{l_2} \\ \alpha_{l_3} \\ \vdots \\ \alpha_{l_{n-1}} \\ \alpha_{l_n} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad (5.3)$$

The  $m_1, m_2, \dots, m_n$  are the number of processors on the  $level_1, level_2, \dots, level_n$ . Also, the  $\alpha_{l_0}, \alpha_{l_1}, \dots, \alpha_{l_n}$  are corresponding workload fraction.

Finally, the speedup is:

$$Speedup = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0} = |-\det A|$$

### 5.3 Hypercube Network Store and Forward Switching Scenario

According to a  $2 - D$  hypercube Fig. 3.1, the flow matrix is

$$A = \begin{bmatrix} \binom{2}{0} & \binom{2}{1} & \binom{2}{2} \\ 1 & -(\sigma + 1) & 0 \\ 1 & -\sigma & -(\sigma + 1) \end{bmatrix} = \begin{bmatrix} 1 & 2 & 1 \\ 1 & -(\sigma + 1) & 0 \\ 1 & -\sigma & -(\sigma + 1) \end{bmatrix} \quad (5.4)$$

, which is investigated in Regular Network Chapter.

According to a  $3 - D$  hypercube, the flow matrix is

$$A = \begin{bmatrix} \binom{3}{0} & \binom{3}{1} & \binom{3}{2} & \binom{3}{3} \\ 1 & -(\sigma + 1) & 0 & 0 \\ 1 & -\sigma & -(\sigma + 1) & 0 \\ 1 & -\sigma & -\sigma & -(\sigma + 1) \end{bmatrix} = \begin{bmatrix} 1 & 2 & 2 & 1 \\ 1 & -(\sigma + 1) & 0 & 0 \\ 1 & -\sigma & -(\sigma + 1) & 0 \\ 1 & -\sigma & -\sigma & -(\sigma + 1) \end{bmatrix} \quad (5.5)$$

The speedup is  $|- \det A|$ .

A general case,  $D$ -dimension network, the flow matrix is : We use  $\sigma^*$  to represents  $-(\sigma + 1)$ .

$$A = \begin{bmatrix} \binom{n}{0} & \binom{n}{1} & \binom{n}{2} & \cdots & \binom{n}{n-2} & \binom{n}{n-1} & \binom{n}{n} \\ 1 & \sigma^* & 0 & \cdots & 0 & 0 & 0 \\ 1 & -\sigma & \sigma^* & \cdots & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & \sigma^* & 0 & \cdots & 0 \\ 1 & -\sigma & -\sigma & -\sigma & \sigma^* & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ 1 & -\sigma & -\sigma & \cdots & -\sigma & -\sigma & \sigma^* \end{bmatrix}$$

## 5.4 General Case Store and Forward Switching Scenario

$$\begin{bmatrix} 1 & m_1 & m_2 & \cdots & m_{n-2} & m_{n-1} & m_n \\ 1 & -(\sigma + 1) & 0 & \cdots & 0 & 0 & 0 \\ 1 & -\sigma & -(\sigma + 1) & \cdots & 0 & 0 & 0 \\ 1 & -\sigma & -\sigma & -(\sigma + 1) & 0 & \cdots & 0 \\ 1 & -\sigma & -\sigma & -\sigma & -(\sigma + 1) & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ 1 & -\sigma & -\sigma & \cdots & -\sigma & -\sigma & -(\sigma + 1) \end{bmatrix} \times \begin{bmatrix} \alpha_{l_0} \\ \alpha_{l_1} \\ \alpha_{l_2} \\ \alpha_{l_3} \\ \vdots \\ \alpha_{l_{n-1}} \\ \alpha_{l_n} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} \quad (5.6)$$

The  $m_1, m_2, \dots, m_n$  are the number of processors on the  $level_1, level_2, \dots, level_n$ . Also, the  $\alpha_{l0}, \alpha_{l1}, \dots, \alpha_{ln}$  are corresponding workload fraction.

The speedup is

$$Speedup = \frac{T_{f,0}}{T_{f,n}} = \frac{\omega T_{cp}}{\alpha_0 \omega T_{cp}} = \frac{1}{\alpha_0} = \frac{\det A}{\det A^*} = \left| \frac{\det A}{(\sigma^*)^{n-1}} \right|$$



# **Chapter 6**

## **Conclusion and Future work**

### **6.1 Conclusion**

In this work we investigate two problems. One problem is closed-form solutions for equivalence computation of divisible workload in mesh and toroidal networks and the other problem is scheduling divisible workloads from multiple sources in mesh and toroidal networks of processors.

We propose a flow matrix closed-form equation to present the equivalence, which allows a characterization of the nature of minimal time solution and a simple method to determine when and how much load to distribute for processors.

Also, we propose the use of a reduced Manhattan distance Voronoi diagram algorithm (RMDVDA) to minimize the overall processing time of these workloads by taking advantage of the processor equivalence technique. Three case studies with 10 sources of workloads are presented to illustrate the general approach for multiple sources of workloads.

In the first phase, a Manhattan distance Voronoi diagram is used to obtain a network cluster division. In the second phase, we propose an efficient algorithm to obtain near-optimal load distribution among processors represented by equivalent processors. The algorithm minimizes the number of processors

utilized.

Various factors, for example data injection position, data injection fraction, virtual cut-through switching and store and forward switching, the ratio of computation time over communication time, that influence the load distribution are shown in the numerical experiment. Experimental evaluation through simulations demonstrates that a task can be finished in the same sub-optimal time and yet save over 30% of processor resources in mesh network and 11% – 17% in toroidal network.

## 6.2 Future Work

There are three future projects need to pay attention.

- Given virtual cut-through and store and forward scenario, the hypercube network multi-source suboptimal algorithm minimize the makespan.
- Given data injection workload, which are some dynamic workload queues, how to find the suboptimal algorithm to minimize the makespan.
- Given the workload fractions distribution, how to choose the appropriate data injection positions. The objective to minimize the cost function, which has relationship with Earth Mover Distance [30] and Wasserstein Distance [36].
- Other topology networks, for example connected cubic network graph [37], heterogeneous networks [38], Gaussian network [39] .
- Other constrain assumption, for example the front-end processor with finite-size buffer.

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