```
** EE140 Lab3 : CMOS Operational Amplifier Design **

.lib 'model_ee140_1.sp' TT

** Circuit Netlist **

   ** Power Supplies/Sources **

      V1 vdd 0 dc=1.5 ac=0
      Vcm cm 0 dc=0.75

      * Differential Voltage *
        Vid1 cm gate_M3 ac=1
        Vid2 gate_M5 cm ac=1

      * Transient Analysis
        *Vid1 cm gate_M3 SIN(0 0.00009 1000 0 0 0)
        *Vid2 cm gate_M5 SIN(0 0.00009 1000 0 0 180)

      * Common Mode Analysis
        *Vid2 cm gate_M5 ac=1

      * Output Swing Analysis and Common Mode Input Range
        *Vswp swp 0 dc=0.75

      * Settling time analysis
        Vpul pul 0 PULSE(0.5 0.9 0.1p 0.1p 0.1p 50n 100n)

 ** End Power Supplies/Sources**

*** Amplifier ***

   ** First Stage **

        * Transistors *

        x7 tail vbias vdd vdd pmos l=130n w=86905n
              x3 drain_M2 out_2 tail vdd pmos l=130n w=138775n
              x5 out_1 pul tail vdd pmos l=130n w=138775n
              x2 drain_M2 drain_M2 0 0 nmos l=130n w=9230n
              x4 out_1 drain_M2 0 0 nmos l=130n w=9230n

   ** End First Stage **

   ** Second Stage **

        * Transistors *

              x6 out_2 out_1 0 0 nmos l=130n w=17420n
              x9 out_2 vbias vdd vdd pmos l=130n w=86905n

              * End Transistors *

   ** End Second Stage **

   * Biasing *

           * Transistors *
        x1 vbias vbias vdd vdd pmos l=130n w=41080n

        * End Transistors *

        * Resistors *

                   Rbias vbias 0 6k

        * End Resistors *

* End Biasing *

* Compensation/Loading *

        * Capacitors *

        CL out_2 0 2p
                    Cc node out_2 2p

        * End Capacitors *

  * RHP Zero Linear Resistor *

  xR node vdd out_1 out_1 nmos l=130n w=1040n
```

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          * End Linear Resistor

** End Circuit Netlist **

** Analysis **
   .TF V(out_2) Vid1
   .op
   .TRAN 1n 150n
   *.ac dec 10 10 2000meg

* Output Swing
  *.DC Vswp 0.749 0.751 0.00001

* Common Mode Input Range
   *.DC Vswp 0 1.5 0.0001

** End Analysis


** Control Information **

   .options post=2 nomod

** End Control Information **
.END
```