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EE140 Operational Amplifier

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1 Introduction

As the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers in CMOS technology becomes more critical. This technology has become an integral part of many integrated circuit chips fabricated today in a number of application areas. These amplifiers offer a number of advantages in terms of power dissipation, die area, and compatibility with digital circuits when compared to their bipolar counterparts.

In this paper we design and simulate a specific, widely used operational amplifier architecture, showing in detail how the formulation of the design variables takes place through a number of equations derived and calculated by hand. We then simulate the amplifier using HSPICE, presenting performance measures such as unity-gain bandwidth, open-loop gain, and settling time. We show how the proposed amplifier meets the specifications set in place by the project guidelines. We conclude with a discussion of the characteristics of the amplifier and the overall experience of the design project.

1.1 Circuit Schematic

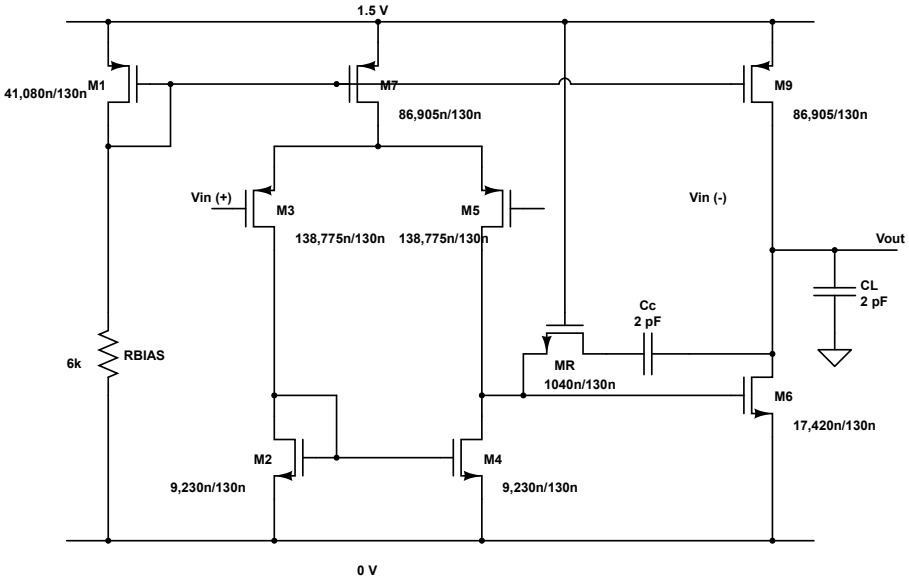

Figure 1: Two stage op-amp considered in this paper.

2 Part I: Hand Analysis

For the purposes of designing this amplifier, the design approach is as follows. First, we lay the groundwork for all important equations that must be considered in order to meet the specifications. We note dependencies and realize variables that enable design control. We then begin with the most rigorous specifications and choose our variables to be within margins that exceed the requirements, to provide a safety cushion against non-idealities. We keep all constraints in mind and finalize a design. We confirm that the requirements are met.

2.1 Equations

In this section, all of the relevant equations required to meet the specifications are listed for the purposes of demonstrating the interdependencies between variables and to illustrate the design process of the amplifier.

Specifications to be met:

- Gain ≥ 1500
- Output Swing : 1.2V
- Settling Time : 8ns with 0.4V step
- Unity Gain Frequency $\geq 600MHz$
- Common Mode Input Range: 0.8V
- CMRR $\geq 75dB$
- PSRR $\geq 60dB|_{DC}$ $50dB$ at 1MHz
- Power Dissipation: 1.5mW

2.1.1 Settling Time

To meet this specification, we will design our amplifier to have a slew rate that is one tenth of the settling time. Although this is not a one to one correspondence with the specification, settling time and slew rate are closely related, and achieving the above margin is a good indication that the spec has been met.[1]

$$SR = \frac{10V_0}{T_{s|0.1\%}}$$
$$T_{s|0.1\%} = 8ns \quad with \quad 0.4VStep$$
$$SR = \frac{10(0.4)}{8ns}$$
$$SR = 500\frac{V}{\mu S}$$
$$SR = \frac{I_{xm}}{C}$$
$$\boxed{\frac{I_{xm}}{C} \geq 5 \times 10^8 V/s}$$

where C is the largest capacitance in the circuit, and Ixm is the limiting current.

2.1.2 Unity Gain Frequency

$$ugf = \frac{gm_I}{C}$$
$$ugf = 2\pi 600MHz$$
$$\boxed{\frac{gm_I}{C} \geq 2\pi 600MHz}$$

2.1.3 Phase Margin

Phase margin, settling time, and unity gain frequency are all closely related and impact the stability of the circuit in feedback. Aiming for a target phase margin that is conducive to meeting the above two specs,

$$PM = 60^\circ$$
$$\omega_{p2} \geq tan(60) \times 2\pi 600Mhz$$
$$\boxed{\frac{gm_{II}}{C_I + C_{II}} \geq tan(60) \times 2\pi 600MHz}$$

[1] C. T. Nguyen, Lecture 24, April 25, 2013

2.1.4 Gain

Total Gain: $A_v = A_{v_1} A_{v_2}$

$$A_{v_1} = gm_3 \left(\frac{\frac{V_{A4}}{I_{D3}} \frac{V_{A5}}{I_{D3}}}{\frac{V_{A4}}{I_{D3}} + \frac{V_{A5}}{I_{D3}}} \right) \qquad A_{v_2} = -gm_6 \left(\frac{\frac{V_{A6}}{I_{D6}} \frac{V_{A9}}{I_{D6}}}{\frac{V_{A6}}{I_{D6}} + \frac{V_{A9}}{I_{D6}}} \right)$$

$$A_v = \frac{-gm_3 gm_6}{I_{D3} I_{D6}} \left(\frac{V_{A4} V_{A5}}{V_{A4} + V_{A5}} \right) \left(\frac{V_{A6} V_{A9}}{V_{A6} + V_{A9}} \right) [2]$$

Using the relation $\frac{gm}{I_D} = \frac{2}{r_0}$ gives us

$$A_v = \frac{-4}{V_{ov3} V_{ov6}} \left(\frac{\frac{1}{\lambda_n} \frac{1}{\lambda_p}}{\frac{1}{\lambda_n} + \frac{1}{\lambda_p}} \right)^2$$

$$A_v = \frac{32.65}{V_{ov3} V_{ov6}}$$

$$\boxed{\frac{32.65}{V_{ov3} V_{ov6}} \geq 1500}$$

2.1.5 Output Swing

In order to satisfy an output swing of 1.2V we must satisfy the following:

$$V_{out,max} = V_{DD} - V_{ov_9} = 1.35V$$

$$V_{out,min} = V_{ov_6} = 0.15V$$

$$\boxed{V_{ov9} \leq 0.15V}$$

$$\boxed{V_{ov6} \leq 0.15V}$$

[2] Paul Gray, Robert Meyer, "Analysis and Design of Analog Integrated Circuits" (Wiley and Sons, 2010), 423

2.1.6 Common Mode Rejection Ratio

$$\text{CMRR} = |\frac{A_{dm}}{Acm}|$$

The common mode rejection ratio is only dependent upon the first stage of the amplifier, because the second stage is a single ended input and output.

$$\begin{aligned}\text{CMRR} &= 2gm_3r_{07}gm_2(r_{03}||r_{02}) \\ &= \frac{4}{V_{ov3}V_{ov2}}\left(\frac{\frac{1}{\lambda_n}\frac{1}{\lambda_p}}{\frac{1}{\lambda_n}+\frac{1}{\lambda_p}}\right)\end{aligned}$$ [3]

$$\boxed{\frac{11.43}{V_{ov3}V_{ov2}} \geq 75dB}$$

2.1.7 Power Supply Rejection Ratio

In calculating the PSRR, we will neglect the variations due to the positive supply, V_{DD}. This is because $PSRR_+ \to \infty$ for low frequencies with perfect matching [4]. This analysis is shown in G&M page 431.

Instead, we will calculate the PSRR that emerges due to variations from the V_{SS} supply, which in this case is ground.

$$A_- = \frac{v_o}{vss} = \frac{r_{09}}{r_{06}+r_{09}} = \frac{\frac{1}{\lambda_p}}{\frac{1}{\lambda_n}+\frac{1}{\lambda_p}}$$ [5]

$$PSRR = \frac{A_{dm}}{A_-}$$

$$\boxed{\frac{A_{dm}}{0.5714} \geq 60dB}$$

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[3] Paul Gray, Robert Meyer, "Analysis and Design of Analog Integrated Circuits" (Wiley and Sons, 2010), 427

[4] Paul Gray, Robert Meyer, "Analysis and Design of Analog Integrated Circuits" (Wiley and Sons, 2010), 431

[5] Paul Gray, Robert Meyer, "Analysis and Design of Analog Integrated Circuits" (Wiley and Sons, 2010), 431

2.1.8 Common Mode Input Range

When V_{IC} is reduced to the point where $V_{GD_3} = V_{GD_5} = V_{t_3} = V_{t_5}, M3$ and $M5$ operate at the edge of saturation. Thus, we define the lower end of the common mode input range to be :

$$V_{IC} \geq V_{t_3} + V_{t_2} + V_{ov_2}$$
$$V_{IC} \geq V_{ov_2}$$

The specification calls for a common mode input range that is $0.8V$ inside the output swing range. This gives us a constraint on V_{ov_2}

$$V_{IC_{min}} = 0.125V$$
$$\boxed{V_{ov_2} \leq 0.125V}$$

If V_{IC} is too high, we have $M7$ falling into the triode region. Examining the drain voltage of $M7$,

$$V_{DS_7} = V_{IC} - V_{GS_3} - V_{DD} = V_{IC} - V_{t3} - V_{ov_3} - V_{DD}$$

Therefore, V_{IC} must satisfy the following:

$$V_{IC} < V_{DD} - |V_{t_3}| - |V_{ov_3}| - |V_{ov_7}|$$
$$V_{IC} < 1.5 - 0.3 - |V_{ov_3}| - 0.15$$
$$V_{IC} < 1.05 - |V_{ov_3}|$$

From the specification,

$$V_{IC_{max}} = 0.925V$$
$$0.925 < 1.05 - |V_{ov_3}|$$
$$\boxed{|V_{ov_3}| < 0.125}$$

2.2 Design Equations and Sizing

In this section, we illustrate the design process of the amplifier. With the knowledge of the equations and constraints, we are able to make design decisions. These design decisions are based partly on intelligent speculations and in a large part on the equations and constraints. We complete the design with dimensions for each transistor and the value of the compensating capacitor, C_c. Assume all bulks are tied to the sources.

For consistency with the load capacitance, we choose C_c to be 2pF. This gives us the following:

2.2.1 Slew Rate

$$\frac{I_{xm}}{2pF} \geq 500000000$$

$$I_{xm} \geq 1mA$$

2.2.2 Unity Gain Frequency

$$\frac{gm_I}{2pF} \geq 2\pi 600MHz$$

$$gm_I \geq 7.53mS$$

2.2.3 Output Swing

$$V_{ov9} \leq 0.15V$$

$$V_{ov6} \leq 0.15V$$

To have a comfortable margin, we set $V_{ov6,9} = 0.09V$

2.2.4 Gain

$$\frac{32.65}{V_{ov3}V_{ov6}} \geq 1500$$

With $V_{ov6} = 0.09$,

$$v_{ov3} \leq 0.24V$$

To reduce capacitances and minimize power and current consumption, set all channel lengths to the minimum value, $L_{min} = 130nm$.

2.2.5 Sizing of M7, M9

As we can see from the settling time constraint, the circuit requires the maximum current we have available given the power restriction. With this in mind, we choose a reasonable value from experience and set the current through M9 and M7 to be 400 microamps and bias the output at half of the supply voltage. In addition, we match transistors 7 and 9 to ensure that the settling time specification is met, since both transistors supply current through large capacitors.

$$0.5k'_p(W/L)(V_{ov})^2(1 + 0.15(V_{SD}) = 400\mu A$$

$$0.5k'_p(W/L)(0.09)^2(1 + 0.15(0.75) = 400\mu A$$

$$W/L_{7,9} = 86905/130$$

2.2.6 Sizing of M1

In order to meet the power dissipation requirement, the current through M1 must be no more than 200 microamps. To ensure that we minimize power consumption, we bias M1 to draw 180 microamps.

$$0.5k'_p(W/L)(V_{ov})^2(1 + 0.15(V_{ov} + V_t) = 180\mu A$$

$$0.5k'_p(W/L)(0.09)^2(1 + 0.15(0.39) = 180\mu A$$

$$W/L_1 = 41102/130$$

2.2.7 Sizing of M3, M5

$$gm_3 = \sqrt{2k'_pW/L(I_D)})$$

$$0.00753 = \sqrt{2k'_pW/L(200\mu A)})$$

$$W/L_{3,5} = 138763/130$$

2.2.8 Sizing of M2, M4

From common mode input range,

$$V_{ov2,4} \leq 0.125V$$

At equality we have,

$$0.5k'_n(W/L)(V_{ov})^2(1 + 0.2(V_{DS}) = 200\mu A$$

The drain-source voltage of M4 is equal to its gate-source voltage at DC since M2 is diode connected. With this in mind,

$$0.5k'_n(W/L)(0.125)^2(1 + 0.2(0.425) = 200\mu A$$

$$W/L_{2,4} = 9238/130$$

2.2.9 Sizing of M6

$$0.5k'_n(W/L)(V_{ov})^2(1 + 0.2(0.75) = 400\mu A$$

$$0.5k'_n(W/L)(0.09)^2(1 + 0.2(0.75) = 400\mu A$$

$$W/L_6 = 17433/130$$

2.2.10 RHP Zero

We want to set the resistor, R_z, to a value such that the zero introduced by the circuit is pushed out to infinity. To do this we set,

$$R_z = 1/gm_{II}$$

$$gm_{II} = k'_n W/L(V_{ov}) = 6mS$$

However, from experience we know that in simulation this transconductance will increase. To design for a safe margin of error, we use a value of gm on the order of $7.6mS$.

$$R_z = 131\Omega$$

$$R_z = L/(Wk'_n(V_{GS} - V_t))$$

$$W/L_r = 973/130$$

2.2.11 Frequency Response

We would like to impart a phase margin of 60 degrees or better to offer a circuit that is stable under unity gain feedback and yields a quick settling time for sharp rising signals. To this end, we must push the second pole out past the value shown in the equations section above. In order to satisfy this, we must meet the following constraint,

$$C_I + C_{II} \leq 1.16 \times 10^{-12}$$

The calculations involving the derivation of the capacitances is shown in a MATLAB script below and we can see that the requirement is met. We have included the estimated areas and relevant perimeters of the drain and source of the transistors as per the project guidelines.

Contents


```
% Frequency Response MATLAB Script
```

Derivation of all parameter values

```
mu_n = 0.025; % units: m^2/(Vs)
mu_p = 0.010; % units: m^2/(Vs)

e_ox = 3.9*8.854E-12; % units: F/m
t_ox = 2.6E-9; % units: m

c_ox = e_ox/t_ox; % units: F/m^2

k_n = mu_n*c_ox; % units: A/V^2
k_p = mu_p*c_ox; % units: A/V^2
```

Determination of all parasitics

```
% relevant parasitic capacitances: cgd4, cdb4, cgd5, cdb5, cgs6, cgd6,
% cdb6, cgd9, cdb9, cdb_r, cgs_r, csb_r, cgd_r
syms W4 L4 W5 L5 W6 L6 W9 L9 W_r L_r vdb4 vdb5 vdb6 vdb9 av_II

% Device Dimensions

W3 = 138763E-9;
L3 = 130E-9;
W5 = W3;
L5 = 130E-9;
W9 = 86905E-9;
L9 = 130E-9;
W6 = 17433E-9;
L6 = 130E-9;
vdb4 = 0.12;
vdb5 = 0.12;
vdb6 = 0.75;
vdb9 = 0.75;
gm_II = 7.6E-3;
ro_6 = 1/(0.2*400E-6);
ro_9 = 1/(0.15*400E-6);
rout = (1/ro_6+1/ro_9)^(-1);
av_II = gm_II*rout;
W_r=973E-9;
L_r=130E-9;
W4=9238E-9;
L4 =130E-9;
```

```
% Device Capacitances

c_j = 8E-4; % units: F/m^2
c_jsw = 8E-10; % units: F/m
LD = 2.5E-8; % units: m

% gate-drain
cgd4 = W4*LD*c_ox; % units: F
cgd5 = W5*LD*c_ox; % units: F
cgd6 = W6*LD*c_ox; % units: F
cgd9 = W9*LD*c_ox; % units: F
cgd_r = W_r*LD*c_ox; % units: F

% gate-source
cgs6 = (2/3)*W6*L6*c_ox + cgd6; % units: F
cgs_r = (2/3)*W_r*L_r*c_ox + cgd_r; % units: F


% drain-body & source-body

lambda_4 = L4/2; % units: m
lambda_5 = L5/2; % units: m
lambda_6 = L6/2; % units: m
lambda_9 = L9/2; % units: m
lambda_r = L_r/2; % units: m

cdb4 = ( W4*(5*lambda_4)*c_j + (W4 + 2*(5*lambda_4))*c_jsw ) / sqrt(1+vdb4/0.8); % u
cdb5 = ( W5*(5*lambda_5)*c_j + (W5 + 2*(5*lambda_5))*c_jsw ) / sqrt(1+vdb5/0.8); % u
cdb6 = ( W6*(5*lambda_6)*c_j + (W6 + 2*(5*lambda_6))*c_jsw ) / sqrt(1+vdb6/0.8); % u
cdb9 = ( W9*(5*lambda_9)*c_j + (W9 + 2*(5*lambda_9))*c_jsw ) / sqrt(1+vdb9/0.8); % u
csb_r = ( W_r*(5*lambda_r)*c_j + (W_r + 2*(5*lambda_r))*c_jsw ); % units: F
```

Equations

```
C_I = cdb5 + cdb4 + cgd4 + cgd5 + cgs_r + cgs6 + csb_r + cgd6*(1+av_II);
C_II = cdb6 + cdb9 + cgd9 + cgd6 + cgd_r;

% Approximations:

% C_I = cgd4 + cgd5+ cgs6 + (1+av_II)*cgd6;
% C_II = cgd6 + cgd9;
```

Final Result

```
C_I_plus_C_II = C_I + C_II
```

```
C_I_plus_C_II =

   6.6042e-13
```

Published with MATLAB® 7.12

3 Part II: Simulation

We go from the design parameters we have just derived and simulate the op-amp in hspice. We make adjustments to certain dimensions as necessary for biasing. For instance, the widths of all transistors must be adjusted slightly such that they comply with the 65nm technology used for this design.

We have met all of the specifications called for and have done so adequately. Graphs, tables and simulated values are now shown to substantiate the performance of this op-amp.

3.1 Transistor and Bias Summary

3.1.1 Biasing and small signal parameters

As we can see, all bias currents are within 10% of hand calculated values. The overdrive voltage of $M1, 7, 9$ were further reduced to increase efficiency.

```
Using: /bin/time /share/instsww/synopsys/C-2009.09/hspice/sparcOS5/hspice CMOS2.sp
 ****** HSPICE -- C-2009.09 32-BIT (Aug 24 2009) sunos ******
  Copyright (C) 2009 Synopsys, Inc. All Rights Reserved.
  Unpublished-rights reserved under US copyright laws.
  This program is protected by law and is subject to the
  terms and conditions of the license agreement from Synopsys.
  Use of this program is your acceptance to be bound by the
  license agreement. HSPICE is the trademark of Synopsys, Inc.
  Input File: CMOS2.sp
 lic:
 lic: FLEXlm: v8.5b
 lic: USER:   ee140-cw             HOSTNAME: quasar
 lic: HOSTID: 83846a81             PID:      29407
 lic: Using FLEXlm license file:
 lic: 27005@license-srv.eecs.berkeley.edu
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 25-oct-2013/2012.06
 lic: FLOATING license(s) on SERVER license-srv.eecs.berkeley.edu
 lic:
 Init: read install configuration file: /share/instsww/synopsys/C-2009.09/hspice/meta.cfg
1****** HSPICE -- C-2009.09 32-BIT (Aug 24 2009) sunos ******
 ******
 b1;2c** ee140 lab3 : cmos operational amplifier design **

  ******  circuit name directory
 circuit number to circuit name directory
   number circuitname                    definition         multiplier
        0 main circuit
        1 x7.                            pmos               1.00
        2 x3.                            pmos               1.00
        3 x5.                            pmos               1.00
        4 x2.                            nmos               1.00
        5 x4.                            nmos               1.00
        6 x6.                            nmos               1.00
        7 x9.                            pmos               1.00
        8 xr.                            nmos               1.00
        9 x1.                            pmos               1.00
 **warning** (model_ee140_1.sp:14) both nodes of element x2.csubn defined in subckt nmos            are connected together.


 **diagnostic** set option symb=1 internally to help for convergence.
 ************************************************************************
 ******  option summary
 ******
 runlvl  = 3         bypass  = 2
  Opening plot unit= 15
 file=CMOS2.pa0

1****** HSPICE -- C-2009.09 32-BIT (Aug 24 2009) sunos ******
 ******
 b1;2c** ee140 lab3 : cmos operational amplifier design **

  ******  operating point information tnom=  25.000 temp=  25.000 *****
 ***** operating point status is all       simulation time is     0.
    node    =voltage      node    =voltage      node    =voltage

 +0:cm      = 950.0000m 0:drain_m2= 401.9613m 0:gate_m3 = 950.0000m
 +0:gate_m5 = 950.0000m 0:node    = 401.9613m 0:out_1   = 401.9613m
 +0:out_2   = 933.4493m 0:tail    =   1.3126  0:vbias   =   1.1236
 +0:vdd     =   1.5000


 ****  voltage sources

 subckt
 element  0:v1       0:vcm      0:vid1     0:vid2
  volts      1.5000   950.0000m    0.         0.
  current -980.3783u    0.         0.         0.
  power      1.4706m    0.         0.         0.

     total voltage source power dissipation=    1.4706m       watts


 **** resistors

 subckt
 element  0:rbias
  r value    6.0000k
  v drop     1.1236
  current  187.2650u
  power    210.4092u
```

```
**** mosfets


subckt   x7         x3         x5         x2         x4         x6
element  1:m0       2:m0       3:m0       4:m0       5:m0       6:m0
model    1:pmos_int 2:pmos_int 3:pmos_int 4:nmos_int 5:nmos_int 6:nmos_int
region     Saturati   Saturati   Saturati   Saturati   Saturati   Saturati
 id      -384.6046u -192.3023u -192.3023u  192.3023u  192.3023u  408.5087u
 ibs        0.         1.8741f    1.8741f    0.         0.         0.
 ibd        1.8741f   10.9804f   10.9804f   -4.0196f   -4.0196f   -9.3345f
 vgs     -376.4098m -362.5871m -362.5871m  401.9613m  401.9613m  401.9613m
 vds     -187.4129m -910.6258m -910.6258m  401.9613m  401.9613m  933.4493m
 vbs        0.       187.4129m  187.4129m    0.         0.         0.
 vth     -300.0000m -322.5532m -322.5532m  300.0000m  300.0000m  300.0000m
 vdsat    -67.8811m  -36.0201m  -36.0201m   90.6678m   90.6678m   90.6678m
 vod      -76.4098m  -40.0339m  -40.0339m  101.9613m  101.9613m  101.9613m
 beta     148.4499m  266.8115m  266.8115m   41.6572m   41.6572m   88.4927m
 gam eff  200.0000m  200.0000m  200.0000m  200.0000m  200.0000m  200.0000m
 gm        10.0769m    9.6106m    9.6106m    3.7770m    3.7770m    8.0234m
 gds       59.3594u   32.7517u   32.7517u   41.8227u   41.8227u   87.7737u
 gmb        1.2661m    1.0709m    1.0709m  470.4566u  470.4566u  999.3933u
 cdtot     52.2643f   74.0037f   74.0037f    5.3447f    5.3447f    9.4365f
 cgtot    119.2690f  190.4558f  190.4558f   12.6673f   12.6673f   23.9073f
 cstot    116.1417f  181.7564f  181.7564f   12.3389f   12.3389f   23.2838f
 cbtot     49.1370f   65.3043f   65.3043f    5.0163f    5.0163f    8.8129f
 cgs       90.4137f  144.3779f  144.3779f    9.6027f    9.6027f   18.1233f
 cgd       28.8553f   46.0779f   46.0779f    3.0647f    3.0647f    5.7840f


subckt   x9         xr         x1
element  7:m0       8:m0       9:m0
model    7:pmos_int 8:nmos_int 9:pmos_int
region     Saturati     Linear   Saturati
 id      -408.5087u    0.      -187.2650u
 ibs        0.         0.         0.
 ibd        5.6655f  3.609e-25    3.7641f
 vgs     -376.4098m    1.0980  -376.4098m
 vds     -566.5507m -927.1472f -376.4098m
 vbs        0.         0.         0.
 vth     -300.0000m  300.0000m -300.0000m
 vdsat    -67.8811m  722.9214m  -67.8811m
 vod      -76.4098m  798.0387m  -76.4098m
 beta     157.6764m    4.3164m   72.2807m
 gam eff  200.0000m  200.0000m  200.0000m
 gm        10.7032m    0.         4.9065m
 gds       66.9674u    3.4447m   29.7707u
 gmb        1.3448m    0.       616.4566u
 cdtot     49.0984f    1.2098f   23.8729f
 cgtot    119.2690f    1.7956f   56.3785f
 cstot    116.1417f    1.2098f   54.9024f
 cbtot     45.9711f  624.0000a   22.3969f
 cgs       90.4137f  897.8202a   42.7386f
 cgd       28.8553f  897.8202a   13.6399f




****     small-signal transfer characteristics

     v(out_2)/vid1                          =    6.6453k
     input resistance at             vid1   =  1.000e+20
     output resistance at v(out_2)          =    6.4624k



         ***** job concluded
1****** HSPICE -- C-2009.09 32-BIT (Aug 24 2009) sunos ******
 ******
 b1;2c** ee140 lab3 : cmos operational amplifier design **

  ******  job statistics summary tnom=  25.000 temp=  25.000 *****

  ******  HSPICE Threads Information  ******

  Command Line Threads Count                :     1
  Available CPU Count                       :     4
```

Figure 2: Summary of biasing and small signal parameters simulated in hspice

3.1.2 Transistor Dimensions

All transistor sizes are within 10% of the expected values from the hand calculations.

Transistor	Width	Length	———
$M1$	$41,080$nm	130nm	
$M2$	9230nm	130nm	
$M4$	9230nm	130nm	
$M3$	$138,775$nm	130nm	
$M5$	$138,775$nm	130nm	
$M6$	$17,420$nm	130nm	
$M7$	$86,905$nm	130nm	
$M9$	$86,905$nm	130nm	
$MR4$	1040nm	130nm	

Figure 3: Table of device dimensions.

3.2 Performance Summary

Parameter	Specification	Circuit Performance	Spec Met?
DC Gain	1500	6645	Yes
Common Mode Input Range	$0.8V$	$1.44V$	Yes
Output Swing	$1.2V$	$1.34V$	Yes
Power Dissipation	1.5mW	1.47mW	Yes
Unity Gain Frequency	600 MHz	1.63GHz	Yes
Settling Time	8ns	7.64ns rising, 3.03ns falling	Yes
CMRR	75dB	90.7dB	Yes
PSRR at DC	60dB	102.7dB	Yes
PSRR at 1MHz	50dB	107.7dB	Yes
Lmin	130nm	130nm	Yes
Wmin	195nm	1040nm	Yes
Temperature	$25C$	$25C$	Yes

Figure 4: Table of simulated specifications

3.3 DC Gain, Phase Margin, and Unity Gain Frequency

The graphs below show the simulated results of the amplifier's open loop gain, frequency response, and phase margin at unity gain.

3.3.1 DC Gain

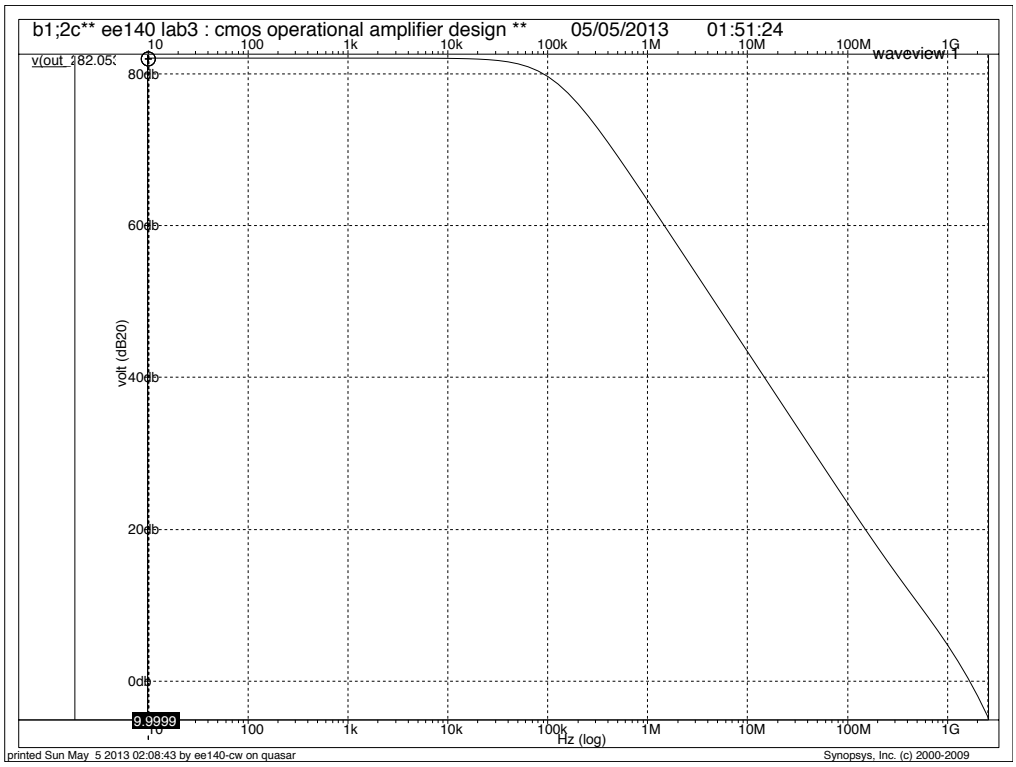

Figure 5: The differential gain of the amplifier is $82.05dB$

3.3.2 Unity Gain Frequency

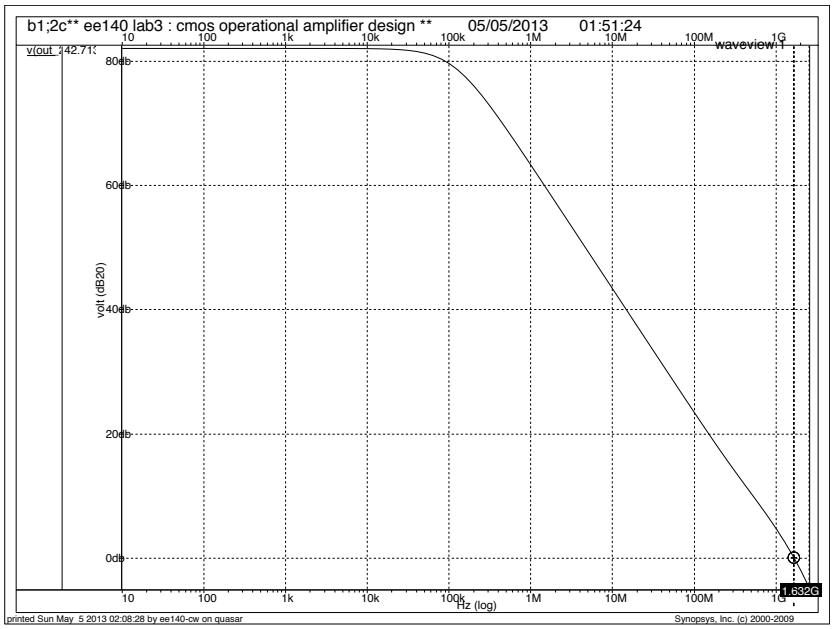

Figure 6: The unity gain frequency of the amplifier is $1.63GHz$

3.3.3 Phase

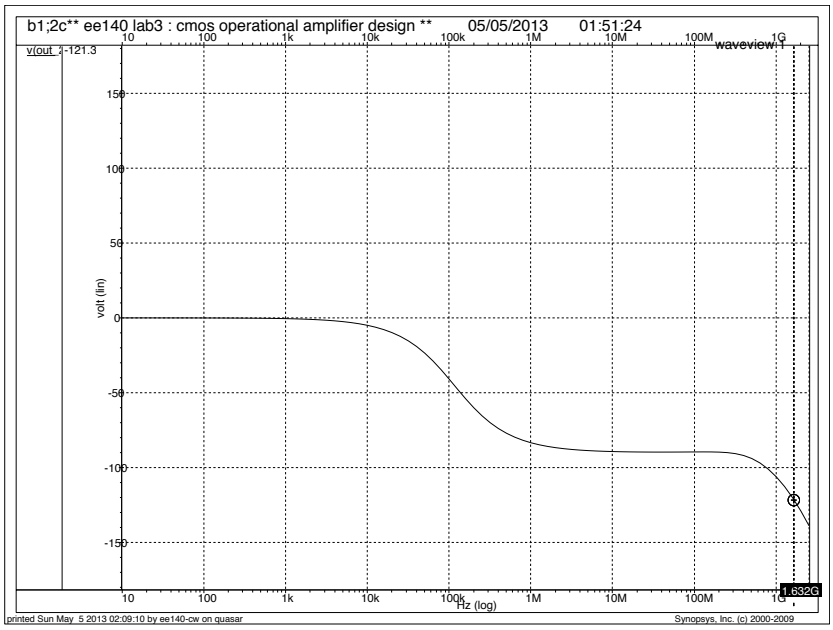

Figure 7: The phase at unity gain is -121.39^o. The phase margin at unity is 58.6^o

3.4 CMRR and PSRR

The graph below shows the amplifier's common mode rejection ratio and power supply rejection ratio. By taking the ratio of the common mode gain to the differential mode gain, we compute the common mode rejection ratio. By taking the ratio of the power supply gain to the differential mode gain, we compute the power supply rejection ratio. These values can be found in figure 4 above.

Note that the power supply gain from the negative source can be computed by the equation offered in section 2.1.7. With the amplifier providing a gain on the order of 74dB at low frequencies and roughly 60dB at $1MHz$, it is clear that $PSRR\_ > 60dB$.

3.4.1 Common mode gain

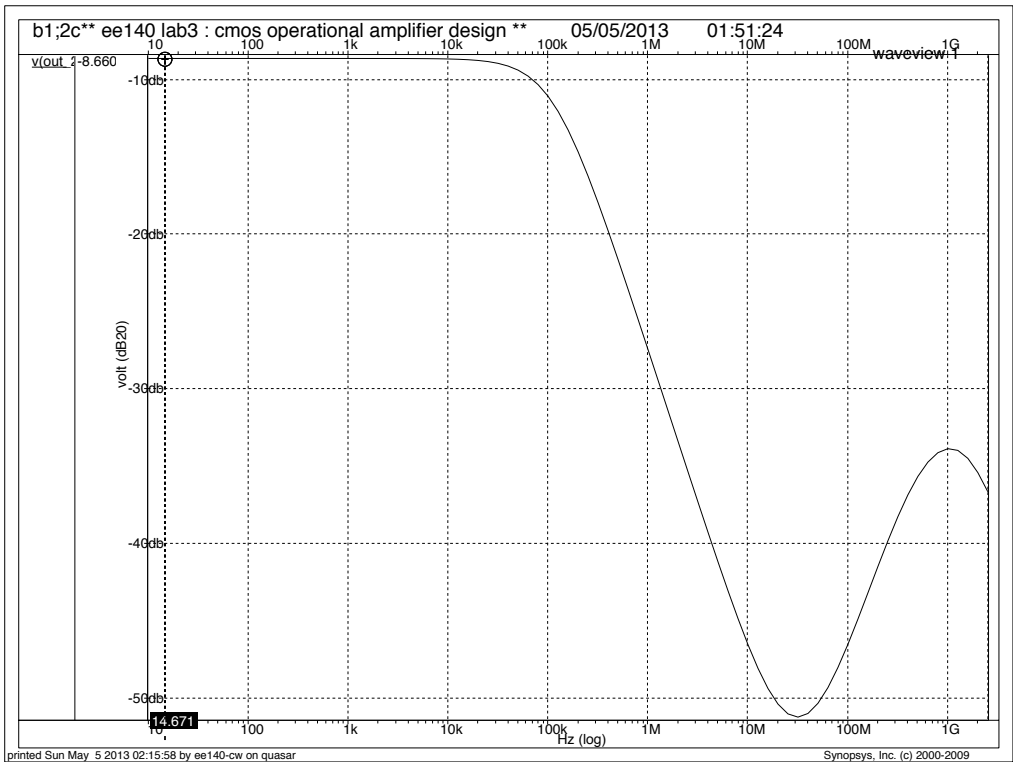

Figure 8: The common mode gain of the amplifier is $-8.66dB$

3.4.2 Power supply gain at DC

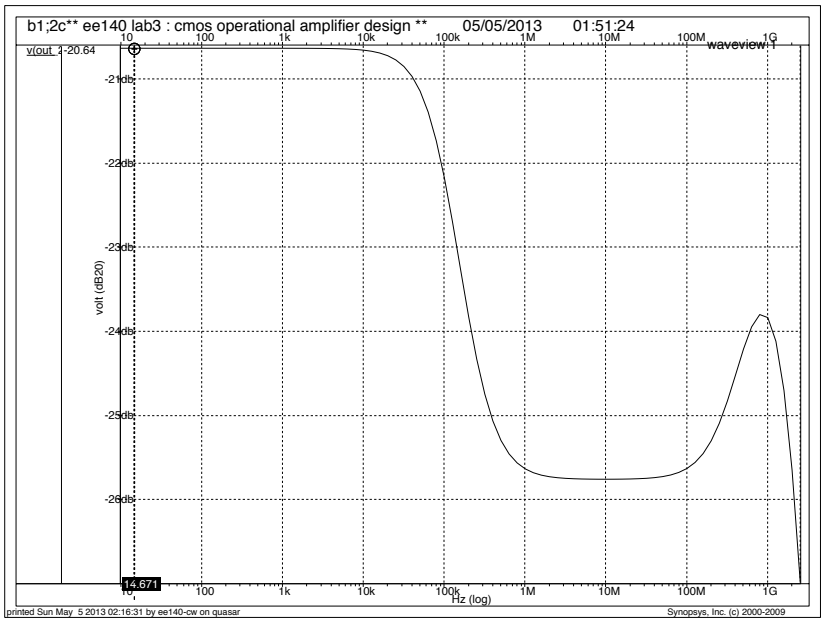

Figure 9: The power supply gain at DC is $-20.64dB$

3.4.3 Power supply gain at 1MHz

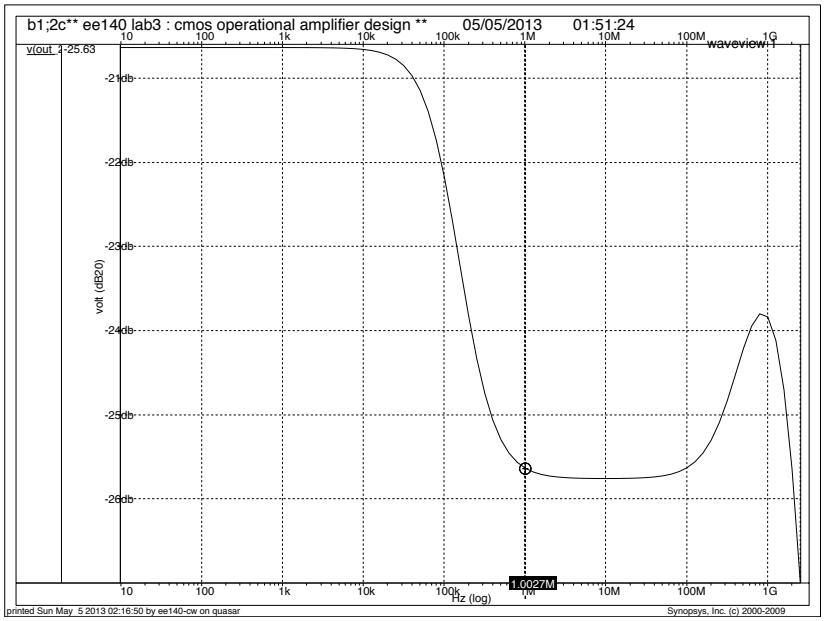

Figure 10: The power supply gain at $1MHz$ is $-25.64dB$

3.5 Common Mode Input Range

This is defined as the range of voltages at which $dVout/dVin$ becomes $1/2$ in unity gain feedback. To show this, we put the op amp into unity gain configuration and sweep the DC voltage at the input from 0 to V_{DD}. The graphs below show the maximum and minimum of this range. This amplifier exceeds the specification by a relatively large margin. This is partly due to tying the bulk to V_{DD} in transistors $3, 5$. This was done because the body effect on the input transistors can be used to increase the range[6]. The total common mode input range of the amplifier is listed in the table in figure 4.

3.5.1 Common Mode Input Range, minimum

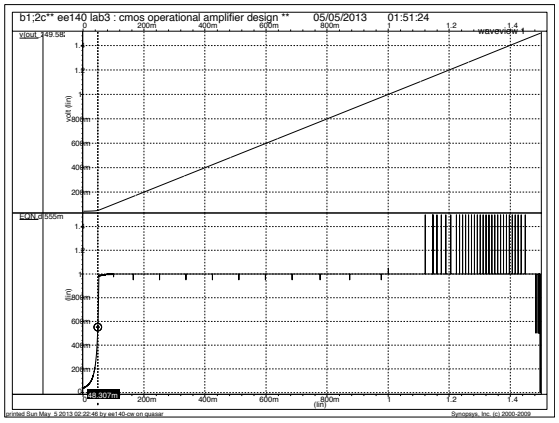

Figure 11: The minimum value corresponds to an output voltage of $49.6mV$

3.5.2 Common Mode Input Range, maximum

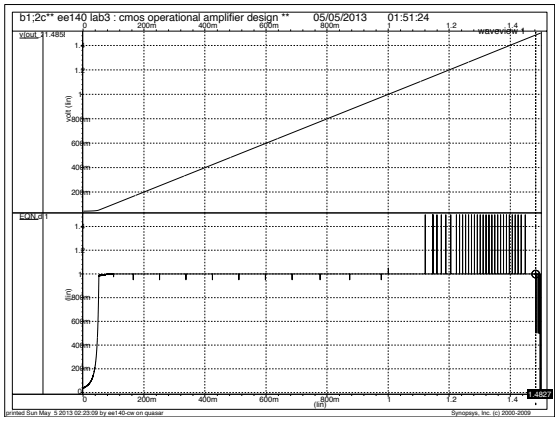

Figure 12: The maximum value corresponds to an output voltage of $1.486V$

3.6 Output Swing

This is defined as the range of voltages at which $dVout/dVin$ becomes $1/10th$ the nominal differential gain. To show this, we sweep the DC voltage at one of the inputs around its bias points and find the points on the curve where the derivative is approximately equal to $1/10th$ of the nominal gain. This value is approximately equal to $1.2k$. The graphs below show the minimum and maximum of this range. The total output swing of the amplifier is listed in the table in figure 4.

3.6.1 Output Swing, minimum

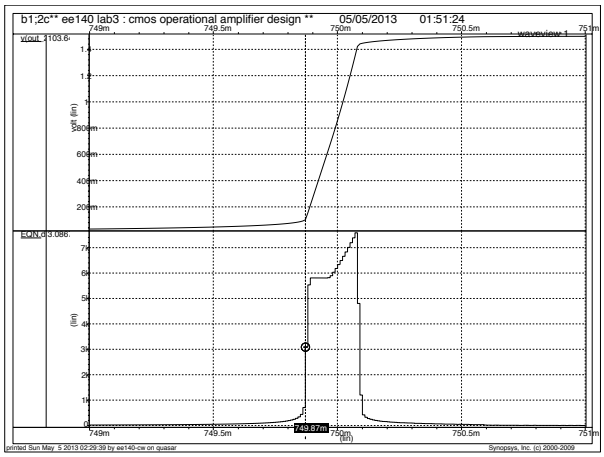

Figure 13: The minimum value corresponds to an output voltage of $0.103V$

3.6.2 Output Swing, maximum

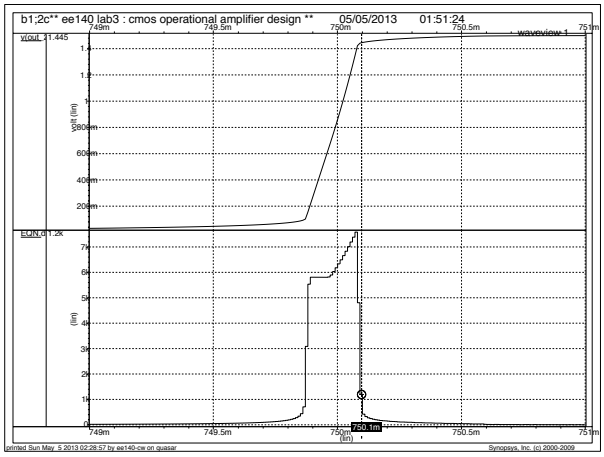

Figure 14: The maximum value corresponds to an output voltage of $1.44V$

3.7 Settling Time

This is the most stringent specification to meet, as it requires relatively large amounts of current to be supplied from the current sources. We measure settling time by putting the op amp into unity gain feedback and applying a $0.4V$ step to the input. We then run a transient analysis in hspice to determine the time it takes for the amplifier's output to converge to within 0.1%. The time it takes to converge must be under 8ns.

Here we apply a step from $0.5V$ to $0.9V$ and measure the time it takes to meet within 0.1% of each, respectively. As we can see, the amplifier has an excellent settling time and converges quickly on each rising and falling edge of the input.

3.7.1 Settling Time

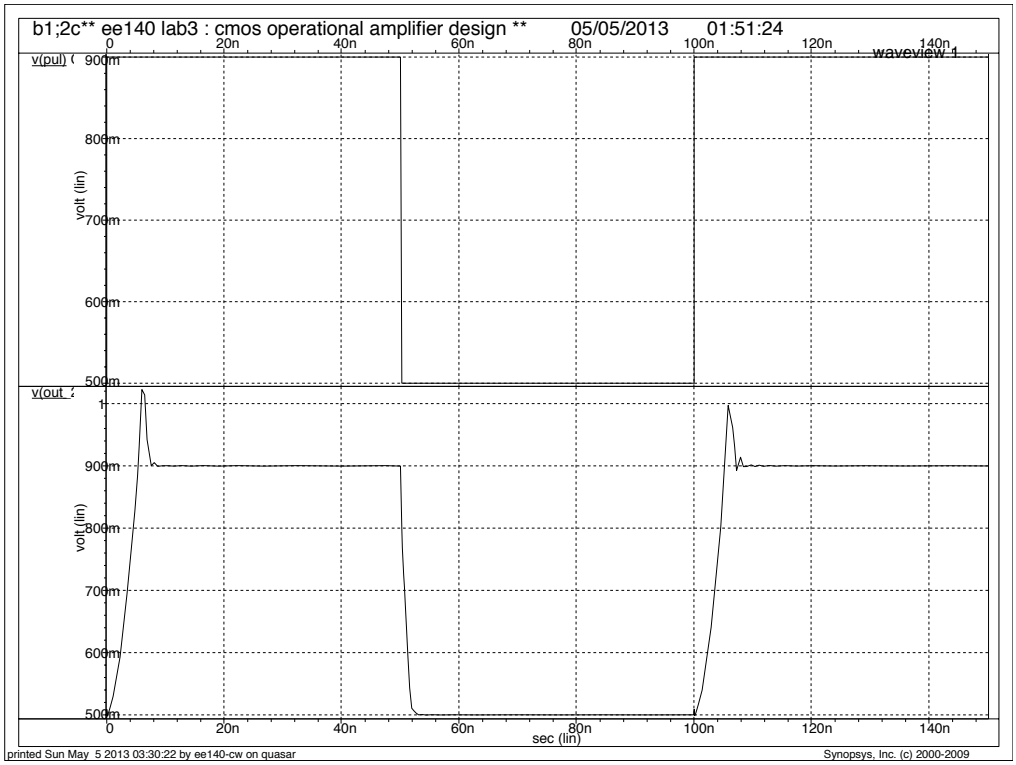

Figure 15: $0.4V$ step input and amplifier response

3.7.2 Settling Time, rising input

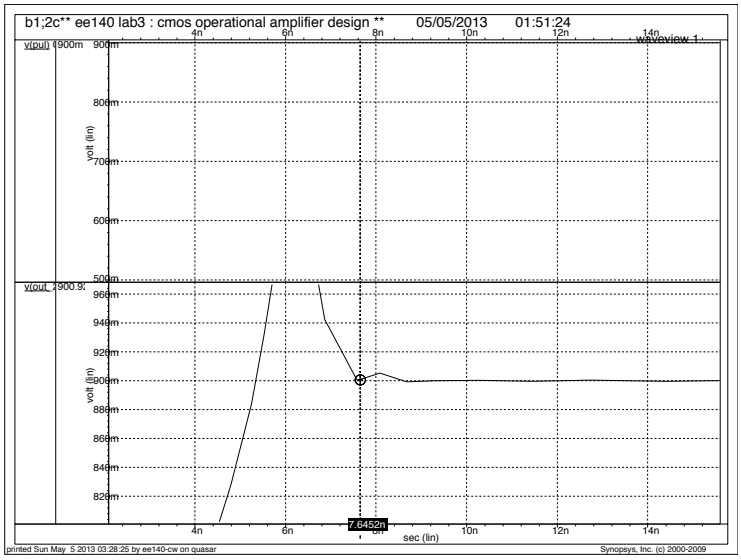

Figure 16: The time it takes to converge on a rising input is $7.64ns$

3.7.3 Settling Time, falling input

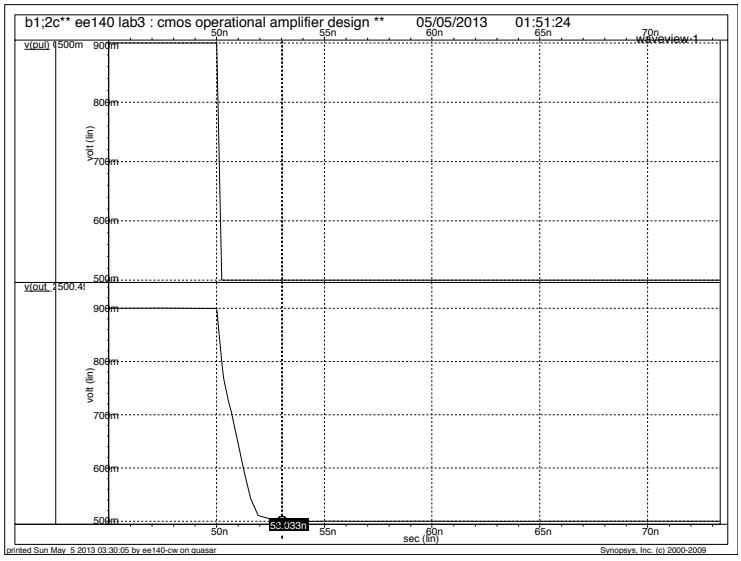

Figure 17: The time it takes to converge on a falling input is $3.03ns$

4 Conclusion

We have shown the design process of an analog integrated circuit CMOS operational amplifier, and we have shown how equations we have derived throughout the semester participate in this process. We have seen how tradeoffs must be made between certain parameters in order to provide an amplifier that is balanced and meets a wide range of specifications. For the most part, the amplifier considered in this paper is ideal for use in digital circuits or mixed signal circuits where the characteristics of the stages connected to the op-amp are known in advance. This amplifier provides a good gain for digital signals (digital signals typically do not require as much gain as their analog counterparts), a wide bandwidth, stellar phase margin for gains down to and below unity, a very quick settling time, and consumes very little power. Furthermore, the amplifier has a very good power supply rejection ratio which offers outstanding performance in digital circuits with high levels of switching noise. Overall, the amplifier we have designed is a stable, low power op-amp that is the quintessential CMOS operational amplifier utilized by engineers throughout the world.

The design of this op amp was a scrupulous and testing process, and a tremendous learning experience as well. To see how all of the many variables depended on each other required me to think in a way that I have never before and forced me to stretch and expand my mind to such great heights. Arguably, a better way to design a circuit like this is to write a geometric program and have a computer automatically compute a robust design given the parameters and specifications. This implies that the circuit designer can spend more time doing real design, *i.e.*, carefully analyzing the optimal trade-offs between competing objectives and less time doing parameter tuning or wondering whether a certain set of specifications can be achieved. However, for the purposes of this course and the learning experience required to become a competent circuit designer, it is necessary to do this type of analysis by hand and think about the circuit ourselves, rather than have a computer do the thinking for us. At the end of the day, I can say that I have a solid grasp and comprehension of the way a relatively large MOS circuit like this operates. I realize the interdependencies between variables like dimension, transconductance, and overdrive voltage, and I acknowledge the tradeoffs required to satisfactorily meet an extensive range of specifications. Overall, the wisdom and erudition bestowed upon me as a result of successfully completing this project is immense, and it was undeniably worth the effort.

5 Miscallaneous

5.1 hspice code

```
** EE140 Lab3 : CMOS Operational Amplifier Design **

.lib 'model_ee140_1.sp' TT

** Circuit Netlist **

   ** Power Supplies/Sources **

      V1 vdd 0 dc=1.5 ac=0
      Vcm cm 0 dc=0.75

      * Differential Voltage *
        Vid1 cm gate_M3 ac=1
        Vid2 gate_M5 cm ac=1

      * Transient Analysis
        *Vid1 cm gate_M3 SIN(0 0.00009 1000 0 0 0)
        *Vid2 cm gate_M5 SIN(0 0.00009 1000 0 0 180)

      * Common Mode Analysis
        *Vid2 cm gate_M5 ac=1

      * Output Swing Analysis and Common Mode Input Range
        *Vswp swp 0 dc=0.75

      * Settling time analysis
        Vpul pul 0 PULSE(0.5 0.9 0.1p 0.1p 0.1p 50n 100n)

    ** End Power Supplies/Sources**

   *** Amplifier ***

      ** First Stage **

           * Transistors *

           x7 tail vbias vdd vdd pmos l=130n w=86905n
                 x3 drain_M2 out_2 tail vdd pmos l=130n w=138775n
                 x5 out_1 pul tail vdd pmos l=130n w=138775n
                 x2 drain_M2 drain_M2 0 0 nmos l=130n w=9230n
                 x4 out_1 drain_M2 0 0 nmos l=130n w=9230n

      ** End First Stage **

      ** Second Stage **

           * Transistors *

                 x6 out_2 out_1 0 0 nmos l=130n w=17420n
                 x9 out_2 vbias vdd vdd pmos l=130n w=86905n

                 * End Transistors *

      ** End Second Stage **

      * Biasing *

                * Transistors *

                x1 vbias vbias vdd vdd pmos l=130n w=41080n

                * End Transistors *

                * Resistors *

                          Rbias vbias 0 6k

                * End Resistors *

        * End Biasing *

        * Compensation/Loading *

                * Capacitors *

                CL out_2 0 2p
                            Cc node out_2 2p

                * End Capacitors *

          * RHP Zero Linear Resistor *

          xR node vdd out_1 out_1 nmos l=130n w=1040n
```

```
          * End Linear Resistor

** End Circuit Netlist **

** Analysis **
   .TF V(out_2) Vid1
   .op
   .TRAN 1n 150n
   *.ac dec 10 10 2000meg

* Output Swing
  *.DC Vswp 0.749 0.751 0.00001

* Common Mode Input Range
   *.DC Vswp 0 1.5 0.0001

** End Analysis


** Control Information **

   .options post=2 nomod

** End Control Information **

.END
```

References

[1] Gray, Paul R., Meyer G. Robert, Analysis and Design of Analog Integrated Circuits. Wiley, New York, 5th Edition, 2010.

[2] Nguyen, Clark "Choosing Cc". Berkeley. 11 Apr. 2013. Lecture

[3] Nguyen, Clark "Settling Time, PSRR, Feedback I". Berkeley. 25 Apr. 2013. Lecture

Acknowledgements

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