Jason D. Chadwick

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Summary

Ph.D. Candidate in Computer Science with a proven track record of research and industry experience in quantum computer systems and architecture. Specialized in developing and implementing low-level software optimizations for large-scale, fault-tolerant quantum computation, with direct experience in implementing and decoding error correction codes, compiling quantum programs, and optimizing control pulses. Proven ability to make impactful contributions to industrial software, including integrating novel pulse-level optimizations and crosstalk modeling into Intel's core C++ compiler and Python hardware interface.

Education

Ph.D. Candidate, Computer Science, University of Chicago 2022–present
Studying quantum computer systems and architecture, advised by Fred Chong.
My research focuses on co-design optimizations that narrow the gap between existing hardware and fault-tolerant quantum computation. I have worked on research in the areas of hardware implementation of qLDPC codes, low-latency surface code decoding, mitigating burst errors, control pulse engineering, device calibration, circuit compilation, and high-radix computation.

B.S. Physics, Carnegie Mellon University 2018–2022
Minor in Computer Science
GPA 3.95

Professional Experience

Quantum Computing Intern, Intel Summer 2025
Implemented accurate simulation of capacitive crosstalk in quantum dots into the company's C++ compilation and simulation infrastructure. Implemented and explored several novel ideas for more efficient crosstalk mitigation. My analysis of hardware cost versus compensation effectiveness directly informed the design of next-generation hardware, leading to insights projected to reduce crosstalk compensation hardware complexity by more than 50%.

Quantum Computing Intern, Intel Summer 2024
Discovered new pulse schedules for two-qubit operations in silicon spin qubits, resulting in up to 54% reduction in errors and spurring the exploration of novel chip designs to take advantage of these gains. Incorporated this work into existing Python hardware interface and C++ compiler stack, creating an internal pulse library interface that is now a core part of Intel's software stack. Created compilation and simulation software for hardware-informed exploration of the QEC code design space, providing guidance for Intel's quantum roadmap. First-author paper published in *Physical Review A* based on this work.

Undergraduate Researcher, University of Chicago Spring 2021–Summer 2022
Optimized short-duration control pulses for high-radix quantum logic gates, motivating a new compiler design that takes advantage of mixed-radix operations. Presented research at QCE 2022 and contributed key results to papers at ASPLOS 2023 and ISCA 2023.

Undergraduate Intern, Princeton Plasma Physics Laboratory Summer 2020
As part of the Department of Energy SULI program, designed a neural network to predict fusion plasma cross-sectional density and pressure using only data available in real time during plasma operation, for use in real-time feedback control systems. Work published in *Nuclear Fusion*.

Skills

QEC concepts:	Low-latency/windowed decoding, syndrome extraction circuits, injection, distillation & compilation, circuit-level simulation, noise modeling, qLDPC codes
Programming languages:	Python, Julia, C/C++
Python libraries:	Stim/Sinter, Qiskit, Cirq, QuTiP, ldpc

Awards and Honors

Best Poster, Honorable Mention, QEC25 2025

QSYS Best Paper 1st place, IEEE QCE 2024 2024

QTEM Best Paper 3rd place, IEEE QCE 2023 2023

Crerar Fellowship, University of Chicago 2022
University Honors, Carnegie Mellon University 2022

College Honors, Mellon College of Science, Carnegie Mellon University 2022

Dean's List, High Honors, Mellon College of Science, Carnegie Mellon University 2018–2022

Service

Teaching Assistant, CMSC 22200 Computer Architecture Jan–Mar 2025
Developed autograder and taught lab sessions.

Workshop organizer, QCE 2024 Sept 2024
Organized second edition of "Novel Applications of Optimal Control and Calibration for Quantum Technology" at QCE 2024, featuring invited talks and guided discussions.

Workshop organizer, QCE 2023 Sept 2023
Organized a day-long workshop "Advances in Numerical Quantum Optimal Control and Characterization Methods" at QCE 2023, featuring invited talks and guided discussions.

Physics Steering Committee, CMU Physics Department 2019–2021
Collaborated with physics department leadership to guide programs and policy.

Publications

† indicates equal contribution

Year	Title and Authors	Publisher	Category
2025	Erasure Minesweeper: exploring hybrid-erasure surface code architectures for efficient quantum error correction **J. D. Chadwick**†, M. H. Teo†, J. Viszlai†, W. Yang†, and F. T. Chong arxiv.org/abs/2505.00066	2025 IEEE International Conference on Quantum Computing and Engineering (QCE)	Refereed conference paper
2025	Short two-qubit pulse sequences for exchange-only spin qubits in 2D **J. D. Chadwick**, G. G. Guerreschi, F. Luthi, M. T. Mądzik, F. A. Mohiyaddin, P. Prabhu, A. T. Schmitz, A. Litteken, S. Premaratne, N. C. Bishop, A. Y. Matsuura, and J. S. Clarke doi.org/10.1103/PhysRevA.111.052616	*Physical Review A* **111**, 052616	Journal article
2025	SWIPER: Minimizing Fault-Tolerant Quantum Program Latency via Speculative Window Decoding J. Viszai†, **J. D. Chadwick**†, S. Joshi, G. S. Ravi, Y. Li, and F. T. Chong doi.org/10.1145/3695053.3731022	52nd International Symposium on Computer Architecture (ISCA)	Refereed conference paper
2024	Averting multi-qubit burst errors in surface code magic state factories **J. D. Chadwick**, C. Kang, J. Viszlai, S. F. Lin, and F. T. Chong doi.org/10.1109/QCE60285.2024.00128	2024 IEEE International Conference on Quantum Computing and Engineering (QCE)	Refereed conference paper

QSYS Best Paper 1st place

2023	Efficient control pulses for continuous quantum gate families through coordinated re-optimization **J. D. Chadwick** and F. T. Chong doi.org/10.1109/QCE57702.2023.00145 QTEM Best Paper 3rd place	2023 IEEE International Conference on Quantum Computing and Engineering (QCE)	Refereed conference paper
2023	Dancing the Quantum Waltz: Compiling Three-Qubit Gates on Four Level Architectures A. Litteken, L. M. Seifert, **J. D. Chadwick**, N. Nottingham, J. M. Baker, and F. T. Chong doi.org/10.1145/3579371.3589106	50th International Symposium on Computer Architecture (ISCA)	Refereed conference paper
2023	Qompress: Efficient Compilation for Ququarts Exploiting Partial and Mixed Radix Operations for Communication Reduction A. Litteken, L. M. Seifert, **J. D. Chadwick**, N. Nottingham, J. M. Baker, and F. T. Chong doi.org/10.1145/3575693.3575726	28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)	Refereed conference paper
2022	Time-Efficient Qudit Gates through Incremental Pulse Reseeding L. M. Seifert†, **J. D. Chadwick**†, A. Litteken, F. T. Chong, and J. M. Baker doi.org/10.1109/QCE53715.2022.00051	2022 IEEE International Conference on Quantum Computing and Engineering (QCE)	Refereed conference paper
2021	Prediction of electron density and pressure profile shapes on NSTX-U using neural networks M. D. Boyer and **J. D. Chadwick** doi.org/10.1088/1741-4326/abe08b	*Nuclear Fusion* 61 046024	Journal article

Under Review

Year	Title and Authors	Publisher	Category
2025	A transversal-logic-equipped surface code architecture for readout-constrained spin qubits **J. D. Chadwick**, W. Yang, J. Viszlai, and F. T. Chong	Under review	Refereed Conference Paper
2025	Operating two exchange-only qubits in parallel M. T. Mądzik, F. Luthi, G. G. Guerreschi, F. A. Mohiyaddin, F. Borjans, **J. D. Chadwick**, M. J. Curry, J. Ziegler, S. Atanasov, P. L. Bavdaz, E. J. Connors, J. Corrigan, H. Ekmel Ercan, R. Flory, H. C. George, B. Harpt, E. Henry, M. M. Islam, N. Khammassi, D. Keith, L. F. Lampert, T. M. Mladenov, R. W. Morris, A. Nethwewala, S. Neyens, R. Otten, L. P. O. Ibarra, B. Patra, R. Pillarisetty, S. Premaratne, M. Ramsey, A. Risinger, J. Rooney, R. Savytskyy, T. F. Watson, O. K. Zietz, A. Y. Matsuura, S. Pellerano, N. C. Bishop, J. Roberts, and J. S. Clarke arxiv.org/abs/2504.01191	Under review	Journal article

Talks

Year	Title	Venue	Category
2025	Erasure Minesweeper: exploring hybrid-erasure surface code architectures for efficient quantum error correction	2025 IEEE International Conference on Quantum Computing and Engineering (QCE)	Conference talk
2025	Short two-qubit pulse sequences for exchange-only spin qubits in 2D	APS March Meeting 2025	Conference talk
2024	Averting multi-qubit burst errors in surface code magic state factories	2024 IEEE International Conference on Quantum Computing and Engineering (QCE)	Conference paper talk
2024	Dynamic mitigation of time-varying noise in surface code magic state factories	APS March Meeting 2024	Conference talk
2023	Efficient control pulses for continuous quantum gate families through coordinated re-optimization	2023 IEEE International Conference on Quantum Computing and Engineering (QCE)	Conference paper talk

Patents

Year	Title	Description
2023	SYSTEMS AND METHODS FOR OPTIMIZED PULSES FOR CONTINUOUS QUANTUM GATE FAMILIES THROUGH PARAMETER SPACE INTERPOLATION	Methods related to those described in “Efficient control pulses for continuous quantum gate families through coordinated re-optimization”, *QCE 2023*.