Lab 4: Synchronous Sequential Circuits

Jason Zhang

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Part I

2. Export the subcircuit schematic as an image and include it in your report.

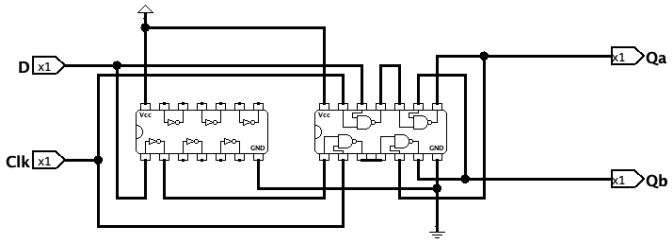

Figure 1: A schematic of the gated D-latch.

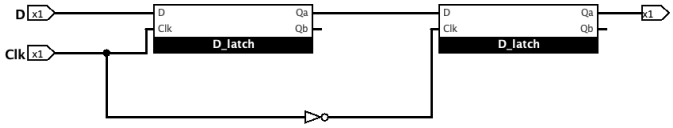

Figure 2: A schematic of the D flip-flop.

3. For the D latch and the flip flop, are there any input combinations of Clk and D that should NOT be the first you test with the *Poke* tool? List them if applicable.
for D latch: Clk = 0, D = 1 and Clk = 0, D = 0
for flip flop: Clk =0, D = 1 and CLk = 0, D = 0

Part IIa

2. Export the subcircuit schematic as an image and include it in your report.

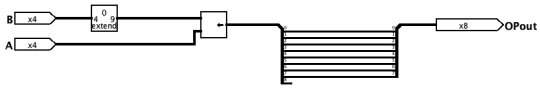

Figure 3: A schematic of op5.

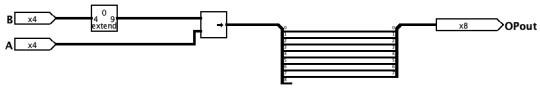

Figure 4: A schematic of op6.

3. Include a screenshot of your simulated test vectors for op5, op6, and op7.

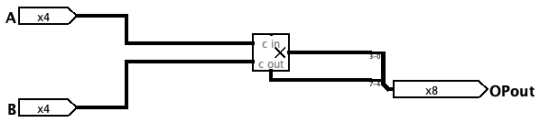

Figure 5: A schematic of op7.

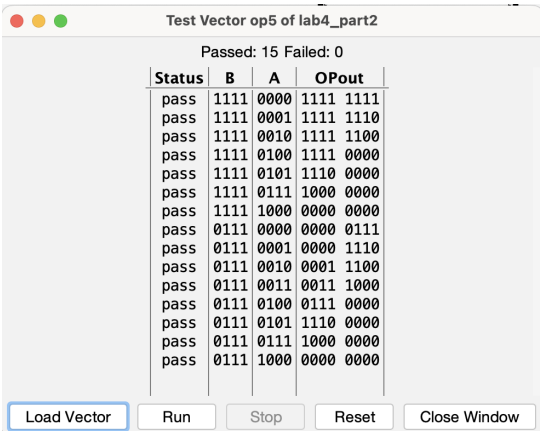

Figure 6: A simulation of op5.

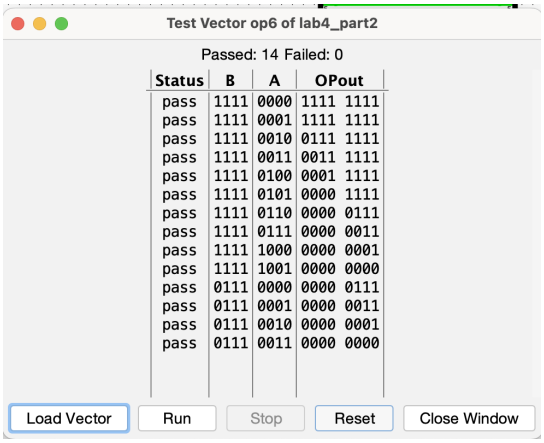

Figure 7: A simulation of op6.

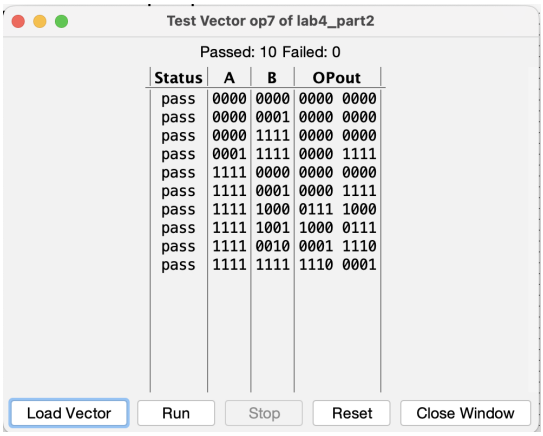

Figure 8: A simulation of op7.

Part IIb

3. Include a screenshot of your simulated timing diagram demonstrating ALUreg starting at 0x0 and increasing by 1 until 0x0f.

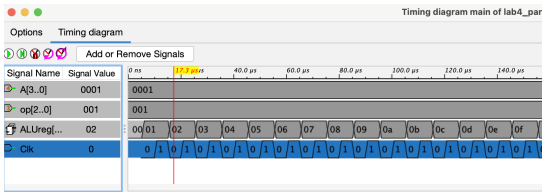

Figure 9: A timing simulation demonstrating incrementing.

4. Include a screenshot of your simulated timing diagram demonstrating a shifting operation where ALUreg goes from at 0x01 and doubling until 0x00.

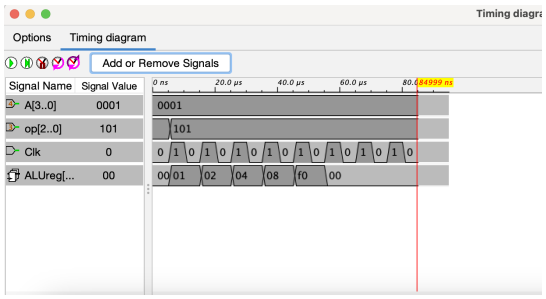

Figure 10: A timing simulation demonstrating doubling.

Part III

2. What is the behaviour of the 8-bit shift register when *Load_n = 1* and *ShiftRight = 0*? Briefly explain in your prelab.
   The value of the out put is all 0 as the shift choose the output as the value and not allowed load value to come in. The out put is 0 as original output for all.

3. Export the subcircuit schematic as an image and include it in your report.

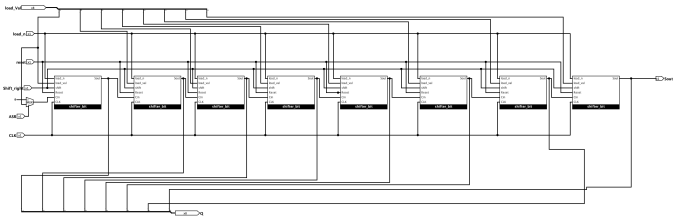

Figure 11: A schematic of the 8-bit shift register.

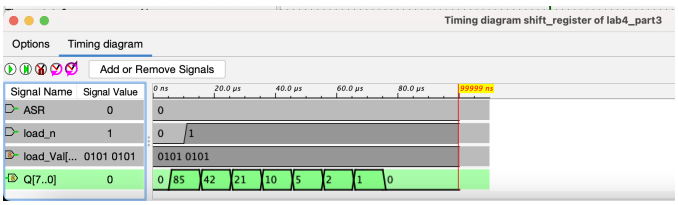

Figure 12: 8-bit shift register's test cases 1

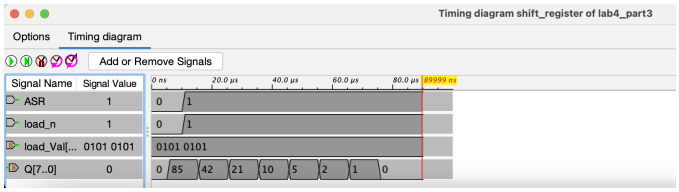

Figure 13: 8-bit shift register's test cases 2

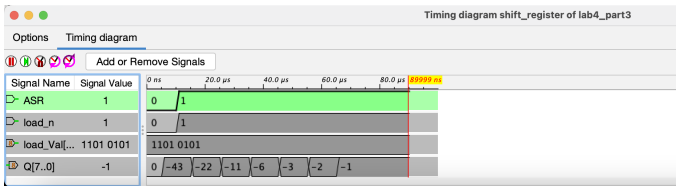

Figure 14: 8-bit shift register's test cases 3