Lab 7: Memory and Video

Jason Zhang

March 13, 2023

1 Part I

1. What happens if both signals are off when the clock goes high? What happens when both signals are on? Experiment with these signals to confirm your guess and write the behaviour in your prelab report.
   The data will not be written in the memory and the read output would be preserved.
   If both signals are on, the data would be write in the memory and also be written.

2. Draw a schematic describing this circuit as part of your preparation.

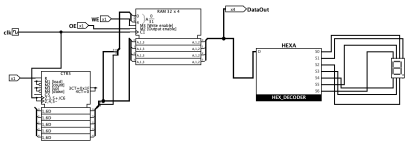

Figure 1: Schematic of Part 1.

3. Test your modules with *Poke* and the Logisim clock to verify its correctness. Include a few screenshots that shows the contents of the memory unit during your simulation.

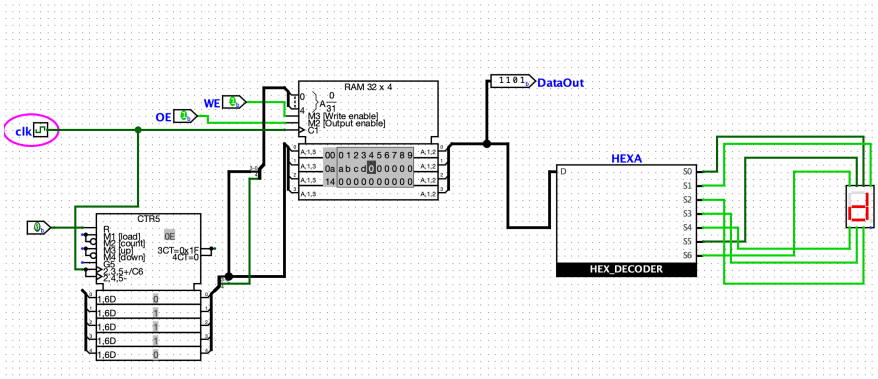

Figure 2: A simulation of the Memory.

2 Part II

3 Part III (Bonus)

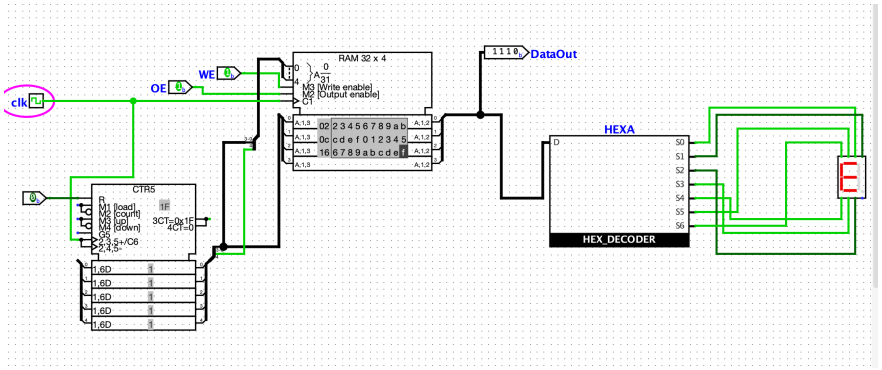

Figure 3: A simulation of the Memory.

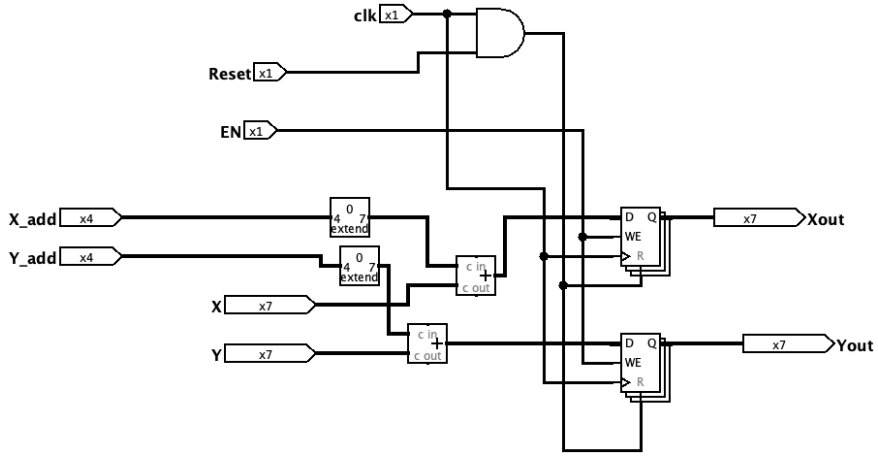

Figure 4: A simulation of the datapath.

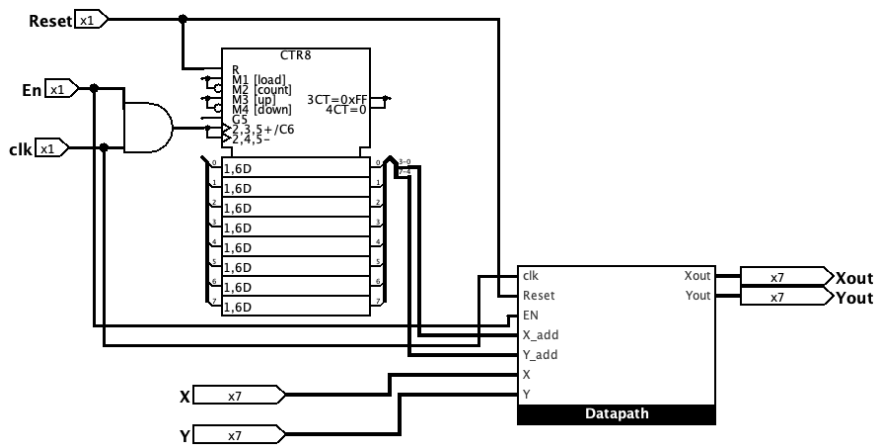

Figure 5: A simulation of the FSM.

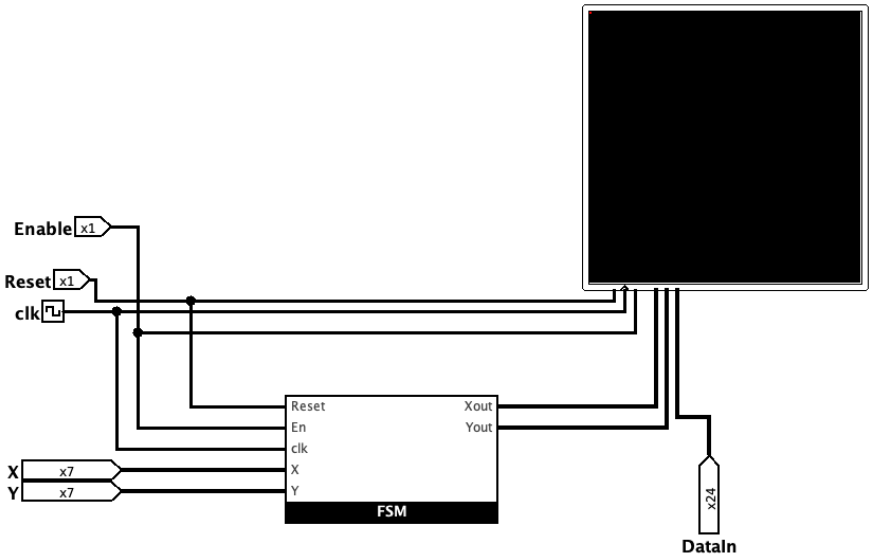

Figure 6: A simulation of the vedio.

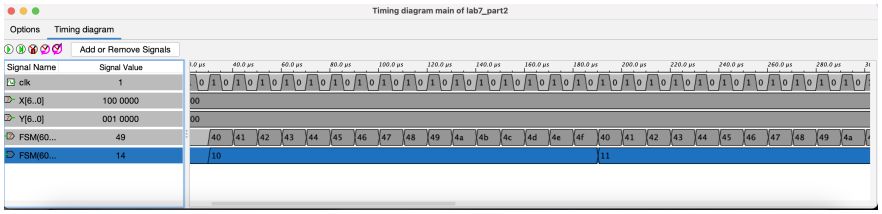

Figure 7: A timing diagram of the vedio.

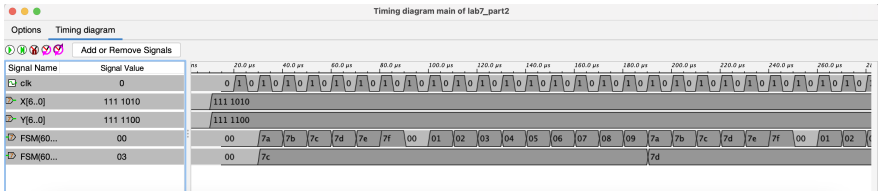

Figure 8: A timing diagram of the vedio.