

# Lab 4: Synchronous Sequential Circuits

Jason Zhang

February 6, 2023

## Part I

2. Export the subcircuit schematic as an image and include it in your report.

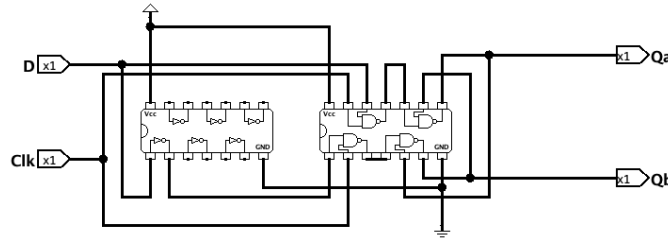


Figure 1: A schematic of the gated D-latch.

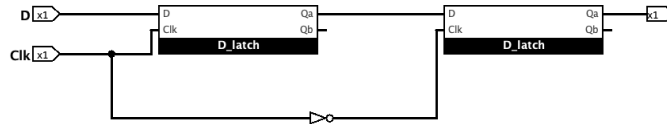


Figure 2: A schematic of the D flip-flop.

3. For the D latch and the flip flop, are there any input combinations of Clk and D that should NOT be the first you test with the *Poke* tool? List them if applicable.  
for D latch: Clk = 0, D = 1 and Clk = 0, D = 0  
for flip flop: Clk = 0, D = 1 and Clk = 0, D = 0

## Part IIa

2. Export the subcircuit schematic as an image and include it in your report.

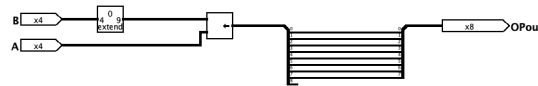


Figure 3: A schematic of op5.

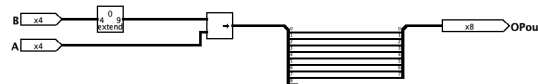


Figure 4: A schematic of op6.

3. Include a screenshot of your simulated test vectors for op5, op6, and op7.

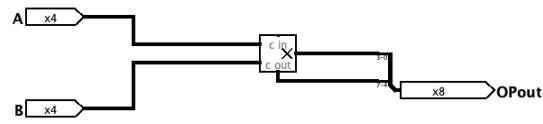


Figure 5: A schematic of op7.

Test Vector op5 of lab4\_part2

Passed: 15 Failed: 0

Status	B	A	OPout
pass	1111	0000	1111 1111
pass	1111	0001	1111 1110
pass	1111	0010	1111 1100
pass	1111	0100	1111 0000
pass	1111	0101	1110 0000
pass	1111	0111	1000 0000
pass	1111	1000	0000 0000
pass	0111	0000	0000 0111
pass	0111	0001	0000 1110
pass	0111	0010	0001 1100
pass	0111	0011	0011 1000
pass	0111	0100	0111 0000
pass	0111	0101	1110 0000
pass	0111	0111	1000 0000
pass	0111	1000	0000 0000

Load Vector Run Stop Reset Close Window

Figure 6: A simulation of op5.

Test Vector op6 of lab4\_part2

Passed: 14 Failed: 0

Status	B	A	OPout
pass	1111	0000	1111 1111
pass	1111	0001	1111 1111
pass	1111	0010	0111 1111
pass	1111	0011	0011 1111
pass	1111	0100	0001 1111
pass	1111	0101	0000 1111
pass	1111	0110	0000 0111
pass	1111	0111	0000 0011
pass	1111	1000	0000 0001
pass	1111	1001	0000 0000
pass	0111	0000	0000 0111
pass	0111	0001	0000 0011
pass	0111	0010	0000 0001
pass	0111	0011	0000 0000

Load Vector Run Stop Reset Close Window

Figure 7: A simulation of op6.

Test Vector op7 of lab4\_part2

Passed: 10 Failed: 0

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0000	0001	0000 0000
pass	0000	1111	0000 0000
pass	0001	1111	0000 1111
pass	1111	0000	0000 0000
pass	1111	0001	0000 1111
pass	1111	1000	0111 1000
pass	1111	1001	1000 0111
pass	1111	0010	0001 1110
pass	1111	1111	1110 0001

Load Vector Run Stop Reset Close Window

Figure 8: A simulation of op7.

## Part IIb

3. Include a screenshot of your simulated timing diagram demonstrating ALUreg starting at 0x0 and increasing by 1 until 0xf.

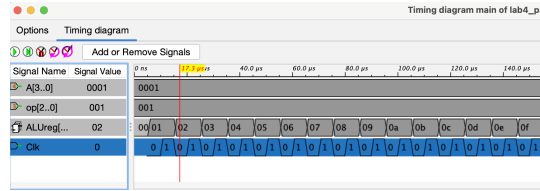


Figure 9: A timing simulation demonstrating incrementing.

4. Include a screenshot of your simulated timing diagram demonstrating a shifting operation where ALUreg goes from at 0x01 and doubling until 0x00.

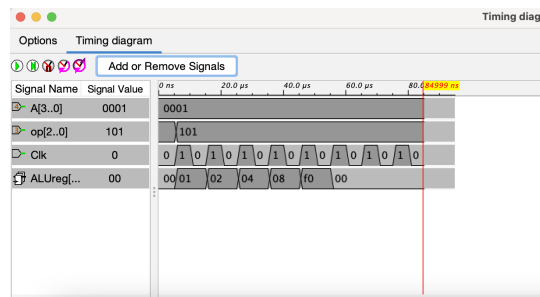


Figure 10: A timing simulation demonstrating doubling.

## Part III

2. What is the behaviour of the 8-bit shift register when  $Load_n = 1$  and  $ShiftRight = 0$ ? Briefly explain in your prelab.  
The value of the out put is all 0 as the shift choose the output as the value and not allowed load value to come in. The out put is 0 as original output for all.
3. Export the subcircuit schematic as an image and include it in your report.

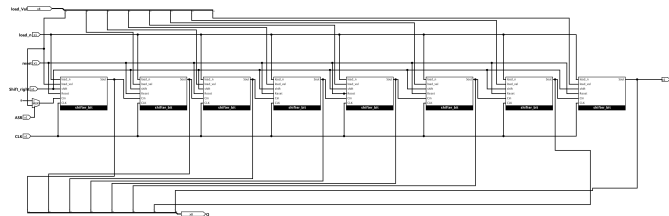


Figure 11: A schematic of the 8-bit shift register.

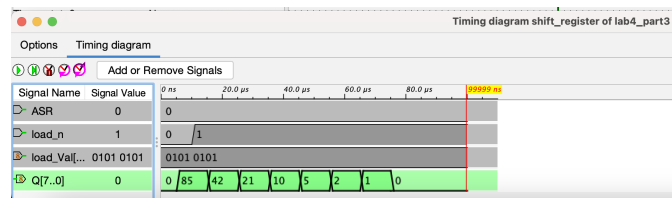


Figure 12: 8-bit shift register's test cases 1

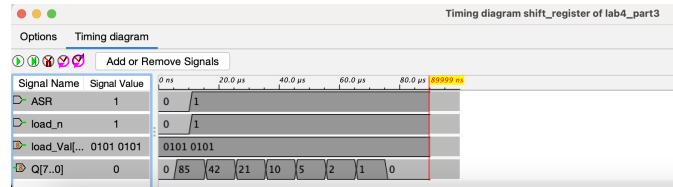


Figure 13: 8-bit shift register's test cases 2

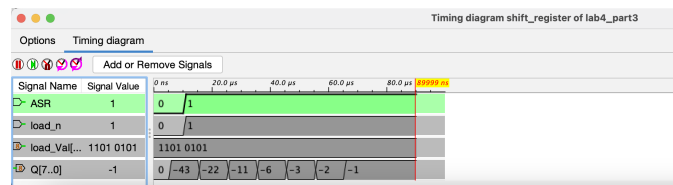


Figure 14: 8-bit shift register's test cases 3