

# Lab 3: The Arithmetic Logic Unit

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## Part I

2. Export the subcircuit schematic as an image and include it in your report.

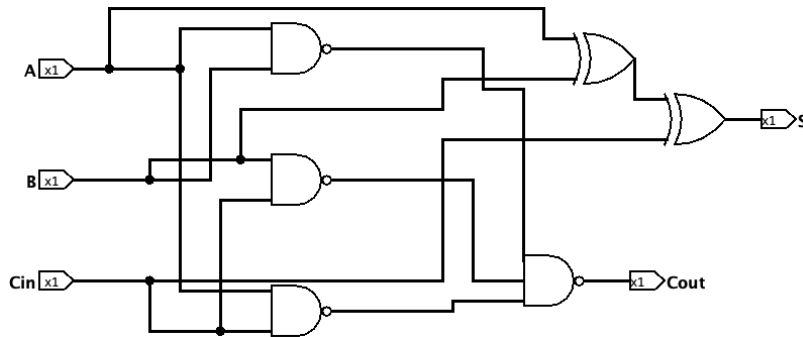


Figure 1: A schematic of ripple\_carry4.

3. Include a screenshot of your simulated test vector for the 4-bit Ripple Carry Adder.

Test Vector ripple\_carry4 of lab3

Passed: 8 Failed: 0

Status	A	B	Cin	S	Cout
pass	0000	0000	0	0000	0
pass	0000	0000	1	0001	0
pass	0000	1111	0	1111	0
pass	1111	0000	0	1111	0
pass	0001	1111	0	0000	1
pass	0000	1111	1	0000	1
pass	1111	0000	1	0000	1
pass	1111	0001	0	0000	1

Load Vector Run Stop Reset Close Window

Figure 2: A simulation ripple\_carry4.

## Part II

1. Export the subcircuit schematic of each operation as an image and include it in your report.
2. Include a screenshot of your simulated test vectors for op3, op4, and op5.
3. Export the ALU schematic as an image and include it in your report.

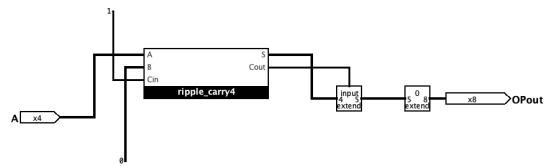


Figure 3: A schematic of op0.

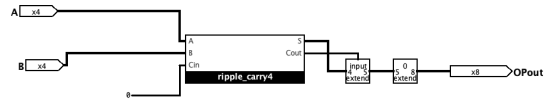


Figure 4: A schematic of op1.

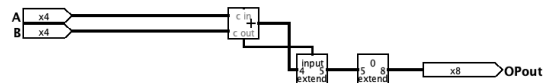


Figure 5: A schematic of op2.

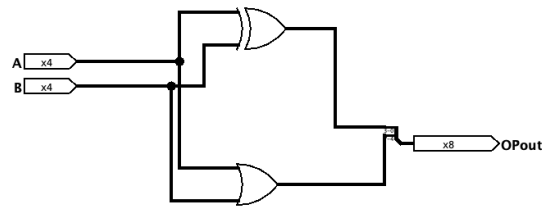


Figure 6: A schematic of op3.

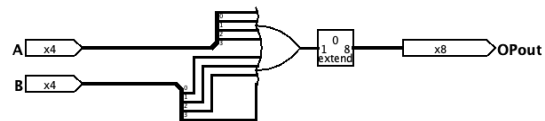


Figure 7: A schematic of op4.

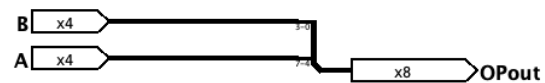


Figure 8: A schematic of op5.

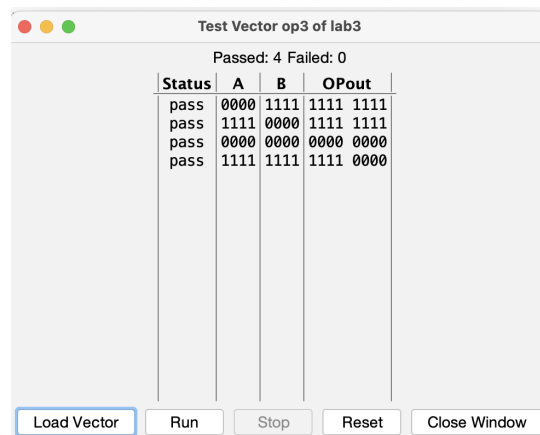


Figure 9: A simulation of op3.

Test Vector op4 of lab3

Passed: 10 Failed: 0

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0000	0001	0000 0001
pass	0000	0010	0000 0001
pass	0000	0100	0000 0001
pass	0000	1000	0000 0001
pass	0001	0000	0000 0001
pass	0010	0000	0000 0001
pass	0100	0000	0000 0001
pass	1000	0000	0000 0001
pass	1111	1111	0000 0001

Load Vector Run Stop Reset Close Window

Figure 10: A simulation of op4.

Test Vector op5 of lab3

Passed: 12 Failed: 0

Status	B	A	OPout
pass	0000	0000	0000 0000
pass	0000	0001	0001 0000
pass	0000	0010	0010 0000
pass	0000	0100	0100 0000
pass	0000	1000	1000 0000
pass	0000	1111	1111 0000
pass	0001	0000	0000 0001
pass	0010	0000	0000 0010
pass	0100	0000	0000 0100
pass	1000	0000	0000 1000
pass	1111	0000	0000 1111
pass	1111	1111	1111 1111

Load Vector Run Stop Reset Close Window

Figure 11: A simulation of op5.

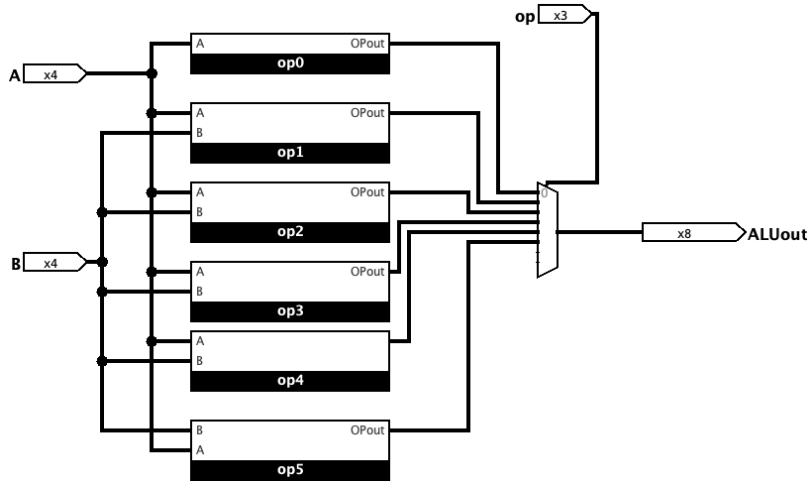


Figure 12: A schematic of the ALU.