Lab 6: Finite State Machines

Jason Zhang

March 4, 2023

1 Part I

1. Complete Table 1 below.

Table 1: State Encodings

State	Encoding
A	000
B	001
C	011
D	010
E	110
F	111
G	101

2. Complete Table 2 below.

Table 2: Encoded State Transition Table for Robo-Snail

Current State	W	Next State
000	0	000
000	1	001
001	0	000
001	1	011
011	0	110
011	1	010
010	0	110
010	1	111
110	0	000
110	1	101
111	0	110
111	1	111
101	0	000
101	1	011

3. Derive equations for each of your next state outputs below.

$$S_0' = S_0 \cdot W + \overline{S_2} \cdot \overline{S_1} \cdot W + S_2 \cdot W$$
$$S_1' = \overline{S_2} \cdot S_1 + S_0 \cdot W + S_1 \cdot S_0$$
$$S_2' = \overline{S_2} \cdot S_1 \cdot \overline{S_0} + S_2 \cdot S_1 \cdot W + S_1 \cdot S_0 \cdot \overline{W}$$
$$S_3' =$$
$$S_4' =$$
$$S_5' =$$
$$S_6' =$$

4. Export the subcircuit schematic as an image and include it in your report.

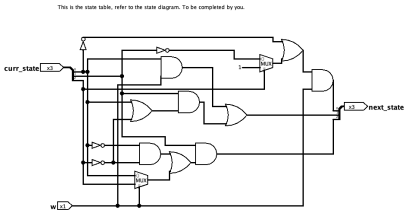

Figure 1: A schematic of part1_state_table.

5. Complete Table 3 below.

Table 3: Encoded Output Table for Robo-Snail

State	Output
000	0
001	0
010	0
011	0
101	1
110	0
111	1

6. Derive the equation for your output logic below.

$$Z = S_2 \cdot S_0$$

7. Export the subcircuit schematic as an image and include it in your report.

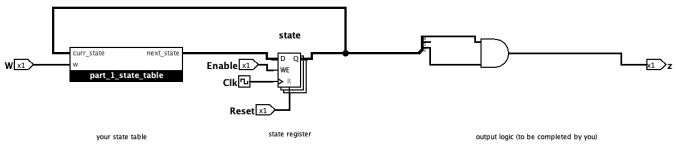

Figure 2: A schematic of part1_FSM.

2 Part II

1. Complete Table 4 below.

Table 4: Encoded State Transition Table for Part II

State	Next State
0000	0001
0001	0011
0011	0010
0010	0110
0110	0111
0111	0101
0101	0100
0100	1000
1000	0000

2. Draw the state transition diagram and include it in Figure 3.

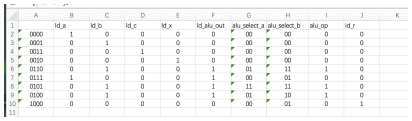

Figure 3: The state transition diagram for Part II

3. Simulate your circuit using a variety of input settings.

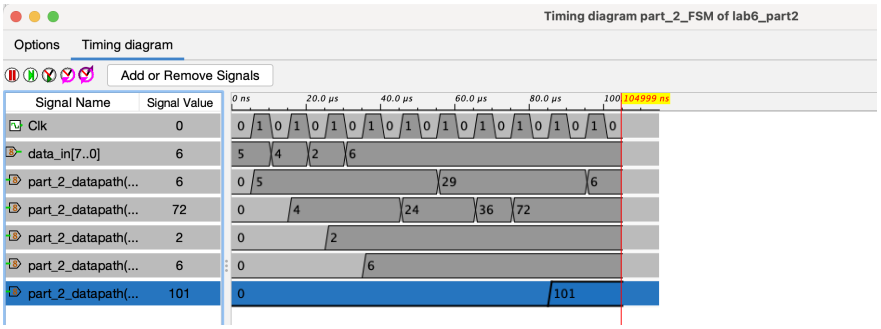

Figure 4: Test Case for Part 2.

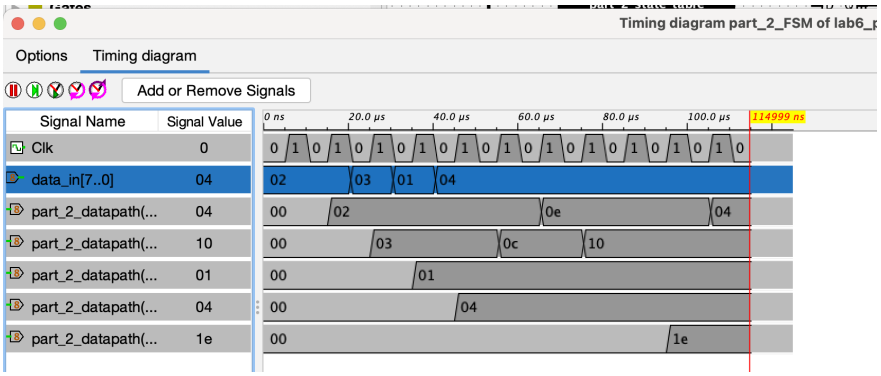

Figure 5: Test Case for Part 2.

3 Part III

1. Draw a schematic for the datapath of your circuit. It will be similar to the handout. You should show how you will initialize the registers, where the outputs are connected, and include all the control signals that you require.
2. Draw the state diagram that controls your datapath.

Figure 6: State diagram that controls the datapath in Part 3.

3. Draw the schematic for your controller module.

Figure 7: Controller Module in Part III.

4. Draw the top-level schematic showing how the datapath and controller are connected as well as the inputs and outputs to your top-level circuit.

Figure 8: Top level schematics schematic in Part III.

5. Simulate your circuit using a variety of input settings.

Figure 9: Test Case for Part 3.

Figure 10: Test Case for Part 3.