Computer Architecture HW4

B07902129 何政勳

1. Modules explanation

   a. Control

      Control module takes one input, which is the opcode, and outputs three control signals, which are ALUOp_o, ALUSrc_o and RegWrite, whenever the input is changed. There are only two kinds of opcode in this homework, so the ALUOp_o and ALUSrc_o will both be either 0 or 1. The RegWrite is always 1 in this homework.

   b. ALU Control

      ALU control module takes two inputs, which are the function code in the instruction and the ALU opcode from the controller. After comparing the function code and the ALU opcode, this module outputs a 3-bits select signal to the ALU whenever the input is changed.

   c. Sign Extend

      Sign extend module takes one input, which is the 12-bits immediate in the instruction. It extends the immediate to 32-bits by copying the most significant bit 20 times.

   d. ALU

      ALU module takes three input, which are data1, data2 and the ALU control signal from ALU control module. ALU gives two output, which are a 32-bits result and a zero signal, when any of the input is changed. ALU performs the corresponding arithmetic operation based on the 3-bits ALU control from ALU control module.

   e. Adder

      Adder module takes two input and outputs the sum of the inputs when any of the inputs is changed.

   f. MUX32

      MUX32 module takes three input, two of them are 32-bits data and one of them is a select signal. This module outputs one of the inputs based on the signal.

   g. CPU

      CPU module takes three input, which are clock signal, reset signal and start signal. Clock signal is sent to PC module and Register module. Reset signal and start signal are sent to PC module to control the execution order of instructions.

      CPU module connects all the modules mentioned above along with the PC module, Instruction_memory module and the Registers module. 19 additional wires are used to connect those modules together in my implementation. Those wires connect each module as the Figure 1 in homework specification.

2. Development Environment
    a. OS: Windows10
    b. Compiler: iverilog