CDA 3201L FINAL LAB PROJECT
3-STORY ELEVATOR CONTROLLER

***Demonstration Due Date**: Friday, April 24th by end of class.*

***Report Due Date**: Sunday, April 26th by 11:59PM.*

Specifications

Design and implement a finite state machine which controls the operation of an elevator in a 3-story building. The finite state machine (FSM) has 5 inputs: *reset (*takes device to idle state*), start* (enables operation of elevator), *up* (moves up one floor at a time), *down* (moves down one floor at a time), and *setAlarm.* The FSM has three outputs: *door (*if door == 0, door is closed, if door == 1, door is open), *alarm*, *floor* (display the floor the elevator is currently on using a 7-segment display). The operation of the device is as follows:

- The device must begin in an *idle* state in which the elevator is on the first floor with the door open and the elevator alarm disabled. After the start input is set, the device will be enabled for operation. Until then, the device must stay on the first floor with the door open, alarm off.
- Setting the *start* input will enable the device for operation.
- Setting either the *up* or *down* inputs will trigger **3** events:
    1. The door must close
    2. The elevator will move up/down one floor
    3. Once it reaches the next floor, the door must remain open.
    - *Note*: *This is not a magical elevator and cannot wrap around from the third floor to the first floor or vice-versa.*
- Setting the *reset* input will *asynchronously* put the elevator back in its *idle* state
- Setting the *setAlarm* input will have two effects:
    - The elevator door must close, and the elevator will remain on that floor until the alarm is disabled.
    - An alarm light will begin to flash.
- The floor that the elevator currently resides will be displayed on a 7-segment display and Binary-BCD Decoder (74LS247N). Your lecture textbook describes how to use the decoder.
- The (flashing) alarm light will be displayed on an LED.
- You are free to use any TTL chips in the lab.

Deliverables

1**) (60%) You must demonstrate** the functional correctness of this lab on the breadboard, per usual, to get full credit for this portion.
2) **Completion of circuit design in Logisim is mandatory**. If your circuit on the breadboard does not work, you should be able to simulate your design successfully in Logisim (you will receive partial credit depending on percentage of functionality successfully implemented and level of effort). The simulation is not required for the demonstration, but you must still complete the circuit as it is mandatory to include your schematic(s) in the final report.
3) **(40%) Final report:** Use the same template for previous labs. This lab is worth 30% of your overall grade. **YOU MUST** include a schematic of your design. Not doing so will result in a hefty point deduction. **YOU MUST** include the following in the design section:

- State diagram
- State transition table
- Simplification steps (k-map, Boolean simplification, etc.)
- Schematic(s)
- Description in plain English of how and why your design works.

Important: Always state your assumptions! If you make an assumption in your design, state the assumption and justify your reasoning as to why your design decision makes sense. There are cases which may occur during regular operation of the controller that are not mentioned in the specification.

DO NOT WAIT UNTIL THE LAST MINUTE TO START!!!