CDA 3201L
Combinational Logic Circuits (IV)
Lab 4

***Demonstration Due Date**: Friday, February 13th by end of class.*

***Report Due Date**: Sunday, February 15th by 11:59PM.*

Part A

Design a circuit that implements the functions in the following table:

S_0	S_1	Function
0	0	A+1
0	1	A+B
1	0	A-B
1	1	A-1

S_0 and S_1 are 1-bit control inputs which select the function of the circuit. Inputs A and B are 4-bit numbers in 2s complement form. The output is a 4-bit number in 2s complement form. You are allowed to use only one TTL 7483 4-bit adder to implement all the functions. Any number of other components (except the adder) can be used.

HINT: *Design a combinational logic circuit to modify the input B and the "carry input" of the adder depending on the control inputs S_0 and S_1. A multiplexer may be useful here…..*

Questions (Answer these in a separate section in your lab report)

1. Is the output valid for the following input combinations:
   $S_0 = 0$, $S_1 = 0$, A = 7, B = 3?
   $S_0 = 0$, $S_1 = 1$, A = 7, B =- 3?
   $S_0 = 1$, $S_1 = 0$, A = -4, B = -5?
2. What is the range of inputs (for both A and B) that will produce the valid output for each of the functions?

IMPORTANT: You must demonstrate your solution to part A on the breadboard. Lab grade will depend on the working of the circuit and will be checked off by the lab instructor. This demonstration must be completed within the window of your lab section meeting.

Note: Use the sheet posted in the lab (to the left of the circuit bins) to find the location of the chip you are looking for. All of the bins are labeled. To find datasheets for a particular chip, use the product search on Jameco. Once you have found the chip, click on the datasheet PDF to find the pin mappings.