CDA 3201L
Sequential Logic Circuits (I)
Lab 5

***Demonstration Due Date**: Friday, February 27th by end of class.*

***Report Due Date**: Sunday, March 1st by 11:59PM.*

Part A

Verify the operation of a JK flip-flop (TTL 7476) on the breadboard by providing appropriate inputs to the J, K, Preset, and Clear pins. Use a function generator as the source of the CLOCK input to the flip-flop.

Part B

Verify the operation of a D flip-flop (TTL 7474) on the breadboard by providing appropriate inputs to the D, Preset, and Clear pins. Use a function generator as the source of the CLOCK input to the flip-flop.

Part C

Configure a JK flip-flop (TTL 7476) to function as a D flip-flop.

Part D

Configure a JK flip-flop (TTL 7476) to function as a Toggle flip-flop.

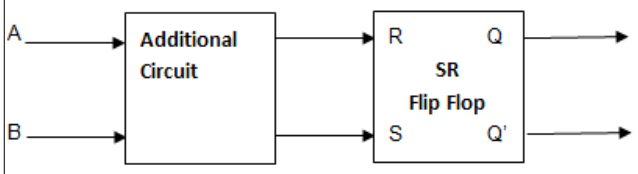
Part E

Build an SR (Set-Reset) Flip flop using logic gates and verify its correctness of operation by comparing the outputs with the truth table. Then modify the functionality of the SR FF by adding additional circuit elements (logic gates) to its input lines.

Your circuit should produce the following output:

Inputs to the Circuit		**SR FF Outputs**	
A	**B**	**Q**	**Q'**
0	0	Previous Q	Previous Q'
0	1	1	0
1	0	0	1
1	1	1	0

This is a black-box diagram of what you are building:



Note: *You must use the clock as an input when building SR FF!*

IMPORTANT: You must demonstrate your solution to part A, B, and C, D, and E on the breadboard. Lab grade will depend on the working of the circuit and will be checked off by the lab instructor. This demonstration must be completed within the window of your lab section meeting.