CDA 3201L
Combinational Logic Circuits (I)
Lab 1

***Demonstration Due Date**: Friday, January 23rd by end of class.*

***Report Due Date**: Sunday, January 25th by 11:59PM.*

Part A

Verify that the NAND operation is functionally complete using De Morgan's law. (Hint: Show that a 2-input NAND gate can implement the functionality of a NOT, AND, and OR gate).

Part B

Simplify the following Boolean expression using the rules of Boolean algebra, and implement the resulting circuit using inverters, 2-input AND gates, and 2-input OR gates.

$$F = \overline{Z}(\overline{X}\,\overline{Y} + X\overline{Y}) + XY + YZ(Y + Z)$$

***Reminder:** Only one demonstration and report required per group. Submit a soft copy of your report in Canvas in PDF format (no other file formats are allowed).*

IMPORTANT: You must demonstrate your solution to part A and B on the breadboard. Lab grade will depend on the working of the circuit and will be checked off by the lab instructor. This demonstration must be completed within the window of your lab section meeting.

Note: Use the sheet posted in the lab (to the left of the circuit bins) to find the location of the chip you are looking for. All of the bins are labeled. To find datasheets for a particular chip, use the product search on Jameco. Once you have found the chip, click on the datasheet PDF to find the pin mappings.