CDA 3201L
Combinational Logic Circuits (III)
Lab 3

***Demonstration Due Date**: Friday, February 6th by end of class.*

***Report Due Date**: Sunday, February 8th by 11:59PM.*

Part A

Design and wire a circuit to implement the Boolean expression $F(x, y, z) = \sum(1, 2, 4, 6, 7)$ using an 8-to-1 multiplexer (74LS151). Verify the operation by checking all input combinations in the Boolean function's truth table.

Part B

Use a 4-to-1 multiplexer (74LS153) to implement the same function $F(x, y, z)$ from Part A. Verify the operation by checking all input combinations in the Boolean function's truth table. You may only use inverters and 4-to-1 multiplexer ICs for this circuit.

Part C

Design a circuit that accepts two 3-bit numbers and generates a 2-bit output based on the scenarios below. Clearly indicate the output encoding in your lab report (you may choose any output encoding you would like).

1. The 3-bit binary number $a_2a_1a_0$ is greater than the other binary number $b_2b_1b_0$.
2. The 3-bit binary number $a_2a_1a_0$ is less than the other binary number $b_2b_1b_0$.
3. The 3-bit binary number $a_2a_1a_0$ is equal to the other binary number $b_2b_1b_0$.

IMPORTANT: You must demonstrate your solution to part A, B, and C on the breadboard. Lab grade will depend on the working of the circuit and will be checked off by the lab instructor. This demonstration must be completed within the window of your lab section meeting.

Note: Use the sheet posted in the lab (to the left of the circuit bins) to find the location of the chip you are looking for. All of the bins are labeled. To find datasheets for a particular chip, use the product search on Jameco. Once you have found the chip, click on the datasheet PDF to find the pin mappings.