

Lab 5 - Sequential Logic Circuits (I)

CDA 3201L-003

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Purpose and Objectives

In this lab we set out to understand the connections between latches, SR, JK, and Data flip flops and how the clock cycle is apart of their design. We will convert between the different flip flops and latches to demonstrate an understanding in how they differ and the outputs that are carried out by them and potentially what these are used for in a computer system.

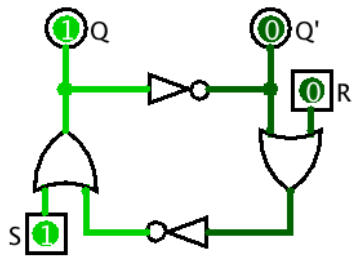
Component List

- Breadboard
- Wiring
- 5v power supply
- TTL 0.5 Htz Function Generator
- 2 x Dual J-K Flip-Flops With Preset And Clear (74LS76)
- 1 x Dual Positive Edge Triggerd D Flip-Flops (74LS74)
- 1 x Quad 2 input NOR Gate (74LS02)
- 2 x Hex Inverter (74LS04)
- 1 x Quad 2 input AND Gate (74LS08)
- 12 x LED
- 12 x Resistor (470 Ohms 5%)

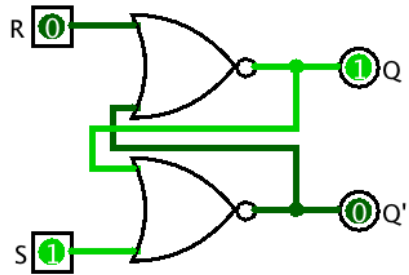
Design

Latches

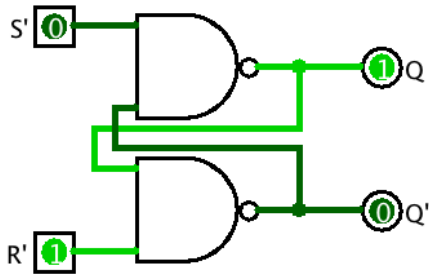
Basic Bistable SR Latch



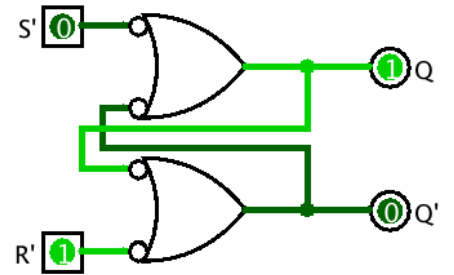
NOR SR Latch



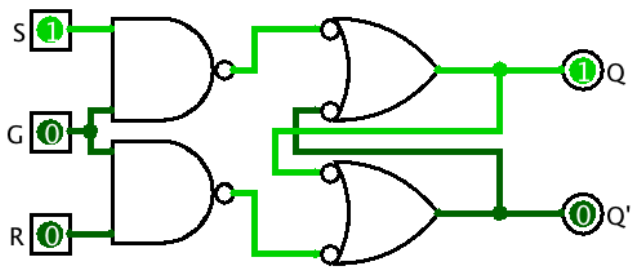
NAND SR Latch



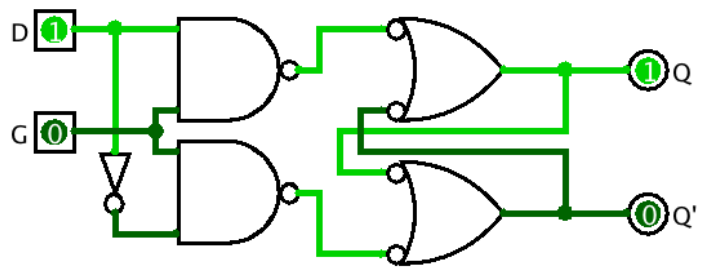
OR SR Latch



Gated SR Latch



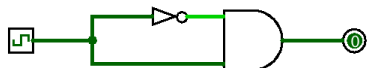
Gated D Latch



Flip Flops

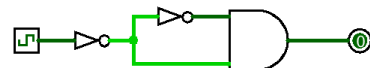
Leading Edge Detector

increase nots to increase duty cycle



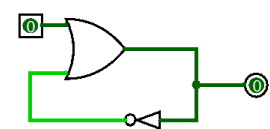
Trailing Edge Detector

increase nots to increase duty cycle

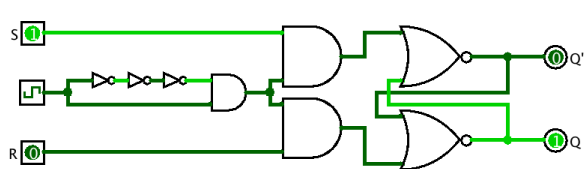


Clock

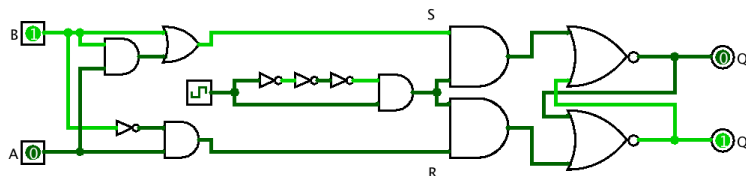
increase nots to increase period



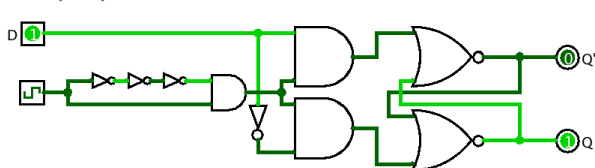
SR Flip Flop



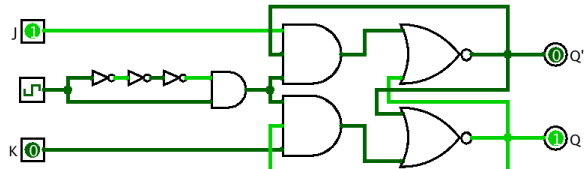
SR Flip Flop w/ Additional Logic



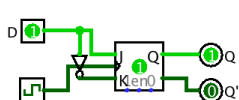
D Flip Flop



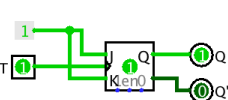
JK Flip Flop



JK Flip Flop as D Flip Flop



JK Flip Flop as T Flip Flop



Test Vectors and Verification

We tested every possible combination of inputs and compared with the truth table.

x	y	Q(A)	Q(B)	Q(C)	Q(D)	Q(E)
0	0	Q(t)	-	-	Q	Q
0	1	0	0	0	0	1
1	0	1	1	1	1	0
1	1	Q'(t)	-	-	Q'	1

Q represents output to the corresponding letter part. Because each flip flop provides the same function as the other parts, each output is the same. The difference lies in the circuit design, however part E required a different output and consequently has different truth values for its output.

Discussion and Conclusion

In this lab we demonstrated how flip flops are created using AND, NOT, and NOR gates and latches

using OR, NOT, and NAND gates. We also discovered that by adding inverters between the clock pulse and the gate for the flip flop, the duty cycle increases. JK flips can easily be converted to Data flip flops by removing one input and splitting the other input into two, inverting one of the branches. This insures that both inputs into the flip flop can not match logical values. Building these helped visualize in a tangible way how latches and flip flops can be used as data storage elements in computers.