# Yi Chien (Jason) Lin

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## RESEARCH

### FPGA/PARALLEL COMPUTING LAB | Graduate Researcher
Sept. 2020 – Present | Los Angeles, CA
Worked with **Professor Prasanna** on AI/ML acceleration on heterogeneous computing.

### DATA PROCESSING SYSTEM LAB | undergraduate Researcher
Sept. 2018 – July. 2020 | Taipei, Taiwan
Worked with **Professor Yi-Chang Lu** on hardware accelerator for DNA sequence alignment.
- Designed Application-Specific Integrated Circuit (ASIC) for sequence alignment with two-piece affine gap tracebacks.
- Implemented Smith-Waterman algorithm using systolic array. **[Link]**

### MICRO SYSTEM RESEARCH LAB | undergraduate Researcher
July. 2019 – Jan. 2020 | Taipei, Taiwan
Worked with **Professor Tzi-Dar Chiueh** on digital circuit design.
- Taped-out a 5 stage pipelined RISC-V CPU on a 1.5mm×1.5mm chip with 180nm technology. **[Link]**
- Perform the entire IC design flow, from design to synthesis, place& route, verification and tape-out.

## PUBLICATION

[1]  **Y. Lin**, B. Zhang, and V. Prasanna. End-to-end gcn inference acceleration using high-level synthesis. In 2021 IEEE 29rd Annual International Symposium on Field-Programmable Custom Computing Machines, 2021. **UNDER REVIEW** .

## EDUCATION

### UNIVERSITY OF SOUTHERN CALIFORNIA | PhD in Electrical Engineering
Sept. 2020 - Present | Los Angeles, CA · Cum. GPA: 3.85/4.0

### NATIONAL TAIWAN UNIVERSITY | BS in Electrical Engineering
Sept. 2016 - June. 2020 | Taipei, Taiwan · Cum. GPA: 3.75/4.3

## WORK EXPERIENCE

### HEWLETT & PACKARD INC.(HP) | Electrical Engineering R&D Intern at Commercial Notebook Team
July. 2019 – July. 2020 | Taipei, Taiwan
- Developed a software that could enhance efficiency of cursor movement. Idea has been patented by HP.
- Developed a system that provides users with different preference settings based on different scenario.

## AWARDS & PATENTS

### 3RD PRIZE | 2019
NTUEE Undergraduate Innovation Award

### PCT/US20/13419 | 2019
"Face Orientation Based Cursor Positioning on Display Screens" Application in progress.

# LANGUAGES

## PROGRAMMING
Verilog/SystemVerilog • High-Level Synthesis • C/C++ • Python

## TOOLS
Xilinx Vitis • Cadence NC-Verilog • Synopsis Design Compiler • Cadence Innovous

## ENGLISH
GRE:
V:154, Q:169, AW:3.5
TOEFL:108
R:29, L:29, W:27, S:23