Yi-Chien (Jason) Lin

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SUMMARY

I am a Ph.D. Candidate at the University of Southern California. My research focus lies at the intersection of Machine Learning and High-Performance Computing. I am particularly interested in accelerating Graph Neural Networks on heterogeneous platforms, and I have published several papers in this area. Details of my works can be found below in the Publication Section.

RESEARCH EXPERIENCE

GRADUATE RESEARCHER | FPGA/Parallel Computing Lab

Sept. 2020 – Present | Los Angeles, CA

Working with **Professor Prasanna** on Graph Neural Network (GNN) training acceleration on heterogeneous platforms.

UNDERGRADUATE RESEARCHER | Digital Circuit Design

Sept. 2018 – July. 2020 | Taipei, Taiwan

- Designed Application-Specific Integrated Circuit (ASIC) for accelerating sequence alignment. **[Link]**
- Taped-out a 5-stage pipelined RISC-V CPU on a 1.5mm×1.5mm chip with 180nm technology. **[Link]**
- Performed the entire IC design flow, from RTL design to synthesis, place & route, verification, and tape-out.

PUBLICATIONS

[1] **Yi-Chien Lin** , Yuyang Chen, Sameh Gobriel, Nilesh Jain, Gopi Krishna Jhaand, and Viktor Prasanna. ***ARGO: An Auto-Tuning Runtime System for Scalable GNN Training on Multi-Core Processor*** . In IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2024 **[Under Review]** .

[2] **Yi-Chien Lin** and Viktor Prasanna. ***HyScale-GNN: A Scalable Hybrid GNN Training System on Single-Node Heterogeneous Architecture*** . In IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2023.

[3] **Yi-Chien Lin** , Bingyi Zhang, and Viktor Prasanna. ***HitGNN: High-throughput GNN Training Framework on CPU+Multi-FPGA Heterogeneous Platform*** . In IEEE Transactions on Parallel and Distributed Systems (TPDS), 2023 **[Under Review]** .

[4] **Yi-Chien Lin** , Bingyi Zhang, and Viktor Prasanna. ***Accelerating GNN Training on CPU+Multi-FPGA Heterogeneous Platform*** . In Latin American High Performance Computing Conference (CARLA), 2022.

[5] **Yi-Chien Lin** , Bingyi Zhang, and Viktor Prasanna. ***HP-GNN: Generating High Throughput GNN Training Implementation on CPU-FPGA Heterogeneous Platform*** . In ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2022.

[6] **Yi-Chien Lin** , Bingyi Zhang, and Viktor Prasanna. ***GCN Inference Acceleration using High-Level Synthesis*** . In IEEE High Performance Extreme Computing Conference (HPEC), 2021.

[7] **Yi-Chien Lin** , Chih-Hung Lin, Ling-Yu Wu, and Chih-Shiuan Lee. ***Face Orientation-based Cursor Positioning on Display Screens*** (WIPO Patent No. WO/2021/145855). 2021.

[8] Jing-Ping Wu, **Yi-Chien Lin** , Ying-Wei Wu, Shih-Wei Hsieh, Ching-Hsuan Tai, and Yi-Chang Lu. ***A Memory-Efficient Accelerator for DNA Sequence Alignment with Two-Piece Affine Gap Tracebacks*** . In IEEE International Symposium on Circuits and Systems (ISCAS), 2021.

EDUCATION

UNIVERSITY OF SOUTHERN CALIFORNIA | Ph.D. in Electrical Engineering

September 2020 - August 2025 (anticipated) | Los Angeles, CA • Cum. GPA: 3.88/4.0

NATIONAL TAIWAN UNIVERSITY | B.S. in Electrical Engineering

September 2016 - June 2020 | Taipei, Taiwan • Cum. GPA: 3.75/4.3

WORK EXPERIENCE & SERVICES

REGISTRATION CHAIR | The 31st IEEE FCCM Conference
May 2023 | Los Angeles, CA

STUDENT VOLUNTEER | The 37th IEEE International Parallel & Distributed Processing Symposium
May 2023 | St. Petersburg, FL

CONFERENCE/JOURNAL REVIEWER
2020 - Present

- IEEE International Parallel & Distributed Processing Symposium (IPDPS)
- ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)
- International Conference for High Performance Computing, Networking, Storage, and Analysis (SC)
- IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)
- IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)

HEWLETT & PACKARD INC. (HP) | Electrical Engineering R&D Intern
July 2019 – July 2020 | Taipei, Taiwan
Proposed a software design to enhance cursor movement efficiency; this idea has been patented by HP.

TEACHING ASSISTANT

- EE451: Parallel and Distributed Computation
- EE457: Computer Systems Organization

AWARDS

VITERBI SCHOOL OF ENGINEERING FELLOWSHIP
Los Angeles, CA. 2020

NTUEE UNDERGRADUATE INNOVATION AWARD Third Prize
Taipei, Taiwan. 2019

RELEVANT COURSE

EE451 Parallel and Distributed Computations • EE457 Computer Systems Organization • EE557 Computer Systems Architecture • EE599 Accelerated Computing using FPGAs • CS567 Machine Learning • CS570 Analysis of Algorithms

PROGRAMMING LANGUAGES

SOFTWARE
C/C++ • Python

PARALLEL PROGRAMMING
Pthreads • MPI • OpenMP • CUDA

HARDWARE
Verilog/SystemVerilog • High-Level Synthesis • oneAPI

HARDWARE DESIGN TOOLS
Xilinx Vitis • Cadence NC-Verilog • Synopsis Design Compiler • Cadence Innovous