

# Yi-Chien (Jason) Lin

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## SUMMARY

I am a Ph.D. Candidate at the University of Southern California. My research focus lies at the intersection of Machine Learning and High-Performance Computing (HPC) Systems. Through my research and teaching experience, I have built a solid background in Computer Architecture, Parallel and Distributed Computations, and ML Hardware. My projects in hardware design and ML accelerator have received 100+ stars on GitHub. I have published extensively and hold a WIPO patent.

## RESEARCH EXPERIENCE

### GRADUATE RESEARCHER | FPGA/PARALLEL COMPUTING LAB

Sept. 2020 – Present | Los Angeles, CA

Working with **Professor Prasanna** on Graph Neural Network (GNN) training acceleration on heterogeneous platforms.

### UNDERGRADUATE RESEARCHER | DIGITAL CIRCUIT DESIGN

Sept. 2018 – July. 2020 | Taipei, Taiwan

- Designed Application-Specific Integrated Circuit (ASIC) for accelerating sequence alignment. [\[Link\]](#)
- Taped-out a 5-stage pipelined RISC-V CPU on a 1.5mm×1.5mm chip with 180nm technology. [\[Link\]](#)
- Performed the entire IC design flow, from RTL design to synthesis, place & route, verification, and tape-out.

## PUBLICATIONS

- [1] Yi-Chien Lin, Zhijie Xu, and Viktor Prasanna. *HEAT: A High-throughput and Energy-efficient Accelerator for Large-scale GNN Training*. In IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM), 2024 [\[Under Review\]](#).
- [2] Yi-Chien Lin, Gangde Deng, and Viktor Prasanna. *A Unified CPU-GPU Protocol for GNN Training*. In ACM International Conference on Computing Frontiers (CF), 2024 [\[Under Review\]](#).
- [3] Yi-Chien Lin, Bingyi Zhang, and Viktor Prasanna. *HitGNN: High-throughput GNN Training Framework on CPU+Multi-FPGA Heterogeneous Platform*. In IEEE Transactions on Parallel and Distributed Systems (TPDS), 2024 [\[Under Review\]](#).
- [4] Yi-Chien Lin, Yuyang Chen, Sameh Gobriel, Nilesch Jain, Gopi Krishna Jhaand, and Viktor Prasanna. *ARGO: An Auto-Tuning Runtime System for Scalable GNN Training on Multi-Core Processor*. In IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2024.
- [5] Yi-Chien Lin and Viktor Prasanna. *HyScale-GNN: A Scalable Hybrid GNN Training System on Single-Node Heterogeneous Architecture*. In IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2023.
- [6] Yi-Chien Lin, Bingyi Zhang, and Viktor Prasanna. *Accelerating GNN Training on CPU+Multi-FPGA Heterogeneous Platform*. In Latin American High Performance Computing Conference (CARLA), 2022.
- [7] Yi-Chien Lin, Bingyi Zhang, and Viktor Prasanna. *HP-GNN: Generating High Throughput GNN Training Implementation on CPU-FPGA Heterogeneous Platform*. In ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2022.
- [8] Yi-Chien Lin, Bingyi Zhang, and Viktor Prasanna. *GCN Inference Acceleration using High-Level Synthesis*. In IEEE High Performance Extreme Computing Conference (HPEC), 2021.
- [9] Yi-Chien Lin, Chih-Hung Lin, Ling-Yu Wu, and Chih-Shiuan Lee. *Face Orientation-based Cursor Positioning on Display Screens* (WIPO Patent No. WO/2021/145855). 2021.
- [10] Jing-Ping Wu, Yi-Chien Lin, Ying-Wei Wu, Shih-Wei Hsieh, Ching-Hsuan Tai, and Yi-Chang Lu. *A Memory-Efficient Accelerator for DNA Sequence Alignment with Two-Piece Affine Gap Tracebacks*. In IEEE International Symposium on Circuits and Systems (ISCAS), 2021.

## EDUCATION

### UNIVERSITY OF SOUTHERN CALIFORNIA | PH.D. IN ELECTRICAL ENGINEERING

September 2020 - August 2025 (anticipated) | Los Angeles, CA • Cum. GPA: 3.88/4.0

### NATIONAL TAIWAN UNIVERSITY | B.S. IN ELECTRICAL ENGINEERING

September 2016 - June 2020 | Taipei, Taiwan • Cum. GPA: 3.75/4.3

## WORK EXPERIENCE & SERVICES

### REGISTRATION CHAIR | THE 31ST IEEE FCCM CONFERENCE

May 2023 | Los Angeles, CA

### STUDENT VOLUNTEER | THE 37TH IEEE INTERNATIONAL PARALLEL & DISTRIBUTED PROCESSING SYMPOSIUM

May 2023 | St. Petersburg, FL

### CONFERENCE/JOURNAL REVIEWER

2020 - Present

- IEEE International Parallel & Distributed Processing Symposium (IPDPS)
- ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)
- International Conference for High Performance Computing, Networking, Storage, and Analysis (SC)
- IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)
- IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)

### HEWLETT & PACKARD INC. (HP) | ELECTRICAL ENGINEERING R&D INTERN

July 2019 – July 2020 | Taipei, Taiwan

Proposed a software design to enhance cursor movement efficiency; this idea has been patented by HP.

### TEACHING ASSISTANT

- EE451: Parallel and Distributed Computation
- EE457: Computer Systems Organization

## AWARDS

### VITERBI SCHOOL OF ENGINEERING FELLOWSHIP

Los Angeles, CA. 2020

### NTUEE UNDERGRADUATE INNOVATION AWARD THIRD PRIZE

Taipei, Taiwan. 2019

## RELEVANT COURSE

EE451 Parallel and Distributed Computations • EE457 Computer Systems Organization • EE557 Computer Systems Architecture • EE599 Accelerated Computing using FPGAs • CS567 Machine Learning • CS570 Analysis of Algorithms

## PROGRAMMING LANGUAGES

### SOFTWARE

C/C++ • Python

### PARALLEL PROGRAMMING

Pthreads • MPI • OpenMP • CUDA

### HARDWARE

Verilog/SystemVerilog • High-Level Synthesis (HLS) • oneAPI

### HARDWARE DESIGN TOOLS

Xilinx Vitis • Cadence NC-Verilog • Synopsis Design Compiler • Cadence Innovous