

Yi Chien (Jason) Lin

✉ yichient@usc.edu

in [jasonlin316](#)  [jasonlin316.github.io](#)  [jasonlin316](#)

RESEARCH

FPGA/PARALLEL COMPUTING LAB | GRADUATE RESEARCHER

Sept. 2020 – Present | Los Angeles, CA

Currently working with **Professor Prasanna** on Graph Neural Network (GNN) training acceleration on heterogeneous platforms (Publication [1]-[3]).

DATA PROCESSING SYSTEM LAB | UNDERGRADUATE RESEARCHER

Sept. 2018 – July. 2020 | Taipei, Taiwan

Worked with **Professor Yi-Chang Lu** on hardware accelerator for DNA sequence alignment.

- Designed Application-Specific Integrated Circuit (ASIC) for sequence alignment (Publication [5]).
- Implemented Smith-Waterman algorithm using systolic array. [\[Link\]](#)

MICRO SYSTEM RESEARCH LAB | UNDERGRADUATE RESEARCHER

July. 2019 – Jan. 2020 | Taipei, Taiwan

Worked with **Professor Tzi-Dar Chiueh** on digital circuit design.

- Taped-out a 5 stage pipelined RISC-V CPU on a 1.5mm × 1.5mm chip with 180nm technology. [\[Link\]](#)
- Performed the entire IC design flow, from RTL design to synthesis, place& route, verification and tape-out.

PUBLICATION & PATENTS

- [1] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. *Accelerating GNN Training on CPU+Multi-FPGA Heterogeneous Platform*. In Latin American High Performance Computing Conference (CARLA), 2022.
- [2] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. *Hp-gnn: generating high throughput gnn training implementation on cpu-fpga heterogeneous platform*. In ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2022.
- [3] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. *Gcn Inference Acceleration Using High-level Synthesis*. In IEEE High Performance Extreme Computing Conference (HPEC), 2021.
- [4] **Yi-Chien Lin**, Chih hung Lin, Ling-Yu Wu, and Chih shiuan Lee. *Face Orientation-based Cursor Positioning on Display Screens*. In WO Patent WO/2021/145855, 2021.
- [5] Jing-Ping Wu, **Yi-Chien Lin**, Ying-Wei Wu, Shih-Wei Hsieh, Ching-Hsuan Tai, and Yi-Chang Lu. *A Memory-efficient Accelerator for Dna Sequence Alignment with Two-piece Affine Gap Tracebacks*. In IEEE International Symposium on Circuits and Systems (ISCAS), 2021.

EDUCATION

UNIVERSITY OF SOUTHERN CALIFORNIA | PH.D. IN ELECTRICAL ENGINEERING

Sept. 2020 – Present | Los Angeles, CA • Cum. GPA: 3.84/4.0

NATIONAL TAIWAN UNIVERSITY | B.S. IN ELECTRICAL ENGINEERING

Sept. 2016 – June. 2020 | Taipei, Taiwan • Cum. GPA: 3.75/4.3

WORK EXPERIENCE & SERVICES

CONFERENCE/JOURNAL REVIEWER

2020 – Present

IPDPS '23, FPGA '23, CSUR '22, ASAP '22, SC '22, TCSVT '22, FPGA '22, FPT '21, SC '21.

HEWLETT & PACKARD INC.(HP) | ELECTRICAL ENGINEERING R&D INTERN AT COMMERCIAL NOTEBOOK TEAM

July. 2019 – July. 2020 | Taipei, Taiwan

Proposed a software design to enhance cursor movement efficiency. This idea has been patented by HP (Patent [4]).

TEACHING ASSISTANT

- EE451: Parallel and Distributed Computation
- EE457: Computer Architecture

AWARDS

VITERBI SCHOOL OF ENGINEERING FELLOWSHIP

Los Angeles, CA. 2020

NTUEE UNDERGRADUATE INNOVATION AWARD THIRD PRIZE

Taipei, Taiwan. 2019

LANGUAGES

PROGRAMMING

Verilog/SystemVerilog • High-Level Synthesis • C/C++ • Python

TOOLS

Xilinx Vitis • Cadence NC-Verilog • Synopsis Design Compiler • Cadence Innovous