Yi-Chien (Jason) Lin

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SUMMARY

I am a Ph.D. Candidate at the University of Southern California, expecting to graduate in August, 2025. My research interests lie at the intersection of Machine Learning (ML) and Systems. My recent work focuses on developing Automated ML Systems, such as an auto-tuning runtime system for GNN training, and automatic model parallelization for LLM serving. I've published extensively in this domain, and my work, ARGO (Publications [4]), was integrated into Deep Graph Library, a state-of-the-art Graph ML framework.

RESEARCH EXPERIENCE

RESEARCH ASSISTANT | FPGA/Parallel Computing Lab

Aug. 2020 – Present | Los Angeles, CA

Working with **Professor Prasanna** on developing ML Systems for Graph ML on emerging heterogeneous platforms.

RESEARCH INTERN | Microsoft Research

May 2024 – Aug. 2024 | Mountain View, CA

Worked with the AI Framework Team on developing solution for automatic model partitioning for LLM serving systems.

PUBLICATIONS

[1] **Yi-Chien Lin**, Woosuk Kwon, Ronald Pineda, and Fanny Nina Paravecino. ***Toward High-Performance LLM Serving: A Simulation-Based Approach for Identifying Optimal Parallelism***. In arXiv preprint arXiv:2411.17651, 2024.

[2] **Yi-Chien Lin**, Zhijie Xu, and Viktor Prasanna. ***xBS-GNN: Accelerating Billion-Scale GNN Training on FPGA***. In Workshops of The International Conference on High Performance Computing, Network, Storage, and Analysis (SC-W), 2024.

[3] **Yi-Chien Lin**, Gangde Deng, and Viktor Prasanna. ***A Unified CPU-GPU Protocol for GNN Training***. In ACM International Conference on Computing Frontiers (CF), 2024.

[4] **Yi-Chien Lin**, Yuyang Chen, Sameh Gobriel, Nilesh Jain, Gopi Krishna Jhaand, and Viktor Prasanna. ***ARGO: An Auto-Tuning Runtime System for Scalable GNN Training on Multi-Core Processor***. In IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2024 **[Best Paper Nominee]**.

[5] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. ***HitGNN: High-throughput GNN Training Framework on CPU+Multi-FPGA Heterogeneous Platform***. In IEEE Transactions on Parallel and Distributed Systems (TPDS), 2024.

[6] **Yi-Chien Lin** and Viktor Prasanna. ***HyScale-GNN: A Scalable Hybrid GNN Training System on Single-Node Heterogeneous Architecture***. In IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2023.

[7] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. ***Accelerating GNN Training on CPU+Multi-FPGA Heterogeneous Platform***. In Latin American High Performance Computing Conference (CARLA), 2022.

[8] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. ***HP-GNN: Generating High Throughput GNN Training Implementation on CPU-FPGA Heterogeneous Platform***. In ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2022.

[9] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. ***GCN Inference Acceleration using High-Level Synthesis***. In IEEE High Performance Extreme Computing Conference (HPEC), 2021.

[10] Jing-Ping Wu, **Yi-Chien Lin**, Ying-Wei Wu, Shih-Wei Hsieh, Ching-Hsuan Tai, and Yi-Chang Lu. ***A Memory-Efficient Accelerator for DNA Sequence Alignment with Two-Piece Affine Gap Tracebacks***. In IEEE International Symposium on Circuits and Systems (ISCAS), 2021.

PATENTS

[1] **Yi-Chien Lin** and Chih-Hung Lin and Ling-Yu Wu and Chih-Shiuan Lee. ***Face Orientation-Based Cursor Positioning on Display Screens.*** In WIPO Patent No. WO/2021/145855), 2021.

EDUCATION

UNIVERSITY OF SOUTHERN CALIFORNIA | Ph.D. in Electrical Engineering
September 2020 - August 2025 | Los Angeles, CA • Cum. GPA: 3.88/4.0

UNIVERSITY OF SOUTHERN CALIFORNIA | M.S. in Electrical Engineering
September 2020 - May 2024 | Los Angeles, CA • Cum. GPA: 3.88/4.0

NATIONAL TAIWAN UNIVERSITY | B.S. in Electrical Engineering
September 2016 - June 2020 | Taipei, Taiwan • Cum. GPA: 3.75/4.3

WORK EXPERIENCE & SERVICES

WORKSHOP CHAIR | The 31st IEEE HiPC Conference
2024 | Bengaluru, India

REGISTRATION CHAIR | The 31st IEEE FCCM Conference
May 2023 | Los Angeles, CA

STUDENT VOLUNTEER | The 37th IEEE IPDPS Conference
May 2023 | St. Petersburg, FL

CONFERENCE/JOURNAL REVIEWER IEEE IPDPS, ACM FPGA, SC, IEEE ASAP
2020 - Present

TEACHING ASSISTANT

- EE451: Parallel and Distributed Computation (Spring '21, Fall '22)
- EE457: Computer Systems Organization (Fall '21)

ELECTRICAL ENGINEERING R&D INTERN | Hewlett & Packard Inc. (HP)
July 2019 – July 2020 | Taipei, Taiwan

AWARDS

CAPITAL ONE FELLOW
USC-Capital One Center for Responsible AI and Decision Making in Finance (CREDIF). 2024

SRC AIHW ANNUAL REVIEW BEST PRESENTATION AWARD
Wilmington, MA. 2024

IPDPS BEST POSTER AWARD Honorable Mention
San Francisco, CA. 2024

VITERBI SCHOOL OF ENGINEERING FELLOWSHIP
Los Angeles, CA. 2020

NTUEE UNDERGRADUATE INNOVATION AWARD Third Prize
Taipei, Taiwan. 2019

SKILLS

PARALLEL PROGRAMMING Pthreads • MPI • OpenMP • CUDA

HARDWARE PROGRAMMING Verilog/SystemVerilog • High-Level Synthesis (HLS) • oneAPI