Yi-Chien (Jason) Lin

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RESEARCH

FPGA/PARALLEL COMPUTING LAB | Graduate Researcher

Sept. 2020 – Present | Los Angeles, CA

Currently working with **Professor Prasanna** on Graph Neural Network (GNN) training acceleration on heterogeneous platforms (Publication [1]-[5]).

DATA PROCESSING SYSTEM LAB | undergraduate Researcher

Sept. 2018 – July. 2020 | Taipei, Taiwan

Worked with **Professor Yi-Chang Lu** on hardware accelerator for DNA sequence alignment.

- Designed Application-Specific Integrated Circuit (ASIC) for sequence alignment (Publication [7]).
- Implemented Smith-Waterman algorithm using systolic array. **[Link]**

MICRO SYSTEM RESEARCH LAB | undergraduate Researcher

July. 2019 – Jan. 2020 | Taipei, Taiwan

Worked with **Professor Tzi-Dar Chiueh** on digital circuit design.

- Taped-out a 5 stage pipelined RISC-V CPU on a 1.5mm$\times$1.5mm chip with 180nm technology. **[Link]**
- Performed the entire IC design flow, from RTL design to synthesis, place& route, verification and tape-out.

PUBLICATIONS & PATENTS

[1] **Yi-Chien Lin** and Viktor Prasanna. ***HyScale-GNN: A Scalable Hybrid GNN Training System on Single-Node Heterogeneous Architecture***. In IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2023.

[2] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. ***HitGNN: High-throughput GNN Training Framework on CPU+Multi-FPGA Heterogeneous Platform***. In IEEE Transactions on Parallel and Distributed Systems (TPDS), 2023 (**Under Review**).

[3] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. ***Accelerating GNN Training on CPU+Multi-FPGA Heterogeneous Platform***. In Latin American High Performance Computing Conference (CARLA), 2022.

[4] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. ***Hp-gnn: generating high throughput gnn training implementation on cpu-fpga heterogeneous platform***. In ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2022.

[5] **Yi-Chien Lin**, Bingyi Zhang, and Viktor Prasanna. ***Gcn Inference Acceleration Using High-level Synthesis***. In IEEE High Performance Extreme Computing Conference (HPEC), 2021.

[6] **Yi-Chien Lin**, Chih-Hung Lin, Ling-Yu Wu, and Chih-Shiuan Lee. ***Face Orientation-based Cursor Positioning on Display Screens*** (WIPO Patent No. WO/2021/145855). 2021.

[7] Jing-Ping Wu, **Yi-Chien Lin**, Ying-Wei Wu, Shih-Wei Hsieh, Ching-Hsuan Tai, and Yi-Chang Lu. ***A Memory-efficient Accelerator for Dna Sequence Alignment with Two-piece Affine Gap Tracebacks***. In IEEE International Symposium on Circuits and Systems (ISCAS), 2021.

EDUCATION

UNIVERSITY OF SOUTHERN CALIFORNIA | Ph.D. in Electrical Engineering

Sept. 2020 - Present | Los Angeles, CA • Cum. GPA: 3.86/4.0

NATIONAL TAIWAN UNIVERSITY | B.S. in Electrical Engineering

Sept. 2016 - June. 2020 | Taipei, Taiwan • Cum. GPA: 3.75/4.3

WORK EXPERIENCE & SERVICES

CONFERENCE/JOURNAL REVIEWER

2020 - Present

IPDPS '23, FPGA '23, CSUR '22, ASAP '22, SC '22, TCSVT '22, FPGA '22, FPT '21, SC '21.

HEWLETT & PACKARD INC.(HP) | Electrical Engineering R&D Intern at Commercial Notebook Team

July. 2019 – July. 2020 | Taipei, Taiwan

Proposed a software design to enhance cursor movement efficiency. This idea has been patented by HP (Patent [6]).

TEACHING ASSISTANT

- EE451: Parallel and Distributed Computation
- EE457: Computer Systems Organization

AWARDS

VITERBI SCHOOL OF ENGINEERING FELLOWSHIP

Los Angeles, CA. 2020

NTUEE UNDERGRADUATE INNOVATION AWARD Third Prize

Taipei, Taiwan. 2019

PROGRAMMING LANGUAGES

HARDWARE

Verilog/SystemVerilog • High-Level Synthesis • oneAPI

SOFTWARE

C/C++ • Python

PARALLEL

MPI • OpenMP • CUDA

HARDWARE DESIGN TOOLS

Xilinx Vitis • Cadence NC-Verilog • Synopsis Design Compiler • Cadence Innovous