Yi-Chien (Jason) Lin

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SUMMARY

I am a Ph.D. Candidate at the University of Southern California. My research interests lie at the intersection of Machine Learning (ML) and Systems. My recent work focuses on developing Automated ML Systems for Graph ML, such as auto-tuning runtime system and FPGA framework that automatically generates hardware designs. I have published extensively in this domain, and one of my works, ARGO (Publications [2]), is available on Deep Graph Library, a state-of-the-art library for Graph ML.

RESEARCH EXPERIENCE

RESEARCH ASSISTANT | FPGA/Parallel Computing Lab

Aug. 2020 – Present | Los Angeles, CA

Working with **Professor Prasanna** on developing ML Systems for Graph Neural Network on emerging heterogeneous platforms.

RESEARCH INTERN | Microsoft Research

May 2024 – Aug. 2024 | Mountain View, CA

Working with the AI Framework Team on developing ML Systems for Multimodal Large Language Models.

PUBLICATIONS

[1] **Yi-Chien Lin** , Gangde Deng, and Viktor Prasanna. ***A Unified CPU-GPU Protocol for GNN Training*** . In ACM International Conference on Computing Frontiers (CF), 2024.

[2] **Yi-Chien Lin** , Yuyang Chen, Sameh Gobriel, Nilesh Jain, Gopi Krishna Jhaand, and Viktor Prasanna. ***ARGO: An Auto-Tuning Runtime System for Scalable GNN Training on Multi-Core Processor*** . In IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2024 **[Best Paper Nominee]** .

[3] **Yi-Chien Lin** , Bingyi Zhang, and Viktor Prasanna. ***HitGNN: High-throughput GNN Training Framework on CPU+Multi-FPGA Heterogeneous Platform*** . In IEEE Transactions on Parallel and Distributed Systems (TPDS), 2024.

[4] **Yi-Chien Lin** and Viktor Prasanna. ***HyScale-GNN: A Scalable Hybrid GNN Training System on Single-Node Heterogeneous Architecture*** . In IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2023.

[5] **Yi-Chien Lin** , Bingyi Zhang, and Viktor Prasanna. ***Accelerating GNN Training on CPU+Multi-FPGA Heterogeneous Platform*** . In Latin American High Performance Computing Conference (CARLA), 2022.

[6] **Yi-Chien Lin** , Bingyi Zhang, and Viktor Prasanna. ***HP-GNN: Generating High Throughput GNN Training Implementation on CPU-FPGA Heterogeneous Platform*** . In ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2022.

[7] **Yi-Chien Lin** , Bingyi Zhang, and Viktor Prasanna. ***GCN Inference Acceleration using High-Level Synthesis*** . In IEEE High Performance Extreme Computing Conference (HPEC), 2021.

[8] **Yi-Chien Lin** , Chih-Hung Lin, Ling-Yu Wu, and Chih-Shiuan Lee. ***Face Orientation-based Cursor Positioning on Display Screens*** (WIPO Patent No. WO/2021/145855). 2021.

[9] Jing-Ping Wu, **Yi-Chien Lin** , Ying-Wei Wu, Shih-Wei Hsieh, Ching-Hsuan Tai, and Yi-Chang Lu. ***A Memory-Efficient Accelerator for DNA Sequence Alignment with Two-Piece Affine Gap Tracebacks*** . In IEEE International Symposium on Circuits and Systems (ISCAS), 2021.

EDUCATION

UNIVERSITY OF SOUTHERN CALIFORNIA | Ph.D. in Electrical Engineering

September 2020 - August 2025 (anticipated) | Los Angeles, CA • Cum. GPA: 3.88/4.0

UNIVERSITY OF SOUTHERN CALIFORNIA | M.S. in Electrical Engineering

September 2020 - May 2024 | Los Angeles, CA • Cum. GPA: 3.88/4.0

NATIONAL TAIWAN UNIVERSITY | B.S. IN ELECTRICAL ENGINEERING
September 2016 - June 2020 | Taipei, Taiwan • Cum. GPA: 3.75/4.3

WORK EXPERIENCE & SERVICES

REGISTRATION CHAIR | THE 31ST IEEE FCCM CONFERENCE
May 2023 | Los Angeles, CA

STUDENT VOLUNTEER | THE 37TH IEEE INTERNATIONAL PARALLEL & DISTRIBUTED PROCESSING SYMPOSIUM
May 2023 | St. Petersburg, FL

CONFERENCE/JOURNAL REVIEWER
2020 - Present

- IEEE International Parallel & Distributed Processing Symposium (IPDPS)
- ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)
- International Conference for High Performance Computing, Networking, Storage, and Analysis (SC)
- IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)
- IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)

HEWLETT & PACKARD INC. (HP) | ELECTRICAL ENGINEERING R&D INTERN
July 2019 – July 2020 | Taipei, Taiwan
Proposed a software design to enhance cursor movement efficiency; this idea has been patented by HP (Publications [8]).

TEACHING ASSISTANT

- EE451: Parallel and Distributed Computation
- EE457: Computer Systems Organization

AWARDS

SRC AIHW ANNUAL REVIEW BEST PRESENTATION AWARD
Wilmington, MA. 2024

IPDPS BEST POSTER AWARD HONORABLE MENTION
San Francisco, CA. 2024

VITERBI SCHOOL OF ENGINEERING FELLOWSHIP
Los Angeles, CA. 2020

NTUEE UNDERGRADUATE INNOVATION AWARD THIRD PRIZE
Taipei, Taiwan. 2019

PROGRAMMING LANGUAGES

SOFTWARE
C/C++ • Python

PARALLEL PROGRAMMING
Pthreads • MPI • OpenMP • CUDA

HARDWARE
Verilog/SystemVerilog • High-Level Synthesis (HLS) • oneAPI

HARDWARE DESIGN TOOLS
Xilinx Vitis • Cadence NC-Verilog • Synopsis Design Compiler • Cadence Innovous