

LAB#A-2

Design Analysis

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Github Link:

https://github.com/jasonlo0509/DCT_HLS_Optimization

Outline

- Objective
- 5 Optimizations (Pragmas)
 - Inner-loop Pipelining
 - Critical Outer-loop Pipepining
 - Array Partitioning
 - Apply Dataflow (Inter-Function Pipelining)
 - Inline (Apply Dataflow to Sub-Funtion)
- Result

Objective

目標：
用 Vivado HLS 分析並將 DCT
優化成每 100 cycles 內可以吃下一筆資料

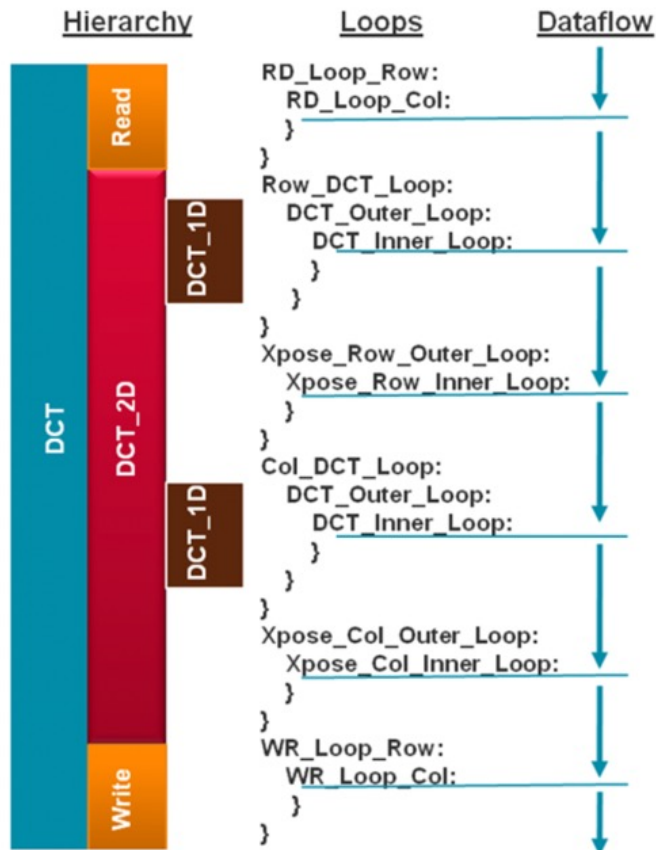


Figure 6-3: Overview of the DCT Design

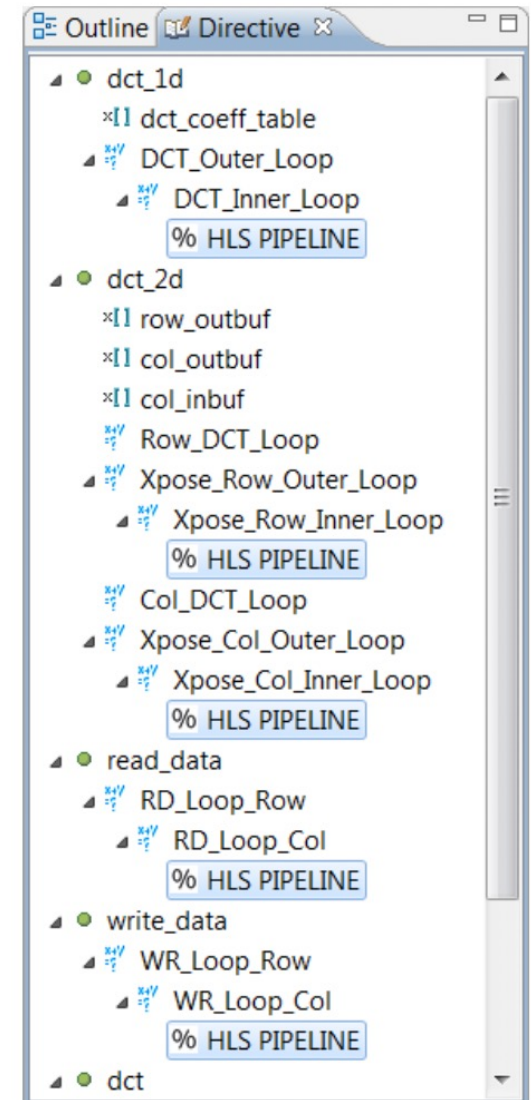
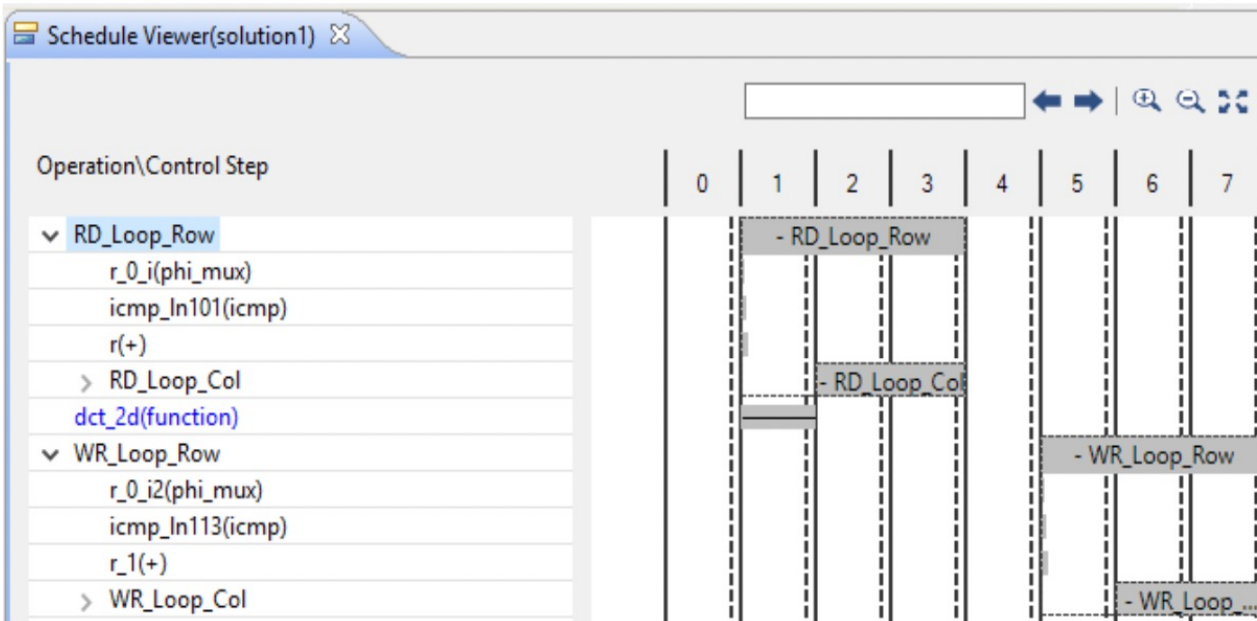
Latency (clock cycles)

		solution1
Latency	min	2935
	max	2935
Interval	min	2935
	max	2935

Utilization Estimates

	solution1
BRAM_18K	5
DSP48E	1
FF	246
LUT	964
URAM	0

Opt1- Inner Loop Pipelining



Opt2- Critical Outer Loop Pipelining

Performance(solution2) ✕

Current Module : dct > dct dct 2d > dct dct 1d2

	Operation\Control S...	C0	C1	C2	C3	C4
1	tmp 21 read(read)					
2	tmp 2 read(read)					
3	DCT Outer Loop					
4	k(phi mux)					
5	exitcond1(icmp)					
6	k 1(+)					
7	tmp 9(+)					
8-...	DCT Inner Loop					
19	tmp s(+)					
20	node 60(write)					

Performance Resource

Properties C Source ✕

File: C:\Vivado_HLS_Tutorial\Design_Analysis\lab1\dct.cpp

```
55
56 DCT_Outer_Loop:
57   for (k = 0; k < DCT_SIZE; k++) {
58     DCT_Inner_Loop:
59     for (n = 0, tmp = 0; n < DCT_SIZE; n++) {
60       int coeff = (int)dct_coeff_table[k][n];
61       tmp += src[n] * coeff;
62     }
63     dst[k] = DESCALE(tmp, CONST_BITS);
64   }
```

Outline Directive ✕

- dct_1d
 - ×[1] dct coeff table
 - ×[1] DCT_Outer_Loop
 - % HLS PIPELINE
 - ×[1] DCT_Inner_Loop
- dct_2d
 - ×[1] row_outbuf
 - ×[1] col_outbuf
 - ×[1] col_inbuf
 - ×[1] Row_DCT_Loop
 - ×[1] Xpose_Row_Outer_Loop
 - ×[1] Xpose_Row_Inner_Loop
 - % HLS PIPELINE
 - ×[1] Col_DCT_Loop
 - ×[1] Xpose_Col_Outer_Loop
 - ×[1] Xpose_Col_Inner_Loop
 - % HLS PIPELINE
- read_data
 - ×[1] RD_Loop_Row
 - ×[1] RD_Loop_Col
 - % HLS PIPELINE
- write_data
 - ×[1] WR_Loop_Row
 - ×[1] WR_Loop_Col
 - % HLS PIPELINE
- dct

Opt3-Array Partitioning

Operation/Control Step

	0	1	2	3	4	5
> [I/O Ports						
▼ [Memory Ports						
dct_coeff_table_7(p0)						
dct_coeff_table_4(p0)						
dct_coeff_table_3(p0)						
src(p0)		read				
dct_coeff_table_2(p0)		read				
dct_coeff_table_6(p0)		read				
src(p1)		ra	ra	ra	read	
dct_coeff_table_1(p0)		read				
dct_coeff_table_0(p0)		read				
dct_coeff_table_5(p0)		ra	ra	ra	read	
dst(p0)		read				
		read				
						write

Schedule Viewer | Resource Viewer

Properties | Warnings | C Source

File: C:\Vivado_HLS_Tutorial\Design_Analysis\lab1\dct.cpp

```

56 DCT_Outer_Loop:
57   for (k = 0; k < DCT_SIZE; k++) {
58     DCT_Inner_Loop:
59     for (n = 0; tmp = 0; n < DCT_SIZE; n++) {
60       int coeff = (int)dct_coeff_table[k][n];
61       tmp += src[n] * coeff;
62     }
63     dst[k] = DESCALE(tmp, CONST_BITS);
64   }
65 }
  
```

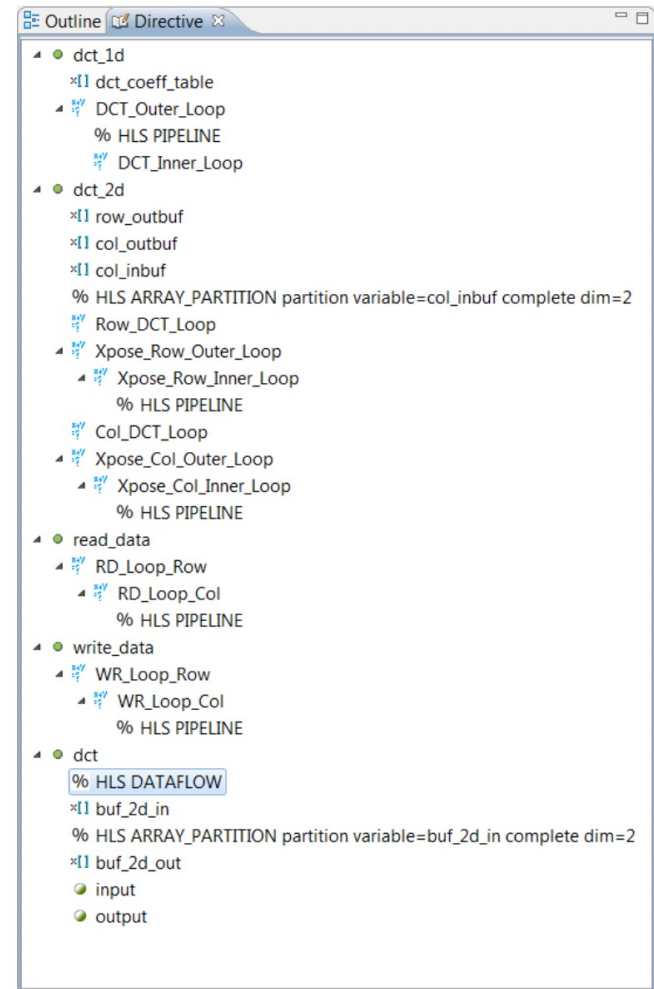
Outline | Directive

```

▲ ● dct_1d
  ×11 dct_coeff_table
  ▲ DCT_Outer_Loop
    % HLS PIPELINE
    ×11 DCT_Inner_Loop
  ▲ ● dct_2d
    ×11 row_outbuf
    ×11 col_outbuf
    ×11 col_inbuf
    % HLS ARRAY_PARTITION variable=col_inbuf complete dim=2
    ×11 Row_DCT_Loop
  ▲ Xpose_Row_Outer_Loop
    ▲ Xpose_Row_Inner_Loop
      % HLS PIPELINE
    ×11 Col_DCT_Loop
  ▲ Xpose_Col_Outer_Loop
    ▲ Xpose_Col_Inner_Loop
      % HLS PIPELINE
  ▲ ● read_data
    ▲ RD_Loop_Row
      ▲ RD_Loop_Col
        % HLS PIPELINE
  ▲ ● write_data
    ▲ WR_Loop_Row
      ▲ WR_Loop_Col
        % HLS PIPELINE
  ▲ ● dct
    ×11 buf_2d_in
    % HLS ARRAY_PARTITION variable=buf_2d_in complete dim=2
    ×11 buf_2d_out
    ● input
    ● output
  
```

Opt4-Apply Dataflow

		solution4	solution5
Latency	min	477	476
	max	477	476
Interval	min	477	343
	max	477	343



```
Outline Directive
├── dct_1d
│   ├── [1] dct_coeff_table
│   └── [1] DCT_Outer_Loop
│       ├── % HLS PIPELINE
│       └── [1] DCT_Inner_Loop
├── dct_2d
│   ├── [1] row_outbuf
│   ├── [1] col_outbuf
│   ├── [1] col_inbuf
│   ├── % HLS ARRAY_PARTITION partition variable=col_inbuf complete dim=2
│   ├── [1] Row_DCT_Loop
│   ├── [1] Xpose_Row_Outer_Loop
│   │   ├── [1] Xpose_Row_Inner_Loop
│   │   │   ├── % HLS PIPELINE
│   │   └── [1] Col_DCT_Loop
│   ├── [1] Xpose_Col_Outer_Loop
│   │   ├── [1] Xpose_Col_Inner_Loop
│   │   │   ├── % HLS PIPELINE
│   └── [1] read_data
│       ├── [1] RD_Loop_Row
│       │   ├── [1] RD_Loop_Col
│       │   │   ├── % HLS PIPELINE
│       └── [1] write_data
│           ├── [1] WR_Loop_Row
│           │   ├── [1] WR_Loop_Col
│           │   │   ├── % HLS PIPELINE
│       └── [1] dct
│           ├── % HLS DATAFLOW
│           ├── [1] buf_2d_in
│           ├── % HLS ARRAY_PARTITION partition variable=buf_2d_in complete dim=2
│           ├── [1] buf_2d_out
│           ├── [1] input
│           └── [1] output
```

Opt5-Inline (Apply Dataflow to Sub-Funtion)

Module Hierarchy		Negative Slack	BRAM	DSP	FF	LUT	Latency	Interval	Pipeline type
▼	dct	-	3	8	1009	1654	476	343	dataflow
▼	dct_2d	-	2	8	684	1171	342	342	none
●	dct_1d	-	0	8	350	200	11	11	none
●	write_data	-	0	0	32	186	66	66	none
●	read_data	-	0	0	29	171	66	66	none

```
Outline Directive
├─ dct_1d
│   └─ dct_coeff_table
├─ DCT_Outer_Loop
│   └─ % HLS PIPELINE
│       └─ DCT_Inner_Loop
├─ dct_2d
│   └─ % HLS INLINE
│       └─ row_outbuf
│           └─ col_outbuf
│               └─ col_inbuf
│                   └─ % HLS ARRAY_PARTITION partition variable=col_inbuf complete dim=2
│                       └─ Row_DCT_Loop
│                           └─ Xpose_Row_Outer_Loop
│                               └─ Xpose_Row_Inner_Loop
│                                   └─ % HLS PIPELINE
│                                       └─ Col_DCT_Loop
│                                           └─ Xpose_Col_Outer_Loop
│                                               └─ Xpose_Col_Inner_Loop
│                                                   └─ % HLS PIPELINE
├─ read_data
│   └─ RD_Loop_Row
│       └─ RD_Loop_Col
│           └─ % HLS PIPELINE
├─ write_data
│   └─ WR_Loop_Row
│       └─ WR_Loop_Col
│           └─ % HLS PIPELINE
├─ dct
│   └─ % HLS DATAFLOW
│       └─ buf_2d_in
│           └─ % HLS ARRAY_PARTITION partition variable=buf_2d_in complete dim=2
│               └─ buf_2d_out
│                   └─ input
│                       └─ output
```


Result

目標：
用 Vivado HLS 分析並將 DCT
優化成每 100 cycles 內可以吃下一筆資料

Performance Estimates

Timing (ns)

Clock		solution1	solution2	solution3	solution4	solution5	solution6
ap_clk	Target	8.00	8.00	8.00	8.00	8.00	8.00
	Estimated	4.14	4.14	6.35	6.35	6.35	6.35

Latency (clock cycles)

		solution1	solution2	solution3	solution4	solution5	solution6
Latency	min	2935	1723	843	477	476	463
	max	2935	1723	843	477	476	463
Interval	min	2935	1723	843	477	343	98
	max	2935	1723	843	477	343	98

每 98 cycles 可以
灌下一筆資料

Utilization Estimates

	solution1	solution2	solution3	solution4	solution5	solution6
BRAM_18K	5	5	5	3	3	3
DSP48E	1	1	8	8	8	16
FF	246	223	520	944	950	1250
LUT	964	1281	1483	1949	1878	1847
URAM	0	0	0	0	0	0

成功！