LAB#A-2
Design Analysis

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Github Link:
https://github.com/jasonlo0509/DCT_HLS_Optimization

Outline

- Objective
- 5 Optimizations (Pragmas)
  - Inner-loop Pipelining
  - Critical Outer-loop Pipepining
  - Array Partitioning
  - Apply Dataflow (Inter-Function Pipelining)
  - Inline (Apply Dataflow to Sub-Funtion)
- Result

Objective

目標：
用 Vivado HLS 分析並將 DCT
優化成每 100 cycles 內可以吃下一筆資料

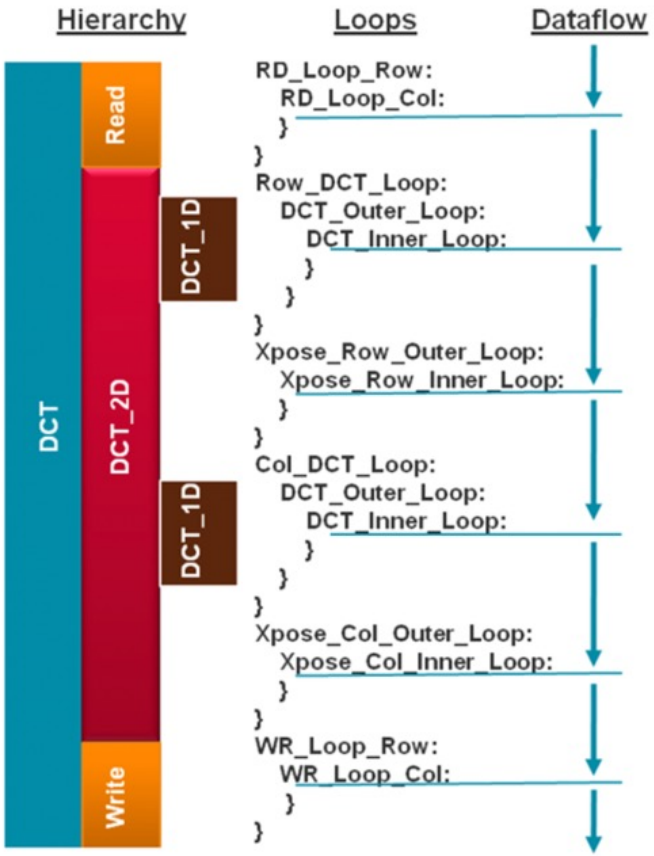


Figure 6-3: **Overview of the DCT Design**

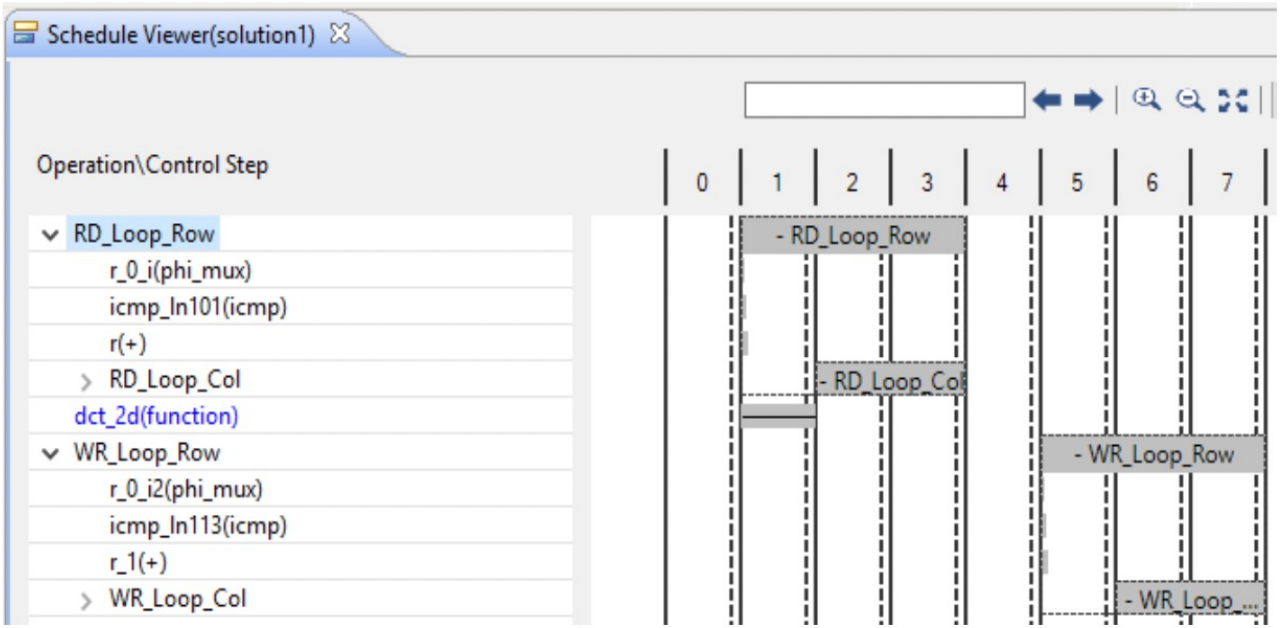
Latency (clock cycles)

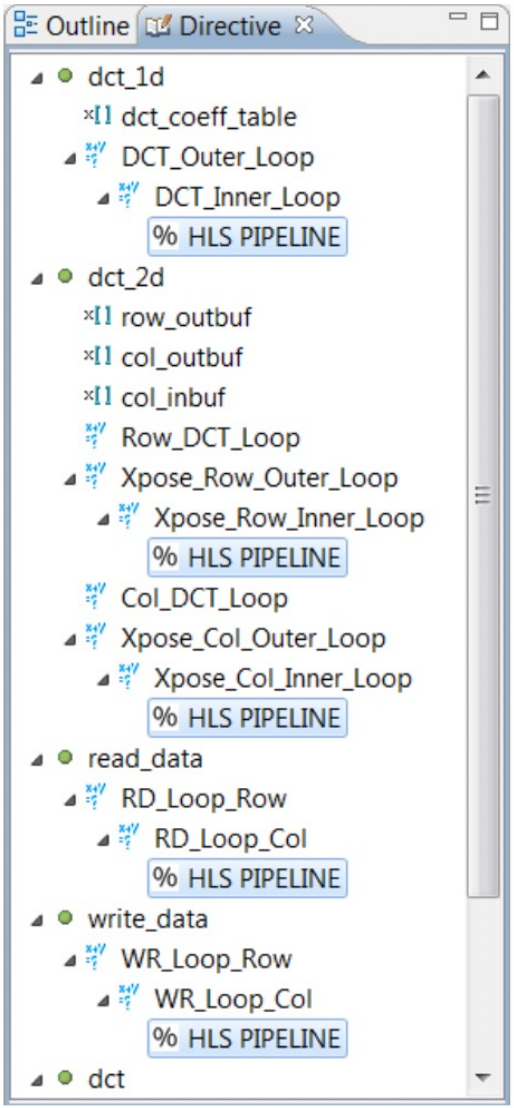
		solution1
Latency	min	2935
	max	2935
Interval	min	2935
	max	2935

Utilization Estimates

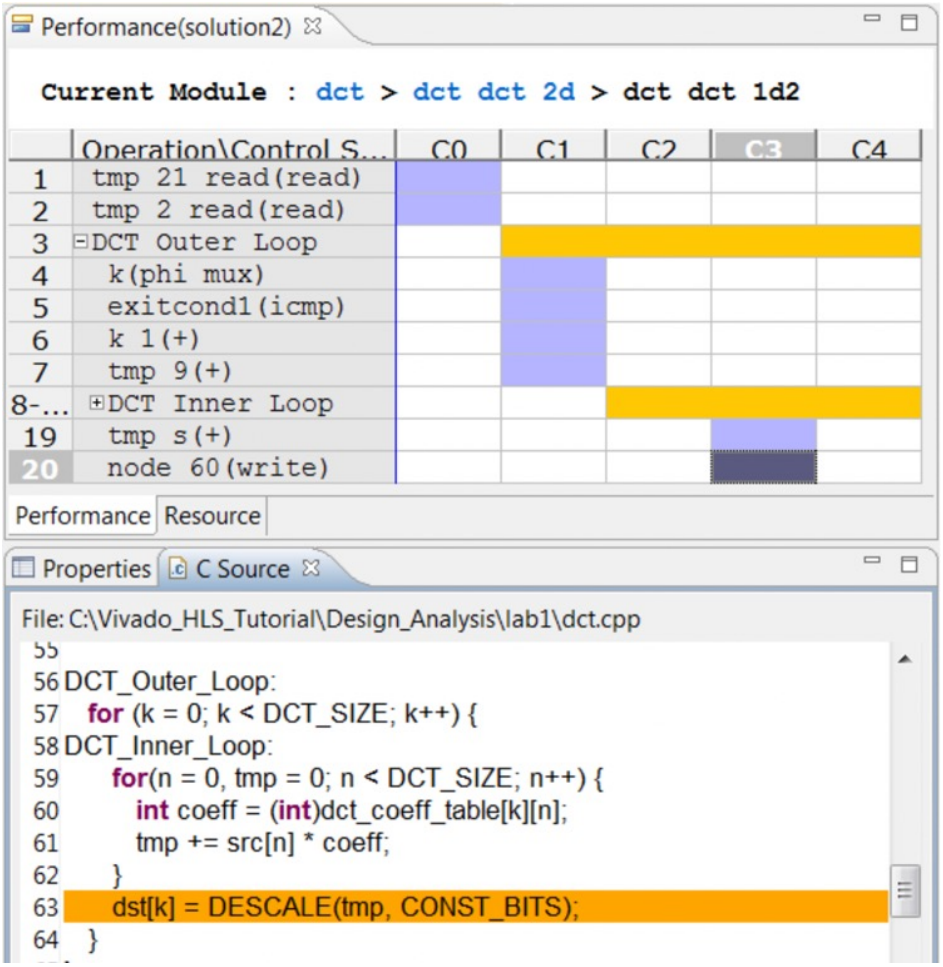
	solution1
BRAM_18K	5
DSP48E	1
FF	246
LUT	964
URAM	0

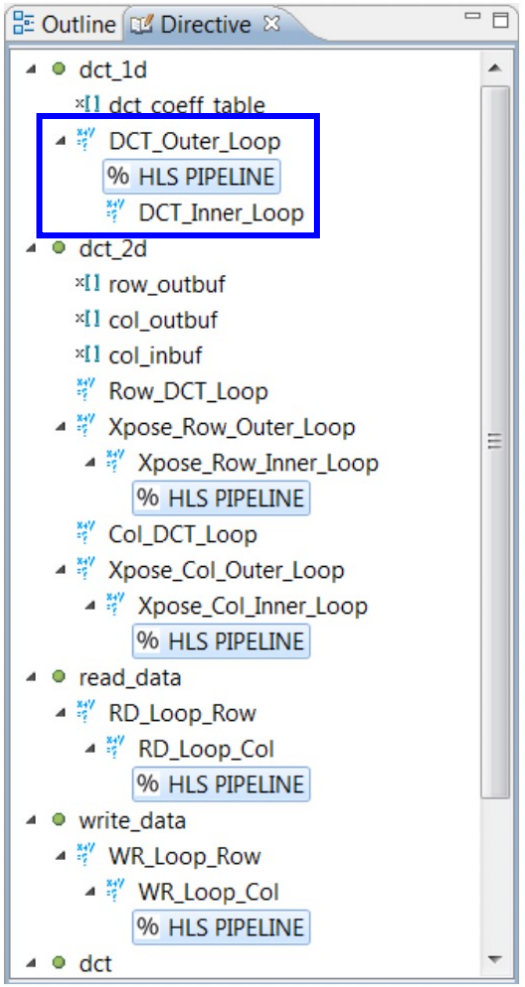
Opt1- Inner Loop Pipelining



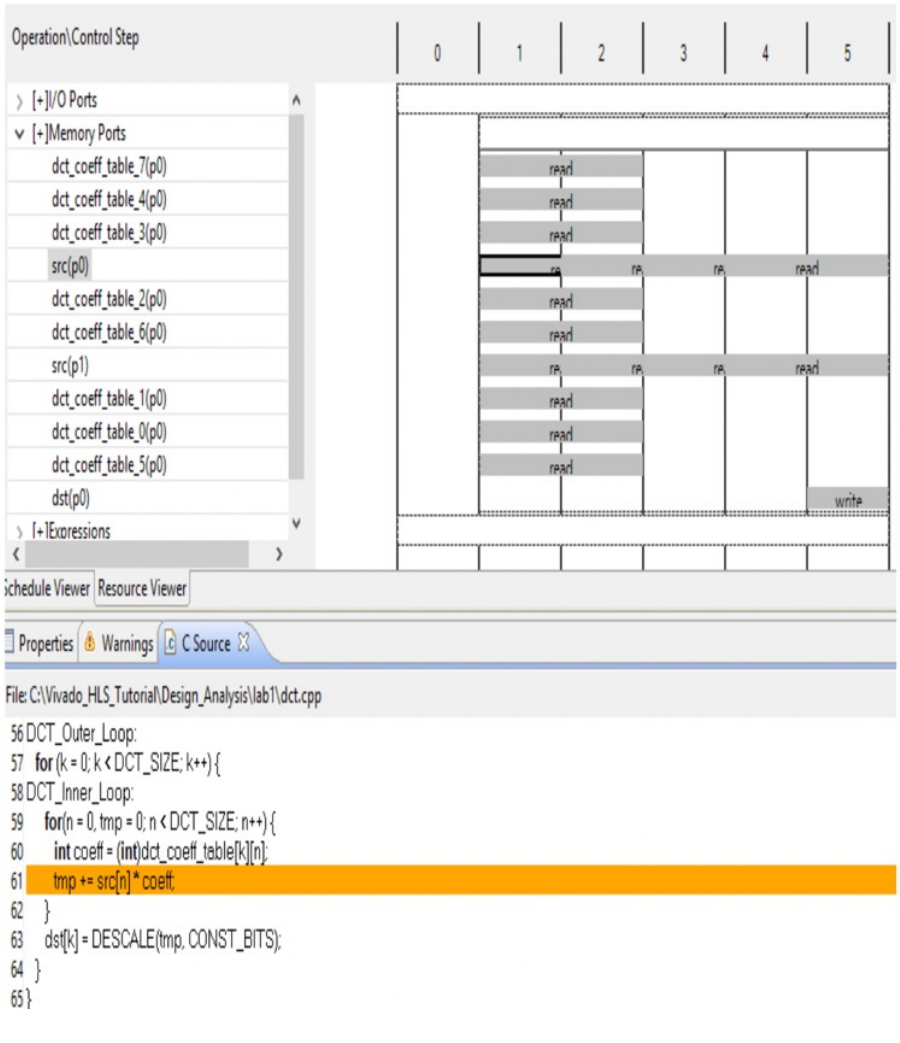


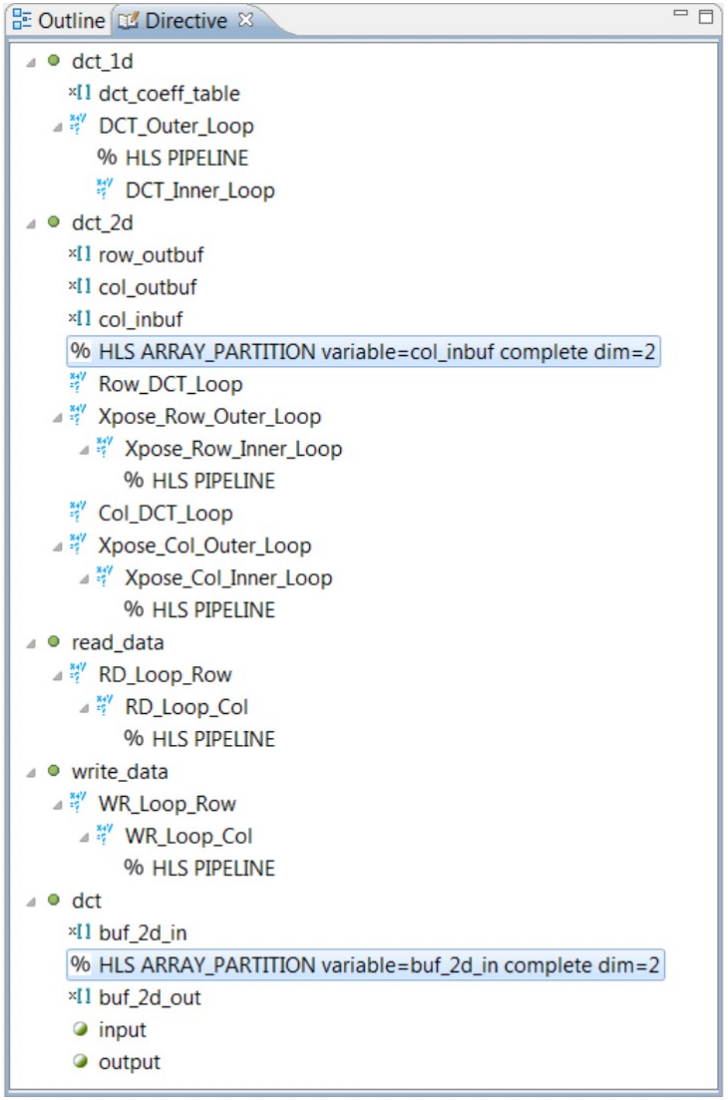
Opt2- Critical Outer Loop Pipelining





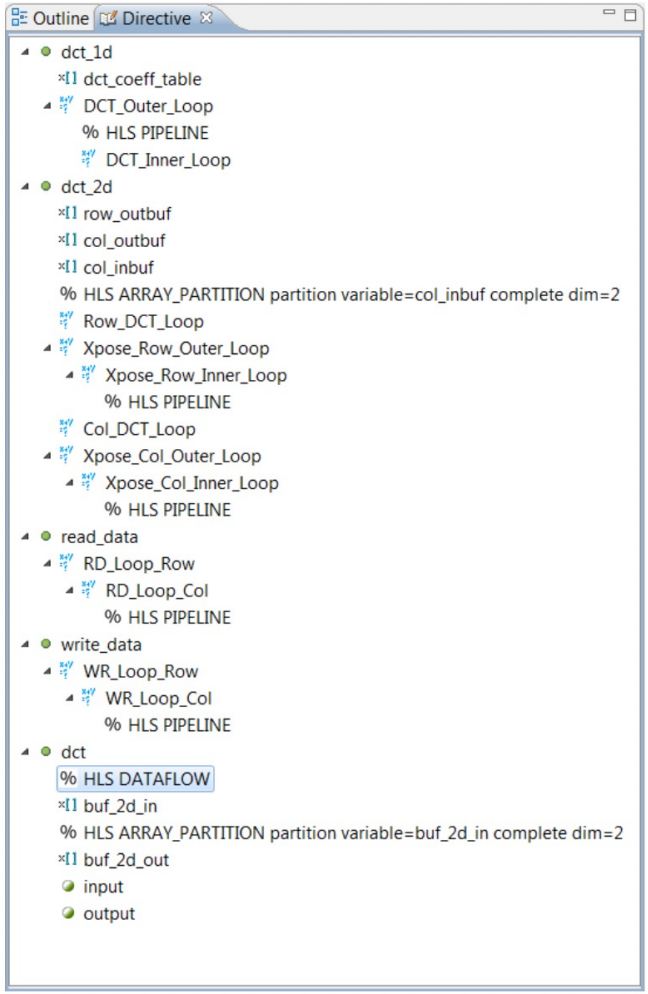
Opt3-Array Partitioning





Opt4-Apply Dataflow

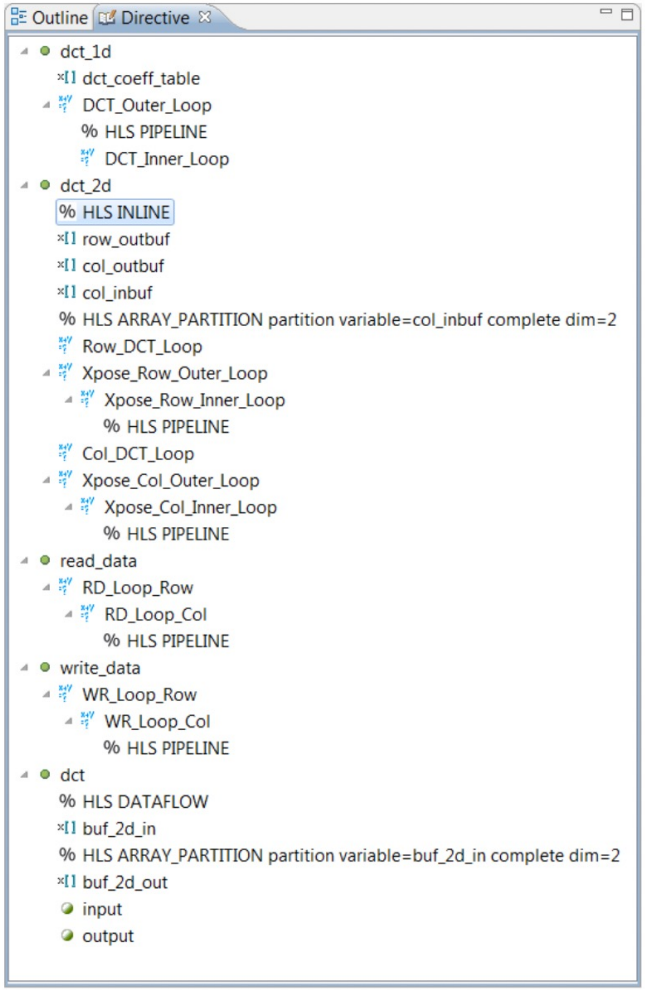
		solution4	solution5
Latency	min	477	476
	max	477	476
Interval	min	477	343
	max	477	343



Opt5-Inline (Apply Dataflow to Sub-Funtion)

Module Hierarchy

	Negative Slack	BRAM	DSP	FF	LUT	Latency	Interval	Pipeline type
dct	-	3	8	1009	1654	476	343	dataflow
dct_2d	-	2	8	684	1171	342	342	none
dct_1d	-	0	8	350	200	11	11	none
write_data	-	0	0	32	186	66	66	none
read_data	-	0	0	29	171	66	66	none



Result

目標：
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優化成每 100 cycles 內可以吃下一筆資料

Performance Estimates

Timing (ns)

Clock		solution1	solution2	solution3	solution4	solution5	solution6
ap_clk	Target	8.00	8.00	8.00	8.00	8.00	8.00
	Estimated	4.14	4.14	6.35	6.35	6.35	6.35

Latency (clock cycles)

		solution1	solution2	solution3	solution4	solution5	solution6
Latency	min	2935	1723	843	477	476	463
	max	2935	1723	843	477	476	463
Interval	min	2935	1723	843	477	343	98
	max	2935	1723	843	477	343	98

每 98 cycles可以灌下一筆資料

Utilization Estimates

	solution1	solution2	solution3	solution4	solution5	solution6
BRAM_18K	5	5	5	3	3	3
DSP48E	1	1	8	8	8	16
FF	246	223	520	944	950	1250
LUT	964	1281	1483	1949	1878	1847
URAM	0	0	0	0	0	0

成功！